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LETTER *Special Section on Nonlinear Theory and its Applications*

Wired CDMA Interface with Adaptivity for Interconnect Capacitances

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SUMMARY Wired CDMA interface with adaptivity for interconnect capacitances is designed to receive transmitted data even under a wide variety of connection topologies. The variable gain amplifier (VGA) is one of key circuit blocks to realize the adaptivity for interconnect capacitances. The system level numerical simulations derive the VGA specifications that the required VGA gain range is from 0.37 to 2.0, which can be realized easily using a multiple-differential-pair technique.

key words: *CMOS analog circuit, variable gain amplifier, CDMA*

1. Introduction

The progress of semiconductor technology for high-level integration faces the problem of enormous wiring in LSI. This brings about not only the increasing occupation area of wiring but also the increase of power consumption to drive long-wiring capacitances. One of the solutions is to use CDMA(Code Division Multiple Access) interface among LSIs or in a LSI [1]–[10]. The interface technique has been proved to be quite useful for dynamically programmable parallel processing LSIs [11], [12]. Figure 1 shows the wired CDMA interface, in which all transmitted signals are summed up on the bus through capacitive coupling after the data are modulated with a pseudo-noise (PN) code specified at each transmitter. In a receiver, the bus signal amplified with a variable gain amplifier (VGA) is demodulated with the same PN code of the transmitter desired to communicate with and integrated over PN code length. Therefore, an assignment of the same PN code for the transmitter and receiver by software corresponds to a virtual direct connection of their digital data stream.

This noise-tolerant interface enables multiple communications with simple wiring. In addition, electronic charge transferred to the CDMA bus from a transmitter is quite small, which gives rise to approximately 10–40 mV signal on the bus, leading to low-power data transmission. The major drawback of the interface is the difficulty to estimate the wiring bus capacitance prior to design because of unknown parasitic capacitance. Also, the number of transmitters and bus length affect the voltage amplitude of the bus lines. To deal with the variance of the bus amplitude under variety of connection topologies, it is imperative to use a VGA to obtain the desired signal level, followed by the correlation function blocks consisting of mixer, integrator and level detector. The level detector outputs binary data based on the integrated voltage. Figure 2 shows the block diagram of the receiver. At each initializing phase, the gain control circuit monitors the integrator output and sets the gain of VGA to keep the integrator output within a desired voltage level.

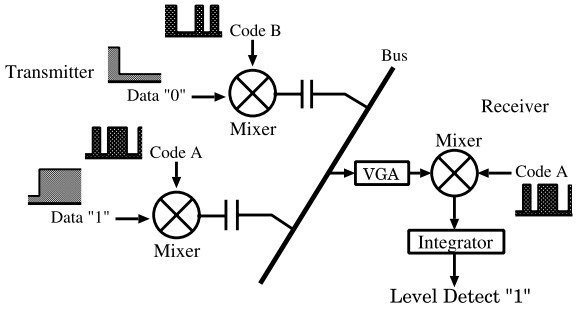

Fig. 1 Data transfer operation of wired CDMA interface.

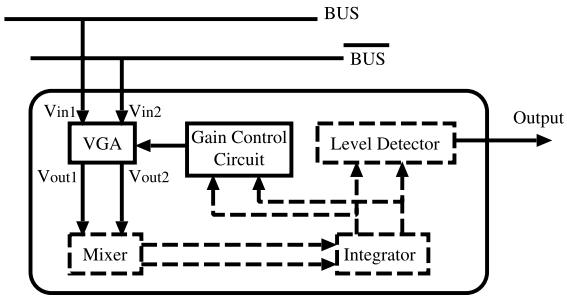

Fig. 2 Block diagram of CDMA interface receiver.

The demodulation of the bus signal consisting of multiplex data demands the use of VGA with wide input range and good gain linearity to avoid transmission bit error. Noted that the VGA for the wired CDMA interface differs from those in conventional wireless and wired communication systems with the long and short distance problem because respective received signal level of CDMA interface does not depend on the distance between a transmitter and a receiver.

This letter describes the design of wired CDMA interface with adaptivity for interconnection focusing on the VGA. Section 2 describes the specifications of VGA for the interface. In Sect. 3, we discuss circuit implementation of

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the VGA suitable for the interface and its control circuits. Section 4 concludes this letter. The circuit blocks which are not focused on in this letter are the same as shown in [5], [6].

2. VGA Specification

There are two key parameters to be specified before VGA circuit design, which are input range and gain linearity of VGA.

2.1 Input Range

We first investigated how the bus amplitude exceeding the input range of VGA affects the final integrator output in the receiver. Using M-sequence PN code [3], we performed system-level numerical simulations for 60 simultaneous data transmissions to clarify VGA specification. We define the maximum bus amplitude as $V_{BUS\,MAX}$ = 0.6V and the limited input range of VGA as ΔV_{inmax} under the simulation conditions shown in Table 1. If the input range of VGA, ΔV_{inmax}, is limited to the maximum bus amplitude, $V_{BUS\,MAX}$, by variable parasitic capacitance of the CDMA bus, all the simulated data are converged into very narrow integrated voltages of ±1.0 V and 0 V according to correlation of receiver's PN code with those of transmitters, as shown in Fig. 3. If ΔV_{inmax} is limited to a half of $V_{BUS\,MAX}$, the relatively small number of the over-range operations keeps the distribution of the integrated output in the similar narrow range. The integrator output distributions of the simulation results shown in Fig. 3 reveal that ΔV_{inmax} could be reduced to one forth of $V_{BUS\,MAX}$ without increasing erratic data transmissions if the reference voltages of level detectors(the pre-fixed threshold levels) are properly set as ±0.5 V. Noted that these two different reference levels realize capability of detecting whether data is being sent with the respective PN code, as described in [2], [3].

2.2 Gain Linearity

Figure 4 shows a simplified gain model of the VGA used in the simulation to evaluate influence of gain variation on the distribution of the integrator outputs. All simulation condition is the same as Table 1. In the following simulations, the linearity, G, is defined as the ratio of the gain at zero to that at the maximum input voltage as shown in Fig. 4. Figure 5 shows the simulation results carried out under the conditions

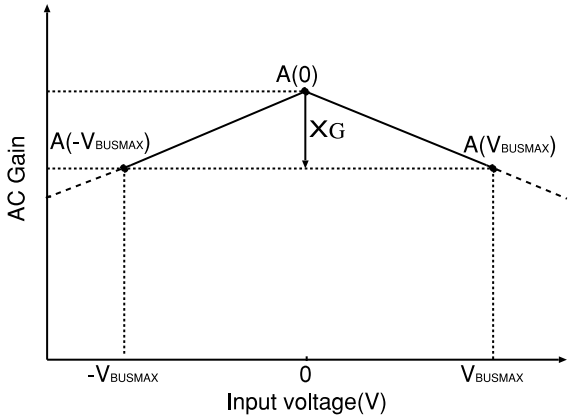

Fig. 4 Gain model of VGA with a linearity parameter for the system-level simulation.

Table 1 Condition of system-level simulation.

Multiplicity(Number of transmitters)	60
Number of receivers(correlated)	60
Number of receivers(uncorrelated)	60
Time constant of integrator	76.8 nsec
VGA gain	3
Chip rate	50 MHz
Data rate	390.625 kHz
Bus amplitude per transmitter	10 mV
Integrator output for unity gain	0.33 V
Integrator output for gain of 3	1 V
Number of data transmissions	100000

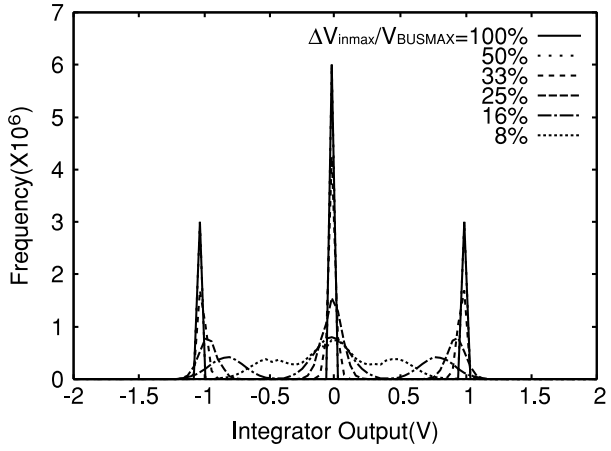

Fig. 3 Simulation result of CDMA interface as a parameter of maximum input range of VGA.

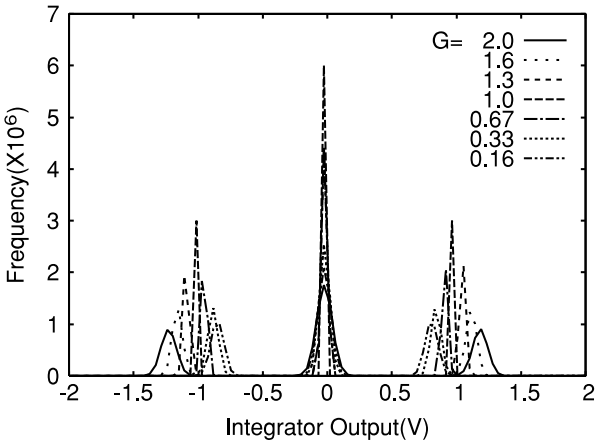

Fig. 5 Simulation result of CDMA interface as a parameter of VGA linearity.

given in Table 1. Figure 5 reveals that the wired CDMA interface is very robust for variation of G. Even variation of G over 50% does not cause fatal error, where $G = 1$ means a constant gain. However, to confirm whether the designed VGA can operate well in the wired CDMA interface, the range of gain linearity must be set. In this study, we set the range of gain linearity from 0.5 to $1.5(1 \pm 0.5)$, which is easy to be realized in circuit design.

Based on the above simulation results, VGA specification to operate well in the wired CDMA interfaces has two conditions: 1) input range over one-fourth of $V_{BUS\,MAX}$ and 2) gain variation within 50% in the input range.

3. Circuit Implementation

We designed the VGA using 0.35 μm CMOS technology, which satisfies the specifications described in Sect. 2.

3.1 VGA Circuit

We used a multiple-differential-pair technique [13], [14] which meets the VGA specifications for the wired CDMA interface. Figure 6 shows the implementation of the VGA. The device ratios of three differential pairs are $n : 1$, $1 : 1$ and $1 : n$, and the ratio of three tail currents is $m : 2 : m$. The gain can be controlled by changing tail current, I_{SS}. Both the input range and the gain linearity are the function of n and m. To satisfy the VGA specifications, n and m in Fig. 6 are chosen.

Figure 7 shows the simulated VGA gain characteristics. This figure demonstrates that two asymmetric differential pairs in Fig. 6 increase the VGA input range. In addition, gain linearity could be improved by keeping the gain variation small over the input range. These features satisfy the requirements for VGA as described in Sect. 2.

As shown in [14], multiple-differential-pair technique can realize better gain linearity than that shown in Fig. 7. However, application of many VGAs in the wired CDMA interface requires reduction of power and occupied area. To cope with it, the number of differential pairs is limited to three.

The common mode output voltage depends on I_{ss} due to the resistor loads to achieve high linearity. However, the variation of output common mode voltage does not affect the final results because common mode feedback circuit in the following integrator eliminates the variation.

Table 2 shows the parameters and characteristics of the VGA using 0.35 μm CMOS technology where m, and n are adjusted to obtain wide input range and good gain linearity at a given gain range.

3.2 Gain Control Circuit

Figure 8 shows the block diagram of a gain control circuit to provide a desired VGA output level. The gain control circuit consists of a digital circuit, comparators, a bias circuit and a variable current sink. The gain control circuit monitors the integrated value and outputs 4-bit data(b_0-b_3) by comparing it to prefixed reference voltage values(V_{ref1}, V_{ref2}). The gain of VGA is then controlled with the 4-bit data to adjust the integrator output to the proper range.

Figure 9 shows variable current sinks for the VGA. Depending on the gain control data from the gain control circuit, the gates of MOSFETs, M1-M4, with different sizes are properly biased.

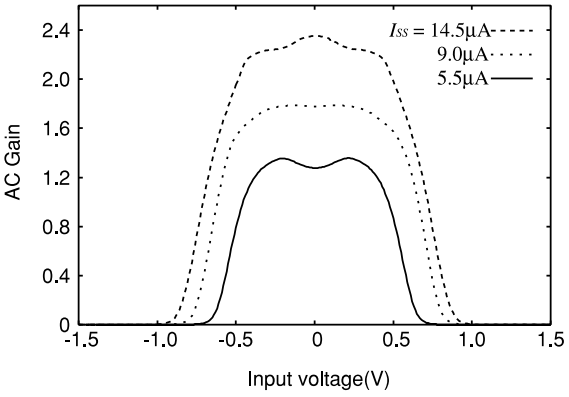

Fig. 7 Simulated gain of the designed VGA.

Table 2 Parameters and characteristics of designed VGA.

n	16
m	6
R	16kΩ
Gain	0.37–2.0
Maximum input voltage	> 0.4V
Bandwidth	> 200 MHz
Power consumption	174.9–1287μW

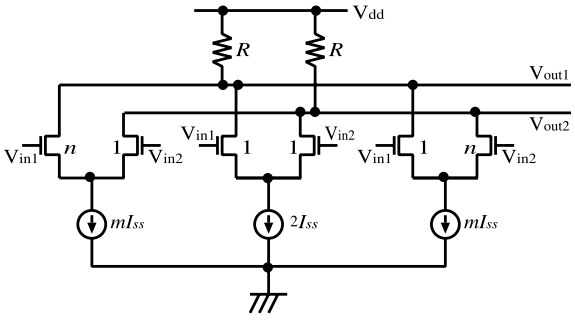

Fig. 6 Schematic of the designed VGA with three differential pairs.

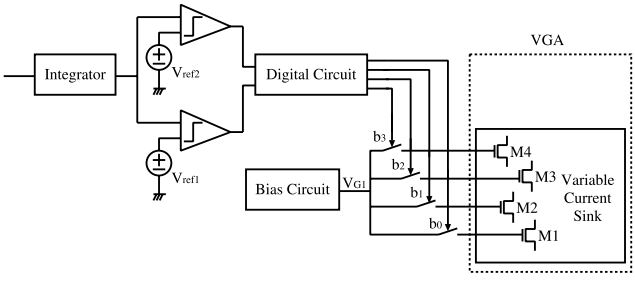

Fig. 8 Block diagram of gain control circuit.

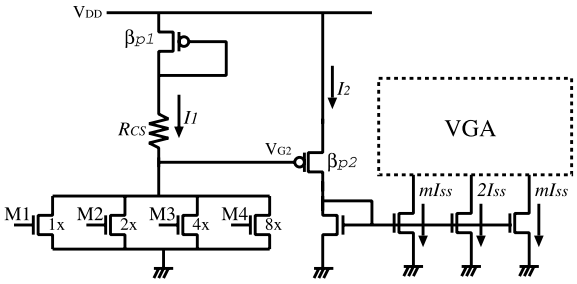

Fig. 9 Schematic of variable current sink.

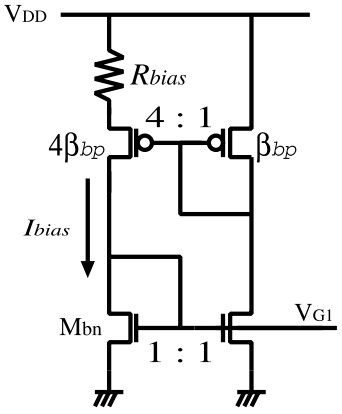

Fig. 10 Schematic of bias circuit.

The bias circuit shown in Fig. 10 [15] is used, whose bias current is given by

$$I_{bias} = \frac{1}{2R_{bias}^2 \beta_{bp}}. \tag{1}$$

The drain of the four MOSFETs (M1-M4) in Fig. 9 are self biased with the load resistance R_{CS} to avoid temperature drift in the VGA gain. The bias voltage V_{G1} in Fig. 8 is provided to the gates of the selected devices of the four MOSFETs (M1-M4) shown in Fig. 9 depending on the gain control 4-bit data(b_0-b_3), while the gate of the unselected ones are biased at 0 V. To properly operate the VGA, at least one of the gates of M1-M4 shown in Fig. 9 must be biased at V_{G1}. For such occasions, I_1 in Fig. 9 can be given by

$$I_1 = kI_{bias}, \tag{2}$$

where k is a function of the gain control 4-bit data. In this situation, I_2 in Fig. 9 is given by

$$I_2 = \frac{\beta_{p2}}{2}\left(\sqrt{\frac{2I_1}{\beta_{p1}}} + RI_1\right)^2. \tag{3}$$

Therefore, gain of the amplifier G_{VGA} can be expressed in the following form.

$$G_{VGA} = \sqrt{\frac{\beta_n \beta_{p2}}{\beta_{p1}\beta_{bp}}}\sqrt{k}\frac{R}{R_{bias}} + \frac{R_{CS}R}{2R_{bias}^2}\frac{\sqrt{\beta_n\beta_{p2}}}{\beta_{bp}}k \tag{4}$$

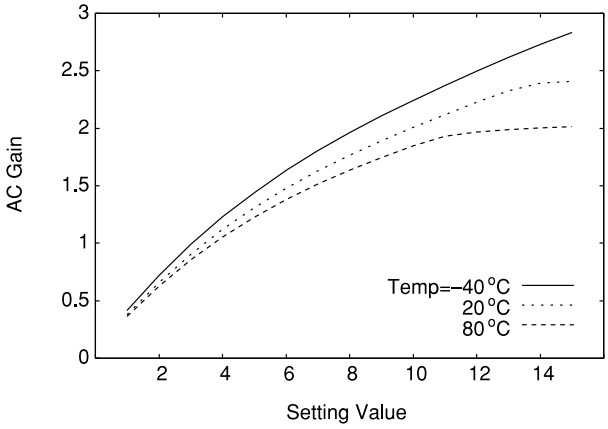

Fig. 11 Simulation results of VGA AC gain controllability.

Equation (4) demonstrates that the VGA gain is not affected by the resistance variation because the resistances can be matched within 1% in a fabricated IC chip. By selecting the adequate parameters, the second term in Eq. (4) becomes larger than the first term, meaning more linear dependence of the VGA gain on the setting value (k).

Figure 11 shows circuit simulation result of VGA as a parameter of 4-bit gain control data. This simulation result reveals that the gain of the designed VGA can be varied from 0.37 to 2.0 in wide temperature range. The designed VGA can realize the CDMA interface with adaptivity for five times variation of interconnect capacitances.

4. Conclusion

The wired CDMA interface with adaptivity for interconnect capacitances is designed, which can receive data correctly even if bus capacitance varies. The VGA is one of key circuit blocks to realize the adaptivity for interconnect capacitances. It is proved that the VGA specifications derived from the system-level numerical simulation can be met with the use of multiple-differential-pair technique. The designed VGA with three differential pairs ensures wide maximum input range for the wired CDMA interface and good linearity. The gain of the designed VGA can be varied from 0.37 to 2.0 in wide temperature range using the designed bias circuit. The designed VGA can realize the CDMA interface with adaptivity for variation of interconnect capacitances.

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References

[1] Y. Yuminaka, K. Itoh, Y. Sasaki, T. Aoki, and T. Higuchi, “A code-

division multiplexing technique for efficient data transmission in VLSI systems," IEICE Trans. Electron., vol.E82-C, no.9, pp.1669–1677, Sept. 1999.

[2] R. Yoshimura, B.K. Tan, T. Ogawa, and K. Taniguchi, "CDMA wired interface," IEICE Trans. Electron. (Japanese Edition), vol.J82-C-II, no.11, pp.631–636, Nov. 1999.

[3] R. Yoshimura, T.B. Keat, T. Ogawa, S. Hatanaka, T. Matsuoka, and K. Taniguchi, "DS-CDMA wired bus with simple interconnection topology for parallel processing system LSIs," 2000 IEEE International Solid-State Circuit Conference, pp.370–371, Feb. 2000.

[4] B.K. Tan, R. Yoshimura, T. Matsuoka, and K. Taniguchi, "An efficient data transmission interface for VLSI systems using code-division multiple access technique," 27th European Solid-State Circuits Conference, pp.176–179, Sept. 2001.

[5] B.K. Tan, R. Yoshimura, Y. Shimizu, S. Shimizu, T. Matsuoka, and K. Taniguchi, "A balanced switched-capacitor charge pump circuit for CDMA bus interface," IEEJ 5th International Analog VLSI Workshop, pp.138–143, May 2001.

[6] H. Iwamura, R. Yoshimura, T. Boon-Keat, T. Matsuoka, and K. Taniguchi, "Error analysis on simultaneous data transfers in CDMA wired interface," Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, pp.408–409, Sept. 2001.

[7] Y. Yuminaka and S. Sakamoto, "An efficient data transmission technique for VLSI systems using multiple-valued code-division multiple access," IEICE Trans. Electron., vol.E85-C, no.8, pp.1581–1587, Aug. 2002.

[8] M. Takahashi, B.K. Tan, H. Iwamura, T. Matsuoka, and K. Taniguchi, "A study on robustness and coupling-noise immunity on simultaneous data transfer CDMA bus interface," International Symposium on Circuits and Systems, vol.IV, pp.611–614, May 2002.

[9] M. Takahashi, B.K. Tan, H. Iwamura, T. Matsuoka, and K. Taniguchi, "Behavior-level-analysis in simultaneous data transfer CDMA bus interface," IEICE Trans. Electron. (Japanese Edition), vol.J86-C, no.2, pp.177–185, Feb. 2003.

[10] Z. Xu, H. Shin, J. Kim, M.F. Chang, and C. Chien, "A 2.7 Gb/s CDMA-interconnect transceiver chip set with multi-level signal data recovery for re-configurable VLSI systems," 2003 IEEE International Solid-State Circuit Conference, pp.82–83, Feb. 2003.

[11] B.K. Tan, R. Yoshimura, T. Matsuoka, and K. Taniguchi, "A novel dynamically programmable arithmetic array (DPAA) processor for digital signal processing," IEICE Trans. Fundamentals, vol.E84-A, no.3, pp.741–747, March 2001.

[12] B.K. Tan, R. Yoshimura, T. Matsuoka, and K. Taniguchi, "Dynamically programmable parallel processor (DPPP): A novel reconfigurable architecture with simple program interface," IEICE Trans. Inf. & Syst., vol.E84-D, no.11, pp.1521–1527, Nov. 2001.

[13] A. Nedungadi and T.R. Viswanathan, "Design of linear CMOS transconductance elements," IEEE Trans. Circuits Syst., vol.CAS-31, no.10, pp.891–894, Oct. 1984.

[14] H. Tanimoto, M. Koyama, and Y. Yoshida, "Realization of a 1-V active filter using a linearization technique employing plurality of emitter-coupled pairs," IEEE J. Solid-State Circuits, vol.26, no.7, pp.937–945, July 1991.

[15] S.D. Willingham, K.W. Martin, and A. Ganesan, "A BiCMOS low-distortion 8-MHz low-pass filter," IEEE J. Solid-State Circuits, vol.28, no.12, pp.1234–1245, Dec. 1993.