



Title	A New Inductance Extraction Technique of On-wafer Spiral Inductor Based on Analytical Interconnect Formula
Author(s)	Shima, Hideki; Matsuoka, Toshimasa; Taniguchi, Kenji
Citation	IEICE Transactions on Electronics. 2005, E88-C(5), p. 824-828
Version Type	VoR
URL	https://hdl.handle.net/11094/51713
rights	copyright©2005 IEICE
Note	

The University of Osaka Institutional Knowledge Archive : OUKA

<https://ir.library.osaka-u.ac.jp/>

The University of Osaka

A New Inductance Extraction Technique of On-Wafer Spiral Inductor Based on Analytical Interconnect Formula

Hideki SHIMA^{†*a)}, Nonmember, Toshimasa MATSUOKA[†], and Kenji TANIGUCHI[†], Members

SUMMARY A new inductance extraction technique of spiral inductor from measurement fixture is presented. We propose a scalable expression of parasitic inductance for interconnects, and design consideration of test structure accommodating spiral inductor. The simple expression includes mutual inductance between the interconnects with high accuracy. The formula matches a commercial field solver inductance values within 1.4%. The layout of the test structure to reduce magnetic coupling between the spiral and the interconnects allows us to extract the intrinsic inductance of spiral more accurately. The proposed technique requires neither special fixture used for measurement-based method nor skilled worker for precise extraction with the analytical technique used.

key words: spiral inductors, interconnect, closed-form expression, inductance extraction, analytical technique

1. Introduction

Spiral inductors fabricated on integrated circuits (IC's) are essential passive components in radio frequency (RF) IC's [1]. An extraction technique of the inductance from measurements with test structures (see Figs. 1(a) and 1(b)) is highly required prior to circuit design because the inductance plays a dominant role in overall circuit performance [2]. Equivalent inductor models [3]–[5] are widely employed for the extraction, which include parasitic interconnects inductance between pads and a spiral. This leads to incorrect extracted inductance of the spirals due to the interconnects effect. On the other hand, measurement-based methods reported in [6] require skilled worker for precise measurements and cumbersome procedures for the extraction by using special fixtures, although the parasitic effect can be de-embedded.

The aim of this paper is to propose a new simple extraction technique of intrinsic inductance using analytical inductance formula of the interconnects together with properly designed test structure. The technique consists of two steps. First, effective inductance including the interconnect effect is extracted from measurements by using a compact inductor model. Second, the effect is de-embedded from the effective inductance using the proposed analytical formula. The analytical technique presented here is quite useful and practical for extracting the intrinsic inductance from measurements without any special measurement fixture.

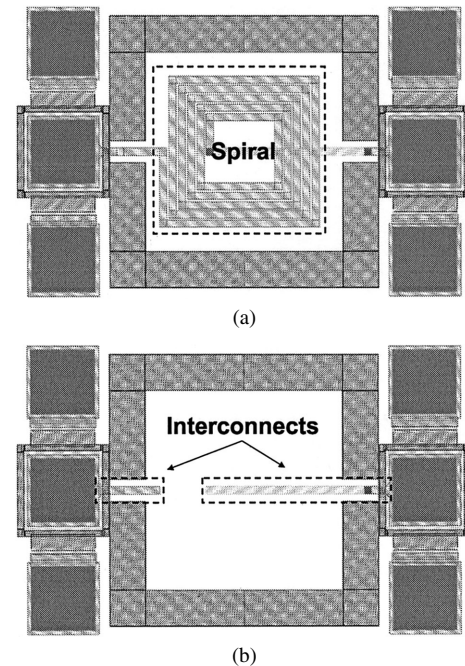


Fig. 1 (a) A layout of square spiral inductor with measurement fixture. (b) The measurement fixture, composed of pads and interconnects, used in Fig. 1(a).

2. Self-Inductance Expression of Interconnects

2.1 Closed-Form Expression

We present an inductance formula of interconnects to de-embed the parasitic inductance L_p . The accurate self-inductance expression of single wire with rectangular cross section [7], [8] is employed to derive the proposed formula (an outline of the derivation is given in Appendix). The derived expression is simple form despite the inclusion of mutual inductance between the interconnects. This can be achieved by using our derivation technique rather than direct calculation of the mutual inductance from Naumann's formula. All geometric parameters of the interconnects, as shown in Fig. 2, are included in the equation: the length of each interconnect l_α and l_β , the wire width w , the wire thickness t , and the gap spacing between interconnects d . This allows us to calculate the parasitic inductance directly from the geometric parameters. Note that the vertical gap between different metal layers is ignored because the gap is

Manuscript received July 13, 2004.

Manuscript revised September 27, 2004.

[†]The authors are with the Graduate School of Engineering, Osaka University, Suita-shi, 565-0871 Japan.

*Presently, with the Texas Instruments Japan Ltd.

a) E-mail: h-shima@ti.com

DOI: 10.1093/ietele/e88-c.5.824

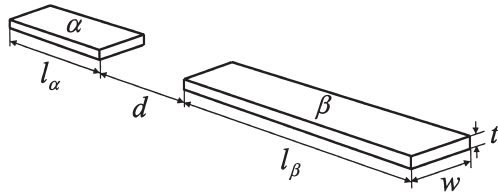


Fig. 2 The geometric parameters of the interconnects. l_α and l_β are the lengths of two segments, d the gap between the interconnects, w the width, and t the thickness.

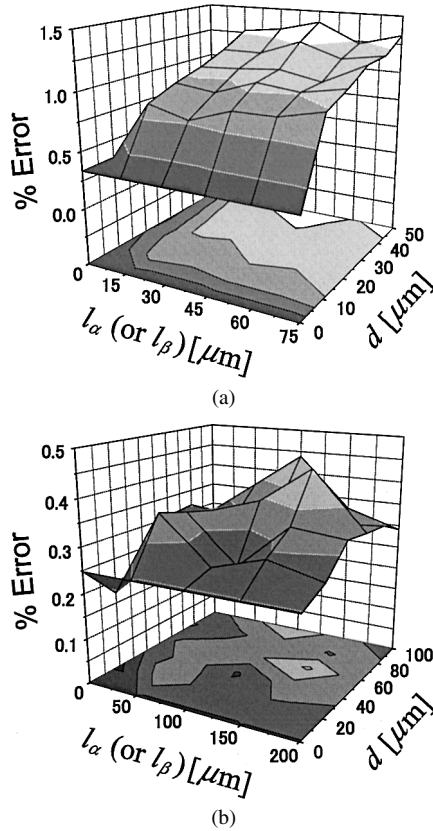


Fig. 3 Error distribution in % of our expression in comparison with a commercial field solver. The overall length $l_\alpha + l_\beta + d$ is $200 \mu\text{m}$ for (a) and $500 \mu\text{m}$ for (b). The width w is $10 \mu\text{m}$ and the thickness t $1 \mu\text{m}$ for both cases.

very small compared with each interconnect length, resulting in negligible effect on mutual inductance. The resulting expression is given by

$$L_p = \frac{\mu_0 l_\alpha}{2\pi} \left\{ \ln \left| \frac{2l_\alpha (l_\alpha + l_\beta + d)}{l_\alpha + d} \frac{1}{GMD} \right| - 1 \right\} + \frac{\mu_0 l_\beta}{2\pi} \left\{ \ln \left| \frac{2l_\beta (l_\alpha + l_\beta + d)}{l_\beta + d} \frac{1}{GMD} \right| - 1 \right\} + \frac{\mu_0 d}{2\pi} \ln \left| \frac{d (l_\alpha + l_\beta + d)}{(l_\alpha + d)(l_\beta + d)} \right| \quad (1)$$

where μ_0 magnetic permeability of vacuum. The GMD geometric mean distance of rectangular cross section is

$$GMD = 0.224 (w + t). \quad (2)$$

2.2 Validation

Figure 3(a) shows the accuracy of our expression compared with those obtained from a field solver, Ansoft Q3D Extractor [9]. The absolute percentage error, z-axis, is defined by $100|L_{\text{formula}} - L_{\text{Q3D}}|/L_{\text{Q3D}}$ where L_{formula} and L_{Q3D} are the inductances of interconnects calculated from our expression and the field solver, respectively. The x-axis indicates the length of either interconnect (l_α or l_β) at the given distance between pads, $l_\alpha + l_\beta + d$, of $200 \mu\text{m}$ while y-axis shows the gap spacing (d). The plot shows the errors are around 1% ranging up to the maximum error of 1.4%. Note that $200 \mu\text{m}$ is the minimum distance between pads for measurement fixtures of spirals.

Figure 3(b) shows the absolute error distribution at the given length of $l_\alpha + l_\beta + d = 500 \mu\text{m}$. The plot shows that the error is less than 0.5%. These results indicate that our formula is accurate enough to extract the intrinsic inductance of on-chip spirals.

3. Design Consideration of Test Structure

To extract accurate intrinsic inductance of spirals from measurements, special attention has to be paid to the layout of test structures to reduce magnetic coupling between the spiral and the interconnects. The layout with minimum coupling allows the components to be treated separately so that the excess inductance due to the interconnects can be simply subtracted from measured results.

Figure 1(a) show the layout to reduce the magnetic coupling for accurate inductance extraction: the interconnects are arranged in line and connected to each port of the spiral. In this configuration, the set of interconnects divide the spiral symmetrically into two pieces. Therefore, total mutual inductance between each interconnect and the half pieces of spiral becomes zero because the currents on each side of the leads are in the opposite direction. Note that the layout will be the best form to extract the intrinsic inductance of spiral in the layouts, although the layout is commonly used as the test structure.

4. Extraction of Intrinsic Inductance

4.1 Extraction Procedure

The details of the analytical extraction method is as follows:

1. Effective inductance including interconnects value is extracted from measured S-parameters of the device under test (DUT) by using a lumped-element inductor model. S-parameters are converted to Y-parameters for the extraction.
2. Desired intrinsic inductance of the spiral is extracted directly from the effective value by subtracting the calculated interconnects inductance (L_p).

Table 1 The layout parameters of spirals and the interconnects connected. For spirals, n is the number of turns, d_{out} the outer diameter, w the metal width, and s the turn spacing. L_{meas} is the extracted measured inductance by using the proposed formula. For the interconnects, l_α and l_β are each interconnect length, and d the gap between the interconnects. The inductors numbered 1-3, 7 and 11 are fabricated with SOI-CMOS process.

Inductor #	L_{meas} [nH]	n	d_{out} [μ m]	w [μ m]	s [μ m]	l_α [μ m]	l_β [μ m]	d [μ m]
1	0.480	1	119	10	3	137	246	23
2	1.02	2	145	10	3	124	246	36
3	1.97	3	171	10	3	111	246	49
4	2.41	3	159.5	8.5	1	122.15	254.15	37
5	3.29	4	215.25	14.25	1	91.4	246.65	75.25
6	3.29	4	217	9	8	89.65	246.65	77
7	3.34	4	197	10	3	98	246	62
8	3.51	4	218.75	3.75	15	87.9	246.65	78.75
9	4.62	4	210.25	9.25	1	96.4	266.65	50.25
10	5.24	5	211.6	10.6	1	95.05	249.65	68.6
11	5.33	5	223	10	3	85	246	75
12	10.1	5	204.6	3.6	1	102.05	284.65	26.6

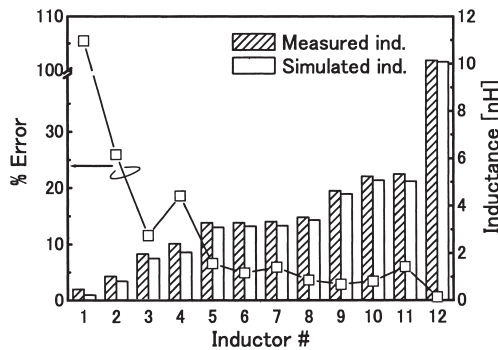


Fig. 4 Comparison between extracted measured and simulated inductances. The open squares are the error percentage, while the bars show the inductance for both measured and simulated results.

Note that the extraction of effective inductance (equivalent value) from Y-parameters is performed in low frequency where the frequency behavior of the parasitic resistance and capacitance can be negligible. The simple lumped model is not valid for the extraction in high frequency.

4.2 Results

The new technique is applied to a set of spirals listed in Table 1. We use a conventional spiral inductor model [5] to extract the effective inductance from measurements. The measured planar spiral inductors have been fabricated on both 0.20- μ m SOI-CMOS and 0.35- μ m CMOS processes.

Figure 4 shows a comparison between measured and simulated inductance of the spirals. The measured values (L_{meas}) are the extracted inductances using the proposed formula, while the simulated results (L_{sim}) are obtained from Ansoft Q3D Extractor. The percentage error defined by $100|L_{meas} - L_{sim}|/L_{sim}$ is plotted against the left axis of the figure. Note that larger extracted inductance results in smaller error because the difference between the extracted and simulated values is nearly constant for all inductors. The errors of inductors over 3nH are typically around 3%-6%, while those of small inductors (#1-4) result in larger errors. These errors are originated from measurement system calibration and in-

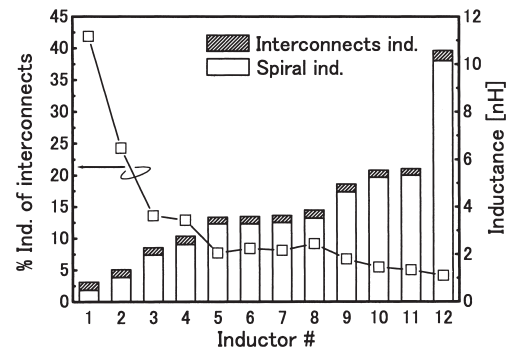


Fig. 5 Impact of interconnects for measured inductors before the spiral extraction. The open squares are the fraction of interconnects inductance for the inductors, while the bars indicate the measured inductance including interconnects estimated by using our expression.

ductor model to extract effective inductance [10]. Therefore, accurate calibration of measurement system and optimum choice of the model are essential to reduce the error of the extracted inductance. Even if the errors exist, for larger inductor, reasonable inductance value is extracted by using our technique.

Figure 5 illustrates the impact of interconnects for measured spirals with fixture. The left axis indicates the fraction of interconnects inductance to the measured total counterpart, where the impact becomes more significant for spirals with small inductance. This originates from the longer interconnect for the small inductors because the size of the fixture is designed to accommodate the largest one. It should be noted that such small inductors are key components for state-of-the-art RF circuits in GHz bands. Hence, de-embedding interconnects is fairly important to estimate the inductance of such spirals.

5. Conclusion

We proposed a scalable expression of interconnect inductance and design consideration of test structure to extract spirals from measurement fixtures. The inductance of interconnects predicted with our formula matches that derived

from the field solver, Ansoft Q3D Extractor, within 1.4% error. With the use of the inductor layout to reduce the magnetic coupling, the measured inductances extracted are in good agreement with the simulated results. The accuracy and simplicity of the technique without special fixtures, offer practical method to extract intrinsic inductance of spirals.

Acknowledgments

This work was supported by Japan Society for the Promotion Science (JSPS) Research for the Future Program, and by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

References

- [1] J.N. Burghartz, D.C. Edelstein, M. Soyuer, H.A. Ainspan, and K.A. Jenkins, "RF circuit design aspects of spiral inductors on silicon," IEEE J. Solid-State Circuits, vol.33, no.12, pp.2028–2034, Dec. 1998.
- [2] J.R. Long and M.A. Copeland, "The modeling, characterization, and design of monolithic inductors for silicon RF IC's," IEEE J. Solid-State Circuits, vol.32, no.3, pp.357–369, March 1997.
- [3] D. Melendy, P. Francis, C. Pichler, K. Hwang, G. Srinivasan, and A. Weisshaar, "A new wide-band compact model for spiral inductors in RFICs," IEEE Electron Device Lett., vol.23, no.5, pp.273–275, May 2002.
- [4] S. Chaki, S. Aono, N. Andoh, Y. Sasaki, N. Tanino, and O. Ishihara, "Experimental study on spiral inductors," IEEE MTT-S Int. Microwave Symp. Dig., vol.2, pp.753–756, May 1995.
- [5] N.M. Nguyen and R.G. Meyer, "Si IC-compatible inductors and LC passive filters," IEEE J. Solid-State Circuits, vol.25, no.4, pp.1028–1031, Aug. 1990.
- [6] T.E. Kolding, "On-wafer calibration techniques for giga-hertz CMOS measurements," Proc. IEEE 1999 Int. Conf. on Microelectronic Test Structures, vol.12, pp.105–110, March 1999.
- [7] F.W. Grover, Inductance Calculations, Van Nostrand, New York, 1946.
- [8] F.W. Grover, "The calculation of the inductance of single-layer coils and spirals wound with wire of large cross section," Proc. Institute of Radio Engineers, vol.17, no.11, pp.2053–2063, Nov. 1929.
- [9] Ansoft Corp., Pittsburgh, PA.
- [10] S.S. Mohan, M.M. Hershenson, S.P. Boyd, and T.H. Lee, "Simple accurate expressions for planar spiral inductances," IEEE J. Solid-State Circuits, vol.34, no.10, pp.1419–1424, Oct. 1999.

Appendix: Derivation of Interconnect Expression

To derive an expression for the parasitic inductance, L_p , of interconnects, an accurate analytical inductance formula of single wire are required. We employ Naumann's formula for self-inductance of a wire [7] given by

$$L_{\text{wire}} = \frac{\mu_0 l}{2\pi} \left(\ln \left| \frac{2l}{GMD} \right| - 1 \right) \quad (\text{A} \cdot 1)$$

where l the wire length and GMD the geometric mean distance determined by the cross section of wire.

Figure A·1 denotes the concept of the derivation using Eq. (A·1). A single wire is composed of three segments

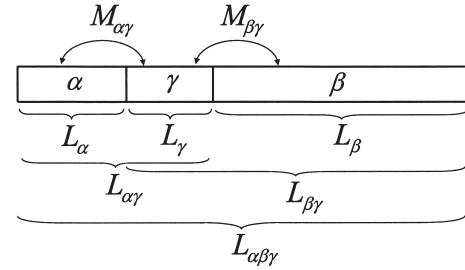


Fig. A·1 Concept to derive self-inductance of interconnects composed of three segments. The details are described in the text.

with rectangular cross section. The segments α and β are the interconnects used as the part of measurement fixture, while γ occupies the gap between the interconnects. With this model, we have the desired inductance L_p as

$$L_p = L_{\alpha\beta\gamma} - (L_\gamma + 2M_{\alpha\gamma} + 2M_{\beta\gamma}) \quad (\text{A} \cdot 2)$$

where, on the right hand side of the equation, L indicates the self-inductance of a wire and M mutual inductance between wires, respectively. The subscript on L identifies a single wire composed from each segment, while the subscript on M two segments relating to the coupling. The notation is also used in the following discussion.

The expression (A·2) can be reduced to a equation composed of single wire inductances calculated from (A·1). Using the model as shown in Fig. A·1, for the mutual inductances, We have

$$2M_{\alpha\gamma} = L_{\alpha\gamma} - (L_\alpha + L_\gamma) \quad (\text{A} \cdot 3)$$

$$2M_{\beta\gamma} = L_{\beta\gamma} - (L_\beta + L_\gamma). \quad (\text{A} \cdot 4)$$

Substituting (A·3) and (A·4) in (A·2) results in the following:

$$L_p = L_{\alpha\beta\gamma} - (L_{\alpha\gamma} + L_{\beta\gamma} - L_\alpha - L_\beta - L_\gamma) \quad (\text{A} \cdot 5)$$

where

$$L_{\alpha\beta\gamma} = \frac{\mu_0 (l_\alpha + l_\beta + d)}{2\pi} \times \left\{ \ln \left| \frac{2(l_\alpha + l_\beta + d)}{GMD} \right| - 1 \right\} \quad (\text{A} \cdot 6)$$

$$L_{\alpha\gamma} = \frac{\mu_0 (l_\alpha + d)}{2\pi} \left\{ \ln \left| \frac{2(l_\alpha + d)}{GMD} \right| - 1 \right\} \quad (\text{A} \cdot 7)$$

$$L_{\beta\gamma} = \frac{\mu_0 (l_\beta + d)}{2\pi} \left\{ \ln \left| \frac{2(l_\beta + d)}{GMD} \right| - 1 \right\} \quad (\text{A} \cdot 8)$$

$$L_\alpha = \frac{\mu_0 l_\alpha}{2\pi} \left(\ln \left| \frac{2l_\alpha}{GMD} \right| - 1 \right) \quad (\text{A} \cdot 9)$$

$$L_\beta = \frac{\mu_0 l_\beta}{2\pi} \left(\ln \left| \frac{2l_\beta}{GMD} \right| - 1 \right) \quad (\text{A} \cdot 10)$$

$$L_\gamma = \frac{\mu_0 d}{2\pi} \left(\ln \left| \frac{2d}{GMD} \right| - 1 \right). \quad (\text{A} \cdot 11)$$



Hideki Shima received the B.S. and M.S. degrees in physics from Shimane University, Shimane, Japan, in 1998 and 2000, respectively. Since 2000, he has been working towards his Ph.D. degree in electronic engineering at Osaka University. In 2005, he joined Texas Instruments Japan, Ltd., Osaka, Japan, where he is currently involved in power management IC design for portable digital consumer power products. His research interests are in passive component modeling and analog circuit design. Mr. Shima

is a member of the IEEE.



Toshimasa Matsuoka received the B.S., M.S. and Ph.D. degrees in electronic engineering from Osaka University, Osaka, Japan, in 1989, 1991 and 1996, respectively. During 1991–1998, he worked for the Central Research Laboratories, Sharp Corporation, Nara, Japan, where he was engaged in the research and development of deep submicron CMOS devices and ultra thin gate oxides. Since 1999, he has been working for Osaka University, where he is Associate Professor now. His current research in-

cludes CMOS RF circuits and device modeling. Dr. Matsuoka is a member of the Japan Society of Applied Physics, the IEEEJ, and the IEEE.



Kenji Taniguchi received the B.S., M.S. and Ph.D. degrees from Osaka University, Osaka, Japan, in 1971, 1973 and 1986, respectively. From 1973 to 1986, he worked for Toshiba Research and Development Center, Kawasaki, Japan, where he was engaged in process modeling and the design of MOS LSI fabrication technology. He was a Visiting Scientist at Massachusetts Institute of Technology, Cambridge, from July 1982 to November 1983. Presently, he is a Professor of Electronics and Information

Systems at Osaka University. His current research interests are in analog circuits, radio frequency circuits, device physics and process technology. Prof. Taniguchi is a member of the Japan Society of Applied Physics. He is a fellow of the IEEE.