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Design of a 500-MS/s stochastic signal detection circuit using a non-linearity reduction technique in a 65-nm CMOS process

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Abstract: A stochastic signal detection circuit that uses a non-linearity reduction technique is designed using a 65-nm CMOS process. The fabricated chip demonstrates the feasibility of stochastic signal detection at 500 MS/s.

Keywords: signal detection, comparator, mismatch, CMOS

Classification: Integrated circuits

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1 Introduction

As CMOS technologies are scaled down for advantages in size and speed, increased device mismatch [1] has become a more serious issue in circuit designs. The supply voltages of RF and analog circuits embedded with digital circuits will decrease to 0.5 V in the near future [2]. Although some calibration techniques have conventionally been used to overcome increasing device mismatch, the architectures of analog signal detection based on conventional A/D converters (ADCs) are approaching their limit in maintaining resolution under such a low voltage supply [3].

A completely new approach to detect a signal using statistics of device noise and mismatch has been proposed by the authors [4]. Recently, a new ADC, referred to as the stochastic ADC, has been reported [5]. It uses device mismatch based on similar architectures. This previous study demonstrates the feasibility of this approach using a 0.18- μm CMOS process, but does not show sufficient scaling advantages.

In the present letter, a signal detection circuit is presented to demonstrate the feasibility of a high-speed-sampling stochastic approach that was designed using a 65-nm CMOS process. We also demonstrate the effectiveness of a non-linearity reduction technique using this approach.

2 Stochastic signal detection

Output D_{OUT} of an ideal comparator ($\Delta_{offset} = 0$) becomes one or zero according to the inequality relation between an input value V_{IN} and the reference value V_{REF} . In a real comparator, the device mismatch, noise, and clock jitter may cause an output error for the small difference $V_{IN} - V_{REF}$, which can be modeled as an error signal Δ_{offset} added to the reference, as shown in Fig. 1 (a). The offset depends on circuit topology, device sizes, and process parameters [1]. Due to device mismatch and process variation, input-referred comparator offset is usually modeled as a Gaussian distribution, as shown in Fig. 1 (b), and their distribution can be estimated by Monte-Carlo analysis under a device mismatch model [1]. Even noises generated in the devices also can be estimated under the assumption of their Gaussian distributions [2, 4]. Thus, the mean and standard deviation of input-referred comparator offsets can be estimated and controlled to a certain extent in the circuit design.

Considering an ensemble of N identical comparators, the probability $Prob(D_{OUT} = 1)$ of obtaining D_{OUT} equal to one for an input value V_{IN} can be estimated as a cumulative distribution function of a Gaussian distribution, as shown in Fig. 1 (b), and is expressed as follows:

$$Prob(D_{OUT} = 1) = \frac{1}{2} + \frac{1}{2} \text{erf} \left(\frac{V_{IN} - V_{REF}}{\sqrt{2} \sigma_{offset}} \right) \approx \frac{n}{N}, \quad (1)$$

where n is the number of comparators for which output D_{OUT} is one. The mean and standard deviation of input-referred offset Δ_{offset} can be obtained from the input voltage giving n/N of 50% and 16 or 84%, respectively. Based

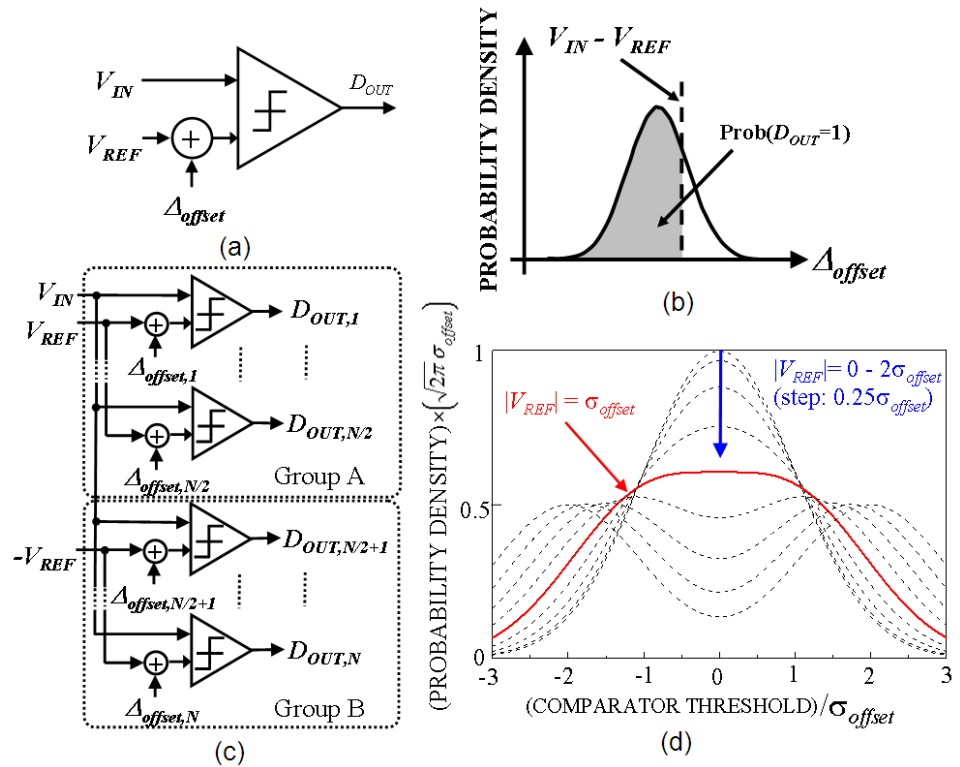


Fig. 1. (a) Comparator with input-referred offset, (b) probability density of Gaussian-distributed comparator offset, (c) two groups of comparators with shared input and different references, and (d) probability density of the comparator threshold (offset plus one of two references).

on comparator offset standard deviation σ_{offset} estimated in circuit design or experimentally as described above, the analog input voltage corresponding to n/N can be restored by operation of the inverse error function as follows:

$$V_{IN} \approx V_{REF} + \sqrt{2} \sigma_{offset} \operatorname{erf}^{-1} \left(2 \left(\frac{n}{N} - \frac{1}{2} \right) \right). \quad (2)$$

In other words, n/N represents the quantized value of the Gaussian cumulative distribution of comparator thresholds.

In conventional flash ADC architectures, in order to achieve the desired resolution, the standard variation of comparator offset must be maintained sufficiently small. On the other hand, this stochastic signal detection technique uses the comparator offset without any calibration. This feature relaxes careful considerations on the comparator offset.

In a previous study [4], we proposed a simple estimation method using two groups of comparators with similar offset distributions and different references, as shown in Fig. 1 (c), for real-time signal detection instead of using Eq. (2). In order to restore the input signal, this method uses the sum of $D_{out,i}$ (i denotes the comparator) of the two groups. Although this technique causes non-linear distortion in the restored signal, which originates in the Gaussian distribution, this distortion can be reduced by optimizing the ref-

erences. Figure 1 (d) shows the probability density of the comparator threshold (reference plus offset) in the two comparator groups, which is the sum of Gaussian distributions with mean $\pm V_{REF}$ and standard deviation σ_{offset} . For $V_{REF} = \sigma_{offset}$, the distribution of the comparator threshold approaches uniformity near zero through this technique. In this case, the non-linearity distortion originating in the comparator offset distribution can be reduced for the input signal located between the two references. This non-linearity reduction technique can be implemented by applying $\pm\sigma_{offset}$ estimated in a Monte-Carlo simulation as reference voltages. The problem caused by a difference between a simulated offset and a real value can be addressed by using a slightly wider margin for a large number of comparators [4].

3 Circuit implementation

In the present study, a high-speed-sampling signal detection circuit shown in Fig. 2 (a) is designed as a prototype using a 65-nm CMOS process. The prototype has a parallel configuration of pre-amplifiers, comparators, and D-latches as well as an adder. Unlike the conventional flash ADC, each comparator shares the reference voltage. The use of the comparator offset

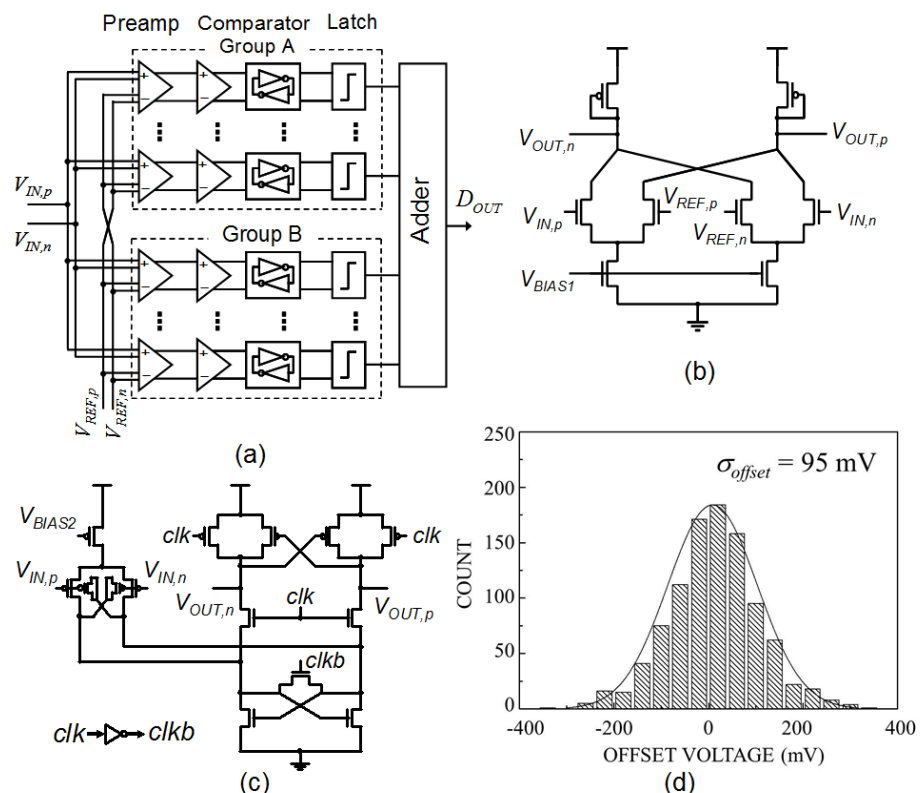


Fig. 2. (a) Architecture of proposed signal detection circuit with non-linearity reduction technique, schematic diagrams of (b) the pre-amplifier and (c) the comparator, and (d) simulated distribution of the offset of the comparators including the pre-amplifiers referred at the pre-amplifier input.

distribution to restore the input signal can eliminate the reference generator used in the conventional ADC. The high-speed-sampling feature can reduce the number of comparators through over-sampling, as mentioned in the previous study [4]. For this implementation, the number of comparators is chosen to be 512 considering the required accuracy based on the previous study [4]. Comparator outputs are followed by D-latch to maintain the outputs on the comparator sampling phase, and summed in the adder to obtain binary output data.

In the single reference case mentioned in Sec. 2, $V_{REF,p}$ and $V_{REF,n}$ in Fig. 2 (a) are the same common-mode level V_{CM} to obtain the zero differential reference. On the other hand, in the two-reference case with non-linear distortion reduction, $V_{REF,p}$ and $V_{REF,n}$ are chosen to be $V_{CM} + \sigma_{offset}/2$ and $V_{CM} - \sigma_{offset}/2$. In this case, the comparators are divided into two groups of 256 comparators with differential references of $-\sigma_{offset}$ and $+\sigma_{offset}$, respectively.

The pre-amplifiers shown in Fig. 2 (b) have low gain (Gain = 3.8 dB) and a wide bandwidth ($BW_{-3dB} = 2$ GHz) for a high-frequency signal. To reduce common noise in the parallel configuration, which degrades the S/N of the output, the comparator topology suppressing the kickback noise, as shown in Fig. 2 (c) [6], is used. Since comparator offsets that originate mainly in device mismatch are used in the present study, small devices were used. Figure 2 (d) shows the input-referred offset distribution obtained in Monte-Carlo simulation. The standard deviation of input-referred offset is expected to be quite large due to small-size transistors used in comparators and pre-amplifiers. With comparator offsets of such magnitude, sufficient resolution would be difficult in conventional circuit techniques.

4 Measurement results

A micrograph of the test chip fabricated in the 12-metal 65-nm CMOS process is shown in Fig. 3 (a). The core area is 1.44 mm^2 . DC-cut capacitors and 100Ω resistive termination for a differential input terminal are embedded on the chip. The measurements are performed with a supply voltage of $V_{DD} = 1.2 \text{ V}$ and an estimation signal amplitude of $\sigma_{offset} = 95 \text{ mV}$. The common-mode level V_{CM} is set to $V_{DD}/2$ ($= 600 \text{ mV}$). The 512 comparators can be divided into two groups of 256 comparators, and each group has a differential reference, as described in Sec. 3.

Figures 3 (b) and 3 (c) show the fast Fourier transform (FFT) spectra of the measured output data for a differential input signal with an amplitude of 200 mV (approximately $2 \sigma_{offset}$) and a frequency of 101.5625 MHz with 500 MS/s sampling. With all 512 comparators acting as a single parallel group, a spurious free dynamic range (SFDR) of 16 dB and a signal-to-noise and distortion ratio (SNDR) of 6.2 dB are achieved. When differential references of $V_{CM} \pm \sigma_{offset}/2$ are set, an SFDR of 26 dB and an SNDR of 8.7 dB are obtained. Although the post-layout simulation results predict an SFDR of 35 dB and an SNDR of 29 dB with the same two references for the same

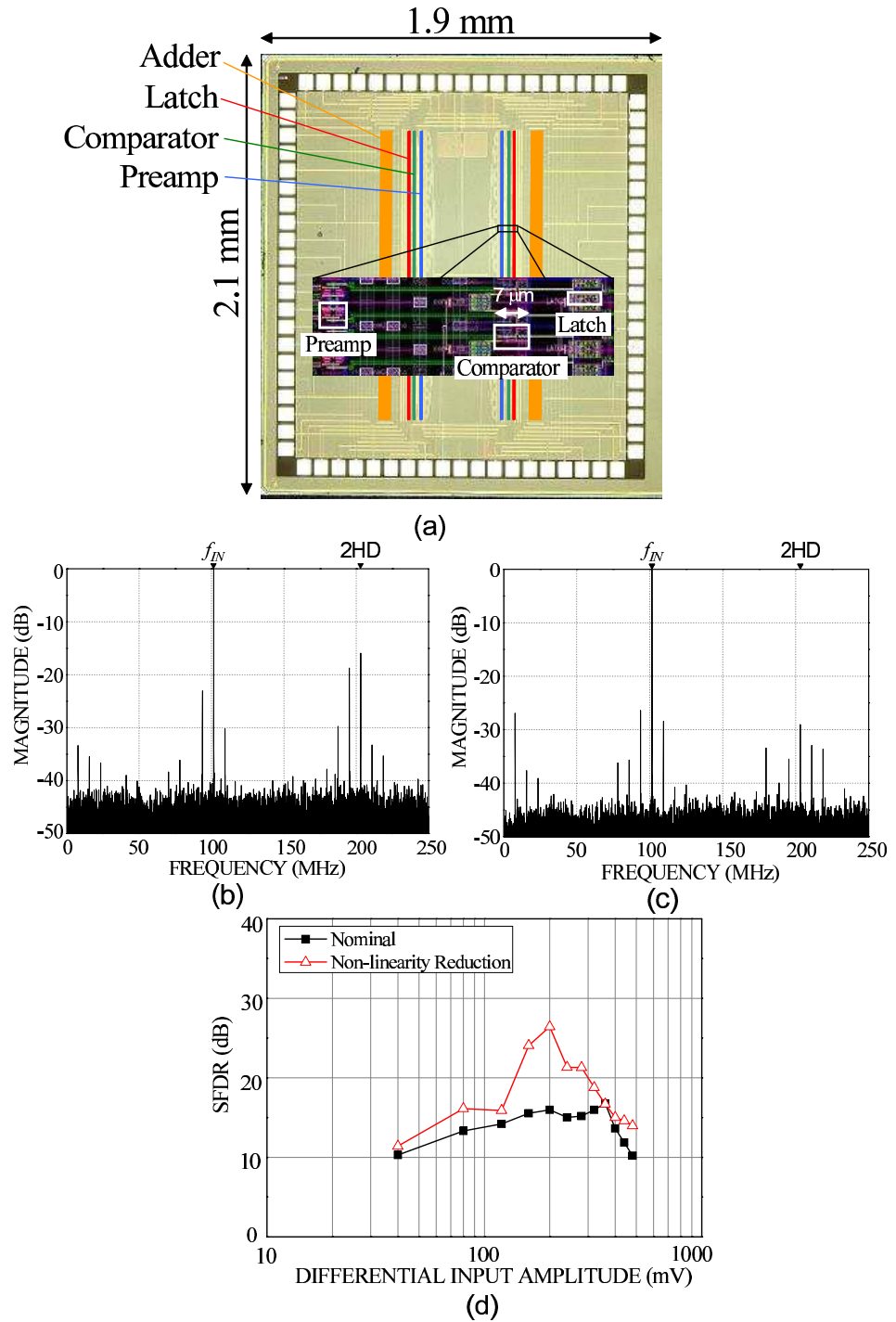


Fig. 3. (a) Microphotograph of the test chip and a screen capture of the layout. FFT spectrum of the output data (25,536 points) for $V_{IN} = 200$ mV, $f_{IN} = 101.5625$ MHz, and $f_{sampling} = 500$ MS/s using (b) the nominal ($V_{REF,p}, V_{REF,n} = V_{CM} + 0$ mV) and (c) the non-linearity reduction technique ($V_{REF,p} = V_{CM} + 45$ mV, $V_{REF,n} = V_{CM} - 45$ mV), and (d) SFDR versus differential input voltage at $f_{IN} = 101.5625$ MHz and $f_{sampling} = 500$ MS/s.

input signal at 1.6 GS/s, a large discrepancy of measured SNDR from the simulated one comes from signal integrity problem of the output buffers. Therefore, in the present letter, we focus only on the SFDR.

Figure 3 (d) shows the SFDR as a function of the differential input signal amplitude. In the single parallel group case, a maximum SFDR of 16 dB is achieved. By setting the differential references to $V_{CM} \pm \sigma_{offset}/2$, a maximum SFDR of 26 dB is achieved near the differential input amplitude of $2 \sigma_{offset}$. The harmonic distortion originating from the comparator offset distribution is reduced by 10 dB in the SFDR using the non-linearity reduction technique. The SFDR becomes better until the differential signal amplitude approaches $2 \sigma_{offset}$, not σ_{offset} . This is because the increase in the fundamental signal component is larger than the increase in harmonic distortion in this input signal amplitude range.

At 500 MS/s, this test chip consumes approximately 51 mW, including 14 mW for pre-amplifiers, 3 mW for the comparators, and 19 mW for the clock buffers. This indicates that a great deal of power is consumed in clock buffers and digital circuits (adder and D-latches) which have full swing operation. The use of small swing differential digital circuits is expected to reduce the power consumption significantly.

5 Conclusion

A high-speed-sampling stochastic signal detection circuit to use comparator offset was investigated experimentally. The high-speed feature can be enhanced using device scaling under relaxed device mismatch. Furthermore, the linearity determined by the comparator threshold distribution was enhanced just by optimizing references.

Since the present study is only a preliminary study, extensive future study is necessary. However, we believe that the present study will help to establish a new solution to the growing problem of device mismatch in nano-scale CMOS technologies.

Acknowledgments

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