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Citation	IEICE Electronics Express. 2015, 12(6), p. 20141233
Version Type	VoR
URL	<a href="https://hdl.handle.net/11094/51718">https://hdl.handle.net/11094/51718</a>
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# A low-power CMOS programmable frequency divider with novel retiming scheme

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**Abstract:** We propose a novel pulse-swallow programmable frequency divider with a D flip-flop for retiming. The proposed scheme reduces the critical delay path of the modulus control (MC) signal extending the MC timing margin. This enables the high-speed operation of the divider. Moreover, unlike the conventional retiming structure, the MC signal is set and reset by a single signal triggered reset circuitry to eliminate the unwanted division ratio offset and the possible malfunction of set-reset (SR) latch. Simulation results show that the proposed divider designed in 130-nm CMOS technology consumes 53  $\mu$ W at 1-GHz operation frequency from a 0.7-V supply voltage. The proposed divider achieves the lowest power consumption among the previously reported dividers at GHz operations.

**Keywords:** pulse-swallow, retiming, SR latch, modulus control, CMOS

**Classification:** Integrated circuits

## References

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## 1 Introduction

With the growing use of modern wireless communication systems, the demand for low-cost, low-power and wider bandwidth circuits with higher level of frequency spectrum purity has greatly increased. Phase-locked loop (PLL) based frequency synthesizer is one of the basic building blocks in modern transceiver systems. High-speed frequency divider and low-phase-noise voltage controlled oscillator (VCO) are main bottlenecks to achieve a low-voltage PLL, which limit the operating frequency of the PLL. To meet the stringent small channel spacing requirement, programmable division ratios are required for frequency synthesizer to provide VCO frequencies with finer steps from a stable low-frequency reference signal. The power consumption, operating frequency range and input sensitivity should be comprehensively considered in the process of divider design.

A conventional frequency divider in pulse-swallow configuration [1] consists of dual-modulus prescaler (DMP) with a division ratio of  $M$  or  $M + 1$  and two programmable counters, referred to as pulse (P) and swallow (S) counters as shown in Fig. 1. Channel selection is performed by changing either the P or S control words ( $P[0:N]$  and  $S[0:N]$ ) [1]. Typically the P counter is fixed and S is varied to allow selection of successive channel values. The speed of the divider is fundamentally limited by the delay time of the DMP modulus control (MC) signal,  $\tau_{MC}$ . If  $\tau_{MC}$  exceeds DMP output period, the total division ratio goes wrong and the system functionality is failed. Reducing this critical delay is the major design consideration. A set-reset (SR) latch followed by a D flip-flop to allow pipelining of the MC signal was found effective to reduce the delay path [2]. Also, employing a timing window generation by using a finite-width pulse generator was also known to be effective [3]. Nevertheless, these architectures [3, 4] inherently possess an unwanted division ratio offset of one with relative timing and the possibility of malfunction of the SR latch in the structure.

In this letter we present a pulse-swallow programmable frequency divider that resolves the problems associated with the existing architecture. Retiming both P

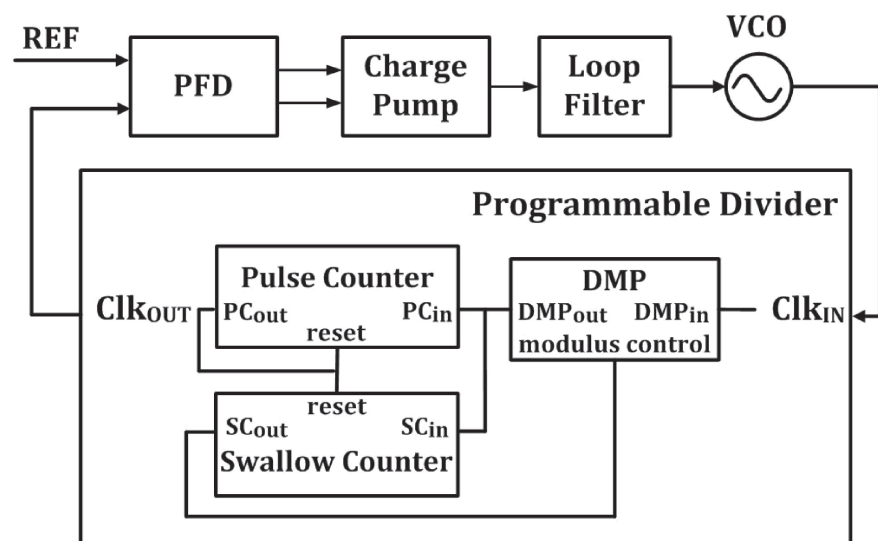


Fig. 1. Block diagram of conventional PLL.

and S counters with a D flip-flop decreases  $\tau_{MC}$  to eliminate the malfunction of the SR latch and avoid the unwanted division ratio offsets. This letter is organized as follows. In Section 2, the problems of the conventional retimed divider configuration is reviewed, and the proposed novel modified retiming scheme is described. Section 3 shows the simulation results and Section 4 draws the conclusions of this work.

## 2 Divider architecture

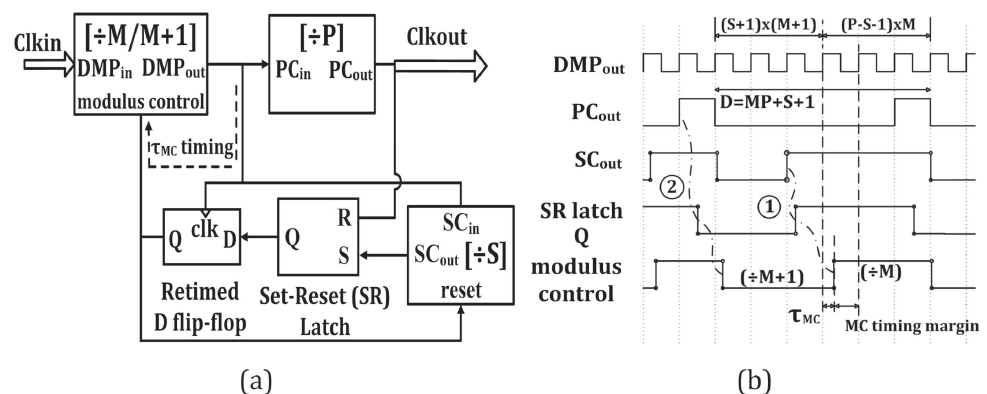
## 2.1 Conventional retiming architecture

The conventional pulse-swallow frequency divider with MC signal retiming [4] is shown in Fig. 2(a) where a SR latch is shown explicitly. It is a conventional implementation, consisting of DMP ( $\div M/M + 1$ ), P counter ( $\div P$ ), and a S counter ( $\div S$ ). The DMP begins the operation by dividing  $M + 1$  until the S counter is full. The SR latch is then set, changing the DMP division to  $M$  after the MC delay  $\tau_{MC}$  and disabling the S counter. This division continues until the P counter is full and the SR latch is reset. A D flip-flop is added to retime the MC signal. It is noted that the SR latch is modified from the standard one so that  $\overline{SC_{out}} PC_{out}$  is not allowed as a pair of inputs instead of  $SC_{out} PC_{out}$ . This divider configuration has two problems: 1) a large  $\tau_{MC}$ , 2) unwanted division ratio offset with a possible malfunction of the SR latch.

### 2.1.1 Large $\tau_{MC}$

The delay time of the MC signal ( $\tau_{MC}$ ) to switch the DMP modulus in the given timing margin of the conventional divider is determined by the critical delay path drawn by dotted line in Fig. 2(a). Fig. 2(b) shows its timing diagram, in which the outputs of the DMP ( $DMP_{out}$ ), P counter ( $PC_{out}$ ), S counter ( $SC_{out}$ ), SR latch, and D flip-flop (modulus control) are shown. Transition ① in Fig. 2(b) describes a process in which the DMP division ratio is changed from  $M + 1$  to  $M$ . After the S counter completes its counting,  $SC_{out}$  sets MC signal via SR latch and changes the DMP division ratio from  $M + 1$  to  $M$ . The MC signal changes its state after  $\tau_{MC}$  given by

$$\tau_{MC} = \tau_S + \tau_{SR} + \tau_{DFF}, \quad (1)$$



**Fig. 2.** (a) Conventional pulse-swallow divider with MC retiming and (b) its timing diagram.

where  $\tau_S$ ,  $\tau_{SR}$ , and  $\tau_{DFF}$  show the delays of S counter, the SR latch transition and D flip-flop, respectively. If  $\tau_{MC}$  becomes too large, the MC signal would not be able to switch the DMP modulus in a given timing margin which might lead to wrong division ratio. The timing margin is defined as the difference between the one clock period of the  $DMP_{out}$  and  $\tau_{MC}$ .

### 2.1.2 Unwanted division ratio offset

In the conventional divider, MC signal set and reset are triggered by different signals, i.e.,  $SC_{out}$  and  $PC_{out}$ , respectively. This causes the unwanted division ratio offset of one. Transition ② shows a process in which the DMP division ratio is changed from  $M$  to  $M + 1$  after the completion of the P counter. MC signal and  $SC_{out}$  are reset at the next rising edge of the  $DMP_{out}$ . This leads to division ratio of  $(S + 1) \times (M + 1)$  rather than  $S \times (M + 1)$ . After the completion of S counter, the  $SC_{out}$  is set, and MC signal is set at the next rising edge of the  $DMP_{out}$  as illustrated in the transition ①. Thus, the division ratio in the next duration is given by  $(P - S - 1) \times M$ . Thus, the total division ratio,  $D$  is given by

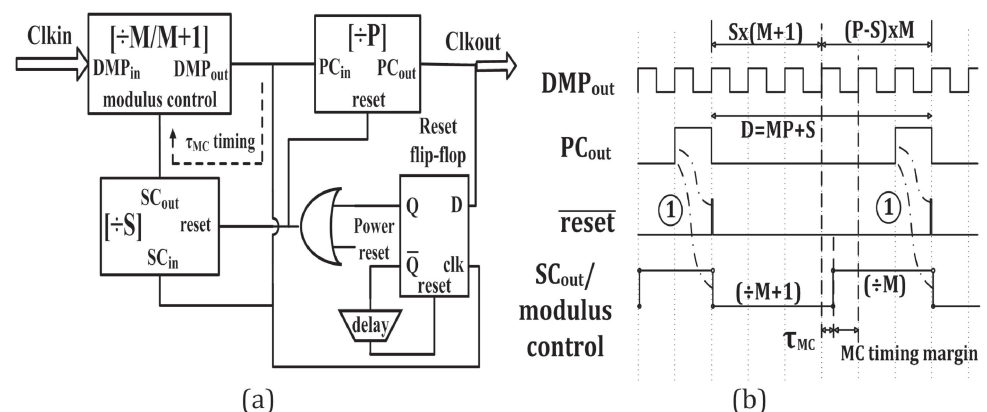
$$D = (S + 1) \times (M + 1) + (P - S - 1) \times M = MP + S + 1. \quad (2)$$

It indicates that  $D$  has an offset of one greater than the original setting value complicating the selection of control words for counters.

## 2.2 Proposed novel modified retiming scheme

The proposed architecture employs a  $D$  flip-flop to retime the divider, as shown in Fig. 3(a). Unlike conventional complex reset circuitry with a SR latch and flip-flop, we trigger the set and reset of the divider using a single signal, i.e.,  $PC_{out}$ . The reset circuitry is designed through tapping the divider output  $Clk_{out}$  and feeding it as input to the D flip-flop clocked with  $DMP_{out}$ . An OR gate, which is placed between the output of the Reset flip-flop (D flip-flop) and the reset signal of the counters, is used to turn off the whole divider as an external power reset.

Fig. 3(b) shows its timing diagram, in which  $SC_{out}$  is identical to MC signal, and  $\overline{reset}$  represents the output of the OR gate which resets the counters. Initially, the DMP divides the  $Clk_{in}$  by  $M + 1$ . After S pulses of the DMP output, the S counter ( $SC_{out}$ ) changes the modulus of the DMP from  $M + 1$  to  $M$ . Differently



**Fig. 3.** (a) Proposed architecture using modified retiming scheme and (b) its timing diagram.

from the conventional retiming scheme architecture shown in Fig. 2,  $\tau_{MC}$  of the proposed divider is given by

$$\tau_{MC} = \tau_S, \quad (3)$$

which is determined by only the delay of the S counter  $\tau_S$  and is shorter than that of the conventional retiming scheme architecture shown in Eq. (1). At the same time, the P counter has also counted S pulses of DMP or  $S \times (M + 1)$  cycles. It then counts remaining  $(P - S)$  pulses of DMP output corresponding to  $(P - S) \times M$  cycles and outputs a cycle of  $Clk_{out}$ . From the above analysis, the division ratio of the proposed divider is given by

$$D = S \times (M + 1) + (P - S) \times M = MP + S, \quad (4)$$

which thus eliminates the unwanted division ratio offset.

Transition ① in Fig. 3(b) describes a process in which the division ratio of DMP changes from  $M$  to  $M + 1$ . To ensure that the reset signal for P and S counters is removed before the next clock cycle, the reset signal is fed back to its generating D flip-flop through a delay chain, as shown in Fig. 3(a). Its delay is longer than the time required to reset all the flip-flops so that it guarantees that all the flip-flops are reset and revokes the signal. On the clock cycle immediately following  $Clk_{out}$  high, the pulse is sampled by the D flip-flop, which generates the reset signal for both P and S counters as well as asserts the MC signal. The relative timing of the P and S counters is eliminated because all the falling edges of the P counter, S counter and reset signal of the divider occur on the same clock cycle. This reduces the chance of the wrong division ratio.

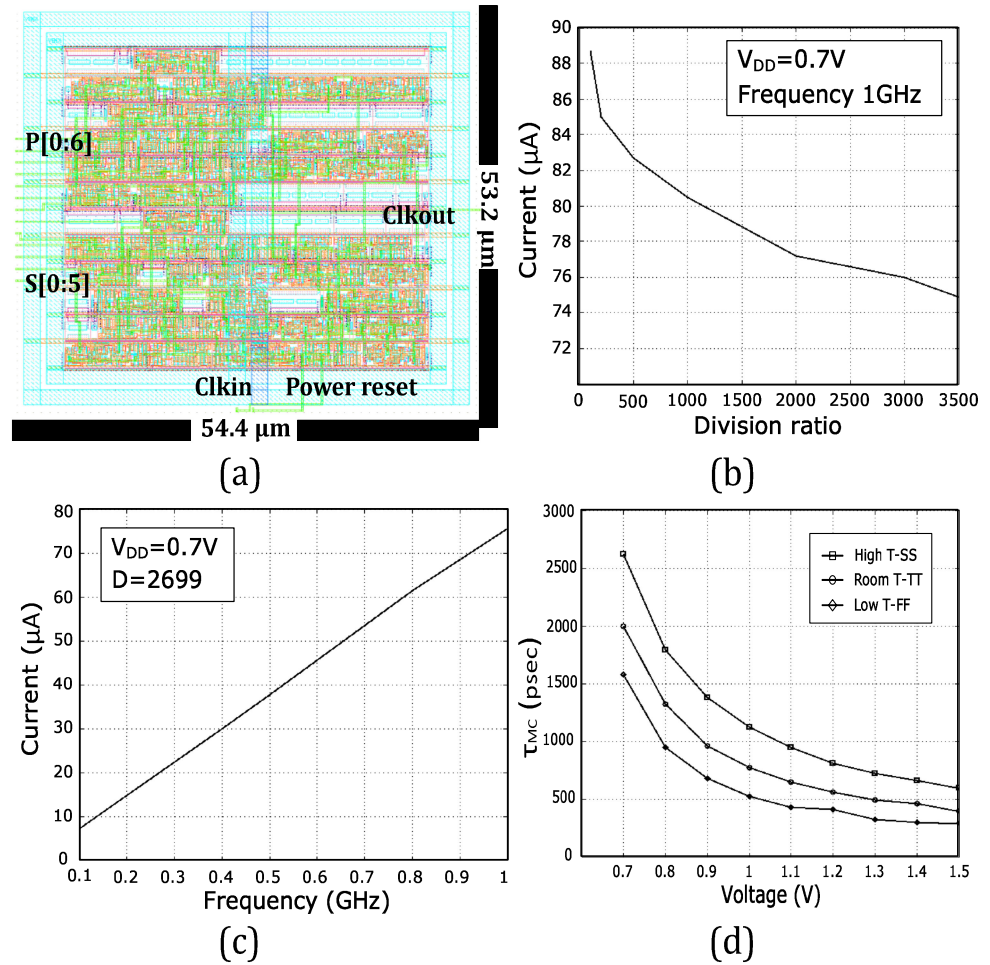
### 3 Simulation results and discussion

The proposed novel retimed frequency divider is designed in 130-nm CMOS standard cells to demonstrate its functionality. For low-power operation, the supply voltage is set to be 0.7 V. The chip area of the proposed retimed divider is  $54.4 \mu\text{m} \times 53.2 \mu\text{m}$  as shown in Fig. 4(a). Simulations are performed by Cadence Spectre circuit simulator including parasitic capacitances based on the physical layout shown in Fig. 4(a).

The division ratio of the DMP is set to 32/33, i.e.,  $M = 32$ . The 7-bit P counter and 6-bit S counter are designed as down counters with active low logic to count the setting code value and the zero state count corresponding to the counters reset operation. By setting codes of  $P[0:6](= P - 1)$  and  $S[0:5](= S - 1)$ , division ratios of  $P$  and  $S$  are determined. The typical settings are  $P[0:6] = 82$  and  $S[0:5] = 42$ , which correspond to  $P = 83$  and  $S = 43$ . In this typical case,  $D = 2699$ .

As the division ratio increases, the current consumption of the divider decreases as shown in Fig. 4(b). Fig. 4(c) shows the simulated current consumption of the retimed divider. As the operating frequency increases, the current increases due to charging and discharging parasitic capacitances. Fig. 4(d) shows  $\tau_{MC}$  of the proposed retimed architecture with dependency on the supply voltage under the process corners of the slow/typical/fast and temperature variation of  $-40/27/120^\circ\text{C}$ .





**Fig. 4.** (a) Physical layout, (b) division ratios versus current consumption at 1 GHz operation, and (c) operating frequency versus current consumption ( $D = 2699$ ) of the designed retimed divider, and (d)  $\tau_{MC}$  of the designed retimed divider ( $D = 2699$ ) shown in Fig. 3(a)

Table I shows the simulated performance of the proposed divider compared with previously published dividers at similar frequency and supply voltage. At 0.7-V supply voltage, the proposed divider consumes 53  $\mu\text{W}$  power at 1-GHz operating frequency. The figure of merit (FOM) used to compare the results is defined as the power consumption at the operating frequency. The proposed divider has FOM of 53 nW/MHz and an operating frequency range of 100 MHz–1 GHz.

To compare the proposed architecture with the previous reports, the MC delay  $\tau_{MC}$  normalized by the maximum operation frequency ( $f_{op,max}$ ) is used. The value of  $\tau_{MC}f_{op,max}$  of the modified retimed scheme is smaller than the conventional retimed architectures [4, 5] at similar conditions (supply voltages). Through modified retiming scheme, the normalized MC delay is approximately improved by four times when compared to retimed divider architecture [4] designed in 180-nm CMOS process at 1.8-V supply.

**Table I.** Simulated performance comparison of frequency dividers

	[4]	[5]	[6]	[7]	This work
Technology [nm]	180	180	180	130	130
Supply Voltage [V]	1.8	1.8	1.5	0.7	0.7
Power Consumption [ $\mu$ W]	–	3010	3200	210	53
Frequency [GHz]	4.5–9	0.5–3.5	1.7	0.2–1	0.1–1
$\tau_{MC}$ [psec]	200 (@1.8 V)	–	–	–	2000 (400-@1.5 V)
$\tau_{MC}f_{op,max}$	1.8	–	–	–	2 (0.4-@1.5 V)
FOM [nW/MHz]	–	860	1880	247	53

#### 4 Conclusion

A programmable pulse-swallow frequency divider with novel modified retiming scheme is proposed in this work. The MC signal retiming reduces the MC delay  $\tau_{MC}$ , providing higher operating speed. Unlike conventional structures, simple reset circuitry using a D flip-flop is presented. Simulation results show that the proposed divider has smaller  $\tau_{MC}$  with low power consumption and that the normalized MC delay is approximately improved by four times compared to the previously published designs at similar conditions. The proposed divider designed in 130-nm CMOS technology consumes 53  $\mu$ W at 1-GHz operation frequency from a 0.7-V supply voltage.

#### Acknowledgments

The IC in this study is designed as part of the chip fabrication program of the VDEC at the University of Tokyo in collaboration with Cadence Design Systems. In addition, the authors would like to thank also SPChange, LLC. for their technical support.