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Citation	IEICE Transactions on Electronics. 2008, E91-C(8), p. 1375-1378
Version Type	VoR
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LETTER

Design of a 0.5 V Op-Amp Based on CMOS Inverter Using Floating Voltage Sources

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SUMMARY This letter presents a 0.5 V low-voltage op-amp in a standard 0.18 μm CMOS process for switched-capacitor circuits. Unlike other two-stage 0.5 V op-amp architectures, this op-amp consists of CMOS inverters that utilize floating voltage sources and forward body bias for obtaining high-speed operation. And two improved common-mode rejection circuits are well combined to achieve low power and chip area reduction. Simulation results indicate that the op-amp has an open-loop gain of 62 dB, and a high unity gain bandwidth of 56 MHz. The power consumption is only 350 μW.

key words: *operational amplifier, CMOS inverter, floating voltage source, forward body bias*

1. Introduction

Digital compatibility in low-voltage, low-power mixed-signal IC design will force analog circuits to operate with supply voltage close to the transistor threshold voltage V_{TH} in the near future. The supply voltage for low-power digital circuits is predicted to drop to 0.5 V within the next few decades [1], and at the same time, V_{TH} needs to remain as a relatively large constant to keep the off transistor leakage within tolerable limits [2]. As a result, a large V_{TH} at low supply may force the transistor to operate in weak inversion, thereby inducing poor performance of analog circuits, such as low operation speed. Several 0.5 V CMOS operational amplifiers (op-amps) designed in standard V_{TH} devices have been recently reported [3]–[5]. However, small unity gain bandwidths limit their applications to below a sampling frequency of 10 MHz.

In this letter, we take advantage of CMOS inverter's high transconductance and good compatibility with digital circuits, as well as utilize floating voltage sources and forward body bias for obtaining high-speed operation. At the same time, the following problems in CMOS inverter are improved; (i) no accurate control of the quiescent current, (ii) poor common-mode rejection in differential applications, and (iii) difficulty in control of the output DC common-mode voltage to maintain a constant voltage, such as $V_{DD}/2$. A high performance 0.5 V op-amp based on CMOS inverters is designed, which has high unity gain bandwidth at low-power consumption in comparison with other works.

Manuscript received February 14, 2008.
Manuscript revised April 3, 2008.

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DOI: 10.1093/ietele/e91–c.8.1375

2. Proposed Op-Amp

Figure 1 shows the proposed two-stage op-amp which mainly consists of four 0.5 V CMOS inverters using switched-capacitor floating voltage sources (SC-FVS), and two common-mode rejection circuits denoted CMR1 and CMR2. Bodies of the NMOS transistors in the inverters are employed as common-mode feedback terminals, V_{cmfb}, to provide accurate control of the output DC common-mode voltage, independent of variations in process and temperature. There is no risk for latch-up in the circuit when operating at a 0.5 V power supply. Note that this technique requires triple-well CMOS structure.

2.1 0.5 V CMOS Inverter Using Floating Voltage Sources

For a 0.5 V supply, the DC common-mode voltage is set to $V_{CM} = V_{DD}/2$, that is, 250 mV. In order to avoid the weak inversion operation of PMOS and NMOS transistors in the CMOS inverter, a level shifting technique with floating voltage sources (FVS) [6]–[8] is introduced to increase the gate-source voltage $|V_{GS}|$, and thereby achieve high-speed operation. Figure 2(a) shows the increased $|V_{GS}|$ by V_b using FVS circuits.

The implementation of the FVS in Fig. 2(a) had been discussed in [7], [8]. However, all of those circuits were operated at a supply voltage V_{DD} over 1V, not designed for

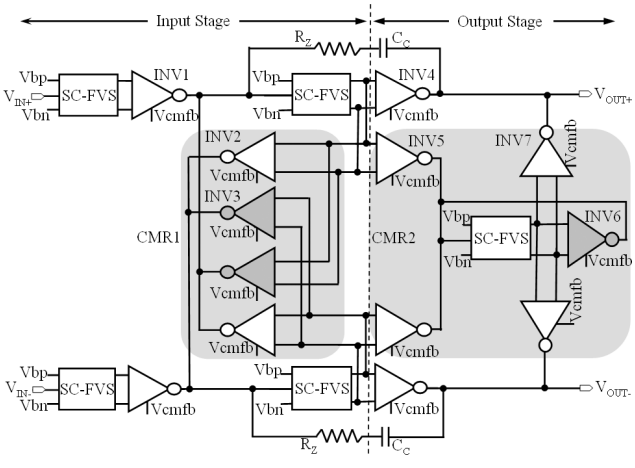

Fig. 1 Proposed op-amp.

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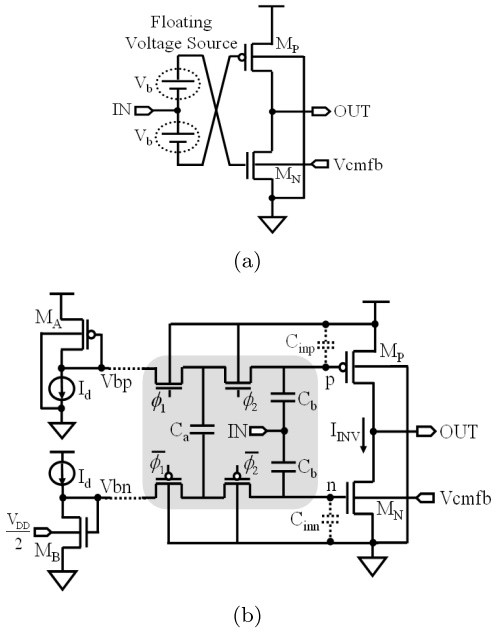

Fig. 2 (a) CMOS inverter using FVS and (b) circuit implementation.

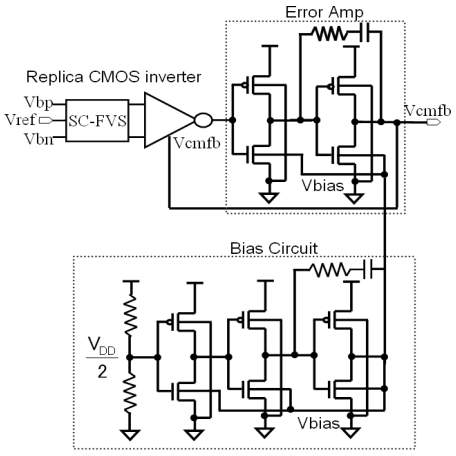

Fig. 3 Common-mode voltage adjustment circuits.

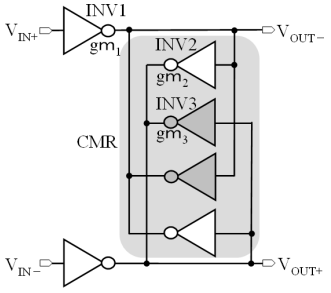

Fig. 4 Transconductor based on CMOS inverters [6].

0.5 V operation. Figure 2(b) provides the circuit implementation of a 0.5 V CMOS inverter using SC-FVS. This SC-FVS circuit increases the gate-source voltage of the transistor M_P and M_N by V_b ($V_b = V_{CM}–V_{bp} = V_{bn}–V_{CM}$). At the same time, forward biased body terminals lower the V_{TH} by approximately 100∼150 mV. Thus, transistors M_P and M_N are forced to operate in the moderate or even strong inversion region ($|V_{GS}| \geq V_{TH}$) even under 0.5 V supply.

As shown in the shaded area in Fig. 2(b), the body terminals of the NMOS and PMOS switches are forward biased, which allows these switches to operate at 0.5 V supply, thereby to provide gate bias voltage for the CMOS inverter. The diode connected transistors M_A, M_B and the current sources provide accurate control of the quiescent current [7] $I_{INV} = I_d(W_{M_P}/W_{M_A})$. All switches are controlled by nonoverlap clocks ϕ_1 ($\overline{\phi_1}$) and ϕ_2 ($\overline{\phi_2}$). Each switching cycle refreshes the capacitors C_b, which keep the voltage difference, $V_{bn}–V_{bp}$, between the inverter input nodes 'n' and 'p.'

A gain degradation is induced by the parasitic capacitance C_{inp} and C_{inn} shown in Fig. 2(b). This gain degradation, equal to $C_b/(C_b + C_{in})$ (assume $C_{inp} = C_{inn} = C_{in}$), can be reduced by the use of the large C_b. The large C_b also alleviates the effect of charge injection during switching. However, large capacitors may also cause area penalty as well as lower operation speed. Therefore, we adopted C_b with the size of above 10 times that of C_{in} while keeping the gain degradation less than 1 dB.

2.2 Setting Output DC Common-Mode Voltage

A replica 0.5 V CMOS inverter and error amplifier [4], shown in Fig. 3, are employed to provide the common-mode feedback voltage for the CMOS inverters shown in Fig. 2. NMOS rather than PMOS devices are chosen for DC common-mode adjustment, which can reduce the total MOS device size. This technique can set the output DC common-mode voltage to $V_{DD}/2$, independent of variations in process and temperature. Also note that the PMOS and NMOS transistors of each inverter need not be carefully sized.

2.3 Common-Mode Rejection Circuits

Common-mode rejection circuits, CMR1 and CMR2, shown in Fig. 1 are well combined in the proposed op-amp to achieve low power and small chip area occupation. Figure 4 shows the original concept of CMR1 circuit consisting of four inverters [6]. The input/output shorted inverters stabilize the common-mode level. Given the total transconductance of INV2 and INV3 under saturation operation, g_{m2} and g_{m3}, the common and differential load resistances seen at output nodes $V_{OUT\pm}$ are approximately $1/(g_{m3}+g_{m2})$ and $1/(g_{m3}–g_{m2})$, respectively [6]. Thereby, the common-mode rejection ratio (CMRR) is given approximately by

$$CMRR \approx \frac{1/r_{tot} + (g_{m3} + g_{m2})}{1/r_{tot} + (g_{m3} - g_{m2})}, \quad (1)$$

where r_{tot} represents the output resistance of inverters at the nodes $V_{OUT\pm}$. This equation indicates that the differential DC gain and CMRR are significantly affected by $g_{m3}–g_{m2}$, and their values become infinite when $g_{m3}–g_{m2} = -1/r_{tot}$ in

theory.

For low-voltage applications, the inverters in Fig. 4 are replaced by the 0.5 V CMOS inverters with SC-FVS blocks shown in Fig. 2(b). As shown as the input stage in Fig. 1, in this work, only four SC-FVS blocks are required, in comparison with those of six required in [7], which also decreases the parasitic capacitances at output node of INV1. At the same time, the feedforward common-mode rejection circuit CMR2 [9] is employed in the output stage to provide large output swing, as well as to allow INV2∼INV5 and their opposite-side inverters to share the same SC-FVS blocks. As a result, only five SC-FVS blocks are required in Fig. 1. This feature enables a small occupation area in comparison even with that of the one-stage structure in [7].

3. Simulation Results

The proposed op-amp is designed in 0.18 μm CMOS process with standard 0.5 V V_{TH} devices. The floating voltage source, V_b, shown in Fig. 2(a) is set to approximately 150 mV. The floating capacitors, C_b of 2pF, are utilized in such a way to balance the influence of the parasitic capacitances and area occupation. Table 1 shows the width of transistors used in the inverters with gate length of 360 nm.

As shown in Table 1, the width of the transistors in INV2 and INV3 in Fig. 1 are set to 1/4 times those of INV1, to reduce power consumption in CMR1, as well as to avoid significant degradation of CMRR based on Eq. (1). Eq. (1) also indicates that the width of the transistors in INV3 should be designed to be slightly smaller than that in INV2 to increase the differential DC gain by about 10 dB. The width of the transistors in INV5 and INV6 are set to 1/3 and 2/3 times that of INV4, respectively, while INV7 has the same size as INV4, in order to maintain a large drivability. The total power consumption is approximately 350 μW. The improved common-mode rejection topology reduces the number of SC-FVS blocks to only five, resulting in a chip area reduction in comparison with [7].

Figure 5 shows the transient response of a single 0.5 V CMOS inverter with SC-FVS (all nodes' initial voltages are 0V at time = 0 s). For an input DC voltage of $V_{DD}/2$ shown in Fig. 2(b), the voltages at nodes 'p' and 'n,' V_p and V_n, reach 100 mV and 400 mV, respectively, and the output voltage V_{out} reaches 250 mV rapidly (nonoverlap clock ϕ_1, ϕ_2 is 10 MHz).

Figure 6 shows the differential and common-mode gain characteristics of the proposed op-amp, in which the CMRR maintains a relatively high level even in the high frequency range.

Figure 7 indicates the corner simulation results of the proposed op-amp. Under typical conditions (TT, 25°C), the op-amp has an open loop DC gain up to 62 dB, a unity gain bandwidth of 56 MHz and a phase margin of 60° with a 20pF load. The curves denoted 'ff' and 'ss' indicate the simulation results under fast (FF, −25°C) and slow (SS, 75°C) conditions, respectively. The main characteristics of the proposed op-amp, compared with those of other 0.5 V op-amp designs are summarized in Table 2. It can be seen that the figure-of-merit η [4] is improved, which indicates that a

Table 1 Device sizes in the proposed op-amp in Fig. 2.

Device	W_P/W_N
INV1	5 μm×12/4.2 μm×12
INV2	5 μm×3/4.2 μm×3
INV3	4.2 μm×3/3.6 μm×3
INV4, INV7	5 μm×24/4.2 μm×24
INV5	5 μm×8/4.2 μm×8
INV6	5 μm×16/4.2 μm×16
R_Z, C_C	2.2k Ω, 4pF

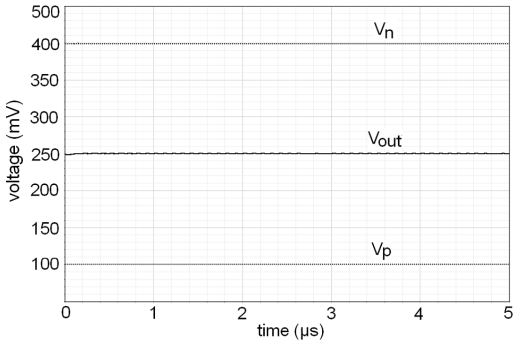

Fig. 5 Transient response of a 0.5 V CMOS inverter using FVS. (f_{CLK} = 10 MHz)

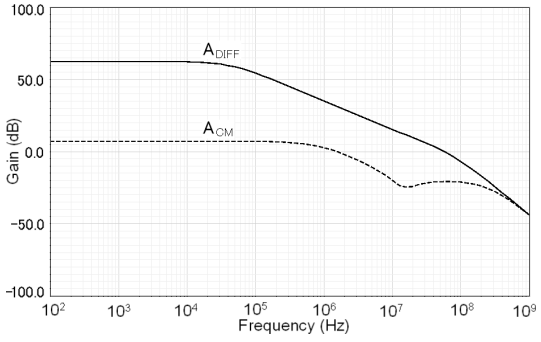

Fig. 6 Differential and common-mode gain.

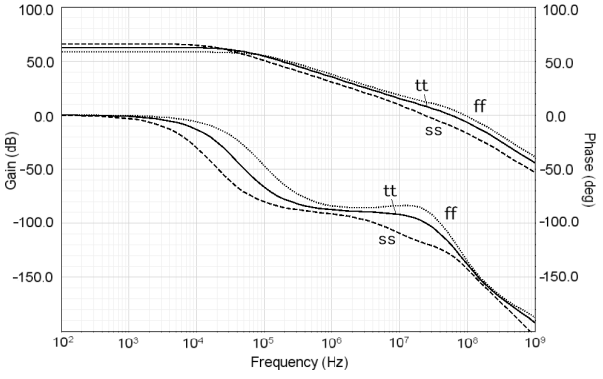

Fig. 7 Corner simulations of the proposed op-amp in open loop.

Table 2 Comparison with other 0.5 V designs [3], [4].

Parameter	Ref. [4] Body Input	Ref. [4] Gate Input	Ref. [3]	This Study
Supply [V]	0.5	0.5	0.5	0.5
DC Gain [dB]	48	72	>61	62
GBW [MHz]	2.4	15	41	56
CMRR [dB]	78	85	48	55
Load C_L [pF]	20	20	10	20
Power [μW]	100	100	510	350
$100\eta*$ [1/V]	24	150	40	160

$*\eta = \frac{GBW \cdot C_L \cdot V_{DD}}{Power}$ [4]

high unity gain bandwidth op-amp is achieved at a very low power consumption.

4. Conclusion

A 0.5 V op-amp based on CMOS inverters is proposed, which utilizes switched-capacitor floating voltage source and forward body bias to increase the gate-source voltage of transistors, thereby achieving high-speed operation. Two improved common-mode rejection circuits are well combined for obtaining low power and chip area reduction. Simulation results indicate a high unity gain bandwidth of 56 MHz with a load of 20pF at power consumption of only 350 μW. The effectiveness is certified by an improved figure of merit η in comparison with other op-amp designs.

Acknowledgments

This work is supported by the Semiconductor Technology Academic Research Center (STARC), the Japan Society for the Promotion of Science (JSPS) Global COE Program "Center for Electronic Device Innovation," and the VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc. and Cadence design systems, Inc.

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