SUMMARY An ultralow power constant reference current circuit with low temperature dependence for micropower electronic applications is proposed in this paper. This circuit consists of a constant-current subcircuit and a bias-voltage subcircuits, and it compensates for the temperature characteristics of mobility $\mu$, thermal voltage $V_T$, and threshold voltage $V_{TH}$ in such a way that the reference current has small temperature dependence. A SPICE simulation demonstrated that reference current and total power dissipation is 97.7 nA, 1.1 $\mu$W, respectively, and the variation in the reference current can be kept very small within $\pm$4% in a temperature range from $-20$ to $100\degree C$.

key words: CMOS, reference, subthreshold, weak inversion, low power, temperature dependence

1. Introduction

One of the promising areas of research in microelectronics is the development of ultralow power analog LSIs that consist of subthreshold MOSFETs, or MOSFETs that are operated in the region of weak inversion. To construct such LSIs, we must first develop voltage and current references that can operate with low-power dissipation of a few micro watts or less. We herein describe one such low power reference, a current reference that uses a subthreshold MOSFET in the subthreshold region. The purpose of this work is to operate in the linear and saturation regions. Resistors are not used. However, the circuit is not enough for the discussion on the temperature dependence on its output reference current. The circuit is not enough to use as a reference current under an environment where the temperature changes because the output current that they proposed increases proportionally as the temperature increases (see Appendix).

There are few reports on the premise of operating in the subthreshold region. The purpose of this work is to offer a design method for a constant current reference circuit that works at the subthreshold region over a large temperature range. This paper is organized as follows: circuit configurations and operation principles are described in Sect.2, simulation results are presented in Sect.3, and we conclude the paper in Sect.4. Note that all the simulations were performed using SPICE BSIM3 level 49 model and 0.25 $\mu$m TSMC-CMOS parameters.

2. Circuit Configuration

The current reference circuit we describe consists of a constant-current subcircuit and a bias-voltage subcircuit. The latter supplies a bias voltage to the former.

2.1 Constant-Current Subcircuit

Figure 1(a) shows the constant current subcircuit. It is based on the $\beta$-multiplier self biasing circuit (Fig.1(b)) and uses a MOS resistor $M_R$ instead of an ordinary resistor $R$. We operate all MOSFETs in this circuit in the weak-inversion region except for the MOS resistor in the strong-inversion and triode region. This circuit has two advantages compared with the basic $\beta$ multiplier: the first is that it needs no resistor of high resistance that occupies a large area on an LSI chip, and the second is that it can achieve a zero temperature coefficient of current for an appropriate bias voltage $V_{BIAS}$ for the MOS resistor. This circuit works as follows.
where \( \alpha \) are the same, Eq. (3) can be rewritten as

\[
I = KL_0 \exp \left( \frac{V_{GS} - V_{TH} - V_{OFF}}{\eta VT} \right) \tag{1}
\]

\[
I_0 = \mu COX V_T^2 (\eta - 1),
\]

where \( K \) is the aspect ratio (=channel width/channel length), \( \mu \) is the mobility, \( COX \) is the gate-oxide capacitance, \( V_T \) is the thermal voltage \( (V_T = k_B T/q) \), \( \eta \) is the subthreshold swing parameter, \( V_{TH} \) is the threshold voltage, \( V_{OFF} \) is the offset voltage difference between the threshold voltage in the strong inversion and that in the subthreshold region, and \( I_0 \) is called the pre-exponential factor. Voltage \( V_{OFF} \) depends on the channel width and can be given by

\[
V_{OFF} = V_{OFF0} + \frac{V_{OFFW}}{W},
\]  
where \( V_{OFF0} \) is the large-channel-width offset voltage, \( V_{OFFW} \) is a positive coefficient, and \( W \) is the channel width.

In the circuit in Fig. 1(a), the gate-source voltage \( V_{GS,A} \) in transistor \( M_A \) must be equal to the sum of the gate-source voltage \( V_{GS,B} \) in \( M_B \) and the drain-source voltage \( V_{DS} \) in \( M_R \), or

\[
V_{GS,A} = V_{GS,B} + V_{DS}.\tag{3}
\]

Because the currents \( I \) through the transistors \( M_A \) and \( M_B \) are the same, Eq. (3) can be rewritten as

\[
V_{DS} = \alpha_{A,B} + \eta V_T \ln \left( \frac{K_B}{K_A} \right),\tag{4}
\]

where \( \alpha_{A,B}(= V_{OFFA} - V_{OFFB}) \) is the difference in the offset voltages, and \( K_A \) and \( K_B \) are the aspect ratios of transistors \( M_A \) and \( M_B \). The resistance \( R_{M_R} \) of MOSFET \( M_R \) operated in the triode region is given by

\[
R_{M_R} = \frac{1}{\mu COX \left( \frac{W}{L} \right)(V_{BIAS} - V_{TH})}.\tag{5}
\]

We find from Eqs. (1),(2),(4), and (5) that the current \( I \) through \( M_A \) and \( M_B \) is given by

\[
I = \frac{V_{DS}}{R_{M_R}} = \left( \alpha_{A,B} + \eta V_T \ln \left( \frac{K_B}{K_A} \right) \right) \times \mu COX \left( \frac{W}{L} \right)(V_{BIAS} - V_{TH}).\tag{6}
\]

The subthreshold MOS current [3],[4] for a drain-source voltage \( V_{DS} \) higher than 0.1 V is given by

\[
I = KI_0 \exp \left( \frac{V_{GS} - V_{TH} - V_{OFF}}{\eta VT} \right) \tag{1}
\]

\[
I_0 = \mu COX V_T^2 (\eta - 1),
\]

Because the currents \( I \) through \( M_A \) and \( M_B \) is given by

\[
V_{OFF} = V_{OFF0} + \frac{V_{OFFW}}{W},
\]

where \( V_{OFF0} \) is the large-channel-width offset voltage, \( V_{OFFW} \) is a positive coefficient, and \( W \) is the channel width.

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\]
2.3 Bias-Voltage Subcircuit

The next part is to construct a subcircuit that supplies bias voltage $V_{BIAS}$ to the constant-current subcircuit. This bias-voltage subcircuit must generate a constant voltage that is independent of temperature. Although a bandgap reference circuit [5] is widely used to obtain a constant voltage, it is not suitable for our purpose because, for low-current operation in the subthreshold region, it needs large resistors of high resistance. However, Buck and others proposed a new CMOS bandgap reference circuit without resistors [6]. We modified their circuit to operate in the subthreshold region and to generate a bias voltage for the constant-current subcircuit.

Figure 3 shows the circuit configuration. The circuit consists of two diode-connected transistors (MD1, MD2) and $n$ differential pairs (M1-M2, M3-M4, ..., M2n-1-M2n) connected in a cascade. We set the aspect ratios of transistors such that

$$K_{D1} > K_{D2},$$
$$K_1 > K_2,$$
and $K_2 > K_{2i-1} \ (i = 2, 3, \ldots, n).$  \ (11)

The circuit produces a constant voltage on the output terminal $V_{REF}$. The output voltage is equal to the sum of the voltage across MD2 and the gate-to-gate voltages of the differential pairs. As shown later, the $V_{REF}$ voltage shows a negative TC, whereas the gate-to-gate voltages show a positive TC; this enables us to generate a zero-TC voltage.

The details of the circuit operation are as follows. The diode-connected MOSFETs MD1 and MD2 are operated in the subthreshold region, and their gate-source voltages $V_{GS,D1}$ and $V_{GS,D2}$ are given by

$$V_{GS,Di} = V_{TH} + V_{OFF,Di} + \beta V_T \ln \left( \frac{I_B}{K_{Di}I_0} \right)$$
(i = 1, 2),  \ (12)

where $I_B$ is the current through the MOSFETs. The temperature coefficient of this gate-source voltage is given by

$$\frac{\partial V_{GS,Di}}{\partial T} = \frac{\partial V_{TH}}{\partial T} + \frac{\beta V_T}{T} \ln \left( \frac{I_B}{K_{Di}I_0} \right)$$

The bias voltage circuit. It consists of two diode-connected transistors and $n$ differential pairs.

Fig. 3

This equation includes $I_0$, but the temperature dependence of $I_0$ can be ignored because $I_0$ is contained in a logarithmic function. For ordinary MOSFET parameters, the gate-source voltage across MD2 shows a negative TC.

The difference $\Delta V_{GS,D}$ of the gate-source voltages in MD1 and MD2 can be expressed as

$$\Delta V_{GS,D} = V_{GS,D2} - V_{GS,D1} = \beta_{D2,Di} + \beta V_T \ln \left( \frac{K_{Di}}{K_{D2i}} \right),$$
\ (14)

where $\beta_{D2,Di} = (V_{OFF,D2} - V_{OFF,Di})$ is the positive offset voltage as shown in Fig. 4. This voltage difference is applied to the left differential pair M1-M2. The resultant currents $I_1$ and $I_2$ in the differential pair are given by

$$I_i = K_i I_0 \exp \left( \frac{V_{GS,Di} - V_S - V_{OFF,i} - V_{TH}}{\eta V_T} \right),$$
\ (i = 1, 2)

where $V_S$ is the common source node voltage of the differential pair. Current $I_2$ is copied into $I_4$ of the next differential pair. Because the currents in transistors M3 and M4 are $I_1$ and $I_2$, the gate-source voltages $V_{GS,3}$ and $V_{GS,4}$ are given by

$$V_{GS,3} = V_{TH} + V_{OFF,3} + \eta V_T \ln \left( \frac{I_1}{K_3 I_0} \right)$$
\ (16)

and

$$V_{GS,4} = V_{TH} + V_{OFF,4} + \eta V_T \ln \left( \frac{I_2}{K_4 I_0} \right).$$
\ (17)

The gate-to-gate voltage $\Delta V_{GG}$, or the difference of the gate-source voltages ($\Delta V_{GG} = V_{GS,3} - V_{GS,4}$) in the differential pair M3-M4 is given by

$$\Delta V_{GG} = \beta_{3,4} + \beta V_T \ln \left( \frac{K_3 I_1}{K_4 I_2} \right),$$
\ (18)
where
\[ \beta = \beta_{D2,I1} + \beta_{2,1} + \beta_{3,4}. \]  

We set the aspect ratios such that
\[ K_4K_1K_{D2} > K_3K_2K_{D1}, \]  
then \( \Delta V_{GG} \) shows a positive TC. In the same way, the successive differential pairs generate their gate-to-gate voltages. These voltages are added together in the array of the differential pairs. The output of the circuit is the sum of \( V_{GS,D2} \) and the total of the gate-to-gate voltages. To produce enough output voltage to drive the MOS resistor in the strong-inversion region, we used a number of differential pairs. The output voltage of the circuit can be given by
\[ V_{REF} = V_{GS,D2} + (n - 1)\Delta V_{GG}. \]  

We can obtain a constant voltage with a zero TC, adjusting the size of transistors and the number of differential pairs.

Figure 5 shows the simulated results for the output voltage of the circuit. In the simulation, the ratio of each of the transistor pairs shown in Table 1 was assumed, and the number of differential pairs was set to 5 (i.e., \( n = 5 \)). An almost constant voltage can be obtained in the temperature range, and the TC of the voltage is zero at room temperature. The voltage variation with the temperature can be suppressed within \( \pm 1\% \). This variation is mainly ascribed to the non-linearity of the gate-source voltages of the diode-connected transistors. Though both voltages of \( V_{GS,D2} \) and \( \Delta V_{GG} \) in Eq. (21), where \( V_{GS,D2} \) is negative and \( \Delta V_{GG} \) is positive, are nearly proportional to the temperature, they still have little nonlinear temperature dependence. Therefore, the output voltage changes nonlinearly as shown in Fig. 5.

### 3. Constructing the Current Reference Circuit

The current reference circuit we describe can be constructed by combining the constant current subcircuit and the constant voltage subcircuit. Figure 6 shows the entire configuration of the circuit. We modified the configuration of the constant-current subcircuit and added a source-coupled amplifier, to ensure the same current flowing in \( M_A \) and \( M_B \). To use the source-coupled amplifier, we adapted a cascode configuration of nMOSFETs in the constant-current subcircuit. The source-coupled amplifier and the constant-current subcircuit construct the unity gain configuration. The voltage of \( V_A \) is monitored by the non-inverting terminal of the unity gain circuit, and then the output voltage of \( V_B \) is set at the same voltage with \( V_A \). This ensures the same current value in transistors \( M_A \) and \( M_B \). AC analysis of this unity gain circuit shows that the phase margin at the unity gain frequency is 45 degree, and the circuit is stable.

Figure 7 shows the simulated results for the output current \( I_{REF} \). In this simulation, the ratio of \( K_B/K_A \) was set to 1.06. The variation in the current can be suppressed within \( \pm 4\% \) in the temperature range from −20 to 100°C.

The circuit is insensitive to a change in power supply voltage because of the feedback control with the source-coupled amplifier. Figure 8 shows the bias voltage \( V_{REF} \) and the output current as a function of the supply voltage. The circuit can operate at a low power voltage of 1.2 V. The variation in the bias voltage and the output current can be suppressed within \( \pm 0.19\% \) and \( \pm 0.60\% \), respectively, in the supply voltage range from 1.2 to 3 V. Table 2 summarizes the performance of this current reference.

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**Table 1** Example of MOSFET’s ratios.

<table>
<thead>
<tr>
<th>( K_{D2} )</th>
<th>( K_{D1} )</th>
<th>( K_3 )</th>
<th>( K_2 )</th>
<th>( K_{i=3,5,7,9} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.06</td>
<td>1.25</td>
<td>3</td>
<td>3</td>
<td></td>
</tr>
</tbody>
</table>

![Fig. 5 Output of bias-voltage circuit as a function of temperature, simulated with parameters given in Table 1.](image)

![Fig. 6 Current reference circuit consisting of bias voltage subcircuit and constant-current subcircuit.](image)
Fig. 7  Output of current reference circuit as a function of temperature, simulated with parameters given in Table 1.

Fig. 8  Bias-voltage and output current as a function of supply voltage.

Table 2  Performance summary.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.25 µm, 1-poly 5-metal CMOS</td>
</tr>
<tr>
<td>VDD</td>
<td>1.5 V</td>
</tr>
<tr>
<td>IREF</td>
<td>97.7 nA (T = 25°C)</td>
</tr>
<tr>
<td>VREF</td>
<td>727 mV (T = 25°C)</td>
</tr>
<tr>
<td>Power</td>
<td>1.1 µW (T = 25°C)</td>
</tr>
<tr>
<td>∆IREF/IREF</td>
<td>± 4% (T = −20 to 100°C)</td>
</tr>
<tr>
<td></td>
<td>± 0.60% (VDD = 1.2 to 3 V)</td>
</tr>
<tr>
<td>∆VREF/VREF</td>
<td>± 1% (T = −20 to 100°C)</td>
</tr>
<tr>
<td></td>
<td>± 0.19% (VDD = 1.2 to 3 V)</td>
</tr>
</tbody>
</table>

The temperature dependence on the output current is somewhat larger than expected from Eq. (10). This was mainly caused by the variation in the bias-voltage with temperature that is shown in Fig. 5. Further improvements will be made possible by modifying the bias-voltage subcircuit. Equation (10) shows that the temperature that gives a zero TC increases as overdriving voltage \( V \) increases (see Fig. 2). Therefore, if we can construct a bias-voltage circuit that produces a voltage with an appropriate positive TC, then we will be able to create an improved current-reference circuit that shows a zero TC over a wide temperature range. We are now developing such a modified bias-voltage circuit.

4. Conclusion

We described an ultralow power constant current reference circuit with little temperature dependence. This circuit consists of a constant-current subcircuit and a bias-voltage subcircuit. and is useful as a reference current for a micropower application in an environment where the temperature changes. This circuit compensates for the temperature characteristics of mobility \( \mu \), thermal voltage \( V_T \), and threshold voltage \( V_{TH} \) in such a way that the reference current has small temperature dependence. A SPICE simulation demonstrated that the reference current is 97.7 nA, and the variation in the reference current and the bias voltage can be kept very small within ± 4% and ± 1% in a temperature range from −20 to 100°C. The total power dissipation is extremely low, 1.1 µW. Standard CMOS technology can be used without a resistor.

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References


Appendix: Temperature Coefficient of Oguey and Aebsicher’s Current Reference

The output current in their circuit [2] is given by

\[
I = n^2 \mu C_{ox} K V_f^2 K_{off},
\]

where \( n \) is a correction factor of low drain-source voltage \( (n = \beta_{lin}/\beta_{sat}) \), and \( K_{off} \) is a function of the geometrical ratios of transistors. The TC is given by

\[
TC_I = \frac{1}{I} \frac{dI}{dT} = \frac{1}{\mu} \frac{d\mu}{dT} + \frac{1}{V_f^2} \frac{dV_f^2}{dT}
\]

and is reduced to

\[
TC_I = -\frac{m}{T} + \frac{2}{T}.
\]

Because the value of \( m \) is about 1.5 for ordinary MOSFETs, the temperature coefficient is always positive, and the current will increase as the temperature increases.
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