Paper

A Low Power Analog Matched-Filter with Smart Sliding Correlation

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A low power analog matched filter circuit with smart sliding correlation is proposed for direct sequence code division multiple access (DS-CDMA) despreading process. The influence of level shifter mismatch on the trade-off between speed, power and resolution of the analog correlator circuit is investigated with respect to technology scaling. The optimization in power, acquisition time and areal efficiency is considered. Simulation with code length of 127 reveals that the analog matched filter circuit provides good linearity, and dissipates only 22 mW at a voltage supply of 3.3 V and an operational clock frequency of 128 MHz, using 0.35 μm CMOS technology.

Keywords: code division multiple access, matched filter, analog correlator, wireless applications, despreading process, analog signal processing, switched-capacitor circuits, spread spectrum.

1. Introduction

In recent years, Direct Sequence Code Division Multiple Access (DS-CDMA) technique becomes popular in wireless communication systems due to its high capacity and robustness against interference and noise [1] [2]. In DS-CDMA, all users share the same carrier frequency, but are assigned unique Pseudo Noise (PN) codes for spreading. The desired user's signal is separated from those of other users after performing despreading process using the same PN code as a transmitter sending the desired signal [3]. The matched filter (MF) in a receiver is known as the fastest method for acquisition of DS-CDMA signals. The MF calculates a cross correlation between an input signal and a filtering coefficient employed for modulation. Power consumption of the MF is a key issue in multimedia hand-held terminals.

A number of MFs had been proposed such as digital MFs [4] [5], charge-coupled device (CCD) MF [6], surface-acoustic wave (SAW) MF [7]. However, it is difficult to reduce the power consumption in digital implementation because taking correlation is a very computationally expensive processing. In addition, it requires high speed analog-to-digital converter (ADC) to digitize the received signal. This leads to high dissipation power at high-speed applications. To avoid the power consumption of a high speed ADC, analog domain is used for recovering the received information [8]. CCD devices yield high cost and power dissipation because of high-voltage clocking. On the other hand, although the SAW devices do not require carrier synchronization circuits, the insertion loss is a serious problem. Recently, a CMOS switched capacitor matched filter that uses analog signal processing has been demonstrated [9] [11]. The reported (MF) circuits has achieved a maximum processing rate of 128MHz with 75mW power consumption using code length of 64 and requires more than 64 non-overlapping clocks to drive the switches. This is achieved only at the expense of chip area because a large number of capacitors and switches are used. Although this is a significant step toward the realization of low power consumption CDMA, a considerable amount of improvement in power consumption and chip area is still required.

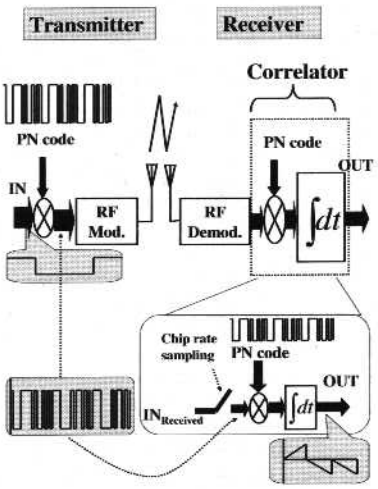

Fig. 1. Simplified wireless DS-CDMA system.

We had proposed a new analog correlator circuit (ACC) for DS-CDMA despreading process [12] [13]. ACC has a good ability to cancel off the charge error, and capacitance mismatch is small because it is either cancelled off or being reduced due to the ACC's noise rejection

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capability. ACC implemented with 0.6μm CMOS technology dissipates only 3.4 mW at a voltage supply of 5 V and an operational clock frequency of 128 MHz using code length of 127. Control sequence for the proposed circuit is simple, as it requires only three clock phases. ACC has a good ability to cancel off the charge error due to parasitic capacitances and equipped small chip area as a minimum number of devices are used compared to the reported circuits [11].

This paper proposes a low power analog matched filter (AMF) using this ACC technique. The proposed AMF uses seven ACC to realize smart sliding correlation. The remainder of the paper is organized into six sections. Section 2 gives an overview of DS-CDMA and describes how correlation is used in despreading process. Section 3 introduces analog correlator circuit principle of operation. Section 4 describes the trade-off between speed, power, and resolution of the level shifter for its optimized design. In Sec. 5 the block diagram of analog matched filter is discussed. Section 6 shows physical layout and simulation results of the analog matched filter circuit. In Sec. 7 we summarize the main results.

2. DS-CDMA Basic Structure

Figure 1 depicts a simplified wireless DS-CDMA system. In the transmitter the serial data bit stream is spreaded with a PN sequence code. In the receiver, despreading is accomplished by performing a discrete-time correlation of the baseband-received signal with the PN code using discrete-time correlation i.e., multiplying the received signal by the PN code followed by integration. This discrete-time correlation (C_{DT}) is defined as

$$C_{DT} = \sum_{i=1}^{L} S_R(i)\ PN(i), \quad \cdots\cdots\cdots\cdots\cdots\cdots (1)$$

where $S_R(i)$ is the chip-rate sampled value of the received input signal, $PN(i)$ is the PN code with L code length. When the two signals are in-phase, the output of the correlator becomes positive. And when they are out-of-phase, the output becomes negative. Thus, the correlator output contains the original data bits in its sign. Because of the random nature and high frequency content of the PN code, the spectrum of spreaded data is relatively flat and much wider in bandwidth than the original signal.

3. Analog Correlator Circuit (ACC)

For simplicity and clarity, a single-ended representation of ACC is shown in Fig. 2(a) [12] [13]. The level shifter is introduced to decouple the output node voltage on the correlator circuit. Theoretically, the level shifter is ideal, i.e. its gain equals unity. During the sampling phase (ϕ_1 and $\bar{\phi}_3$ according to switching sequence which shown in Fig. 2(b)), electric charge is stored at the sampling capacitor, C_C. At the integrating phase (ϕ_4 and $\bar{\phi}_3$), the storage charge is then injected into the load capacitance C_L. The amount of electric charge injected to the load capacitance is given by

$$Q_{CL} = C_C(V_{IN+} - V_{IN-}). \quad \cdots\cdots\cdots\cdots\cdots\cdots (2)$$

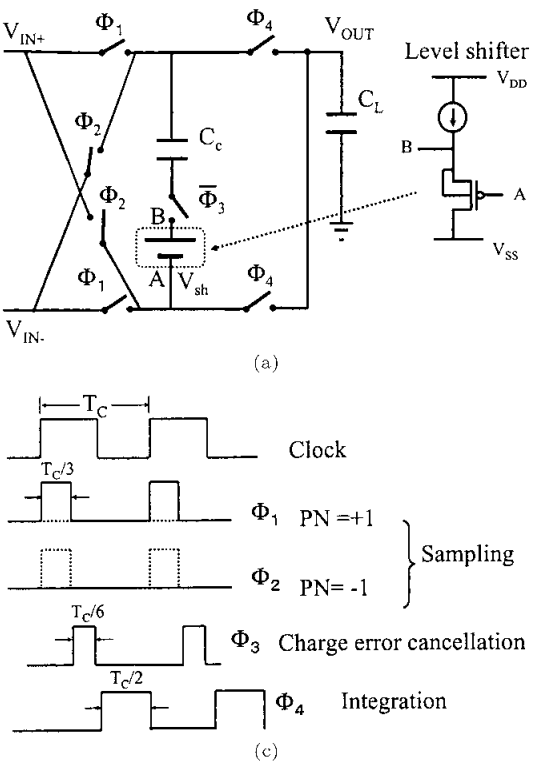

Fig. 2. (a) Single-ended analog correlator circuit, and (b) switching sequence (sampling, charge erro cancellation and itegration) phases.

As a result, signal voltage swing ΔV for one charging cycle resulted from the charge injecting is given by

$$\Delta V = \frac{C_C(V_{IN+} - V_{IN-})}{C_L}. \quad \cdots\cdots\cdots\cdots\cdots\cdots (3)$$

The voltage swing is independent of voltage at the output node V_{OUT}. Hence, linearity can be achieved. This is because the level shifter elevates the input voltage by V_{sh}. Because the level shifter shown in Fig. 2(a) has low output resistance, the switch $\bar{\phi}_3$ is added to protect the signal charge during charge error cancellation phase [12] [13]. Discharging the same amount of charge from C_L is simple by just interchanging V_{IN+} and V_{IN-} (ϕ_2), i.e. injecting the same amount of negative charge into C_L.

As reported in [12] [13] the charge errors can be solved by using bottom-plate sampling, charge error cancellation technique and fully differential circuitry as shown in Fig. 3. On the other hand, the effect of top-plate parasitic capacitance (C_{tp}) is negligible small. The switch (ϕ_3) is momentarily closed according to the switch sequence shown in Fig. 2(b) converting the differential charge on the parasitic capacitances to a common-mode charge effectively eliminating the charge error. At the end of each cycle, the output nodes of the fully differential correlators (V_{OUT+} and V_{OUT-}) will be shorted (ϕ_{RST}) to redistribute electric charges and set the output nodes of the correlators back to reference point. The ACC circuit requires only three non-overlapping clocks (sampling, charge error cancellation, and integration) phases, which reduces the complexity of the control se-

quence. Eventually, this leads to less switching and low power consumption.

In practical case, due to channel length modulation in the level shifters (the level shifter's gain G < 1), Eq. (3) can be rewritten as follows [13]

$$\Delta V = \frac{C_C(V_{IN+} - V_{IN-})}{C_L} + \frac{C_C(G-1)(V_{OUT} - V_{IN-})}{C_L}. \quad \cdots\cdots\cdots (4)$$

Taking the channel length modulation effect into consideration using transistor size of W/L=9.6μm/0.6μm in 0.35μm CMOS technology, the output deviated but at a range of less than 8% although every signals swing varied at maximum 10%. This result is similar to our previous design with 0.6μm CMOS technology [13].

As the nonlinearity of the source and drain junction capacitances associated with the transistor switches can introduce errors in the sampling process. To minimize this effect, the sampling capacitor can be increased and/or the switch sizes decreased. Doing either of these increases the settling time constant ($\tau = R_{ON} \times (C_C + C_L)$), where R_{ON} is the on-resistance of the integration switch so there is a trade-off between operating bandwidth and nonlinearity error. The smallest switch sizes (W/L=0.7μm/0.4μm) were used to minimize the nonlinearity error while the sampling capacitors (C_C = 140fF) and the load capacitors (C_L = 44 C_C) were used those still permitted 128MHz operation. The charge injection error of switches (0.3μV), kT/C noise voltage of C_C (0.2mV) and the noise voltage of the level shifter (44μV) are negligible small.

Even though the input voltage amplitude is only 3 mV, the output of the correlator becomes 26 mV. This means that 10-bit resolution at the input can be relaxed to 7-bit at the output. Ideally, as shown in Eq. (2), the level shifter mismatch does not influence the input resolution. However, in practical case there are non-idealities and parasitic capacitances in the level shifters, by which the level shifter mismatch limits input resolution indirectly. The circuit simulation including the level shifter mismatch as input offset voltages reveals that only a few tenth of the level shifter mismatch influences on output signal. Based on this result, the input resolution is assigned to only σ of the level shifter mismatch given by

$$\sigma(\Delta V_{th}) = \frac{A_{Vth}}{\sqrt{WL}}, \quad \cdots\cdots\cdots\cdots\cdots\cdots (5)$$

where A_{Vth} is the matching proportionality constant for threshold voltage. In our design with 0.35μm CMOS technology, the input resolution is estimated as σ=2.7mV. This estimation for input resolution is sufficient for the ACC. As described in Sec. 4, lower input resolution can be achieved by decreasing the level shifter mismatch using very wide level shifter which dissipates large power.

As shown in Eq. (3), the charge injected into the load capacitance depends on C_C and $V_{IN+} - V_{IN-}$. Mismatch between C_{C+} and C_{C-} can be kept under 2% by applying layout technique such as using unit square capacitor [16]. Depending on its implementation, mismatch of $V_{IN+} - V_{IN-}$ may range from 0.2 - 5%. However, due to the noise rejection ability of the correlation circuit, the effect of capacitance mismatch is tolerable [12] [13].

Comparison with this ACC with reported works is shown in Table 1. The power consumptions in the table are normalized assuming the same number of taps, the same frequency, and the same power supply voltage. As reported in [13] the ACC's power consumption includes all clock power to sequence the switches and parasitic wiring capacitance. According to these results, this ACC circuit achieves a small area and low power consumption relatively, resulting in suitability for AMF as described in Sec. 5.

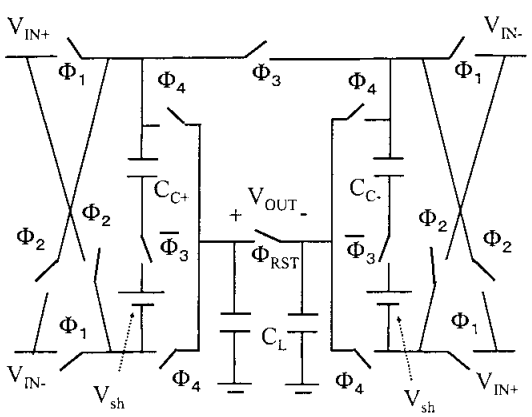

Fig. 3. Fully differential analog correlator circuit.

4. Speed-Power-Resolution Trade-off of ACC

There is a trade-off between speed-power and resolution of ACC. To improve the input resolution, large devices have to be used so that the capacitive loading of the circuit nodes increases and more power is required to attain a certain speed performance. This trade-off has been documented at [14]. The speed performance (gain-bandwidth) of the level shifter is given by

Table 1. Comparison with other reported analog correlator circuits.

	Core Area	Power	Power supply voltage	Technology
Passive circuit[11]	0.45mm^2†, 64 Tap (7000μm^2/Tap)	4mW @ 64Mchips/s (39nJ/Mchips/Tap/V^2)	5.0V	1.2μm
S/H circuit[15]	0.25mm^2, 15 Tap (17000μm^2/Tap)	2.22mW @ 16.67Mchips/s (820nJ/Mchips/Tap/V^2)	3.3V	0.35μm
Proposed circuit	0.05mm^2, 128 Tap (390μm^2/Tap)	1mW @ 128Mchips/s (6nJ/Mchips/Tap/V^2)	3.3V	0.35μm

† this value is based on our calculations for area of one analog correlator circuit [13].

$$Speed \approx \frac{g_m}{2\pi C_{gs}} \approx \frac{3I}{4\pi(V_{gs}-V_{th})C_{ox}WL}. \quad \cdots\cdots (6)$$

The power consumption (P)of the level shifter is a function of the supply voltage and the current consumption.

$$Power \approx I \times V_{DD} \quad \cdots\cdots (7)$$

On the other hand, the input resolution that can be achieved by the circuit is proportional to the matching accuracy of the devices. The relative input resolution can be given by

$$\frac{1}{resolution^2} \approx \frac{A_{Vth}^2}{WLV_{DD}^2}. \quad \cdots\cdots (8)$$

From the equations (6)-(8), following formula approximately can be derived:

$$\frac{Speed \times resolution^2}{Power} \alpha \frac{1}{C_{ox}A_{Vth}^2} \quad \cdots\cdots (9)$$

This means that for a given technology, if high speed and low input resolution are required, this can only be achieved by consuming power.

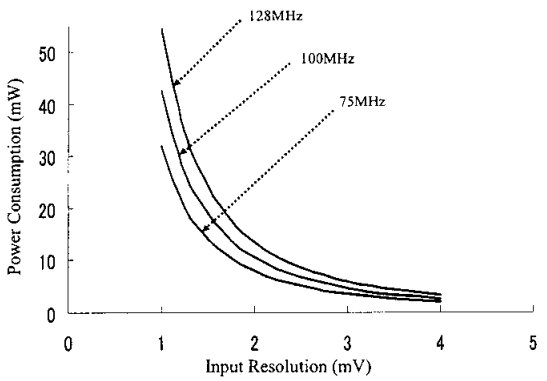

Fig. 4. Trade-off between power consumption and input resolution (0.6μm CMOS technology).

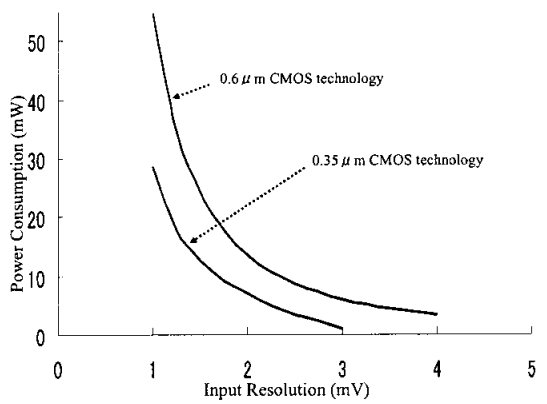

Fig. 5. Trade-off between power consumption and input resolution (operating frequency of 128 MHz).

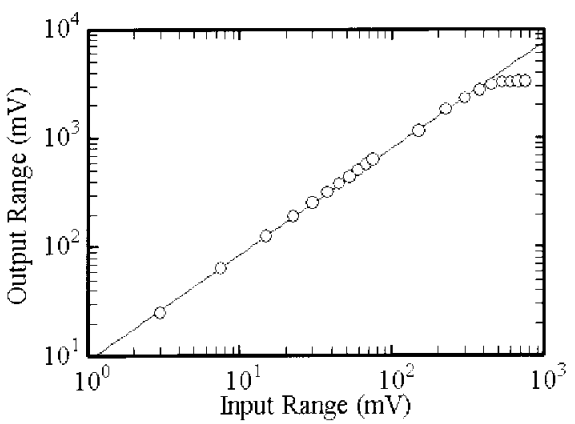

Fig. 6. Simulation results of analog correlator transfer characteristics.

Figure 4 depicts the simulation results of the trade-off between input resolution and power consumption using 0.6μm CMOS technology and speed as a parameter. On the other hand, when the technology scales down the trade-off becomes better. This means that, e.g., for the same speed and accuracy, less power is needed when technology is scaled down. The ACC realized using 0.6μm CMOS technology dissipates 3.4mW and has minimum input resolution of 4mV at operation speed of 128MHz [12], [13]. When the same circuit has been realized using advanced fabrication technology (0.35μm CMOS technology), it dissipates 1mW and its minimum input resolution is 3mV at the same operation speed of 128MHz as shown in Fig. 5.

Figure 6 shows the linear behavior of the analog correlator designed using 0.35μm CMOS technology, which is a plot of its transfer characteristics. The maximum input range is limited by output saturation toward voltage suppply of 3.3V.

5. Analog Matched Filter with Smart Sliding Correlation

Figure 7 shows block diagram of AMF. Before despreading can proceed, the internal MF's PN sequence must be aligned or synchronized to the same sequence embedded in the incoming received signal. This is accomplished by first acquiring a coarse open-loop alignment and then closing a feedback loop to track and maintain the alignment.

In Fig. 7, the acquisition and tracking use seven ACC which are designed to process both in-phase (D_A) and out-of-phase (D_A) signals. Acquisition is performed as a straightforward sequential search through all possible chip phases, commonly known as "sliding correlation" as shown in Fig. 8. All ACC are used, so seven phase alignments can be checked on each pass cutting the search time in one seventh. Approximately, the acquisition time of sliding correlation is given by

$$T_{acq} = a + \frac{b}{N}, \quad \cdots\cdots (10)$$

where N is the number of correlators, a and b are constants. When the correlation peak from any of the seven ACC is detected, the clock phase is locked and tracking mode is entered. Tracking pulse allows only one ACC that has correlation peak to work and stops the other

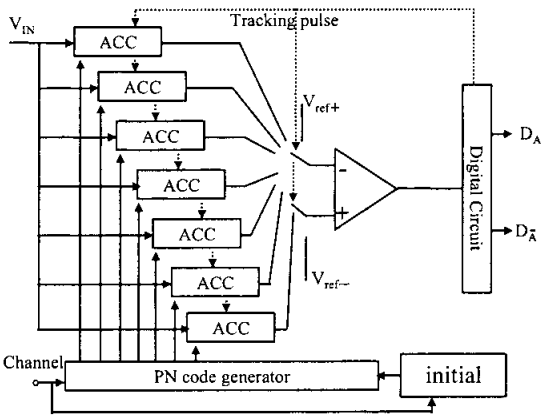

Fig. 7. Block diagram of the analog matched filter.

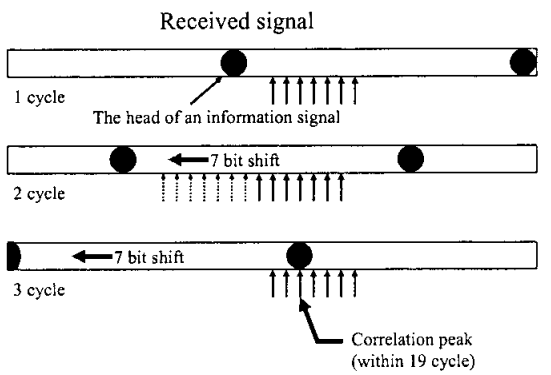

Fig. 8. Sliding correlation process to detect the correlation peak.

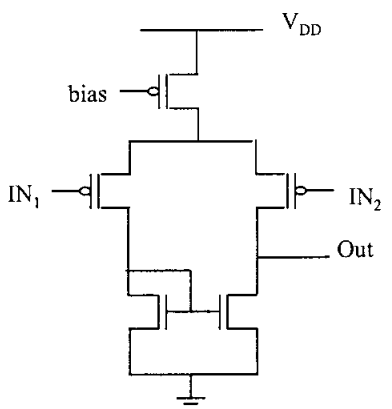

Fig. 9. Comparator circuit.

six. Therefore the ACCs' power dissipation of 7 mW can be reduced approximately by seven times to 1 mW. As each ACC dissipates 1 mW and the PN code generator together with the output selector (fully differential comparator and digital circuit) consumes 21 mW. In this implementation with a PN sequence of 127 chips and using seven ACC, the correlation peak can be detected within 19 cycle (127 x 19 clocks). We call this technique "smart sliding correlation." The ACC is adequate to realize a smart sliding correlator because of its small occupied area and low power consumption. As the ACC is large noise margin, the simple comparator

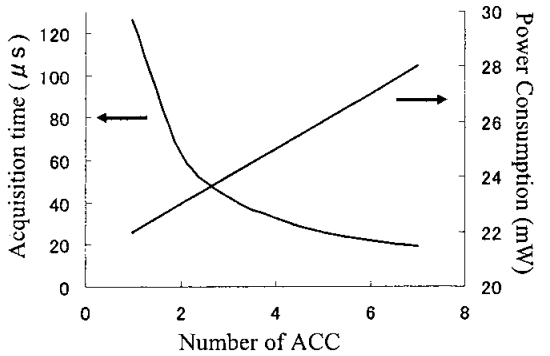

Fig. 10. Trade-off between power and acquisition time in smart sliding correlation.

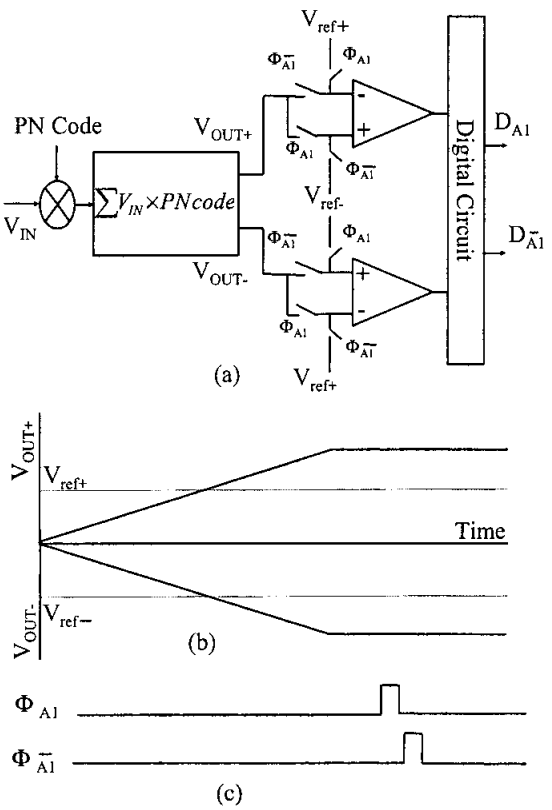

Fig. 11. (a) Analog correlator circuit together with fully differential comparator and digital circuit to process both in-phase and out-off-phase signals, (b) ACC integrating output and (c) Comparison switching sequence.

shown in Fig. 9 can be used for "smart sliding correlation" described above.

Theoretically, the power consumption of the AMF during acquisition is given by

$$P = P_d + P_{comp} + NP_{ACC}, \quad \cdots\cdots\cdots\cdots \quad (11)$$

where P_d, P_{comp} and P_{ACC} are the power consumption of digital circuit, comparator and ACC respectively. The acquisition time is given by Eq. (10). There is a trade-off between power consumption and acquisition time for different number of ACCs as shown in Fig. 10. To minimize the product of P and T_{acq}, the optimum number of ACCs to realize AMF circuit is given by

$$N_{opt} = \sqrt{\frac{b(P_d + P_{comp})}{aP_{ACC}}}. \quad \cdots\cdots\cdots\cdots\cdots\cdots (12)$$

In our case (L=127), N_{opt} is 51. In practical case, only seven ACC is used to realize AMF, because the output of PN code generator (seven linear feedback shift register) is used effectively and uncomplicated digital circuit are used. Using only seven ACC save chip area of AMF circuit.

Figure 11 shows a more detailed view of ACC process for both D_A and $D_{\bar{A}}$ signals. As the PN code has a high correlation with itself and low correlation with the others, the noise level of the other channels is usually low. This allows to use smaller load capacitance (C_L) of the ACC (Fig. 2(a)), which make the output nodes V_{OUT+} and V_{OUT-} saturate before the final output is obtained at the end of the clock cycles (L-th sampling phase for PN codes) as shown in Fig. 11(b). The value of the load capacitance is limited by the maximum of the interference level due to other channels. As we have calculated the interference due to 10 channels using the same taps for L=127. The value of this interference which is only 7% is acceptable for using C_L=44C_C to realize the correlator circuit. Then, the fully differential comparator compares between the saturated output voltages (V_{OUT+} and V_{OUT-}) and (V_{ref+} or V_{ref-}) according to the switching sequence which shown in Fig. 11(c). If the received signal and the PN code are in-phase, D_A becomes high. On the other hand, if they are out-of-phase, $D_{\bar{A}}$ becomes high. The same technique is applied for all of the seven ACC. The levels of V_{ref+} and V_{ref-} are set to 2.65 and 0.65 V, respectively, in the designed ACC (0.35μm CMOS technology). The digital circuit generates the tracking pulse according to the comparator outputs.

6. Physical Layout and Simulation Results

The AMF circuit had been designed using 0.35 μm triple-metal double polysilicon CMOS process. The designed circuit contains a clock generator for three phases (sampling, charge error cancellation, and integration). The physical layout of the AMF is shown in Fig. 12. The seven correlators make up the large dense block at the top of the layout. The PN code generator runs in a horizontal row at the bottom of the layout. The output selector which consists of fully differential comparator and digital circuit is located on the right. The layout size of 350 μm x 625 μm is sufficiently small.

The circuit dissipates 22 mW (this includes all clock power to sequence the switches and parasitic wiring capacitance) with code length of 127 at voltage supply of 3.3V and operational clock frequency of 128MHz. The power is estimated from circuit simulations including parasitic capacitances based on the layout. The PN code used in this simulation is M-sequence with 127 code length. Figure 13 shows the simulation results of ACC outputs during acquisition using code length of 127. When the acquisition routine detects the peak, the clock phase is locked and the tracking mode is entered. The specifications of the designed AMF circuit

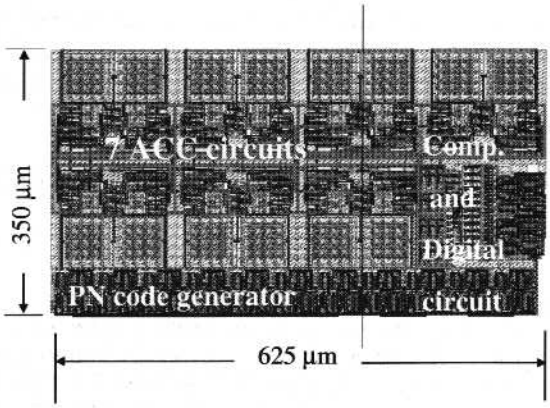

Fig. 12. Physical layout of analog matched filter circuit.

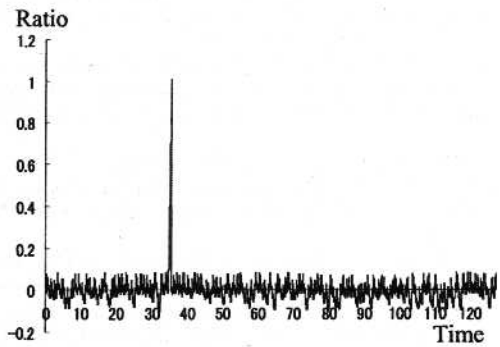

Fig. 13. A simulation example of correlation peak from analog correlator during acquisition.

Table 2. Analog matched filter circuit specifications.

Power supply	3.3 V
Resolution	3 mV
PN code length	127
Maximum clock frequency	128 MHz
Output signal format	Analog/Digital
Power dissipation	22 mW
Process	0.35 μm CMOS
Chip size	350 μm x 625 μm

are shown in Table 2.

7. Conclusion

A low power AMF circuit with smart sliding correlation is proposed for DS-CDMA despreading process. This circuit is suitable for the use of the compact ACCs, because of its small occupied area and low power. The AMF circuit is designed using 0.35 μm CMOS technology, considering the trade-off between speed, power and resolution in the ACC, and between total power, areal efficiency and acquisition time in the smart sliding correlation. Simulation with code length of 127 reveals that the AMF circuit provides good linearity and dissipates only 22 mW at a voltage supply of 3.3 V and an operational clock frequency of 128 MHz using 0.35μm CMOS technology.

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