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DIGITAL IMPLEMENTATION OF THIRD HARMONIC DISTORTION REDUCTION IN FOURTH-ORDER ΔΣ D/A CONVERTER

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Abstract

This paper presents a reduction technique of third harmonic distortion (HD3) in a ΔΣ digital-to-analog converter (DAC) for low-power wireless transmitter applications. It has digital-centric circuits, such as ΔΣ modulator as well as a simple digital pre-distortion circuit for HD3 reduction. The experimental results using FPGA reveal the effectiveness of the digital pre-distortion.

1. Introduction

Increase of demand for wireless communication requires the low-power and high-precision wireless transmitter. A ΔΣ-based transmitter is one of solutions for the problem of power efficiency and resolution [1] because a power amplifier can operate at the highest efficiency point in this architecture. In addition, the ΔΣ-based transmitter is digital-centric

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architecture, which can improve the disadvantages originating in analog circuits, such as the signal voltage swing and the chip size [2].

In this study, we design a fourth-order ΔΣ digital-to-analog converter (DAC) with 12-bit resolution for a transmitter used in IEEE 802.15.4 applications. It is designed in FPGA for evaluation. Especially, a reduction technique of third harmonic distortion (HD3) is focused.

2. Designed ΔΣ DAC Architecture

The digital baseband codes modulated in offset-QPSK are input to two DACs for quadrature up-conversion. The fundamental frequency of input signal is determined according to the chip rate and symbol rate in direct sequence spread spectrum technique. It is important that signal frequency in the DAC is nearly constant.

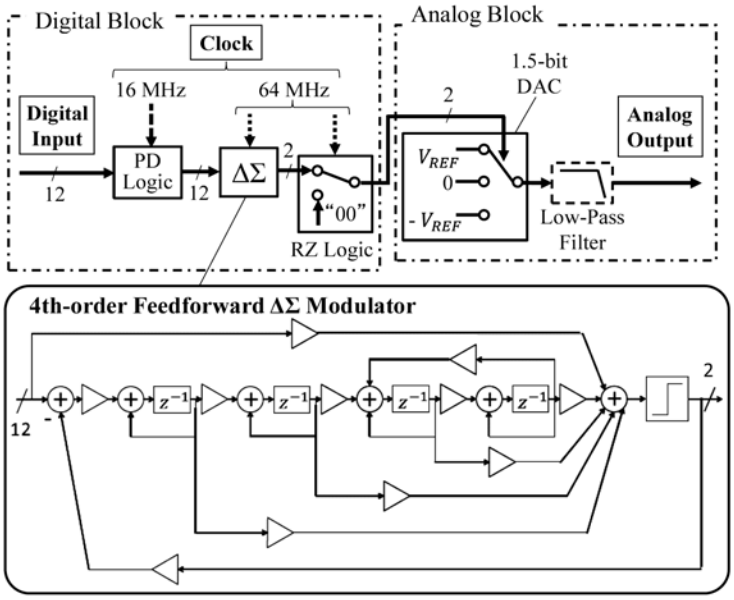

Figure 1. Designed ΔΣ DAC.

The block diagram of designed ΔΣ DAC with 12-bit resolution is shown in Figure 1. It has digital logic and analog baseband blocks. The former contains the pre-distortion (PD) logic circuit, the fourth-order feed-forward

ΔΣ modulator (DSM), and a return-to-zero (RZ) logic circuit. The latter has 1.5-bit DAC and an analog filter if needed before up-conversion. To achieve high precision and high stability, the DSM operates at 64 MHz clock signal for high over sampling ratio (OSR). The RZ logic circuit prevents inter-symbol interference between digital logic and analog baseband modules.

The digital PD circuit alters the input code and decreases HD3 by using the HD3 reduction technique [3]. It is also useful to relax required filter specifications in the following signal filtering. The 1.5-bit DAC outputs three kinds of differential analog voltages according to digital code. This digital-centric design is expected to reduce power consumption and chip size.

3. Digital Pre-distortion

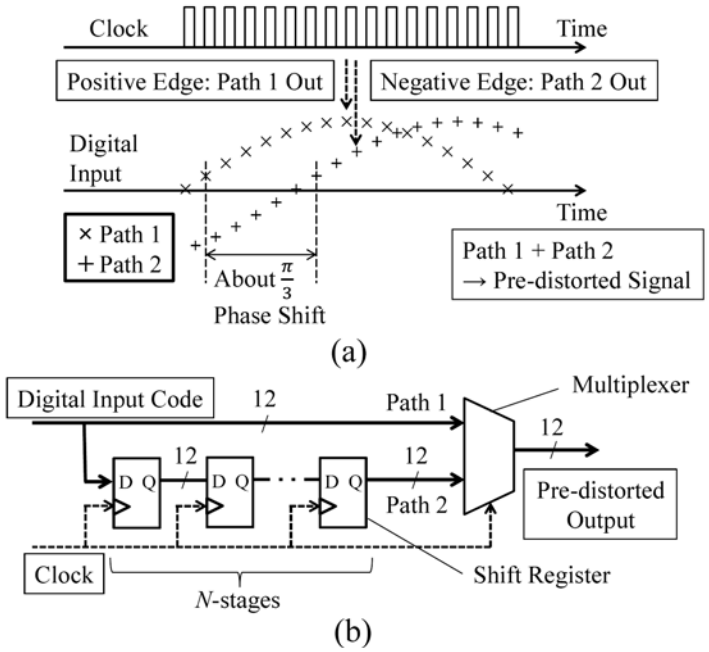

Figure 2. (a) Principle and (b) block diagram of digital pre-distortion circuit.

A digital PD circuit can be designed using some shift registers in series and a multiplexer, as shown in Figure 2. Assuming pseudo-sine wave as input, one of interleaved code of the original input comes directly to one side

of the multiplexer (Path 1), while another interleaved code enters another side through digital delay circuits composed of series shift registers (Path 2). The multiplexer generates pre-distorted output overlapping two sine waves by switching paths 1 and 2 at positive and negative edges of the clock, respectively. Based on the low-distortion sine wave generation technique for analog-to-digital convertor (ADC) and DAC tests [3], the digital delay circuit must correspond to $\pi/3$ phase shifter to reduce HD3 which mostly dominants signal-to-noise-and-distortion ratio (SNDR) in differential constitution. The DSM generates HD3 components through its third-order nonliniarity from the pre-distorted input signal with fundamental frequency. Two HD3 output components have the phase difference of π and cancel each other.

For this HD3 reduction technique, the number of shift registers N is given by

$$N = \frac{f_{clk}}{6 f_{BB}}, \tag{1}$$

where f_{clk} is a clock frequency of the digital PD circuit and f_{BB} is a fundamental input frequency. As described in Section 2, f_{BB} can be constant in wireless applications. In this design, $f_{BB} = 500$ kHz and $f_{clk} = 16$ MHz. From Equation (1), $N = 5$. The integer constraint for N may cause phase error from $\pi/3$ between the two paths. As seen later, this problem is not so important. This digital PD technique can be extended easily for other harmonic distortion reduction in the same manner [3].

For reduction of in-band third-order intermodulation distortion (IMD3) for two-tone signal, phase of each tone signal must be interleavingly shifted in the opposite direction $(+\pi/3$ or $-\pi/3)$ [4]. In this study, however, both phases of the two-tones are interleavingly shifted in the same direction, so this technique shows little IMD3 reduction.

4. FPGA Experiments

The effectiveness of designed digital PD circuit was evaluated using FPGA with 1.2-V supply. The digital PD circuit, the DSM and the RZ logic

circuit were programmed on an evaluation board with Altera Cyclone II EP2C70. The 12-bit digital input codes corresponding to single-tone signal at f_{BB} frequency were generated in an external 14-bit ADC on the board from an external signal source. To generate analog output, the external 14-bit DAC on the board was used with limitation of three values instead of 1.5-bit DAC. In this work, without analog filter described in Section 2, the analog output was evaluated by a spectrum analyzer (Agilent 8562EC) and a differential probe (Tektronix P6247, attenuation 10 : 1). The clock frequencies were set as shown in Figure 1.

Figure 3 shows the result that the digital PD reduces the power of the HD3 component for f_{BB} of 500 kHz. The HD3 reduction was –13.4 dB, resulting in improvement of 7.1 dB in SNDR. Compared with the case of no HD3 reduction technique, the fundamental component power decreased by only 1.25 dB due to the signal separation described in Section 3. The similar evaluation for the IMD3 reduction with two-tone signal demonstrated only a few dB reduction, as expected in Section 3.

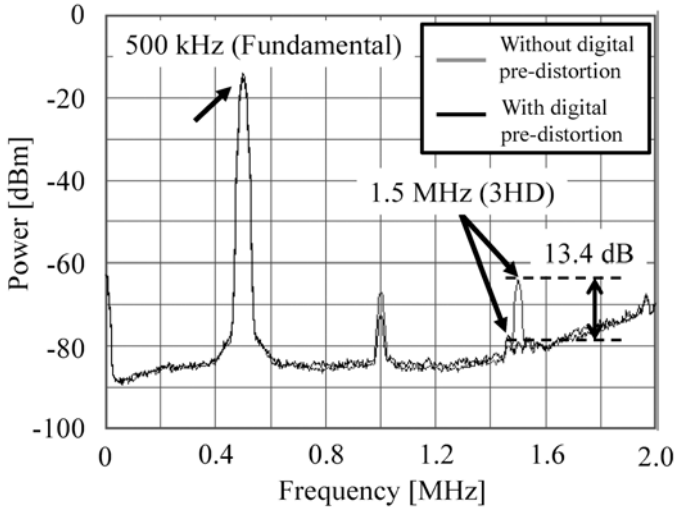

Figure 3. Output spectrum of designed DAC.

The dependence of HD3 reduction on the frequency f_{BB} is shown in Figure 4. Although the HD3 reduction had optimum of –18.5 dB at 547 kHz,

the reduction below –10 dB was observed within a wide frequency range over 200 kHz. This behavior reveals the HD3 reduction factor of $|\cos(3N\pi f_{BB}/f_{clk})/\cos(N\pi f_{BB}/f_{clk})|$, which can be obtained from the theoretical calculation.

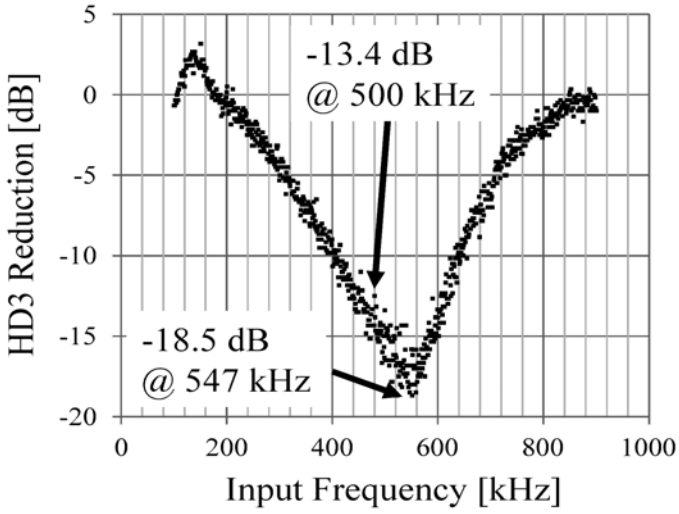

Figure 4. Frequency characteristic of HD3 reduction.

5. Conclusion

A novel fourth-order ΔΣ DAC has been designed with digital-centric design and the digital PD circuit to improve area efficiency and linearity. The effectiveness of the digital PD circuit has been revealed using the FPGA experiments.

Acknowledgement

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References

[1] M. M. Ebrahimi, M. Helaoui and F. M. Ghannouchi, Delta-sigma-based transmitters: advantages and disadvantages, IEEE Microwave Magazine 14(1) (2013), 68-78.

[2] A. Matsuzawa, Digital-centric RF CMOS technologies, IEICE Trans. Electron. E91-C(11) (2008), 1720-1725.

[3] K. Wakabayashi, K. Kato, T. Yamada, O. Kobayashi, H. Kobayashi, F. Abe and K. Niitsu, Low-distortion sinewave generation method using arbitrary waveform generator, J. Electronic Testing 28(5) (2012), 641-651.

[4] K. Kato, F. Abe, K. Wakabayashi, C. Gao, T. Yamada, H. Kobayashi, O. Kobayashi and K. Niitsu, Two-tone signal generation for ADC testing, IEICE Trans. Electron. E96-C(6) (2013), 850-858.