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A CMOS LOW-DROPOUT REGULATOR WITH A DYNAMIC-BIASED GAIN STAGE

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Abstract

This paper presents a CMOS low-dropout (LDO) regulation with a dynamic-biased gain stage. The dynamic-biased gain stage which has the dynamic adjustable output resistance, current and gain is designed as a second stage driving the power transistor. A LDO regulator with the proposed gain stage has been implemented in a 0.18μm standard CMOS process and occupies 0.11mm^2 chip area. The experimental results show that the proposed LDO regulator can be stable without any additional on-chip compensation capacitors or complex circuit. The LDO regulator provides a full load transient response of settling time less than 15μs with a 2.2μF load capacitor and the voltage

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variation is less than 40mV. Furthermore, the load regulation and line regulation are 321μV/mA and 1.8mV/V, respectively.

1. Introduction

Power management is a very important issue in portable electronic applications [1]. Although linear regulators have a better transient response, less noise than the switching regulators, they are relatively inefficient. So the low-dropout (LDO) regulators, which are able to provide effective stabilization of the output voltage even when the difference between input and output voltage is less than 0.3V, are used more and more in electric equipments especially in communication systems [2].

The LDO regulators usually use a large-sized PMOS transistor as the power transistor to drive high load current while achieving low dropout voltage. If we use a large off-chip load capacitor, then the large gate capacitance of the PMOS power transistor creates a low-frequency non-dominant pole while the large off-chip load capacitor generates the low-frequency dominant pole. So the uncompensated LDO regulator is unstable. The conventional compensation techniques usually use the zero generated by the load capacitor and its equivalent series resistance to achieve the frequency compensation. So it has a narrow bandwidth and requires a huge load capacitor and equivalent series resistance. Furthermore, we should carefully choose the value of the load capacitor and its equivalent series resistance to ensure the stability of the LDO regulator, otherwise the LDO regulator will oscillate when the zero locates at too low (e.g., beyond the dominant pole) or too high frequency (e.g., far behind the unity-gain frequency).

Different approaches have been reported to achieve the frequency compensation [3-7]. The simple and effective approach is inserting a voltage buffer between the error amplifier and the power transistor. For example, in the literature [3], an emitter-follower has been adopted as a voltage buffer to drive the PMOS power transistor. The low output resistance of the emitter-follower allows the pole at the gate of the power transistor to move to higher

frequency. A current feedback amplifier is used in the LDO regulator to achieve the fast transient response and high slew rate [4]. In order to further improve the LDO regulator performances, the buffer impedance attenuation technique is proposed to realize an intermediate stage for driving the power transistor [5]. The method can greatly improve the efficiency of the LDO regulator for low load current, while it can achieve the frequency compensation and good transient response. A voltage-controlled current source is proposed to generate the low frequency compensation zero instead of relying on the zero generated by the load capacitor and its equivalent resistance [6]. However, most of the reported LDO regulators require additional on-chip capacitors for the frequency compensation.

In this paper, we propose a LDO regulator with a dynamic-biased gain stage. Compared with the other reported LDO regulators with voltage or current buffers, the proposed compensation method is much more simple, effective and efficient. Furthermore, the proposed LDO regulator can be stable even without any on-chip compensation capacitor.

2. Discussion on the Stability of the LDO Regulators

The circuit topology of a classical CMOS LDO regulator shown in Figure 1 is composed of an error amplifier, a PMOS power transistor, a feedback-resistor network, a voltage reference and a load capacitor C_L with equivalent series resistance (ESR) R_{ESR}. Generally, the feedback resistors R_{f0} and R_{f1} are much larger than the resistor R_L. There are two poles and one zero in the LDO regulator:

$$P_1 = \frac{1}{C_L(R_L + R_{ESR})}, \tag{1}$$

$$P_2 = \frac{1}{C_p R_1}, \tag{2}$$

$$Z_{ESR} = \frac{1}{C_L R_{ESR}}. \tag{3}$$

Here C_p is the input capacitance of the power transistor, R_1 is the output resistance of the error amplifier. The conventional compensation techniques usually use the zero generated by the load capacitor and its ESR to achieve the frequency compensation. So it has a narrow bandwidth and requires a huge load capacitor and ESR.

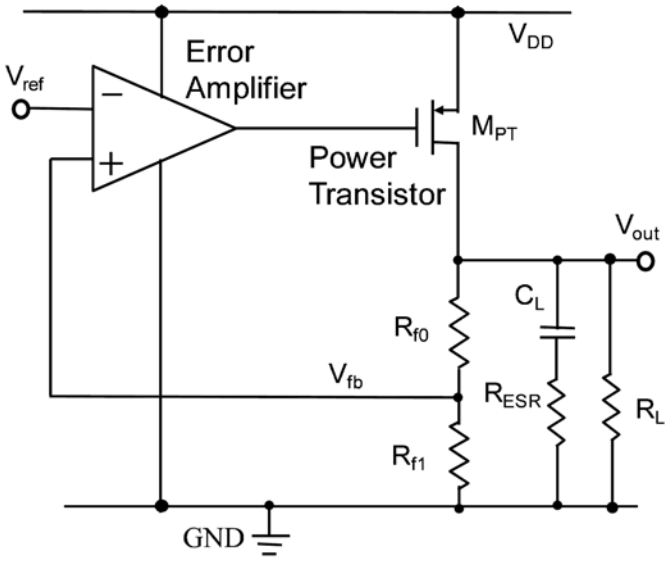

Figure 1. Circuit topology of the conventional LDO regulator.

Figure 2 shows another frequency compensation technique and it can achieve the frequency compensation by adding a voltage buffer between the error amplifier and the power transistor. There are three poles and one zero:

$$P_1' = \frac{1}{C_L(R_L + R_{ESR})}, \tag{4}$$

$$P_2' = \frac{1}{C_p R_{buf}}, \tag{5}$$

$$P_2'' = \frac{1}{C_{buf} R_1}, \tag{6}$$

$$Z_{ESR}' = \frac{1}{C_L R_{ESR}}. \tag{7}$$

Here R_{buf} is the output resistance of the voltage buffer and C_{buf} is the input capacitance of the voltage buffer. As R_{buf} and C_{buf} are much smaller than R_1 and C_p, P_2' and P_2'' locate at much higher frequency than P_2, resulting in the LDO regulator stability even with a small load capacitor and ESR. Furthermore, the unity-gain of the LDO regulator increases with such a small load capacitor, as shown in Figure 3. Increase in the current of the buffer driving the power transistor also can improve the transient response of the LDO regulator for changes in load current and supply voltage.

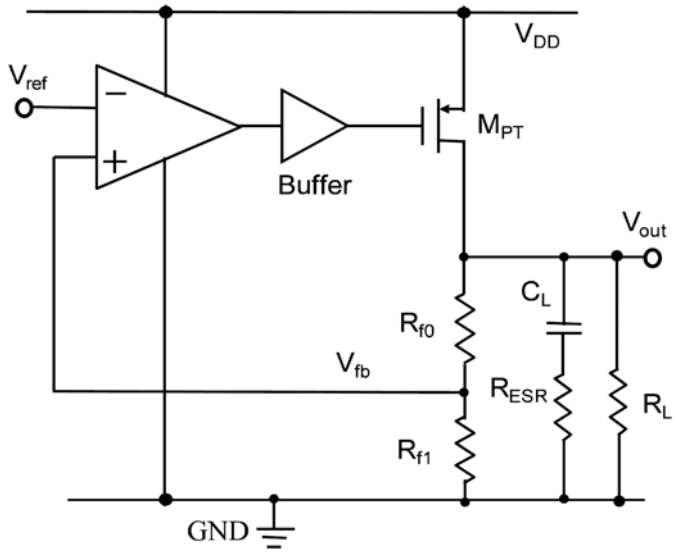

Figure 2. Circuit topology of the LDO regulator with the voltage buffer.

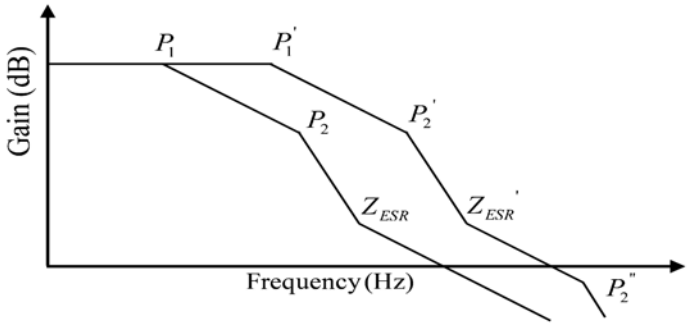

Figure 3. Frequency compensation scheme of the LDO regulators.

Usually, the voltage buffer is realized as a source follower with too insufficient output swing to fully turn on (for PMOS-implemented source follower) or turn off (for NMOS-implemented source follower) the power transistor efficiently. We can adopt other types of voltage or current buffers [4, 7] to achieve the frequency compensation. However, the voltage or current buffers usually require additional current consumption and have complex circuit topologies.

Generally, we should increase the current of the buffer in order to enhance the compensation effect of the buffer. Although the second pole is pushed to higher frequency after adding the buffer, when the load current increases, the dominant pole also moves to higher frequency and the LDO regulator may be unstable. So a current buffer with dynamically-biased shunt feedback is proposed to overcome this issue, which can decrease the output resistance of the buffer and push the second pole to higher frequency when the load current increases. At the same time, the current of buffer also increases as the load current increases. So the supply current becomes low in the low load current condition. This will ensure the efficiency of LDO regulator at whole load current range. However, the compensation effect of the buffer is not sufficient for the stability of the LDO regulator, an additional 10pF compensation capacitor is required to ensure the stability of the LDO regulator.

In the proposed LDO regulator, the dynamic-biased gain stage is not only the second gain stage of the LDO regulator but also has the dynamic frequency compensation effect. Compared with the reported LDO regulator [5], the proposed gain stage has both the dynamic adjustable output resistance and the dynamic adjustable gain. As the load current increases, the current of the stage increases and it can increase the driving current of the large-sized power transistor. The output resistance of the gain stage decreases so that the second pole moves to higher frequency. Moreover, the gain of the stage decreases and this will further ensure the stability of the LDO regulator. In short, the stage has the dynamic adjustable output resistance, current and gain so that it has the dynamic frequency compensation effect and the LDO regulator can be stable without the on-chip compensation capacitor.

Furthermore, the dynamic-biased stage can improve the transient response performance of the LDO regulator.

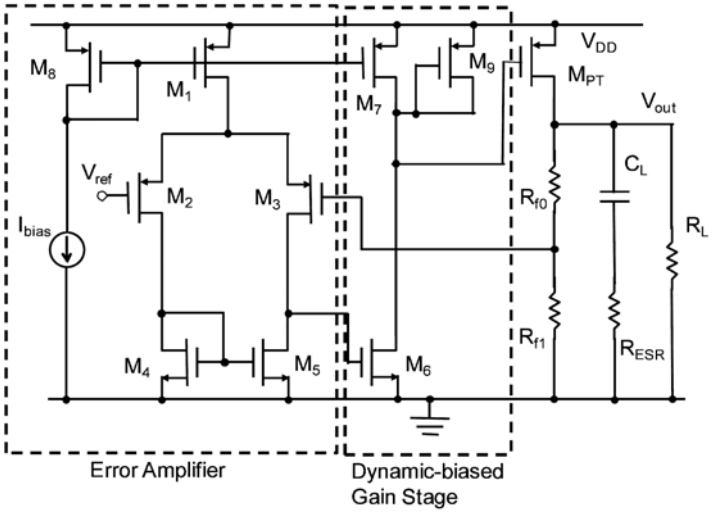

Figure 4. Schematic of the proposed LDO regulator.

3. Proposed Low-dropout Regulator

The schematic of the proposed LDO regulator is shown in Figure 4. The error amplifier and the dynamic-biased gain stage are formed by M1-M7 and M9. Based on the discussion of the LDO regulator with a voltage buffer, it can move the second pole P_2 to a higher frequency P_2'. So the LDO regulator can achieve the frequency compensation without requiring the low-frequency zero generated by the large load capacitor and ESR of the conventional LDO regulator as shown in Figure 1 and it can be stable with a small load capacitor and ESR. The dynamic-biased gain stage has the same compensation effect.

Without the transistor M9, the stage which is composed of M6 and M7 is the conventional gain stage. The output resistance of the gain stage M6 and M7 can be expressed as [8]:

$$R_o = r_{o6} // r_{o7}, \tag{8}$$

where r_{o6} and r_{o7} are the output resistances of the transistors M6 and M7,

respectively. With the transistor M9, the output resistance is:

$$R_o' = r_{o6} // r_{o7} // \frac{1}{g_{m9}} \approx \frac{1}{g_{m9}}. \quad (9)$$

It is similar to the output resistance of the voltage buffer, moving the second pole to a higher frequency and stabilizing the LDO regulator.

As we discussed above, the dynamic-biased gain stages M6, M7 and M9 can decrease the output resistance and push the second pole to high frequency. Furthermore, the gain stage has the dynamic adjustable output resistance. When the load current increases, the output resistance of the gain stage decreases and the second pole is pushed to a higher frequency. So it can achieve the dynamic frequency compensation. Additionally, the current flowing through the transistor M9 is very low at low load current. So the stage has the dynamic adjustable current which can increase the driving current of the power transistor at high load current and ensure the efficiency of the LDO regulator at whole load current range. In the design using a 0.18μm CMOS process in this work, the current that flows through the transistor M9 is only 1μA and 126μA for the load currents of 1mA and 100mA, respectively.

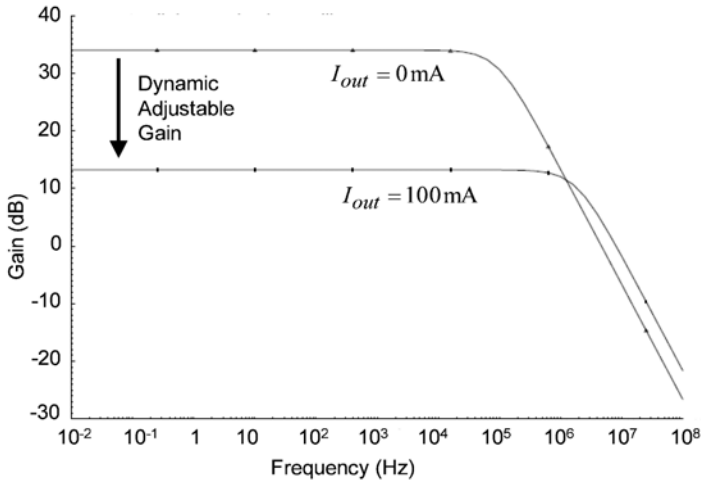

Figure 5. Simulated frequency response of the proposed dynamic-biased gain stage at 0 and 100mA load currents.

Besides the current and the output resistance, the proposed dynamic-biased gain stage has the dynamic adjustable gain. The simulated frequency response of the gain stage in this work is shown in Figure 5. As shown in the simulation results, the gain of the stage is 33dB and 13dB at 0mA and 100mA load currents, respectively. So as the load current increases, the gain of the LDO regulator decreases, and this will further ensure the stability of the LDO regulator.

From the above discussion of the dynamic-biased gain stage, both the dynamic adjustable output resistance and gain have the frequency compensation effect and the LDO regulator can work properly even without the on-chip compensation capacitor. However, we should carefully choose the sizes and currents of the transistors in the circuit especially for the transistors M6 and M9, so the DC gain of the LDO regulator and the error amplifier are high enough and the LDO regulator can still work at high load current. The simulation results in Figure 6 show that the DC gain of the LDO regulator is larger than 53dB even for the load current of 100mA. Furthermore, as shown later in Figure 8, the LDO regulator actually can work properly at 200mA load current and the voltage variation of the output voltage is sufficiently small at the same time.

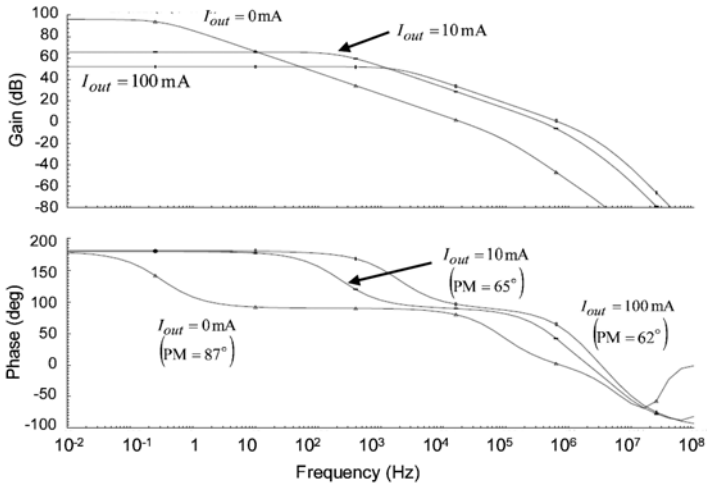

Figure 6. Simulated loop gain of the LDO regulator with the dynamic-biased gain stage.

The proposed LDO regulator was simulated with a 0.18μm CMOS process and the open loop gain results are shown in Figure 6. The load capacitance C_L is 2.2μF, and its ESR is set zero to verify the functionality of the proposed frequency compensation scheme. The phase margin is better than 60° for all cases and the DC gain of the proposed LDO regulator at 0mA, 10mA and 100mA are 91dB, 68dB and 53dB, respectively. The no-load-current bandwidth is 28kHz and the bandwidth is 810kHz for 100mA load current.

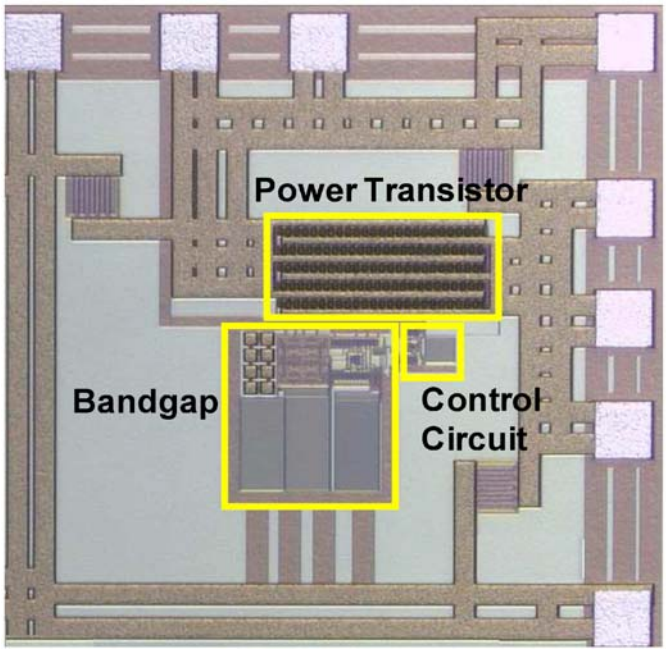

Figure 7. Chip micrograph of the LDO regulator fabricated in 0.18μm CMOS process.

4. Experimental Results

The proposed LDO regulator is designed and fabricated with a 0.18μm CMOS process. The micrograph of the fabricated LDO regulator is shown in Figure 7 and the core area occupation is 0.11mm^2. This chip includes bandgap reference circuit and current source for V_{ref} and I_{bias} as shown in

Figure 4. At room temperature of 27°C, the measured total current drawn I_q is only 43μA for 0mA load current (10μA is consumed by the bandgap reference circuit) and 170μA for 100mA load current $(I_{\max})$. A very low ESR 2.2μF ceramic load capacitor is used in order to verify the functionality of the proposed frequency compensation effect of the dynamic-biased gain stage. The ESR value of the capacitor is less than 50mΩ.

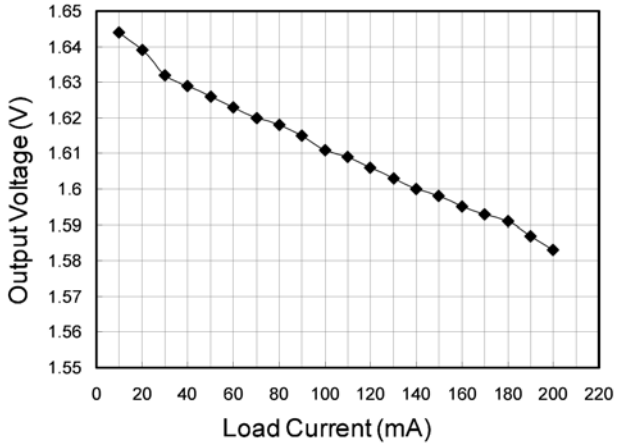

Figure 8. Load regulation of the fabricated LDO regulator $(V_{DD} = 2.65\text{V})$.

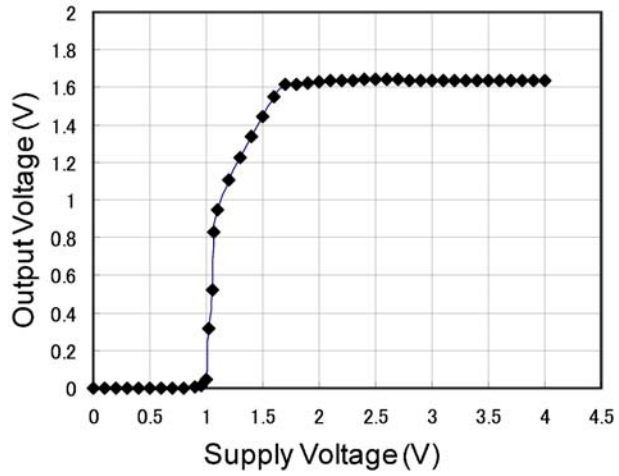

Figure 9. Line regulation of the fabricated LDO regulator (load current: 10mA).

Although the dynamic-biased gain stage can achieve the dynamic frequency compensation, the load regulation performance may be degraded at high load current. It is because the DC gain of the LDO regulator decreases as the load current increases. So we should carefully choose the sizes and currents of the transistors in the circuit especially for the transistors M6 and M9. From the measured load regulation shown in Figure 8, the load regulation is 321μV/mA at 2.65V supply when the load current changes from 0 to 200mA. The experimental result shows that the LDO regulator actually can work properly at 200mA load current and the voltage variation of the output voltage is sufficiently small at the same time. Figure 9 reveals that the line regulation is 1.8mV/V at 10mA load current.

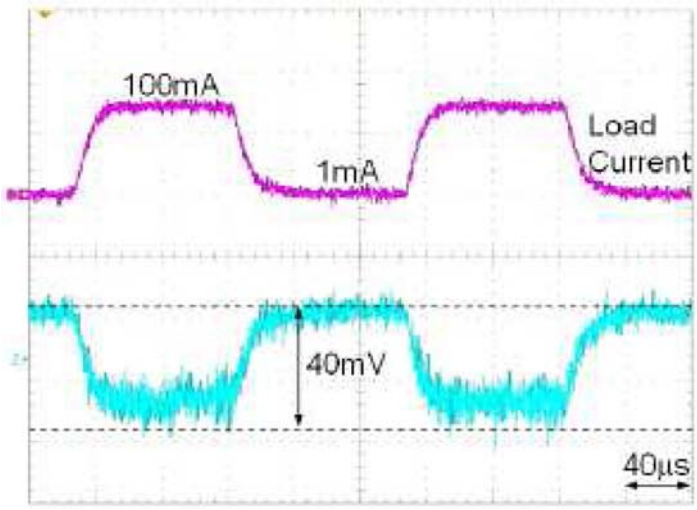

Figure 10. Load transient response of the fabricated LDO regulator (load current frequency: 5kHz, V_{DD} = 2.65 V).

The measured load transient response of the fabricated LDO regulator is shown in Figure 10, where DC-cut output voltage waveform is used for load changes between 1mA and full load current 100mA. The fabricated LDO regulator can recover the output voltage within 15μs for this large load current change and the voltage derivation ΔV_{out} is less than 40mV, which includes output under/overshoots and load regulation variations. The

measured PSRR of the LDO regulator is -56dB at 1kHz and the dropout voltage V_{drop} is 250mV at 100mA load current.

Table 1 summarizes the performance of the proposed LDO regulator compared to several LDO regulators previously reported in the literature. Owing to the dynamic-biased gain stage, the proposed LDO regulator can be stable even without the on-chip compensation capacitor and has good performance.

Table 1. Comparison with recently reported LDO regulators

	[4]	[5]	[6]	This work
Technology (μm)	0.25	0.35	0.5	0.18
V_{out}(V)	2.0	1.8	2.8	1.6
V_{drop}(mV)	N/A	200	N/A	250
$I_{\max}$(mA)	50	200	100	100
I_q(μA)	100	20 @ 0mA 340 @ $I_{\max}$	25	43 @ 0mA 170 @ $I_{\max}$
ΔV_{out}(mV)	<10	<55	<70	<40
Settling time (μs)	<2	<30	<50	<15
C_L(μF)	0.05	1.0	2.2	2.2
Area (mm^2)	0.23	0.264	N/A	0.11
Required ESR zero	No	No	No	No
Loop gain (dB)	>100	>50	42-73	>53
On-chip compensation capacitor (pF)	N/A	10	5	0

5. Conclusion

A CMOS LDO regulator with a dynamic-biased gain stage is presented in this paper. The proposed gain stage has the dynamic adjustable current, output resistance and gain. So it can achieve the dynamic frequency compensation for the LDO regulator and improve the performance of the LDO regulator. In addition, the proposed LDO regulator which is based on the idea of inserting a dynamic-biased gain stage between the error amplifier and the power transistor is implemented in a 0.18μm standard CMOS process. Besides the circuit structure of the gain stage adopted in this paper, we can use other types of dynamic-biased gain stages. However, the circuit topology proposed in this paper is simple but effective. The experimental results show that the LDO regulator with the proposed dynamic-biased gain stage can be stable without on-chip compensation capacitors and has good performance.

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