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A DESIGN FOR ULTRA-LOW-VOLTAGE CMOS DIGITAL CIRCUITS WITH PERFORMANCE CHARACTERISTICS COMPENSATION

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Abstract

A performance characteristics compensation method that exhibits good resistance to process and temperature variations is proposed for ultra-low-voltage CMOS digital circuits. The experimental results show that the stability of the designed digital circuit is significantly improved even when operating in the subthreshold region under a 0.3-0.5 V supply voltage.

1. Introduction

MOSFETs are inclined to operate in subthreshold region with decrease of the supply voltage in low-voltage low-power integrated circuit designs [1]. As a result, the power consumption decreases, but the circuit performance becomes unstable because of more significant effects due to device mismatch and process and temperature variations in the subthreshold region. To compensate for the performance fluctuations, methods that employ the MOSFET body as an adjustable feedback terminal have been reported, of which the control signals are generated by

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additional circuit blocks with functions to monitor the digital circuit delay or inverter threshold voltage [2, 3, 4, 5]. The reported techniques are effective, but the monitor blocks always require large-scale circuits or consume much additional power, and are therefore difficult to implement with a 0.5 V low-voltage supply.

We have previously proposed a technique that employs a simple additional circuitry to compensate for the effects of device mismatch and process and temperature variations [6, 7]. This technique consumes only a small amount of additional power and achieves stable operation of the digital CMOS circuits even in the subthreshold region. In this study, the proposed technique is verified using Monte-Carlo simulations and experimental evaluation of a fabricated chip.

2. Proposed Circuit

The proposed compensation circuits are shown in Figure 1. Compared to traditional CMOS digital circuits, all the PMOS and NMOS bodies are connected together. Figure 1(a) shows that one of them is controlled by a temperature-variation compensation circuit, while the other is controlled by a logic-threshold correction circuit. Both NMOS and PMOS bodies are forward biased to decrease the threshold voltage for higher performance. Note that the triple-well CMOS process is required in this design.

![Figure 1.](image)

**Figure 1.** (a) Compensation of device characteristics variations with body biasing, and (b) the control circuits.
Figure 2. Monte-Carlo simulation results for logic threshold voltages of the inverters under 0.5 V supply (a) without and (b) with the characteristics compensation (1000 trials).

Figure 3. Monte-Carlo simulation results for logic threshold voltages of the inverters under 0.3 V supply (a) without and (b) with the characteristics compensation (1000 trials).

Figure 4. Photomicrograph of the fabricated test chip operating at 0.5 V supply.
Figure 1(b) shows the single MOS transistor with diode connection used to sense the temperature variation and convert it to a voltage signal $V_{NW-Ref}$, using a low-temperature-coefficient resistor. The voltage signal is then amplified by a body biasing inverter to generate the PMOS body control signal $V_{N-Well}$ for the main digital circuits. At the same time, $V_{N-Well}$ is also connected to the PMOS bodies of the logic-threshold correction circuit. To reduce the dependence of performance on the temperature, the gain of the amplifier must be set carefully. In the proposed technique, the inverter with bodies connected to the output node $(V_{N-Well})$ is used as the amplifier for this purpose.

In the logic-threshold correction circuit, the inverter logic threshold voltage is compared with $V_{PW-Ref}$ and the difference is amplified and fed back to the NMOS bodies [8]. This feedback loop accurately sets the logic threshold voltage of the inverters to $V_{ PW-Ref }$ for nominal operation. The stability of the feedback loop is established with an R-C low-pass filter. Thus, the characteristics compensation is realized with consideration of both process and temperature.

3. Circuit Design and Experimental Results

The proposed circuit is designed in a standard 0.18 μm CMOS process with a threshold voltage of approximately 0.45 V. To evaluate the usefulness of the proposed compensation circuit under low-voltage supply, a decimal counter is designed under supply voltages of 0.5 and 0.3 V. The designed counter has four D flip-flops, each of which is composed of two-input NAND logic gates to operate under a supply voltage of 0.3-0.5 V. A resistor with a low temperature coefficient is implemented in the temperature-variation compensation circuits using silicided polysilicon. Unlike the previous work [6], the logic threshold of the inverter is set near 180 and 80 mV ($V_{DD}/2$) under supplies of 0.5 and 0.3 V, respectively. This is because devices with the smallest gate width are used in the decimal counter to reduce power consumption.

Firstly, the logic threshold voltages of the inverters with and without the characteristics compensation circuit are simulated by 1000 trials of Monte-Carlo simulations involving process variations and device mismatches with a 0.5 V supply voltage. The proposed technique can decrease the deviation of the threshold voltage by a factor of 1/2 under a 0.5 V supply, as shown in Figure 2. Under a 0.3 V supply,
similar improvement can be realized by a factor of $3/4$, as shown in Figure 3. The poor improvement factor under the 0.3 V supply compared to that under 0.5 V is attributed to smaller forward body biasing.

**Figure 5.** Experimental results for the fabricated 0.5 V decimal counter. (a) Comparison of the inversed maximum clock frequency, and (b) body biasing voltages in the proposed compensation circuits.

**Figure 6.** Experimental results for the fabricated 0.3 V decimal counter. (a) Comparison of the inversed maximum clock frequency, and (b) body biasing voltages in the proposed compensation circuits.

Figure 4 shows a photomicrograph of the fabricated test chip operating at 0.5 V supply. The compensation circuits appear to occupy a relatively large chip area, because the test digital circuit employed in this study was very simple. The experimental results for the 0.5 V decimal counter are shown in Figure 5. Only the
compensation effect on temperature variations is shown in this figure. The maximum operation speed of the fabricated decimal counter maintains a relatively constant value over a wide temperature range, while the NMOS and PMOS body biasing voltages change appropriately, according to temperature variations.

The experimental results for the 0.3 V decimal counter are shown in Figure 6. Although the compensation effect is less than that for the 0.5 V case, due to more significant subthreshold operation, the proposed technique is still effective considering the temperature dependence of subthreshold operation. In contrast to Figure 5(b), \( V_{P-Well} \) increases slightly with temperature, as shown in Figure 6(b). This is because a diode-connected NMOS transistor used to monitor temperature in our temperature-variation compensation circuit generates the body bias voltage \( V_{N-Well} \) for PMOS transistors. Temperature dependence of NMOS and PMOS transistors’ performance are different and their mismatch varies according to fabrication process and supply voltage. When the mismatch increases, the \( V_{N-Well} \) generated by diode-connected NMOS may be not large enough to compensate performance variation of PMOS side completely, thereby weakening the compensation effect. Accordingly, \( V_{P-Well} \) slightly increases to maintain inverter threshold voltage. Even with such a condition, the proposed simple compensation circuit can have a certain effect at supply voltage as low as 0.3 V supply.

4. Conclusion

The proposed method employs simple circuitry to compensate for performance degradation due to process and temperature variations for 0.5 V ultra-low-voltage CMOS digital circuits. The simulation results show that the deviation of the inverter threshold voltage is significantly reduced, and the experimental results show that the stability of the designed digital circuit is significantly improved, even when operating in the subthreshold region. Furthermore, the proposed technique is still effective under a 0.3 V supply.

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