OUKA
The University of Osaka
Institutional Knowledge Archive

Title	A Study on Soft Error Mitigation for Microprocessor in Bulk CMOS Technology
Author(s)	上村, 大樹
Citation	大阪大学, 2015, 博士論文
Version Type	VoR
URL	https://doi.org/10.18910/52020
rights	
Note	

The University of Osaka Institutional Knowledge Archive : OUKA

https://ir.library.osaka-u.ac.jp/

The University of Osaka

A Study on Soft Error Mitigation for Microprocessor in Bulk CMOS Technology

January 2015

Taiki Uemura

Publication list

Transactions

1. T. Uemura, T. Kato, R. Tanabe, H. Iwata, J. Ariyoshi, H. Matsuyama, and M. Hashimoto, "Exploring Well-Configurations for Minimizing Single Event Latchup," IEEE Trans. Nucl. Sci., vol. 61, no. 6, pp. 3282-3289, Dec. 2014.
2. H. Mori, T. Uemura, H. Matusyama, T. Yamazaki, and T. Soeda, "Detection Technique with Alpha-tracking and Emissivity Comparison," IEEE Trans. Nucl. Sci., vol. 61, no. 6, pp. 3438-3442, Dec. 2014.
3. T. Kato, R. Alano, T. Uemura, Y. Watanabe and H. Matusyama, "Neutron Shielding Effect of Stacked Servers and Its Impact on Reduction of Soft Error Rate," IEEE Trans. Nucl. Sci., vol. 61, no. 6, pp. 345-348, Dec. 2014.
4. T. Uemura, T. Kato, H. Matsuyama, and M. Hashimoto, "Mitigating Multi-Bit-Upset with Well-Slits in 28 nm Multi-Bit-Latch," IEEE Trans. Nucl. Sci., vol. 60, no. 6, pp. 4362-4367, Dec. 2013.
5. T. Uemura, T. Kato, H. Matsuyama, and M. Hashimoto, "Soft-Error in SRAM at Ultra-Low Voltage and Impact of Secondary Proton in Terrestrial Environment," IEEE Trans. Nucl. Sci., vol. 60, no. 6, pp. 4232-4237, Dec. 2013.
6. T. Kato, T. Uemura, H. Mori, Y. Ikeda, K. Suzuki, S. Satoh, and H. Matsuyama, "Impact of Parasitic Bipolar Effect on Single-Event Upset in p-Type Metal-Oxide-Semiconductor Field Effect Transistor with Embedded SiGe," Jpn. J. Appl. Phys., vol. 52, no. 4S, p. 04CC15, Apr. 2013.
7. S. Abe, Y. Watanabe, N. Shibano, N. Sano, H. Furuta, M. Tsutsui, T. Uemura, and T. Arakawa, "Multi-Scale Monte Carlo Simulation of Soft Errors Using PHITS-HyENEXSS Code System," IEEE Trans. Nucl. Sci., vol. 59, no. 4, pp. 965-970, Aug. 2012.
8. R. Harada, S. Abe, H. Fuketa, T. Uemura, M. Hashimoto, and Y. Watanabe, "Angular Dependency of Neutron-Induced Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM," IEEE Trans. Nucl. Sci., vol. 59, no. 6, pp. 2791-2795, Dec. 2012.
9. T. Uemura, Y. Tosaka, H. Matsuyama, K. Takahisa, M. Fukuda, and K. Hatanaka, "Robust Flip-Flop Circuit against Soft Errors for Combinational and Sequential Logic Circuits," Jpn. J. Appl. Phys., vol. 48, no. 4, p. 04C070, Apr. 2009.
10. T. Uemura, R. Tanabe, Y. Tosaka, and S. Satoh, "Soft Error Hardened Latch and Its Estimation Method," Jpn. J. Appl. Phys., vol. 47, no. 4, pp. 2736-2741, Apr. 2008.
11. T. Uemura, Y. Tosaka, and S. Satoh, "Neutron-Induced Soft-Error Simulation

Technology for Logic Circuits," Jpn. J. Appl. Phys., vol. 45, no. 4B, pp. 3256-3259, Apr. 2006.
12. Y. Tosaka, R. Takasu, H. Ehara, T. Uemura, H. Oka, S. Satoh, N. Matsuoka, and K. Hatanaka, "Technological Trends of Soft Error Estimation Based on Accurate Estimation Method," Jpn. J. Appl. Phys., vol. 45, no. 4B, pp. 3185-3188, Apr. 2006.

Proceedings

1. T. Uemura, M. Hashimoto, "Soft Error Immune Latch Design for 20 nm bulk CMOS," in Proc. of 2015 IEEE International Reliability Physics Symposium (IRPS), (to appear), 2015.
2. T. Uemura, M. Hashimoto, "Impact of Package on Neutron Induced Single Event Upset in 20 nm SRAM," in 2015 IEEE International Reliability Physics Symposium (IRPS), (to appear), 2015.
3. T. Uemura, M. Hashimoto, "Investigation of Single Event Upset and Total Ionizing Dose in FeRAM for Medical Electronic Tag," in Proc. of 2015 IEEE International Reliability Physics Symposium (IRPS), (to appear), 2015.
4. H. Mori, T. Uemura, "Critical Charge Dependence of Correlation of Different Neutron Sources for Soft Error Testing," in Proc. of 2015 IEEE International Reliability Physics Symposium (IRPS), (to appear), 2015.
5. T. Kato, T. Uemura, and H. Matsuyama, "High-Accuracy Estimation of Soft Error Rate Using PHYSERD with Circuit Simulation," in Proc. of 2014 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), pp. 345-348, 2014.
6. T. Uemura, T. Kato, R. Tanabe, H. Iwata, H. Matsuyama, M. Hashimoto, K. Takahisa, M. Fukuda, and K. Hatanaka, "Preventing Single Event Latchup with Deep P-well on P-substrate," in Proc. of 2014 IEEE International Reliability Physics Symposium (IRPS), pp. SE.3.1-SE.3.4, 2014.
7. T. Uemura, T. Kato, and H. Matsuyama, "Impact of Parasitic Bipolar Action and Soft-error Trend in Bulk CMOS at Terrestrial Environment," in Proc. of 2013 IEEE International Reliability Physics Symposium (IRPS), pp. 6C.4.1-6C.4.6, 2013.
8. R. Kan, T. Tanaka, G. Sugizaki, R. Nishiyama, S. Sakabayashi, Y. Koyanagi, R. Iwatsuki, K. Hayasaka, T. Uemura, G. Ito, Y. Ozeki, H. Adachi, K. Furuya, and T. Motokurumada, "A 10th Generation 16-core SPARC64 Processor for Mission-critical UNIX server," in 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 60-61, 2013.
9. S. Abe, Y. Watanabe, N. Shibano, N. Sano, H. Furuta, M. Tsutsui, T. Uemura, and T. Arakawa, "Neutron-induced Soft Error Analysis in MOSFETs from a 65nm to a 25 nm Design Rule Using Multi-scale Monte Carlo Simulation Method," in Proc. of 2012 IEEE International Reliability Physics Symposium (IRPS), pp. SE.3.1-SE.3.6, 2012.
10. H. Nakamura, T. Uemura, K. Takeuchi, T. Fukuda, S. Kumashiro, and T. Mogami, "Scaling Effect and Circuit Type Dependence of Neutron Induced Sin-

gle Event Transient," in Proc. of 2012 IEEE International Reliability Physics Symposium (IRPS), pp. 3C.3.1-3C.3.7, 2012.
11. T. Uemura, R. Tanabe, and H. Matusyama, "Mitigation Technique against Multi-bit-upset without Area, Performance and Power Overhead," in Proc. of 2012 IEEE International Reliability Physics Symposium (IRPS), pp. 5B.4.1-5B.4.6, 2012.
12. Y. Ikeda, H. Mori, T. Kato, T. Uemura, M. Yoshida, M. Onoda, and H. Matsuyama, "Investigation of BTI Degradation in LDMOS Transistors," in Proc. of International Conference on Solid State Devices and Materials, pp. 454-455, 2012.
13. T. Kato, T. Uemura, H. Mori, Y. Ikeda, K. Suzuki, S. Satoh, and H. Matsuyama, "Radiation-Induced Parasitic Bipolar Effect in PMOS with Embedded SiGe," in Proc. of International Conference on Solid State Devices and Materials, pp. 847-848, 2012.
14. H. Mori, Y. Ikeda, T. Kato, T. Uemura, and H. Matsuyama, "Lifetime Evaluation on AC Stress in High-K / Metal-Gate with Using Dual-Pulsed-Test-System," in Proc. of International Conference on Solid State Devices and Materials, pp. 122-123, 2012.
15. S. Abe, Y. Watanabe, N. Shibano, N. Sano, H. Furuta, M. Tsutsui, T. Uemura, and T. Arakawa, "Multi-scale Monte Carlo simulation of Soft Errors Using PHITS-HyENEXSS Code System," in Proc. of 2011 12th European Conference on Radiation and Its Effects on Components and Systems, pp. 390-395, 2011.
16. T. Uemura, T. Kato, H. Matsuyama, K. Takahisa, M. Fukuda, and K. Hatanaka, "Investigation of Multi Cell Upset in Sequential Logic and Validity of Redundancy Technique," in Proc. of 2011 IEEE 17th International On-Line Testing Symposium, pp. 7-12, 2011.
17. T. Uemura, T. Sakoda, and H. Matsuyama, "Layout Optimization to Maximize Tolerance in SEILA: Soft Error Immune Latch," in Proc. of 2011 IEEE International Conference on IC Design & Technology, pp. 1-4, 2011.
18. H. Nakamura, K. Tanaka, T. Uemura, K. Takeuchi, T. Fukuda, and S. Kumashiro, "Measurement of Neutron-induced Single Event Transient Pulse Width Narrower Than 100ps," in Proc. of 2010 IEEE International Reliability Physics Symposium (IRPS), pp. 694-697, 2010.
19. T. Uemura, Y. Tosaka, H. Matsuyama, K. Shono, C. J. Uchibori, K. Takahisa, M. Fukuda, and K. Hatanaka, "SEILA: Soft Error Immune Latch for Mitigating Multi-node-SEU and Local-clock-SET," in Proc. of 2010 IEEE International Reliability Physics Symposium (IRPS), pp. 218-223, 2010.
20. S. Abe, Y. Watanabe, N. Shibano, N. Sano, T. Arakawa, H. Furuta, M. Tsutsui, and T. Uemura, "Simulation of Cosmic-ray Neutron Induced Soft Errors Using PHITS and HyENEXSS," in Proc. of International Radiation Effects on Semiconductor Devices for Space Applications, 2010.
21. K. Tanaka, H. Nakamura, T. Uemura, K. Takeuchi, T. Fukuda, and S. Kumashiro, "Study on Influence of Device Structure Dimensions and Profiles on Charge Collection Current Causing SET Pulse Leading to Soft Errors in Logic Circuits," in Proc. of 2009 International Conference on Simulation of Semiconductor Processes and Devices, pp. 1-4, 2009.

22. Y. Tosaka, T. Uemura, H. Ando, H. Matsuyama, K. Shono, K. Takahisa, M. Fukuda, and K. Hatanaka, "Neutron-Accelerated Test of Soft Error in Logic Element and System," in Proc. of International Workshop on Radiation Effects on Semiconductor Devices for Space Radiation, 2008, pp. 85-90.
23. T. Uemura, R. Tanabe, Y. Tosaka, and S. Satoh, "Using Low Pass Filters in Mitigation Techniques against Single-Event Transients in 45nm Technology LSIs," in Proc. of 2008 14th IEEE International On-Line Testing Symposium, pp. 117-122, 2008.
24. Y. Tosaka, R. Takasu, T. Uemura, H. Ehara, H. Matsuyama, S. Satoh, A. Kawai, and M. Hayashi, "Simultaneous Measurement of Soft Error Rate of 90 nm CMOS SRAM and Cosmic Ray Neutron Spectra at the Summit of Mauna Kea," in Proc. of 2008 IEEE International Reliability Physics Symposium (IRPS), pp. 727-728, 2008.
25. T. Uemura, Y. Tosaka, H. Matsuyama, K. Takahisa, and K. Hatanaka, "Robust Flip-Flop against Soft Errors for Combinational and Sequential Logic Circuits," in Proc. of International Conference on Solid State Devices and Materials, pp. 88-89, 2008.
26. T. Uemura, R. Tanabe, Y. Tosaka, and S. Satoh, "Novel Soft Error Hardened Latches and Flip-Flop," in Proc. of International Conference on Solid State Devices and Materials2, pp. 84-85, 2007.
27. T. Uemura, Y. Tosaka, S. Satoh, K. Takahisa, and K. Hatanaka, "Scaling Trends and Mitigation Techniques for Soft Errors in Flip-Flops," in Proc. of International Conference on Solid State Devices and Materials, pp. 284-285, 2006.
28. Y. Tosaka, R. Takasu, H. Ehara, T. Uemura, H. Oka, S. Satoh, N. Matsuoka, and K. Hatanaka, "Technology Trend of Soft Errors based on Accurate Estimation Method," in Proc. of International Conference on Solid State Devices and Materials2, pp. 442-443, 2005.
29. T. Uemura, Y. Tosaka, and S. Satoh, "Neutron-induced Soft-Error Simulation Technology for Logic Circuits," in Proc. of International Conference on Solid State Devices and Materials, pp. 942-943, 2005.
30. Y. Tosaka, H. Ehara, M. Igeta, T. Uemura, H. Oka, N. Matsuoka, K. Hatanaka, "Comprehensive Study of Soft Errors in Advanced CMOS Circuits with 90/130 nm Technology," in IEDM Technical Digest. IEEE International Electron Devices Meeting, pp. 941-944, 2004.

Abstract

This thesis presents techniques developed for mitigating soft error in microprocessors manufactured with bulk CMOS technology. For designing highly reliable microprocessors, a multi-layer approach is necessary ranging from architectural, circuity and transistor process layers. Microprocessors used in mission critical servers can improve their reliability with architectural layer techniques such as error correction code (ECC) parity checking, algorithmic checking, and watchdog timer. However these techniques cannot resolve all soft error issues in a microprocessor. Hence, component-level soft error mitigation in transistor and circuit layers is also required. In microprocessors, the components vulnerable to radiation are SRAM and latch/flip-flop (FF), and multi bit upset (MBU) and single event latchup (SEL) in SRAM, and single bit upset (SBU) and MBU in latches are factors that deteriorate the microprocessor reliability. Therefore, this thesis investigates these SBU, MBU and SEL, and proposes techniques for mitigating them.

This thesis starts with the discussion on the scaling trend of SRAM and FF single event upset (SEU) rates in bulk CMOS technology. Neutron and alpha irradiation tests were performed on SRAMs manufactured in 350, 250, 180, 130, 90, 65, 55, 45, 40, 28 and 20 nm bulk CMOS technologies and FF in 65, 45, 28 and 20 nm bulk CMOS technologies. SRAM soft error rate (SER) per bit reached the maximum in 180 nm for neutron and in 250 nm for alpha. In addition, evaluations on various 90 nm SRAMs show that the SER can change by up to 75% due to process conditions and the number of access ports. The FF SEU rate per bit decreased more than SRAM SER in 20 nm bulk CMOS technology. Consequently, the chip-level processor SER remains at the same level from 65 to 20 nm both in SRAM and FF without soft error mitigation techniques. From this chip level prediction, MBU needs to be mitigated for higher reliability in old technology such as 65 nm. After that, SBU and MBU in FF need to be mitigated because hardware instruction retry (HIR) cannot exclude MBU and some SBU. In addition, SEL in SRAM needs to be taken into consideration whereas SEL in FF is negligibly few since the well width of FF is large enough. From this observation, this thesis discusses techniques for mitigating MBU and SEL in SRAM and SBU and MBU in FF.

In 65 nm and older technology, SRAM SER with ECC, i.e. MBU, is higher than SER in sequential elements. This thesis approaches MBU mitigation in SRAM with optimization of well configuration optimization. First the dependence of SRAM SEU rate on well depth is investigated with and without deep N-well (DNW) through neutron and alpha irradiation tests. After that, an MBU mitigation technique that uses DNW is proposed. While DNW generally raises the SER due to parasitic bipolar action (PBA), the proposed method inserts narrow DNW to increase the distance be-

tween cells that are simultaneously selected in the same well. The neutron irradiation test results show that the proposed method drastically reduces MBU without area overheads.

In finer technologies like 20 nm, SEL in SRAM is a remarkable issue since the narrow well width in SRAM increases the resistance between well-contacts and SRAM cells. This thesis experimentally investigates SEL in SRAM through neutron irradiation tests and shows that altering well configuration could improve SEL immunity. Increasing dose in double-well can mitigate SEL without SEU increase, and at most 60% SEL reduction could be obtained via process tuning. DNW can be easily adopted to attain high SEL prevention efficiency at a cost of additional masks. However, it is necessary to pay attention to a fact that DNW increases SEU rate. Then, deep P-well (DPW) technology was proposed in this thesis. DPW is a more effective solution to eliminate SEL occurrence than increasing doping, and no SEL was observed in our irradiation tests. Furthermore, DPW is helpful to reduce SEU as well. While the adoption of DPW needs an extra cost to newly construct a DPW process, the DPW process development itself is not technically difficult. The SEL prevention by DPW can be expected to be similar or might be better than that of current limit device (CLD).

Since algorithmic techniques, such as parity prediction or residue check, cannot detect MBU in multi-bit latch (MBL), an MBU mitigation technique is proposed for MBL by inserting well-slits between latch bit cells. The area overhead is only 5.4% as an MBL macro for processors including clock buffer and checker. Neutron irradiation tests demonstrate that the proposed mitigation technique does not change the SBU rate and consequently did not degrade processor performance. The proposed mitigation technique can achieve robustness against MBUs, which cannot be detected by the checker and predictor, have not been observed in the proposed MBL even under sixty-hour accelerated irradiation.

It is demanded to mitigate not only MBU but also SBU in FF since algorithmic technique cannot cover all FFs and latches. For mitigating the SBU, a soft error immune latch (SEILA) is proposed. The SEILA introduces multi height cell (MHC) such as double height cell (DHC), triple height cell (THC) and dual clock buffer (DCB) techniques. The MHC technique mitigates SEU originating from charge collection to multiple nodes (CCM), and the DCB technique suppresses data upset caused by single event transient (SET) occurring at local clock (SETLC). SEILA is designed with the DHC and DCB in 65 nm technology and neutron irradiation test is performed. The DCB eliminates SETLC, and the DHC reduces SEU by 99.3%. The neutron irradiation test on SEILAs having different distances between critical nodes shows that SEU mitigation efficiency is sensitive to the distance. In 28 nm technology, SEILA is designed with DHC. The SEU rate in the 28 nm DHC-SEILA is at the same level with the 65 nm DHC-SEILA, while the number of latches is larger in a 28 nm microprocessor than 65 nm one. In 20 nm technology, SEILA is designed with THC for achieving higher SEU suppression and neutron and alpha SEU rates are evaluated. The neutron induced SEU rate in 20 nm THC-SEILA is 14 $\times$ lower than in the 28 nm DHC-SEILA. In alpha irradiation test, no error was observed and SEU rate is less than 1 FIT/Mbit with 90% statistically probability for 0.001 alpha/hour/cm^2.

Finally, this thesis focuses on SRAM SER in ultra-low voltage operation. Keeping

low power consumption in electron devices is crucially important for large scale systems, and further lower power operation will be required in future processors. Power consumption strongly depends on operation voltage, and aggressive voltage scaling is now studied. To cope with this aggressive voltage scaling, SER should be investigated in a wide range of voltage, especially at ultra-low voltage. SEU rate was evaluated through neutron and alpha irradiation tests and simulations. The measurement results show that neutron induced SEU rate at ultra-low voltage dramatically increases, and the SEU rate at around 0.2 V is by two orders of magnitude higher than that at 1.0 V. This result supported by simulation indicates that secondary protons generated by nuclear reaction with neutron collision are contributing to SEU rate of ultra-low voltage SRAM dominantly in terrestrial environment. In future technologies, SEU rate could dramatically increase at low voltage since critical charge also decreases with technology advancement. In SRAMs manufactured with finer lithography such as 16 nm or finer, the contribution of proton direct ionization would be observed even at a voltage much higher than 0.2 V. In this case, soft error can be a primary design concern for both high performance computing based on near-threshold computing and low power consumer and biomedical products.

Soft error mitigation techniques in process and circuit layer which are proposed in this thesis effectively prevent soft error from occurring in SRAM and sequential elements such as FF and latch. Combing these techniques in process and circuit layer with other architecture-level techniques is helpful for further reliability improvement. ECC, parity checking and data resending eliminate SEU occurring in SRAM and register files. The narrow DNW and DPW techniques prevent MBU and SEL occurrence in SRAM. Algorithmic checking and HIR detect and remove SEU in sequential element. The well-slit technique prevents MBU which the algorithmic checking cannot detect. In addition, SEILA reduces SEU in sequential elements to which algorithmic checking cannot be applied like control logic. The processor protected by these techniques attains a low missing rate of SBU, MBU and SEL in SRAM and MBU in sequential elements. This thesis contributes to current and future highly reliable microprocessor design.

Acknowledgments

First of all, I would like to express the deepest appreciation to Prof. Takao Onoye in Osaka University for providing me this precious study opportunity as a doctoral student in his laboratory.

I would like to express my sincere gratitude to Prof. Masanori Hashimoto in Osaka University for the continuous support of my Ph.D study and research. His guidance helped me in all the time of research and writing of this thesis.

I would like to express my appreciation to Prof. Kouji Nakamae and Prof. Yoshinori Takeuchi in Osaka University for detailed review and insightful suggestions.

I would like to express my sincere gratitude to Dr. Yoshiharu Tosaka for giving me a chance of working on the soft error reserch and sinposting the work.

I would like to demonstrate my gratitude to Mr. Hiroshi Namba, Mr. Hideya Matsuyama, Mr. Shigeo Satoh in Fujitsu Semiconcuctor, Mr. Ken Shono in Transphorm, Dr. Hideki Oka in RIKEN for being a receptive to working on the work and their support.

I would like to demonstrate my gratitude to Mr. Ryo Tanabe, Dr. Takashi Kato, Ms. Hiroko Mori, Mr. Shunichi Okano, Mr. Kaina Suzuki in Fujitsu Semiconductor, Dr. Ryozo Takasu in Fujitsu Laboratory, Mr. Ryuji Kan in Fujitsu for their invaluable help in the research.

I would like to demonstrate my gratitude to Prof. Kazutoshi Kobayashi, Dr. Jun Furuta, Mr. Kuiyuan Zhang in Kyoto Institute of Technology, Prof. Nobuyuki Sano in Tsukuba university, Prof. Yukinobu Watanabe in Kyushu University, Dr. Shinichiro Abe in Japan Atomic Energy Agency, Dr. Tohru Mogami, Dr. Ryo Harada in NEC, Dr. Shigetaka Kumashiro, Dr. Masami Hane, Dr. Shiro Kamohara, Mr. Kan Takeuchi, Mr. Hideyuki Nakamura in Renesas Electronics Corporation, Mr. Shumpei Kohri in STARC, Mr. Osamu Kobayashi in D-Crue, Dr. Takahiko Arakawa for their enormous help in the research.

I appreciate the support of Prof. Kenji Takahisa, Prof. Mitsuhiro Fukuda, Prof. Kichiji Hatanaka in Osaka University, Prof. Jun-ichi Hori, Dr. Hiroki Tanaka in Kyoto University, Mr. Olivier Lauzeral, Mr. Cyrille Beltrando, Ms. Anne-Lise Lhomme-Perrot, Mr. Erwin Schaefer in iRoC with the neutron irradiation tests.

I also appreciate the support of Mr. Hiroshi Iwata, Mr. Mitsuaki Igeta, Mr. Tomoya Tsuruta, Mr. Hiroshi Suzuki, Mr. Masataka Sato, Mr. Junji Iwahori in Fujitsu Semiconductor, Mr. Yasushi Kakimura in Fujitsu, Mr. Akifumi Nishiwaki, Mr. Masaki Komaki, Mr. Akio Yamamoto in Fujitsu VLSI with chip implementation and preparing test samples for the irradiation tests.

I would like to thank Mr. Hideo Yamashita, Mr. Tatsumi. Nakada, Mr. Yoshihiko Satsukawa, Mr. Iwao Yamazaki in Fujitsu, Dr. Chihiro J. Uchibori in Fujitsu

Laboratory for great discussions and comments.

I demonstrate my gratitude to Prof. Kazuyuki Hirose, Prof. Daisuke Kobayashi in Japan Aerospace Exploration Agency, Dr. Shinobu Onoda in Japan Atomic Energy Agency, Dr. Eishi Ibe in Hitachi, Mr. Takahiro Kuromiya in Cisco Dr. Kentaro Shibahara for their constructive discussion and advices.

Finally, I give my thank to my family for supporting my livelihood. Espetially, I genuinely express my deepest gratitude and love to my wife, Yoshiko.

Contents

1 Introduction 1
1.1 Permanent error and transient error . . . 1
1.2 Radiation effects . . . 2
1.2.1 Classification . . . 2
1.2.2 Mechanism of soft error . . . 3
1.2.3 Radiation in terrestrial environment . . . 7
Neutron flux . . . 7
alpha flux from device material . . . 10
1.2.4 Test for evaluation of soft error . . . 13
Alpha irradiation test . . . 13
Neutron irradiation test . . . 13
1.2.5 Soft error simulation . . . 15
1.3 Soft error in microprocessor . . . 18
1.3.1 Critical device from soft error perspective . . . 18
1.3.2 Techniques for improving microprocessor reliability . . . 19
1.4 Objectives of this thesis . . . 21

2 Technology trend of SER in bulk CMOS technology 25
2.1 Introduction . . . 25
2.2 Irradiation test procedure . . . 26
2.3 SRAM SER . . . 26
2.3.1 SEU trend on SRAM . . . 27
2.3.2 Cell type dependence on SRAM SER . . . 28
2.3.3 MBU trend in SRAM . . . 30
2.4 FF SER . . . 32
2.5 Chip-level processor SER . . . 33
2.6 Conclusion . . . 37

3 MBU mitigation with narrow deep N-well in SRAM 39
3.1 Introduction . . . 39
3.2 Experimental procedure . . . 40
3.3 Impact of Well depth on SER . . . 42
3.4 Impact of deep-N-Well on SER . . . 42
3.4.1 Neutron test result . . . 43
3.4.2 Alpha test result . . . 44
3.4.3 MBU analysis . . . 46

3.5 MBU mitigation . . . 48
3.5.1 Mitigation technique by narrow DNW . . . 49
3.5.2 Well structure analysis . . . 51
3.5.3 Mitigation efficiency evaluation . . . 51
3.6 Conclusion . . . 53

4 SEL mitigation with deep P-well in SRAM 55
4.1 Introduction . . . 55
4.2 SEL mitigation by deep P-well . . . 57
4.3 Experiment design . . . 57
4.4 Dependence on test type, data pattern and well-tap interval . . . 60
4.4.1 Dependences on test type and data pattern (TEST-1) . . . 61
4.4.2 Dependences on well-tap interval (TEST-2 and -3) . . . 62
4.5 Dependence of SEL on well configurations (TEST-4) . . . 64
4.6 Prevention efficiency on deep P-well (TEST-5) . . . 65
4.7 Discussion . . . 67
4.8 Conclusion . . . 70

5 MBU mitigation with well-slits in sequential element 71
5.1 Introduction . . . 71
5.2 Proposed mitigation technique with well-slit . . . 73
5.3 Irradiation test setup . . . 74
5.4 Experimental results . . . 77
5.5 Conclusion . . . 79

6 SBU mitigation in sequential element 81
6.1 Introduction . . . 81
6.2 Test procedure . . . 82
6.3 SEILA . . . 83
6.3.1 Review of conventional normal and radiation-hard latches . . . 83
6.3.2 Dual clock buffer (DCB) for SETLC mitigation . . . 85
6.3.3 Multi cell height for CCM mitigation . . . 87
6.4 SEU evaluation on SEILA . . . 89
6.4.1 SEU mitigation efficiency in 65 nm DHC-SEILA . . . 90
6.4.2 SEU mitigation efficiency on 28 nm DHC-SEILA . . . 92
6.4.3 SEU mitigation efficiency on 20 nm DHC-SEILA . . . 93
6.5 Conclusions . . . 98

7 SEU rate in SRAM at ultra-Low Voltage 101
7.1 Introduction . . . 101
7.2 Irradiation test procedure . . . 102
7.3 Experimental results . . . 103
7.4 Simulation . . . 107
7.5 Conclusions . . . 110

8 Conclusions 115

A Geometry factor calculation for alpha irradiation test 119
A.1 Geometry factor derivation 119
A.2 Perl code for GF calculation 121
A.3 Calculation example 122

Bibliography 125

List of Tables

1.1 Term definitions of soft error and hard error in the standards. 2
1.2 Definitions of fault, error and failure. 2
1.3 List of SEE phenomena. 4
1.4 Four MCU possible mechanism. 7
1.5 List of neutron and proton irradiation test facility. 16

2.1 List of evaluated SPARC processors. The instruction set architecture (ISP) are SPARC V9 in all model. 28
2.2 SRAM supply voltage and cell area normalized by that of 90 nm. . . 28
2.3 List of SRAM on 90 nm technology generation. SER values at 1.2 V (the last column) in the table were normalized by the average of these six SERs. 31
2.4 List of evaluated processors. 35

3.1 List of test chips. 41

4.1 Summary of test chip designs. The well-tap distances are normalized by that of DESIGN-B. Number in parentheses in well configuration represents the number of variation in dose. 59
4.2 Irradiation test list. 60
4.3 Well process conditions for DESIGN-D. 64
4.4 Normalized resistors of well with and without DPW. 67

5.1 SBU, MCU and MBU error-bit counts. 78
5.2 MCU counts (events) when stored value in neighboring bits are {0, 0}, {0, 1} and {1, 1} on vertical and horizontal sides. 79

6.1 List of tested latches. 83
6.2 Summary of SEU rates in SEILAs at 1.0V. The SEU rates are normalized with the SEU rate in 65 nm SHC-normal latch. Note that the SEU rates in 20 nm THC-SEILAs have no experimental data and the shown SEU rate is the average of SEU rates at 0.9 V and 1.1 V. . 98

8.1 List of countermeasures. 117

List of Figures

1.1 Classification of radiation effect in electron devices. 3
1.2 (Top) 15,000 flight traces of 5.4 MeV alpha particles normally irradiated on a silicon target. (Bottom) Stopping power curve of a 5.4 MeV alpha particle. These plots are generated with stopping and range of ion in matter (SRIM) software [1]. On average, the alpha particles stop at a depth of 27 μm. 5
1.3 Alpha (left) and neutron (right) induced soft error mechanisms. . . . 6
1.4 PBA mechanism. 6
1.5 Bonner balls and plastic schntillator. 8
1.6 Neutron spectra measured in open air and in the building at the Chikushi campus of Kyushu University, Japan. 9
1.7 Comparison of neutron attenuations contributed by the server structure and by the building. The shown flux is normalized with the flux without the server structure in open air. The attenuation by the building is measured with Bonner sphere and the attenuation by the server structure is calculated with PHITS simulation. 9
1.8 Decay chain of lead, which is a part of uranium decay series. The durations written in the boxes are the half-life. 11
1.9 Typical etch pits. 11
1.10 Emissivity values of (a) normal mold resins that are not controlled for alpha particles, (b) low-alpha (LA) mold resin, (c) solder, (d) underfill and Si-wafer, and (e) metals. Capital letters indicate different vendor names, and lowercase letters represent different products. Boxes represent the regions of $\pm 1\sigma$, and the horizontal lines expresses $\pm 2\sigma$, where σ means the standard deviation of the Poisson distribution and it corresponds to the counting uncertainty. 12
1.11 Alpha irradiation test in vacuumed atmosphere. 14
1.12 Alpha flux profile in 5 mm $\times$5 mm region in case that an alpha source whose diameter is 5 mm is placed above the die with 1 mm distance. 14
1.13 Spectra of RCNP, LANSCE, ANITA, and Sea level from JEDEC. Spectra of ANITA and sea level are multiplied by 0.3 and 150 million, respectively. 16
1.14 Total nuclear reaction cross section of high-energy proton and neutron in Si from the database [2]. 17
1.15 Neutron irradiation test setup in RCNP. 17

1.16 Steps of soft error occurrence and simulation tools for neutron and alpha induced soft error. 18
1.17 Structures of microprocessor (left) and core (right). 20
1.18 Data flow in a microprocessor. 20
1.19 Contributions and organization of the thesis. 22

2.1 SRAM SER per area normalized with 90 nm neutron SER characterized in neutron and alpha irradiation tests. Neutron flux is 13,000 times higher than alpha flux. 29
2.2 SRAM SER for alpha and neutron in SPARC V9 processor. Neutron flux is 13,000 times as large as alpha flux. These SERs were calculated from the data of Table 2.1and Figure 2.3. These SERs were normalized with neutron SER in SPARC64 V+ (90 nm). 29
2.3 SRAM SER per bit normalized with 90 nm neutron SER characterized in neutron and alpha irradiation tests. Neutron flux is 13,000 times higher than alpha flux. The test conditions and cell size are shown in Table 2.2. 30
2.4 Physical transistor layouts of SRAM cells of Type 1 and 4 [3]. Ld and Lg are the gate length and drain length. BL and WL stand for the bit line and word line. 30
2.5 Neutron-induced SERs of 90 nm SRAMs evaluated by irradiation tests, normalized with the average SER at 1.2V. 31
2.6 SRAM macro structure with 4col-MUX. 32
2.7 Ratios of SRAM MBU with ECC and 4-col MUX. Error bars represent 99.9% statistical confidence level with one(up)-sided estimation. The up-side estimation can be performed even when no errors are observed, and it is recommended in standards [4, 5]. 33
2.8 Neutron-induced SER of FFs normalized with SER of FFs manufactured with 65 nm double-well process at 1.0 V. Error bars represent 95% statistical confidence level. 34
2.9 Comparison between neutron-induced SRAM and FF SER. These SERs were evaluated with neutron irradiation test on DUT manufactured with double-well process. Error bars in FF data represent 95% statistical confidence level. 34
2.10 Ratio of SER in triple-well to SER in double-well in 65 nm technology. 35
2.11 SERs of FF and SRAM contributing to chip-level processor SER. These SERs are normalized with 65 nm SRAM SER without ECC. . 36

3.1 N- and P-well profile in CHIP-A and -B. 41
3.2 Neutron-induced SBU rates of CHIP-A and -B normalized by SBU rate of CHIP-B at 1.2 V. 42
3.3 Neutron-induced MCU rates of CHIP-A and -B normalized by MCU rate of CHIP-B at 1.2 V. 43
3.4 Alpha-induced SBU rates of CHIP-A and -B normalized by SBU rate of CHIP-B at 1.2 V. 43

3.5 Alpha-induced MCU rates of CHIP-A and -B normalized by MCU rate of CHIP-B at 1.2 V. 44
3.6 Neutron-induced SEU rates in double-well and triple-well normalized by SEU rate at 1.2 V in double-well. 45
3.7 Neutron-induced MCU rates in double-well and triple-well normalized by MCU rate at 1.2 V in double-well. 45
3.8 Neutron-induced SBU rates in double-well and triple-well normalized by SBU rate at 1.2 V in double-well. 46
3.9 Alpha-induced SEU rates in double-well and triple-well normalized by SEU rate at 1.2 V in double-well. 46
3.10 Alpha-induced MCU rates in double-well and triple-well normalized by MCU rate at 1.2 V in double-well. 47
3.11 Alpha-induced SBU rates on double-well and triple-well normalized by SBU rate at 1.2 V in double-well. 47
3.12 Measured neutron-induced MBU ratio (#MBU/#SEU) in double-well (CHIP-B) and triple-well (CHIP-C). 48
3.13 Measured alpha-induced MBU ratio (#MBU/#SEU) in double-well (CHIP-B) and triple-well (CHIP-C). 49
3.14 Proposed MBU mitigation technique. (a) layout of one bit SRAM, (b) cross-section of MBU mitigation structure, and (c) interconnection. N-wells (P-wells) of bit cells in the same word (i.e. the same BL number) were not connected. 50
3.15 (a) Topographic image obtained by AFM, (b) Observed SNDM image, (c) N-type carrier distribution, (d) P-type carrier distribution. . . . 52
3.16 Measured MBU rates in alpha irradiation experiment normalized by MBU rate at 1.2 V in double-well. Pseudo-MBU rates obtained by simulation are also plotted. 52
3.17 Measured MBU rates in neutron irradiation experiment normalized by MBU rate at 1.2 V in double-well. 53

4.1 Schematic of parasitic bipolar transistors contributing to SEL in a typical bulk CMOS structure. 56
4.2 Deep P-well structure. 58
4.3 Well configurations; (a) double-well (2W), (b) ordinary triple-well with deep N-well (DNW) and (c) with deep P-well (DPW). 58
4.4 Two types of test; (a) static and (b) dynamic tests. 61
4.5 TEST-1 result. SEL rates at 1.2 V on CHIP-A (2W) with error bars at 99% cofidential level. SEL rates are normilized by the SEL rate for static test with ALL0 pattern. 62
4.6 TEST-2 result. SEL rates in 55 nm SRAM at 1.2 V on DESIGN-E (2W), DESIGN-F (2W), DESIGN-G (2W), DESIGN-H (2W) and DESIGN-I (2W) with error bars at 99% confidential level with one(up)-sided estimation as a function of well-tap interval. SEL rates are normalized by the SEL rate of DESIGN-D(2W) shown in Figure 4.7. Note that no SELs were observed in DESIGN-E, -F and -H. 63

4.7 TEST-3 result. SEL rates in 90 nm SRAM at 1.2 V on DESIGN-B (2W), DESIGN-C (2W) and DESIGN-D (2W) with error bars at 99% confidential level with one(up)-sided estimation as a function of well-tap interval. SEL rates are normalized by the SEL rate of DESIGN-D (2W). Note that no SELs were observed in DESIGN-B. 63
4.8 TEST-4 result. SEU and SEL rates in six well process conditions listed in TABLE 4.3. SEU and SEL rates are normalized by SEU and SEL rates of W0 (reference), respectively. 64
4.9 N-well and DPW profiles of wafer of W1 , W8, W11, W13. Right mountain-like curves correspond to DPW. 65
4.10 TEST-5 result. SEL rate in W8, W11, W13 of DESIGN-G. SEL rates are normalized by SEL rate of DESIGN-C (2W) with ALL0, static test condition shown in Figure 7. Note that no SELs were observed in W11 and W13. 66
4.11 (a) Cross section and (b) top view of P-well resistor monitor. 67
4.12 TEST-6 result. SEL rates of DESIGN-J at room temperature (RT) and 85 degree Celsius. SEL rates are normilized by SEL rates at 1.3 V. Note that no SELs were observed with CLD and DPW, and at 1.1V and 1.2V with CLD. 68
4.13 TEST-7 results. SEL rates of DESIGN-A and DESIGN-K at room temperature (RT) and 85 degree Celsius. SEL rates are normalized by SEL rate of DESIGN-A (2W) with ALL0, static test condition. Note that no SELs were observed with CLD at 1.2V and with DPW and with CLD and DPW. 69
4.14 Chip level yields measured by wafer level test in 85 and 40 degree Celsius. 70

5.1 Circuits necessary for HIR. 72
5.2 MBL with clock buffer (8-bit). 73
5.3 Proposed MBU mitigation technique using well-slit for MBL. 74
5.4 Neutron test configuration at RCNP. This shows only the target, collimator and DUT boards. The other parts are same with other tests shown in Figure 1.15. 74
5.5 (a) MBL macro placement on the DUT, (a) layout of 8-bit MBL of two madros on DUT, (b) latch layout and (c) schematic of 1-bit latch. 75
5.6 Node values when retention data is (a) 0 and (b) 1. The input data of the latches are the same with the written data during hold operation. 76
5.7 Sensitive area when retention data is (a) 0 and (b) 1. 76
5.8 Test patterns of X-stripe and Y-stripe. 77
5.9 Control logic for 8-bit MBL in the DUT. 77
5.10 Test timing chart for the 28 nm latch array DUT. 78
5.11 MBU counts in neutron irradiation test on macro1 (normal) and macro2 (with well-slit) of 28 nm latches. 80

6.1 Schematic of normal non-robust latch. 83
6.2 SEILA schematic. 84

6.3 SEU and SETLC rates in case that retention data of all latches are 0 or 1 on 65 nm SHC-normal latch. The error bars show statistical error variations at 95% confidence level. 85
6.4 SEU and SETLC rates in case that retention data of all latches are 0 or 1 on 45 nm SHC-normal latch. The error bars show statistical error variations at 95% confidence level. 85
6.5 SEU and SETLC rates in case that retention data of all latches are 0 or 1 on 65 nm SHC-DICE. The error bars show statistical error variations at 95% confidence level. 86
6.6 Error count in TEST1 and TEST2 in 65 nm DHC-SEILA2. The error bars show statistical error variations of 68% confidence level. 87
6.7 CCM mitigation placement. In this placement, when an ion passes through the two critical areas, the ion must go through the cancelling area as well. In addition, when the charge is shared by the two critical areas, the charge must be also shared by the cancelling area. 88
6.8 Voltage variation estimated by device and circuit simulations (a) when the holes are collected to the PMOS drain connected to node3 and the PMOS drain connected to node4 in Figure 6.2and (b) when the holes are collected to the two drains above mentioned and the electrons are collected to the NMOS drain connected to node4. 88
6.9 Layouts of SHC, DHC and THC. 89
6.10 Placement of critical areas and cancelling area. A clock wire is routed in each cell height. Each latch draws clock signal from different two lines for DCB. 90
6.11 SEILA schematic and layout. 91
6.12 SEU rates of normal latch (65 nm SHC-normal latch), SEILAs (65 nm DHC-SEILA, 65 nm DHC-SEILA2) in (a) double-well (b) triple-well. The SEU rates are normalized with the SEU rate in 65 nm SHC-normal latch at 1.0V in double-well. 91
6.13 Latch array layout of the test chip for 65 nm latches. 91
6.14 SEU rates of latches located far or near from well-contacts in (a) 65 nm DHC-SEILA in double-well, (b) 65 nm DHC-SEILA in triple-well, (c) 65 nm DHC-SEILA2 in double-well and (d) 65 nm DHC-SEILA2 in triple-well. 93
6.15 Test timing chart for the 28 nm DUT. 94
6.16 SEU rates in 65 nm normal latch, 65 nm DHC-SEILA2 and 28 nm DHC-SEILA. All latches in this figure are manufactured with double-well process. The SEU rates are normalized with SEU rate in 65 nm normal latch at 1.0V. Error bars represent 90% statistical confidence level. 94
6.17 SEU rates in 28 nm DHC-SEILA of double-well for DATA0 and DATA1. The SEU rates are normalized with SEU rate in 65 nm normal latch at 1.0V. Error bars represent 90% statistical confidence level. 95
6.18 Board configuration for the 20 nm DUT. 96
6.19 Test timing chart for the 20 nm DUT. 96

6.20 SEU rates of 20 nm THC-SEILA in double- and triple-well. The SEU rates are normalized with SEU rate in 65 nm normal latch at 1.0V. Error bars represent 90% statistical confidence level. 97
6.21 SEU rates in 20 nm THC-SEILA for DATA0 and DATA1 with well-contacts (left) and without well-contacts (right). The error bars represent 90% statistical confidence level. 98

7.1 Neutron test configuration at RCNP for 90 nm SRAM. This shows only the target, collimator and DUT boards. The other parts are same with other tests shown in Figure 1.15. 103
7.2 (a) Schematic and (b) layout of SRAM for the irradiation tests. . . . 104
7.3 Timeline of the irradiation test. 104
7.4 Alpha and neutron SEU rates normalized by alpha and neutron SEU rates at 1.0 V, respectively. 105
7.5 A conceptual illustration of SEU rate contribution. 106
7.6 Neutron induced SBU and MCU rates. 107
7.7 Alpha induced SBU and MCU rates. 108
7.8 Simulated structure. 109
7.9 Contribution ratio of each particle in SRAM. 110
7.10 Calculated SEU rate originating from each secondary particle in SRAM. These SEU rates are normalized by the total SEU rate at 1.0 V as 1. 111
7.11 SEU rate comparison between measurement and simulation. 111
7.12 Production numbers of proton, alpha, Si and other heavy ions calculated with PHITS as a function of particle energy. A neutron beam having RCNP energy spectrum is given to Si substrate. 112
7.13 Production probability as a function of proton travel distance calculated from SRIM. 112
7.14 Stopping power of 2.0, 5.0 and 10 MeV protons on silicon, calculated by SRIM. The stopping power and the flight length of proton are lower and shorter than those of alpha, respectively, in comparison with Fig. 1.2. 113

A.1 Locations of alpha source ("1") and DUT chip ("2"). 119
A.2 Alpha dosage profiles on the die (5 mm × 5 mm) when using alpha sources of (a) 5 mm × 5 mm square, (b) 20 mm × 20 mm square, (c) 5 mm ϕ round, (d) 20 mm ϕ round shapes. The distance between the alpha source and the die is 1 mm. The scale of X and Y axes are millimeter, and the Z axis represents GF (non-dimension). 123
A.3 Alpha dosage profiles on the die (4 mm × 4 mm) when using a 8 mm ϕ alpha source. The centers of the source and die are misaligned, and the distance between the centers is (a) 0 mm, (b) 1 mm, (c) 2 mm and (d) 3 mm. The distance between the alpha source and the die is 1.5 mm. The scale of X and Y axes are millimeter and the Z axis represents GF (non-dimension). 124

Chapter 1

Introduction

This thesis focuses on soft error in microprocessors in terrestrial environment and discusses how to mitigate the soft error. This chapter describes the background and objectives of this thesis. First, permanent error and transient error are classified. Next, radiation effects are explained since soft error is one of radiation effects. After that, mechanism of soft error, radiation in terrestrial environment, and soft error measurement and simulation are explained. Then, the structure and reliability of high end microprocessors in mission critical servers, in which soft error is a critical issue, are discussed. Finally, the objective of this thesis is presented.

1.1 Permanent error and transient error

Advancement of CMOS process technology encounters the reliability degradation of manufactured chips. There are two types of errors which degrade the reliability of semiconductor devices; permanent error and transient error. Transient error is defined as nondestructive functional error. Permanent error means an irreversible change in operation, and it is typically associated with permanent damage to one or more elements of a device or circuit [4]. Permanent error is caused by aging effects, such as bias temperature instability (BTI) [6, 7, 8, 9], hot carrier injection (HCI) [10, 11], time dependent dielectric breakdown (TDDB) [12, 13], stress induced voiding (SIV) [14, 15], electro migration (EM) [16, 17] and inter-metal dielectrics TDDB (IMD-TDDB) [18, 19]. In addition, radiation effects invoke permanent and transient error.

Permanent error and transient error are also called hard error and soft error. Especially, when discussing radiation effects, soft error is more popular term. Or rather, in many cases, soft error is defined as nondestructive functional error caused by radiation [4]. Table 1.1 summaries the term definitions of soft error and hard error. In ISO26262 [5], a term, “hazard” is used as the same meaning with soft error. On the other hand, the other standardization documents of JEDEC [4], EIAJEDR4705 [20], IEC60749-38 [21], IEC62396-1 [22] and AEC-Q100-Rev.Gthe [23] use the term of “soft error”. Thus, this thesis also uses the term of “soft error”.

In addition, the occurrence of faulty operations is often divided into three layers or hierarchies; fault, error and failure, as summarized in Table 1.2. This definition is proposed in [24]. Fault is defined as disturbance which can cause error, such as noise. Error is data flip in memory elements such as static random access memories

Table. 1.1 Term definitions of soft error and hard error in the standards.

Standard	[Term]: definition
JESD89A	[Soft error]: an nondestructive functional error by energetic ion strike. [Hard error]: an irreversible change in operation that is typically associated with permanent damage to one or more elements of a device or circuit.
EIAJ-EDR-4705	[Soft error]: an SEU in a latch or memory cell that can be correctly rewritten. [Hard error]: a permanent circuit or device failure.
IEC60749-38	[Soft error]: an erroneous output signal from a latch or memory cell that can be corrected by performing one or more normal functions of the device containing the latch or memory cell. Note that as commonly used, the term refers to an error caused by radiation or electromagnetic pulses and not to an error associated with a physical defect introduced during the manufacturing process.
IEC62396	[Soft error]: an term refers to invalid state changes in digital electronic logic cell(s) that could be induced by atmospheric radiation and which are recoverable by cycling the power off and on.
AECQ100	Following JESD89.
ISO26262	[hazard]: potential source of harm caused by malfunctioning behavior of the item.

Table. 1.2 Definitions of fault, error and failure.

Faulty conditions	Definition
Fault	Local transient noise. Impact is not deterministic on device, circuit and system.
Error	Retention data is flipped in element like memory and latch caused by faults. Impact is not deterministic on circuit and system
Failure	System malfunction caused by error.

(SRAMs), dynamic random access memories (DRAMs), flash memories and sequential elements such as flip-flops (FFs) and latches. Failure means system malfunction, such as sudden shut-down and abnormal operation, and it is caused by error. Incorrect calculation by using super computers can be categorized into failure. Note that the standards [23, 21, 22, 5, 3, 4, 20] do not define the means of the terms, fault, error and failure.

1.2 Radiation effects

1.2.1 Classification

Radiation effects can lead to hard and soft errors. There are three radiation effects in electron devices; displacement damage dose effect (DDD), total ionizing dose effect (TID), and single event effect (SEE). Figure 1.1 categorizes the radiation effects. TID and DDD cause hard error, and SEE can cause soft and hard errors. TID is often observed as the performance degradation of transistor due to total dose in oxide [25]. In

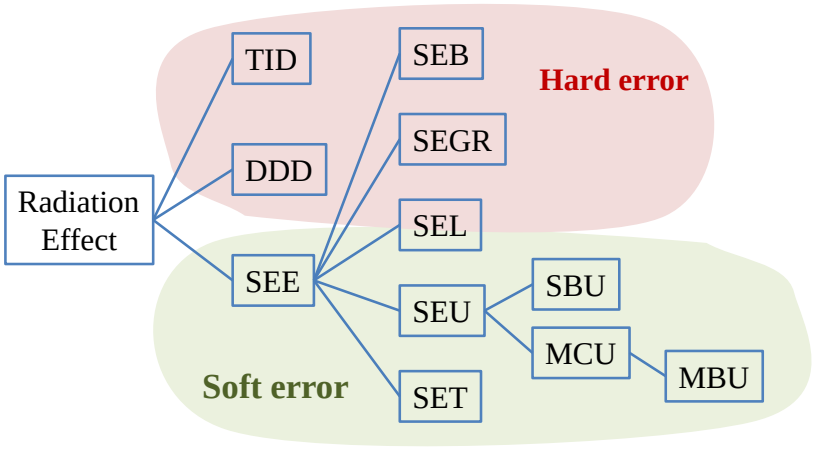


Fig. 1.1 Classification of radiation effect in electron devices.

MOS devices, irradiations induces both the buildup of oxide-trapped charges mainly positively charged in SiO_2, and the generation of interface traps at silicon-oxide interfaces which are either positively or negatively charged in PMOS or NMOS devices. DDD displaces the constituent atom of electron device [26, 27, 28, 29]. The displaced atom and consequent vacant lattice point degrade the performance of the electron devices. DDD is also called bulk damage. Generally, TID and DDD are serious concerns in harsh radiation environment such as in the space, and they are almost negligible in human living environment [25, 26, 27, 28, 29]. For achieving the high reliability of processors used in terrestrial environment, processor designers need to pay attention to SEE. Therefore, this thesis focuses on SEE. Note that TID tolerance is required for a chip in medical electronic tag even in terrestrial environment because the tags are sometimes sterilized by gamma ray. It is reported that ferroelectric random access memory (FeRAM) has enough TID tolerance for such medical electronic tags [30].

SEE is caused by a single event of a particle incident. The charge generated by the incident leads to soft and/or hard errors. Table 1.3 summarizes SEE. SEE includes following phenomena; single event transient (SET), single event upset (SEU), single event latchup (SEL), single event burnout (SEB) and single event gate rupture (SEGR). SEU includes single bit upset (SBU), multiple cell upset (MCU), multiple bit upset (MBU) and they sometimes lead to single event functional interrupt (SEFI). SEB and SEGR are sometime called single event gate damage (SEGD), and they occur mostly in power devices. Therefore, this thesis focuses the other mechanisms of SET, SEL, and SEU.

1.2.2 Mechanism of soft error

In 1979, T. C. May et al. revealed that the cause of soft errors was alpha particles (helium nucleus) from some radioactive contaminants in device materials [31]. At this moment, soft error occurred in dynamic random access memory (DRAM) [31]. Although the memory density and size used in a system exploded, DRAM soft error did not increase much because the electric capacitance for data retention in DRAM

Table. 1.3 List of SEE phenomena.

Abbreviation	Full word	Explanation
SET	Single Event Transient	A momentary voltage excursion (voltage spike) at a node in an integrated circuit caused by a single energetic particle strike.
SEU	Single Event Upset	An error caused by the transient signal induced by a single energetic particle strike.
SBU	Single Bit Upset	SEU in a single bit of memory or sequential element.
MCU	Multiple Cell Upset	A single event that makes several bits fail at one time.
MBU	Multiple Bit Upset	MCU that includes two or more error bits in the same word.
SEL	Single Event Latchup	An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure resulting in the loss of device functionality.
SEB	Single Event Burnout	Burnout of a powered electronic component or part as a result of the energy absorption triggered by a single radiation event.
SEFI	Single Event Functional Interrupt	A soft error that makes a component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and on) to restore operability, unlike SEL, and may result in permanent damage as SEB.
SEGR	Single Event Gate Rupture	Burnout by high-current on the gate in high power FET as a result of the energy absorption triggered by a single radiation event.

did not decrease [32]. Even in enormous memory in a huge system for big data, soft error occurring in DRAM is not a main reliability issue [33]. On the other hand, soft error occurring in complementary metal-oxide semiconductor (CMOS) circuits, such as SRAM, sequential element and other logic, has become a critical concern in electron device reliability.

Next, the process of soft error occurrence due to alpha particle is explained. The alpha particle from the contaminants has around 5.4 MeV energy, and its flight distance is about 27μm in silicon (Si) as shown in Figure 1.2. The alpha emitted from the contaminants travels in silicon and generates electron-hole pairs, i.e. charge, by ionization on the alpha track as shown in Figure 1.3. The generated charge is collected to the drain of a MOSFET by drift and diffusion. When an alpha particle hits NMOS, electrons are collected to the NMOS drain. In case of PMOS hitting, holes are collected to the PMOS drain. The collected charge (Qcoll) becomes noise current and induces voltage variation. When such voltage variation occurs in an SRAM cell, data upset, i.e. soft error, may occur. Here, the collected charge determines whether the data upset occurs or not. When Qcoll is higher than the critical charge (Qcrit) of the circuit, data upset occurs. In other words, Qcrit is the minimum charge to cause soft error. The charge is collected not only by the charge drift-diffusion but also par-

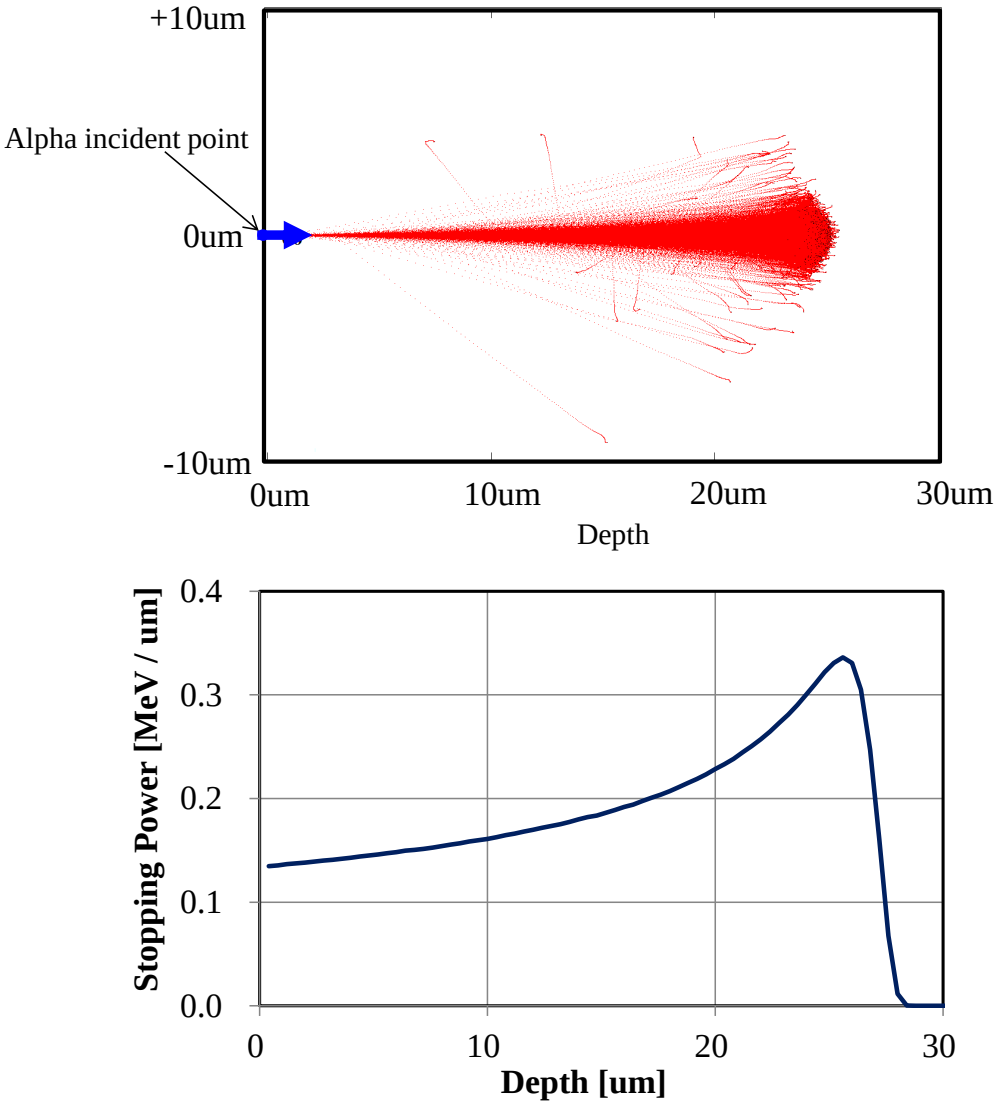


Fig. 1.2 (Top) 15,000 flight traces of 5.4 MeV alpha particles normally irradiated on a silicon target. (Bottom) Stopping power curve of a 5.4 MeV alpha particle. These plots are generated with stopping and range of ion in matter (SRIM) software [1]. On average, the alpha particles stop at a depth of 27 μm.

asitic bipolar action (PBA) as shown in Figure 1.4. The direct ionization generates the same number of electrons and holes, and the electrons are collected to the drain by drift-diffusion as mentioned earlier. In addition, the holes in the well flow to the well tap through the resistive substrate, which elevates the well potential and makes the parasitic bipolar transistor (drain-well-source) turn on. The on bipolar transistor passes current to the drain.

The PBA can cause MCU because the well is shared by some transistors. The well potential elevation is a local phenomenon, but still it is shared by some transistors and consequently some parasitic bipolar transistors turn on. In a result, data upset occurs in multiple SRAM cells. MCU is caused by not only PBA but also other

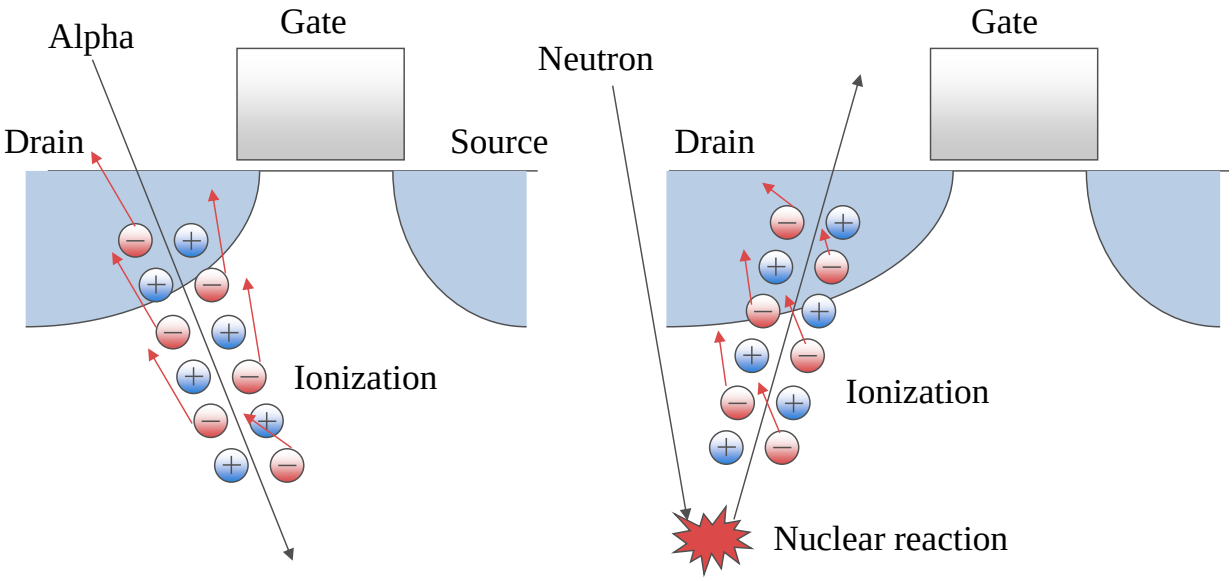


Fig. 1.3 Alpha (left) and neutron (right) induced soft error mechanisms.

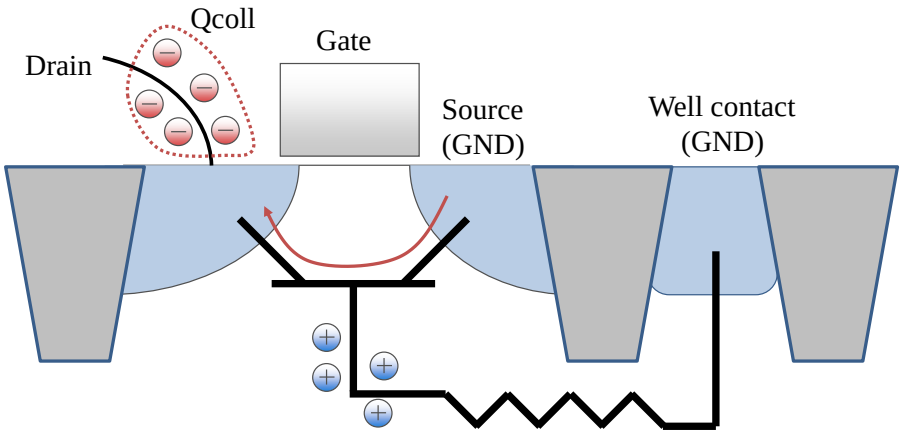


Fig. 1.4 PBA mechanism.

mechanisms. Table 1.4, which comes from [34], lists four possible mechanisms of MCU. It is manifested that the main reasons of MCU were (C) charge sharing and (D) PBA in 130 nm technology [34]. Charge sharing (C) is a phenomenon that the generated charge is collected to the drains of multiple transistors in a well by drift and diffusion. Data bits which share a well are thus vulnerable to both (C) and (D). Furuta et al. reported that in 65 nm FFs, 97% of MCUs occurred in the latches sharing the same P-well, and this suggests that the main reasons of MCU in 65 nm technology are (C) and (D) [35].

Neutron originating from cosmic ray also induces soft error through nuclear reaction with atomic nucleus of transistor materials [36]. The nuclear reaction generates charged secondary particles like protons, alpha particles and heavy ions. The charged particle generates charge (electron-hole pairs) by ionization on the particle track as

Table. 1.4 Four MCU possible mechanism.

Symbol	Name
(A)	Successive hits by one ion
(B)	Multi hits by multiple ions
(C)	Charge drift/diffusion (charge sharing)
(D)	PBA

shown in Figure 1.3. The generated charge is collected to drain by drift and diffusion and it causes soft error, which is similar to the case of alpha particle. To provoke the nuclear fission of Si atomic nucleus, over 5 MeV energy of the neutron is necessary. On the other hand, thermal neutron, whose energy is below 5 MeV, can also induce soft error. This is because thermal neutron has a large cross section (3000 barn) for the reaction with bolon-10 (^{10}B) nucleus and a 0.84 MeV lithium (Li) nucleus and a 1.47 MeV alpha particle are emitted in this reaction. The ^{10}B is contained in the electron devices manufactured using boron phosphorus silicon glass (BPSG) for local oxidation of silicon (LOCOS) in back-end wafer process. In those devices, the contribution of the thermal neutron to SRAM soft error is about four times higher than the high energy neutrons in terrestrial environment [37]. On the other hand, chemical mechanical polishing (CMP) process has superseded LOCOS in back-end wafer process after around 180 nm technology generation, and the thermal neutron-induced soft error had become negligible small. However, thermal neutron-induced soft error is observed again in recent devices [38, 39, 40]. The cause was the B ^{10} in B_2H_6 carrier gases used in the forming process of tungsten (W) contact plug. It is reported that optimizing the process of using B_2H_6 can suppress the soft error caused by thermal neutron [41].

In addition, cosmic ray induces not only neutron but also muon, and the muon may contribute to soft error when Qcrit is below 0.1 fC in future devices

1.2.3 Radiation in terrestrial environment

Neutron flux

Cosmic ray is the most dominant source of soft error in terrestrial environment, and its flux depends on solar cycle, altitude and latitude [4]. The solar cycle have an average duration of about eleven years, and the flux of neutron generated by cosmic ray in the air can change by up to 14%. The flux increases at a high altitude due to a decrease in air shielding. The neutron flux at 4,000 meter altitude is about 20 times higher than that at sea level. The neutron flux at a flight altitude is further higher, and hence avionics needs to pay more attention to soft error. The latitude is also a factor of neutron flux in terrestrial environment because the geomagnetic field, which attenuates the neutron flux, depends on the latitude. An excel-based program for calculating atmospheric cosmic-ray spectrum (EXPACS) [42, 43] calculates the fluxes taking into account the effects of the solar cycle, altitude and latitude.

The neutron flux can be accurately measured with Bonner sphere and/or plastic scintillator [44, 45, 46, 47]. The flux measurement with a combination of Bonner sphere and plastic scintillator, whose setup is exemplified in Figure 1.5, achieved the

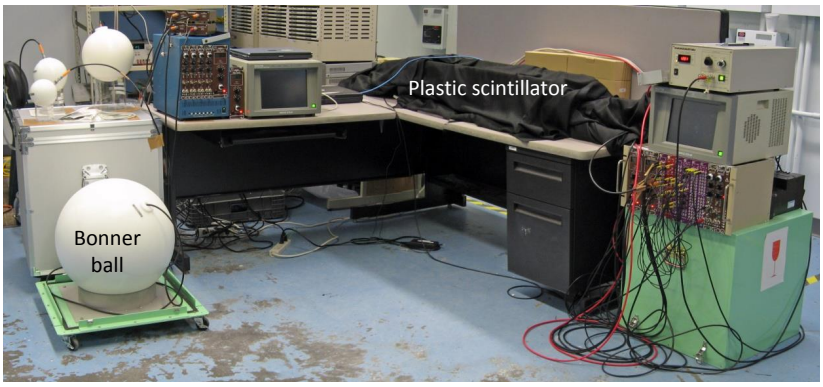


Fig. 1.5 Bonner balls and plastic schntillator.

measurement of wide energy spectrum neutron [45].

Figure 1.6 shows an example of the neutron spectra measured by the Bonner spheres in open air and on several floors of the building at the Chikushi campus of Kyushu university in Japan [47]. Six ^{3}He counters, which can detect thermal neutrons through the reaction of ^{3}He(n, p), are employed in this measurement. The ^{3}He counters are surrounded by polyethylene spheres having different thicknesses of 0, 15, 30, 50, 90 and 200 mm, where 0 mm corresponds to a bare ^{3}He counter without polyethylene. The polyethylene sphere acts as a moderator for incident neutron. The variety of polyethylene thickness thus enables the counters to detect a wide range of neutron energy. As the thickness increases, the Bonner sphere becomes sensitive to higher energy neutrons. The range of neutron energy spectra obtained in our measurement covers from 0.01 eV to 10 GeV. Furthermore, the maximum entropy deconvolution (MAXED) code was employed for accurately unfolding the measured data [48]. The initial spectrum for the unfolding is obtained by EXPACS.

Actual neutron flux injected to electron devices is affected by attenuations due to not only the building but also the equipment structure in which the device is installed. Figure 1.7 exemplifies the neutron attenuation by the server structure and the building [47]. These neutron flux are normalized by that without the server structure in the open air. Here, the microprocessors in flip chip ball grid array (FC-BGA) packages are mounted on the PCB board and the 18 boards are installed in a rack with water cooling system. The total weight and average density is about 1570 kg and 1.1 g/cm^3, respectively. The attenuation due to the building was measured with Bonner spheres, and the attenuation by the server structure was calculated by particle and heavy ion transport code system (PHITS) simulation [49]. Figure 1.7 demonstrates that the neutron flux decreased by 93% at the 1st floor. The difference between the open air and 5th floor corresponds to the attenuation due to the server structure. At the 1st floor, the attenuation thanks to the building is slightly larger than that by the server structure. This result clearly indicates that the main contributor of neutron shielding changes depending on the server location.

Thus, the actual neutron flux given to chips needs to be estimated taking into account solar cycle, altitude, latitude and attenuations by building and equipment.

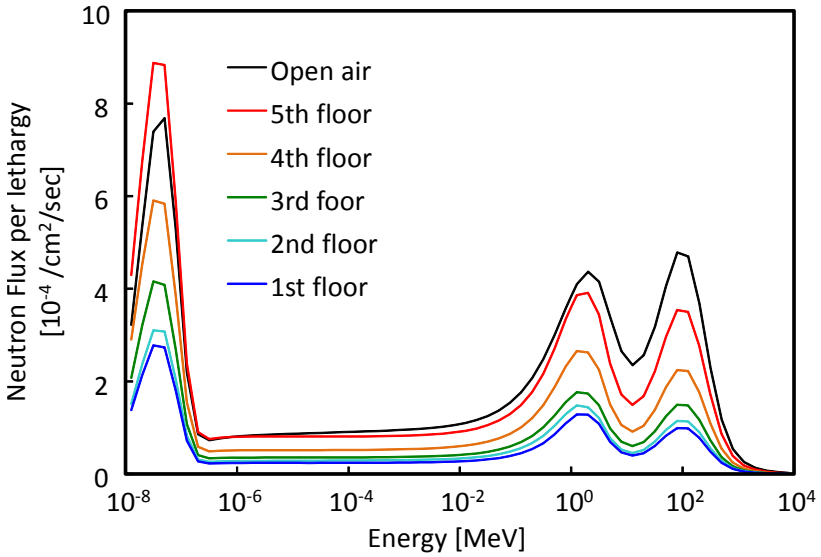


Fig. 1.6 Neutron spectra measured in open air and in the building at the Chikushi campus of Kyushu University, Japan.

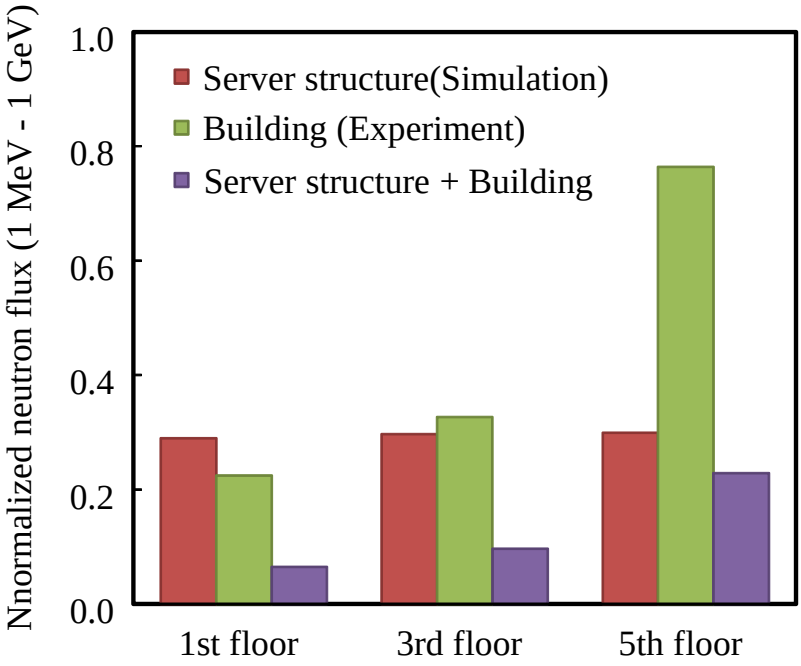


Fig. 1.7 Comparison of neutron attenuations contributed by the server structure and by the building. The shown flux is normalized with the flux without the server structure in open air. The attenuation by the building is measured with Bonner sphere and the attenuation by the server structure is calculated with PHITS simulation.

alpha flux from device material

Alpha flux depends on the amount of radioactive contaminant within 27 μm from transistor. Note that the materials in the area within 27 μm from transistor are mainly SiO_2, lead (Pb) and copper (Cu), and these flight length of the alpha particle is the same or less than the length in Si [50]. The contaminants exist in wafer process material, such as Cu for metal interconnects, package material, such as resin and filler in plastic package, and bump materials, such as tin (Sn), silver (Ag) and lead (Pb). Especially, Pb itself can be radioactive isotope as shown in Figure 1.8. The Pb materials includes ^{210}Pb because of long half-life (22 years). The ^{210}Pb emits alpha particle after two times beta-decay. Note that using Pb in products is restricted by the Restriction of Hazardous Substances (RoHS), and lead-free products are becoming popular [51]. In addition, material companies recently supply low alpha grade material for electron devices, such as low alpha (LA), ultra-low alpha (ULA) and super ultra-low alpha (SULA) grade materials [52]. The alpha-induced soft error can be suppressed by using the low alpha materials with some cost increase (roughly 10X higher cost).

For achieving high reliability quality assurance, the adoption of such low alpha grade materials is mandatory. In the assurance, it is necessary to characterize the alpha emissivity of the low alpha materials accurately for evaluating alpha-induced soft error rate (SER) [53, 54, 55, 52, 56, 57, 58]. Vacuum alpha tracking (VAT) is one of the accurate evaluation methods, and the minimum detectable flux can be lowered to 4.9×10^{-2} alpha/khour/cm^2 [56]. A polymer detector is used in VAT as a solid-state detector (SSD) in a vacuum environment. Columbia resin 39 (CR-39) was used for the SSD because CR-39 offers several advantages such as insensitivity to X- and γ-rays, minimal fading, and high optical transparency [59]. The alpha-tracking technique is outlined briefly as follows. When an alpha particle arrives at the polymer detector, the polymer chain in the illuminated area is cut at the molecular scale. When a polymer detector with molecular nicks is etched by an alkali solution, the nicks are extended into the etch pits at the micrometer scale. After this procedure, the alpha particles can be observed as the etch pits on the polymer detector as shown in Figure 1.9. Keeping the exposure environment vacuum prevents noise radiation due to radon isotopes in the air, and it enables alpha flux evaluation for low emissivity materials. Moreover, this technique excludes alpha particles from the chamber walls, because the sample can have face-to-face contact with the polymer detector. Figure 1.10 shows the alpha emissivity of the following materials measured by VAT; normal mold resins that are not controlled for alpha particles, LA mold resin, solder, under-fill and a silicon wafer, and metal. The emissivity of normal mold resins has a wide distribution of 3.7 - 35 alphas/kh/cm^2, and it depends on the product type, even from the same vendor. This measurement also observed an emissivity distribution of 0.06 - 0.87 alphas/kh/cm^2 in LA mold resin. The alpha emissivity of solder depends not only on the material type but also on the alpha rank, i.e. , standard (STD), ULA, or SULA. This measurement also evaluated the under-fill and the Si-wafer.

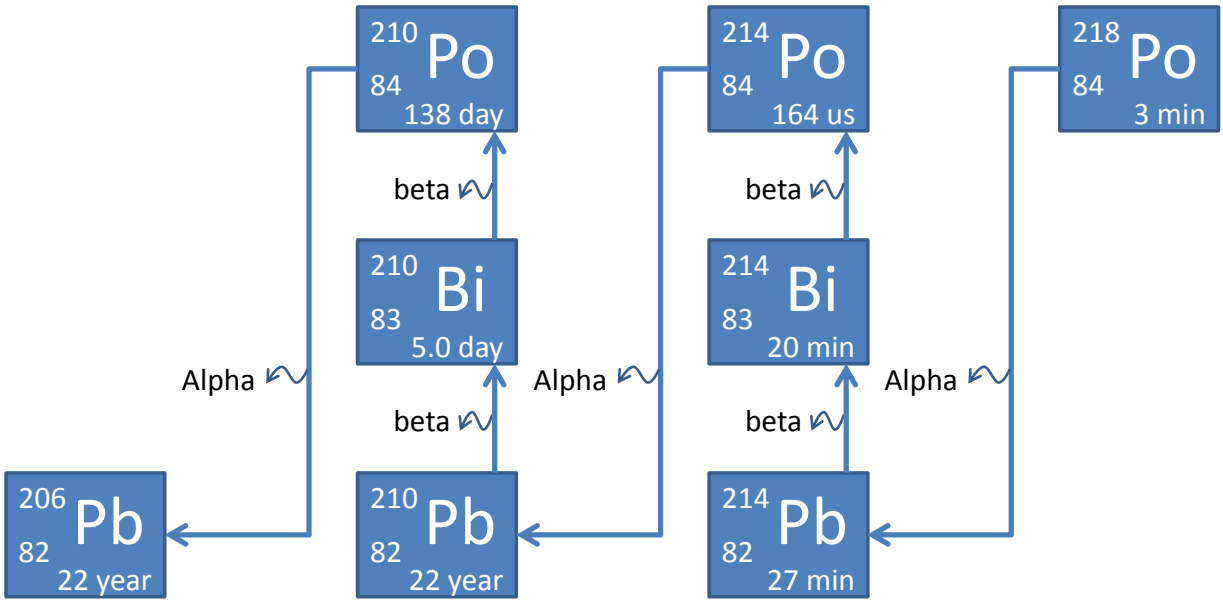


Fig. 1.8 Decay chain of lead, which is a part of uranium decay series. The durations written in the boxes are the half-life.

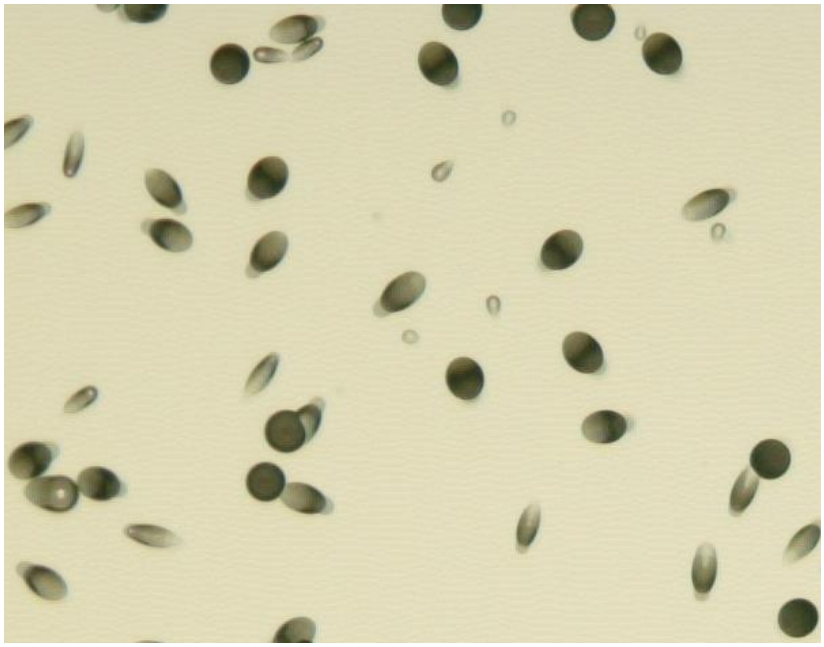


Fig. 1.9 Typical etch pits.

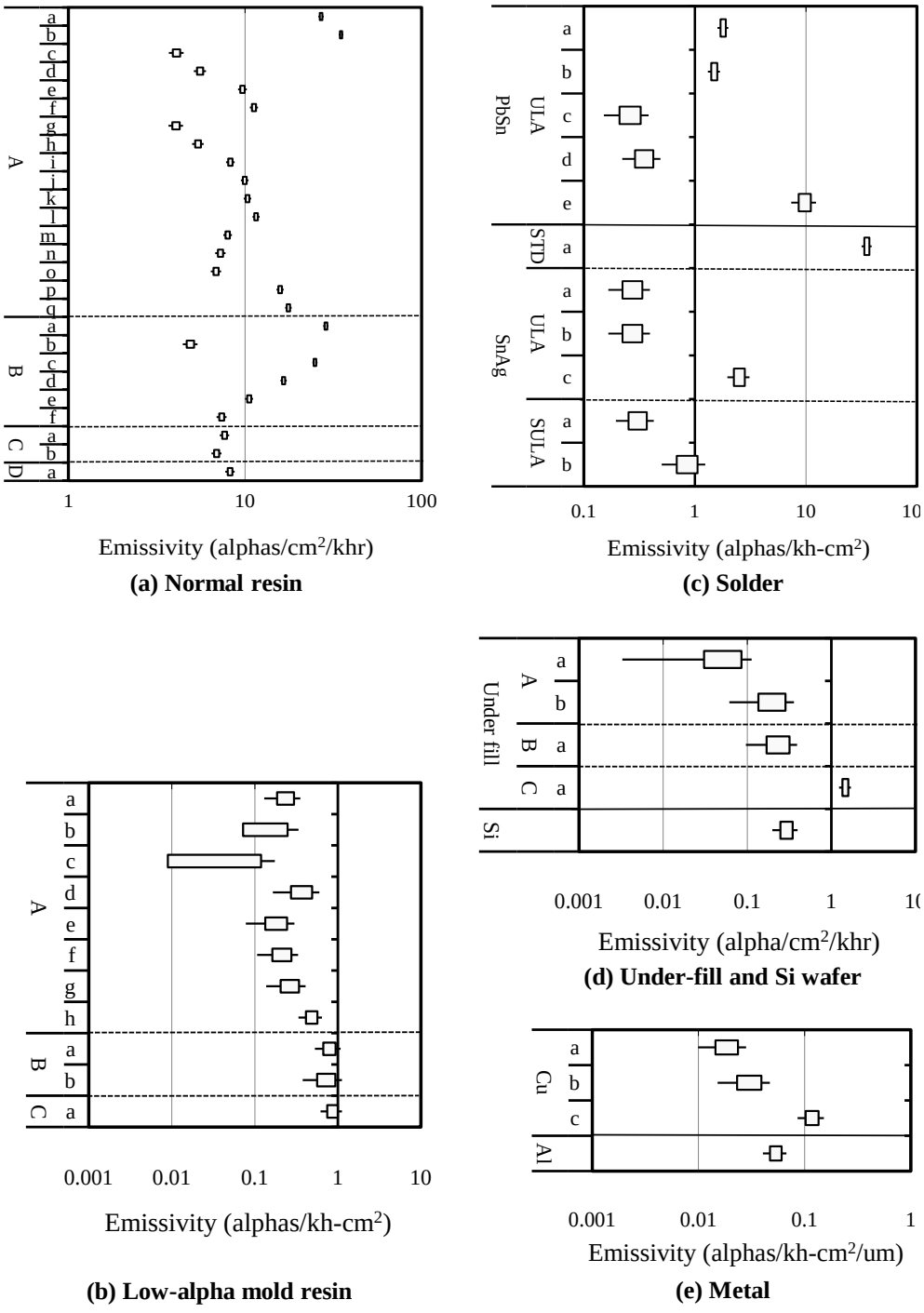


Fig. 1.10 Emissivity values of (a) normal mold resins that are not controlled for alpha particles, (b) low-alpha (LA) mold resin, (c) solder, (d) under-fill and Si-wafer, and (e) metals. Capital letters indicate different vendor names, and lowercase letters represent different products. Boxes represent the regions of $\pm 1\sigma$, and the horizontal lines expresses $\pm 2\sigma$, where σ means the standard deviation of the Poisson distribution and it corresponds to the counting uncertainty.

1.2.4 Test for evaluation of soft error

For choosing soft-error mitigation techniques and ensuring quality in design time, it is crucially important to know SER. For evaluating SER, measurement based test and simulation are two representative approaches. This subsection discusses the former measurement based test. The simulation will be explained in the next subsection.

For evaluating SER of electron devices, measurement based test is widely performed. Although SER evaluation test is often carried out for actual products, it cannot be done for all products since the evaluation time and cost are high. Generally, the test is carried out for element circuits like SRAM and FF, and chip level SER is estimated from the SER of those elements. As mention before, alpha and neutron are the main sources of soft error. Therefore, SERs for alpha and neutron should be evaluated. For such evaluations, accelerated neutron and alpha irradiation tests are performed. In addition, such SER test is important for evaluating efficiencies of soft-error mitigation techniques. The following explains the irradiation test.

Alpha irradiation test

Alpha induced SER is often evaluated with alpha source, Americium-241 (^{241}Am) or Thorium-232 (^{232}Th), where it is easy to use ^{241}Am of less than 10 kBq under Japanese regulations. Figure 1.11 shows a typical setup of alpha irradiation test. For this test, a bare sample die must be irradiated from the side of back-end of line (BEOL). Therefore, wire bonding chips are prepared as device under test (DUT). The test cannot be performed for a chip in flip chip package unless using special techniques such as hot under fill (HUF) technique [60]. The package surface is de-caped using fuming nitric acid for removing the resin between the die and the alpha source. If the die is coated by polyimide, it also should be removed by ethylenediamine or hydrazine. Note that hydrazine is designated as hazardous substances by Japanese regulation. Furthermore, the test is better to be carried out in low pressure atmosphere in a vacuum chamber for reducing the air shielding effect.

The distance between the alpha source and the die is recommended to be less than one millimeter in [4]. If the length is longer than one millimeter, it is necessary to calculate the exposure flux on the die in the irradiation test. The flux is calculated from the alpha source radioactivity, the distance between the alpha source and the die, and the sizes of the alpha source and the die. For such a purpose, geometry factor (GF), which is the ratio of exposure flux on the sample die to the flux of an alpha source, is often used. The GF derivation is included in Appendix A. Note that a larger-sized alpha source is suitable for the irradiation test, because the alpha flux becomes more uniform on the die. If the alpha source is not large enough compared to the die, the flux depends on the location and it is not uniform as shown in Figure 1.12.

Neutron irradiation test

Terrestrial neutron induced SERs can be evaluated by neutron irradiation tests with quasi-monochromatic or spallation neutron beam, where the spallation neutron beam has a widely spread energy spectrum. The test with the spallation neutron beam can evaluate the terrestrial neutron SER by one time irradiation while a number of beam

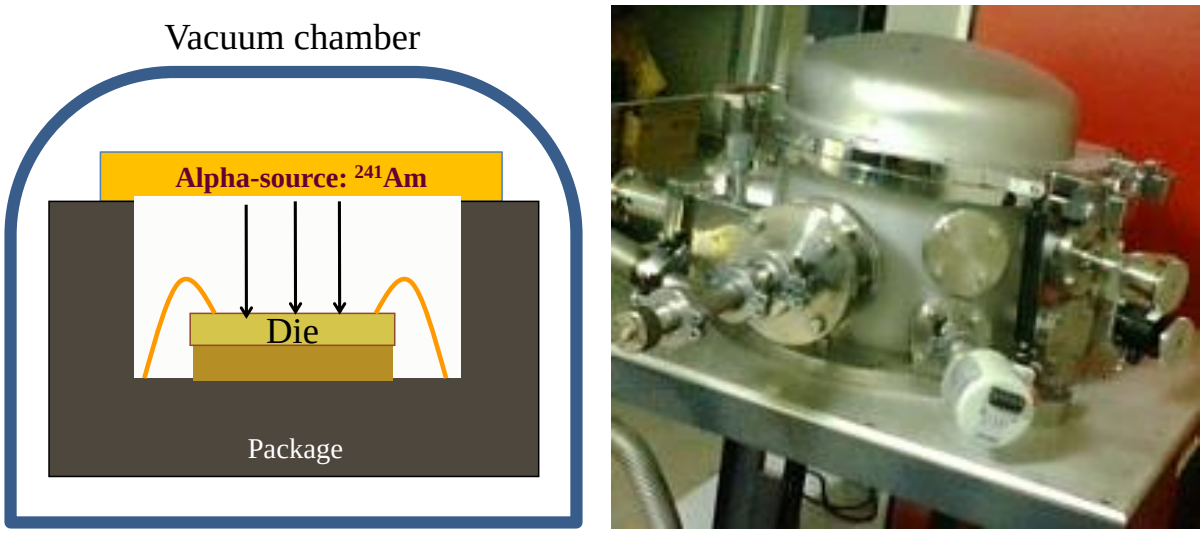


Fig. 1.11 Alpha irradiation test in vacuumed atmosphere.

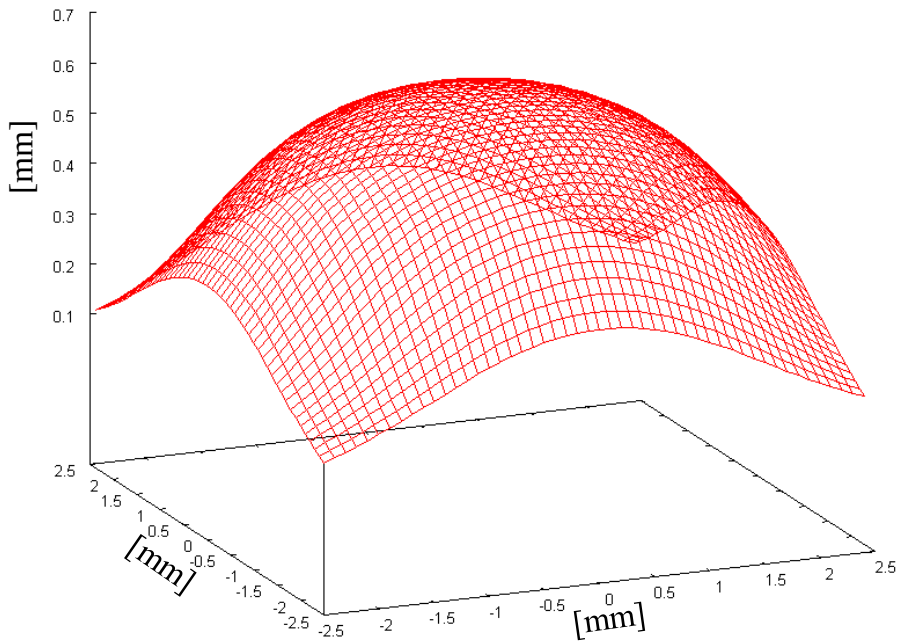


Fig. 1.12 Alpha flux profile in 5 mm ×5 mm region in case that an alpha source whose diameter is 5 mm is placed above the die with 1 mm distance.

irradiation tests are necessary to sweep the neutron energy when quasi-monochromatic beams are used. The spallation neutron beams are available at Research Center for Nuclear Physics (RCNP) at Osaka University, the Weapons Neutron Research (WNR) Center at Los Alamos Neutron Science Center (LANCE), and Atmospheric-like Neutrons from thIck TArget (ANITA) of the Svedberg Laboratory (TSL) at Uppsala University [61, 62, 63]. The energy spectra of these neutron beams are similar with the terrestrial environment spectrum as shown in Figure 1.13 and hence suitable for evaluating SEE for terrestrial neutrons. Table 1.5 also shows a list of neutron irradiation facility. In some cases, proton irradiation test is carried out for estimating neutron-induced SER because high flux proton beam is available at more facilities and the cross sections of proton and neutron to silicon are similar at more than 10 MeV particle energy as shown in Figure 1.14. A cross section is the effective area that governs the probability of scattering, reaction or absorption event. Here (in nuclear and particle physics), the concept of a cross section is used to express the likelihood of interaction between particles. The cross section showed in Figure 1.14 corresponds to the probability of reaction of neutron and proton with Si. However, the test result includes some error because the proton cross section does not perfectly match with the neutron cross section. For accurately estimate neutron SER, neutron beam must be used.

Figure 1.15 exemplifies the neutron irradiation setup at RCNP. Test operators, i.e. human beings, cannot stay in the irradiation room during the beam irradiation, and then they operate measurement equipment, such as LSI tester, and DUTs at the control room. Recent LSI testers can be controlled via USB, but the maximum length of USB cable is not long enough. Thus, a USB extender with LAN cable is useful for such test environment. Soft error can also occur also in the tester in the irradiation room, and the tester may fall into an abnormal operation. In such a case, the tester is turned off and on using a USB-controllable AC tap from the control room.

1.2.5 Soft error simulation

This section explains soft error simulation. As explained in Section 1.2.4, the irradiation tests can evaluate SER effectively. However, the test cannot be carried out for all logic elements since the test cost is high and a normal standard cell library usually has several hundred logic cells. Simulation is a key technology for estimating SER of various elements,.

As explained in Section 1.2.2, neutron induced soft error is produced through the following process:

1) Nuclear reaction between a neutron and an atom in a device
2) Charge deposition by a secondary ion generated by the reaction
3) Charge collection to MOS drain terminal
4) Abnormal circuit behavior triggered by the collected charge

Note that 1) is not necessary in the evaluation of alpha induced SER. PHITS and Geant4, which are simulation codes for particle transport, can calculate 1) and 2) [49, 64, 65]. SRIM can also compute 2) [66, 1, 67]. Technology computer aided design

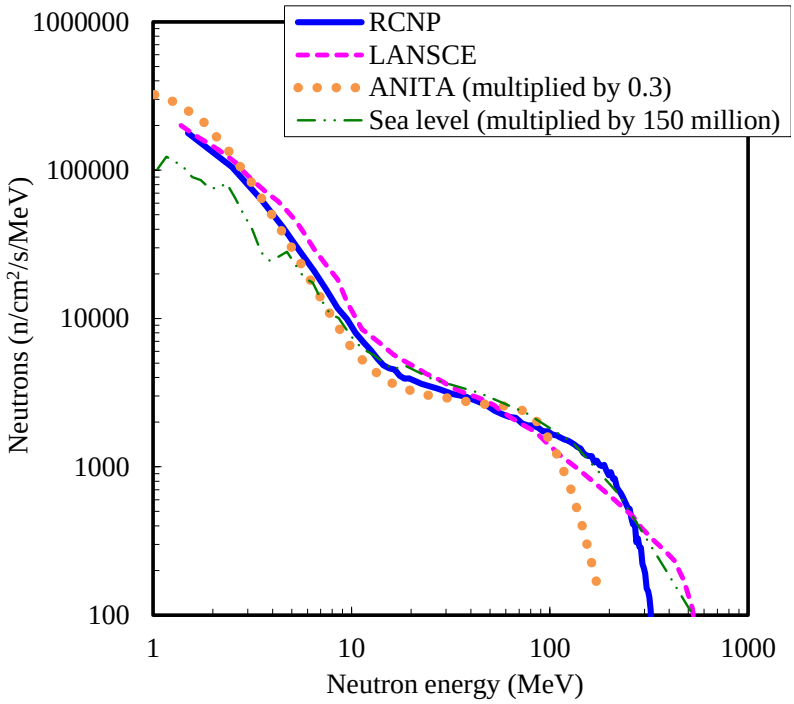


Fig. 1.13 Spectra of RCNP, LANSCE, ANITA, and Sea level from JEDEC. Spectra of ANITA and sea level are multiplied by 0.3 and 150 million, respectively.

Table. 1.5 List of neutron and proton irradiation test facility.

Facility name	Country	Quasi-monochromatic neutron	Broad spectrum neutron	Proton
RCNP at Osaka Univ.	JAPAN	100-392 MeV	<392 MeV	100-392 MeV
J-PARC	JAPAN	-	<400 MeV	-
CYRIC	JAPAN	35-65 MeV	-	<80 MeV
TIARA at JAEA	JAPAN	-	-	10-80 MeV
NIRS	JAPAN	-	-	<70 MeV
WERC	JAPAN	-	-	10-200 MeV
LANL, LANSCE at WNR	USA	-	<800 MeV	-
TSL ANITA at Upsala Univ.	Sweden	10-175 MeV	<180 MeV	<180 MeV
TRIUMF	Canada	-	<400 MeV	65-120 MeV
ISIS	UK	-	<800 MeV	-
CNL at Univ. of California	USA	<65 MeV	-	1-67.5 MeV
UCL	Belgium	-	-	62 MeV

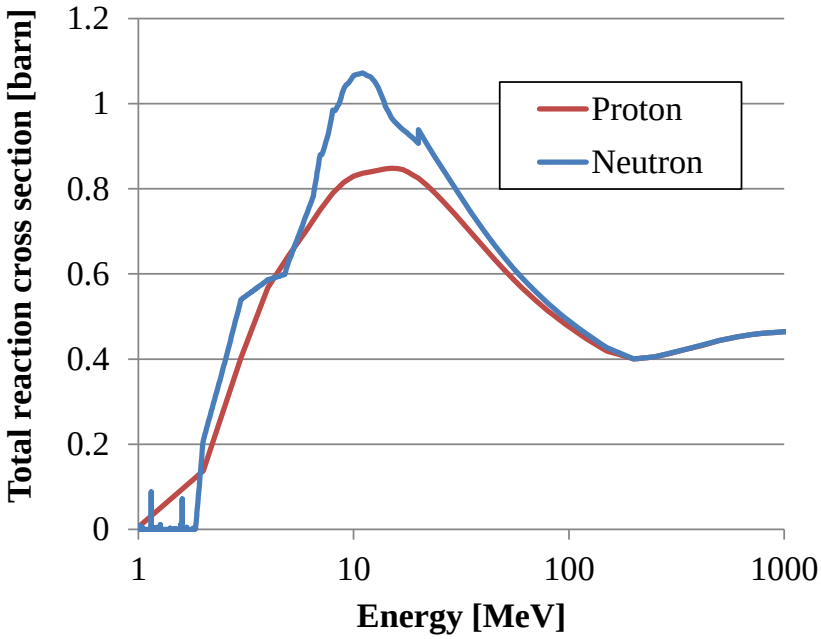


Fig. 1.14 Total nuclear reaction cross section of high-energy proton and neutron in Si from the database [2].

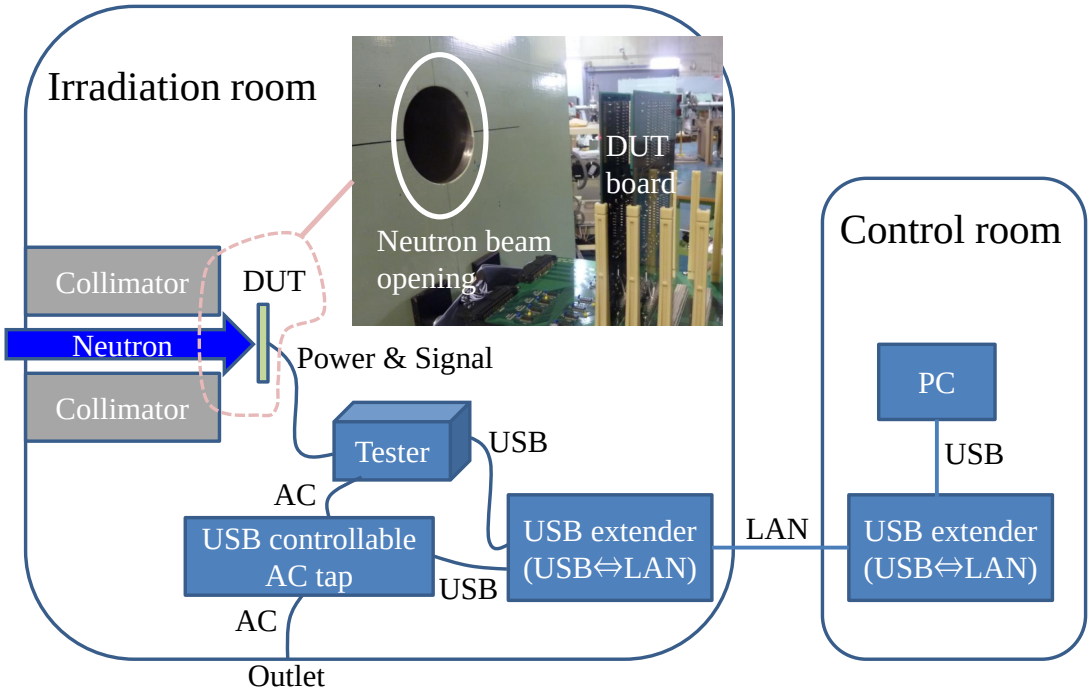


Fig. 1.15 Neutron irradiation test setup in RCNP.

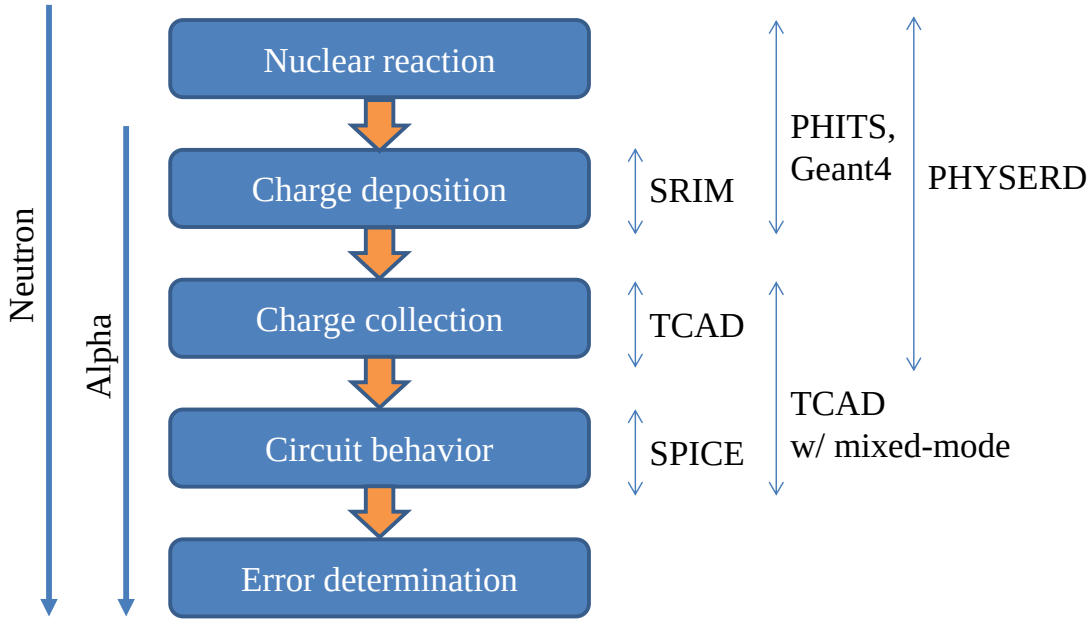


Fig. 1.16 Steps of soft error occurrence and simulation tools for neutron and alpha induced soft error.

(TCAD) device simulation and SPICE circuit simulation are responsible for 3) and 4), respectively [68]. Mixed-mode simulation option in TCAD enables us to calculate both 3) and 4). The neutron passage through the DUT is a random process in time and space, and hence the soft-error occurrence is also a random process. Therefore, to characterize SER, DUT behaviors to neutron injection must be evaluated many times in a Monte Carlo manner. PHYSERD system can calculate SER with multi-scale Monte Carlo simulation for all in 1) - 3) [69, 64, 70]. Furthermore, PHYSERD applied SPICE simulation, which does not use Qcrit method, can achieve highly accurate evaluation [68]. Although many TCAD simulations (over 1000) are necessary in PHYSERD, the cost per processor node in cloud servers is rapidly decreasing recently and now it is 1 USD for 10 hour computation in December 2014 [71]. Therefore, the simulation cost is becoming less critical.

1.3 Soft error in microprocessor

1.3.1 Critical device from soft error perspective

Critical devices concerning soft error reliability in terrestrial environment are human related devices such as devices for health cares and automobiles [72] and devices used for mission critical applications like super computer and enterprise server. The devices for health care, automobile and avionics are manufactured with well-established process technologies like 65 nm technology in 2015. The devices for mission critical applications, which are mainly microprocessors, are manufactured with a cutting-edge process technology, and the chip size is larger than that for other applications. This

means there are many transistors in the microprocessor. Consequently, the microprocessor for mission critical applications includes large memories and many logic elements, which draws a significant concern on soft error.

Enterprise servers for mission critical applications like bank systems generally adopt redundant systems for coping with hardware and software troubles, and the servers are located in different locations for mitigating the risk of earthquakes and terrorist attacks. Although the redundant system can reduce the probability of system down due to soft error occurring in the processors, the processors themselves are also required to attain high reliability. The reliability deterioration incurs short mean time between failures (MTBF) of each single system, and it requires more sophisticated system-level redundancy to overcome short MTBF of individual systems.

Further higher reliability is demanded in devices for supercomputer, which is also called high performance computing (HPC). The recent hardware for HPC consists of over 100,000 electronic devices. In addition, it is not possible to adopt redundant systems in HPC in terms of installation area, power consumption or cost. Therefore, extremely lower error rate is required for microprocessors used in HPCs compared to other devices. Let us exemplify a concrete number. Supercomputer "K," which was the fastest HPC in 2011, consists of 88,128 computing nodes and takes 33.3 hours to execute a 10 petaFLOP benchmark job. To attain a 90% success rate, the failure in time (FIT) rate per computing node should be less than 36 [73]. If the rate exceeds 36 FIT, it is difficult to complete even one job. This means that soft error is not only a factor that determines the reliability but also a factor that limits the computing performance of HPC. Therefore, it is crucially important to investigate and mitigate soft error in microprocessors for mission critical servers and HPC.

1.3.2 Techniques for improving microprocessor reliability

A large majority of microprocessors which have been developed are based on Von Neumann architecture. The microprocessor of Von Neumann architecture consists of a processing unit, a control unit, a memory and input/output (I/O) mechanisms [74]. Recent microprocessors have an extended architecture that contains a few to many cores, cache memory, and I/O as shown in Figure 1.17. The core usually includes an instruction control unit for fetching and decoding, register files, an execution unit and cache memory. The I/O on microprocessors recently contains a memory controller such as DDR, PCI controller and network I/O for communication with other microprocessors. SRAM is mostly used for cache memory in microprocessors. Other part is constructed by combinational logic and sequential elements designed.

Figure 1.18 shows a brief image of data processing in a microprocessor. The register files, the cache memory and the external memory beyond the I/O store data, and the stored data is transported between them. The I/O transfers the data from/to the external memory as block data. The cache memory usually has two or three levels. The fastest access speed is required in the first level (L1) cache and the register files, whereas a large capacity is required for the last level cache (LLC). The arithmetic logic unit (ALU) usually consists of combinational logic and sequential elements. The data is changed by the computation in the ALU, but in I/O, cache memory and register files the data is unchanged. The control logic co-operates with all units in a

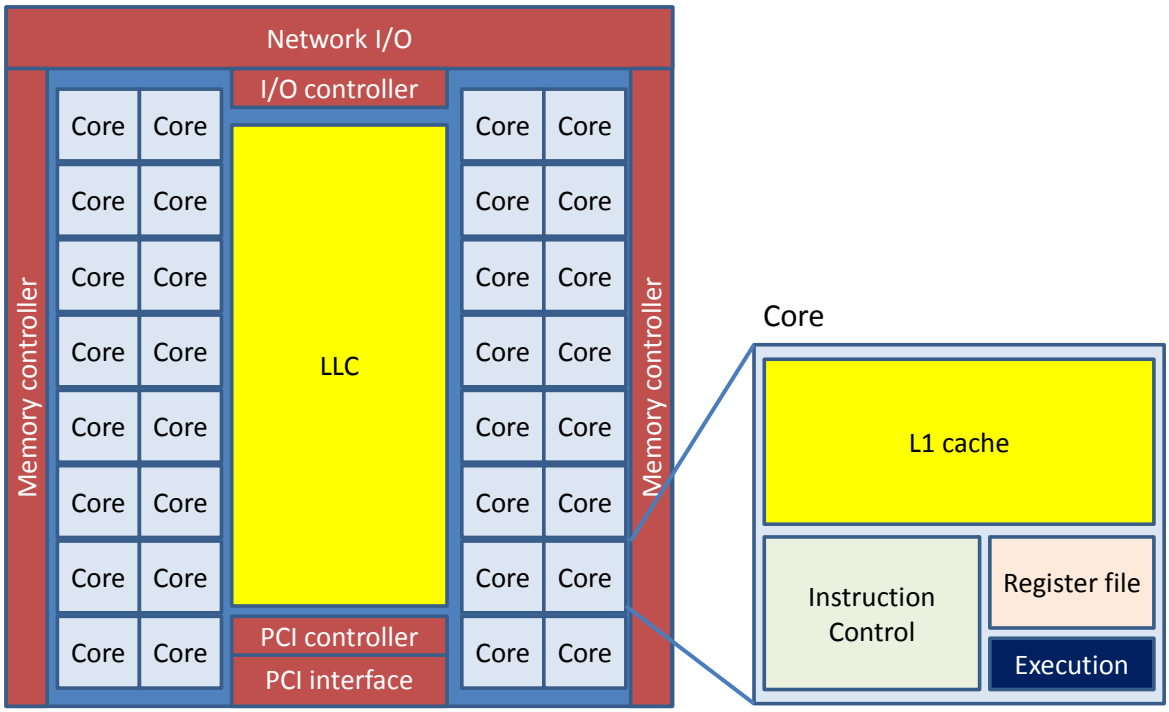


Fig. 1.17 Structures of microprocessor (left) and core (right).

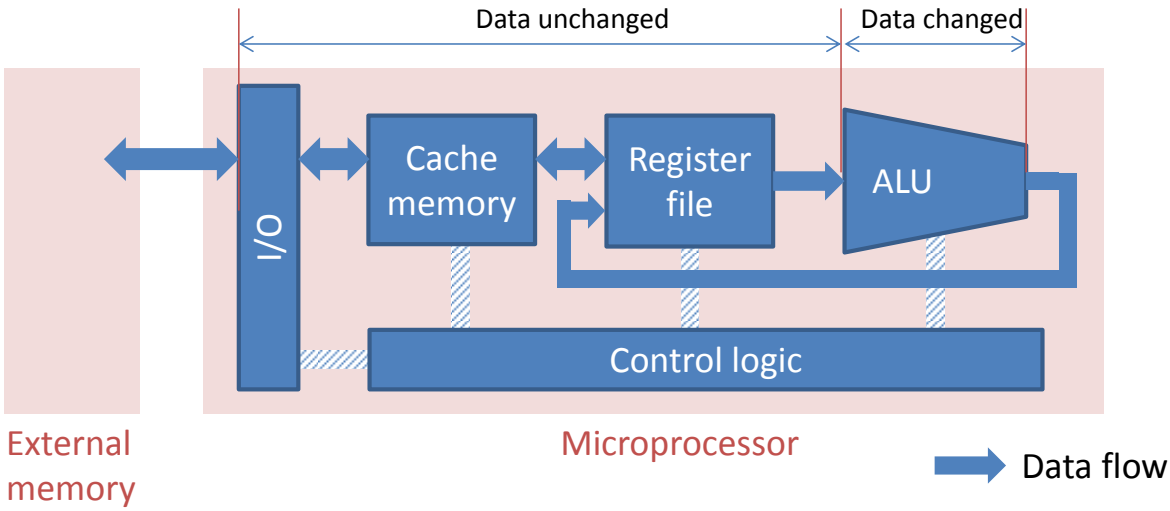


Fig. 1.18 Data flow in a microprocessor.

microprocessor.

In the blocks where the data is unchanged (I/O, cache memory, register file) and the data transportation between those blocks, cyclic redundancy check (CRC), error correction code (ECC), parity check and data resending are used for improving reliability, availability and serviceability (RAS). CRC is used for the block data between the external memory and the I/O. ECC is often used in the last level cache. ECC in the microprocessor cache is generally based on Hamming code. Single error correction, double error detection (SECDED)-ECC, which involves 13% area overhead, is the most popular ECC [75, 76]. Note that Hsiao code and Bose Chaudhuri Hochenghem (BCH) code are sometimes used for much larger data, such as in solid state drive (SSD), to achieve higher RAS. On the other hand, it is difficult to apply ECC to the L1 cache and the register files, since ECC degrades memory access speed. Instead of ECC, parity check and data resending are used. Errors are detected by parity checking. Note that not only ECC but also scribing, poisoning and memory patrol are used in the external memory such as DDR DRAM. An important point here is that SECDED-ECC and parity are very effective to SBU but their effectiveness to MCU is limited.

In the block that alters data (ALU), algorithmic checking is used for error detection because the RAS techniques such as ECC and parity checking used in the data unchanged blocks cannot be applied to the ALU. Algorithmic checking using residue in multiplier is widely used in microprocessors. Details of the algorithmic checking are explained in Section 5.1. The residue checking detects SBU, but may miss MCU. The RAS techniques of ECC and parity checking cannot be applied to the control logic either. Watchdog timer (WDT) technique is sometime used but its coverage of error detection is limited. Therefore, not only MCU but also SBU in sequential elements must be mitigated for reliability improvement of the control logic.

In summary, for achieving high reliability operation of microprocessor, MBU in cache memory, i.e. SRAM, must be reduced, where MBU is the MCU that cannot be corrected by SECDEC-ECC. In addition, SBU and MCU in ALU and control logic, i.e. in sequential elements, need to be mitigated. For SBU mitigation in sequential elements, redundancy-based radiation-hard latches having more than two storage nodes are developed as a circuit-level solution [77, 78, 79]. However, they still suffer from SBU since they are vulnerable in case that the generated charge is collected to multi nodes. Such charge collection to multiple nodes occurs frequently in advanced technologies, and then a novel countermeasure is highly demanded. Furthermore, SEL, which occurs in SRAM manufactured in advanced technologies, cannot be eliminated by architecture-level countermeasures. A circuit-level solution with current-limiting device (CLD) is proposed [141, 142] [80, 81]. However, it requires large area overhead and SRAM redesign. More area-efficient solution is demanded.

1.4 Objectives of this thesis

As discussed in this introduction chapter, soft error in microprocessors used for mission critical applications and HPC is a crucial issue in terms of both reliability and performance. To improve the reliability of microprocessors and extend the MTBF

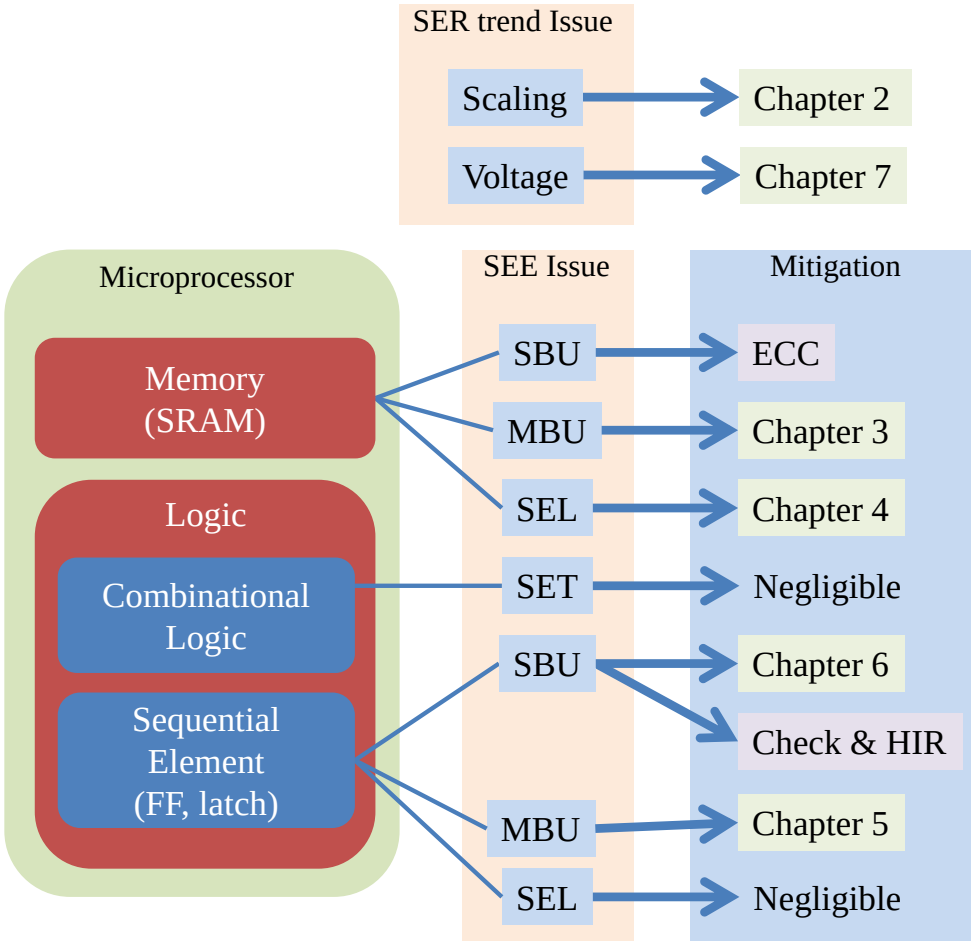


Fig. 1.19 Contributions and organization of the thesis.

of HPC systems, this thesis studies soft error mitigation techniques for the processors and discusses their error mitigation efficiency and overhead through neutron and alpha irradiation tests. This thesis focuses on microprocessors manufactured with conventional bulk CMOS technology. Bulk CMOS transistors are sensitive to soft error compared with other recent expensive transistor devices such as FinFET [82, 83] and silicon on insulator (SOI) transistors [84, 85, 86, 87, 88, 89]. This means that the highest error mitigation efficiency is necessary for bulk CMOS technology.

Circuit elements composing a microprocessor are categorized into two groups; memory and logic circuits. The memory circuit that can be manufactured in ordinary CMOS technology is SRAM. The logic circuit is further categorized into two; sequential cell and combinational logic cell. The contribution of combinational logic cells to the microprocessor-level SER is smaller than that of sequential cells [90]. Thus, this thesis tackles with the soft error occurring in SRAM and sequential cells, such as latch and FF, and mitigates it for improving the reliability of microprocessors.

Figure 1.19 illustrates the contribution and organization of this thesis. To quantitatively discuss SERs of SRAM and sequential cells and the necessity of soft error mitigation techniques, Chapter 2 first investigates the trend of SER on bulk CMOS

technologies. SERs were evaluated through neutron and alpha irradiation experiments on SRAMs manufactured in 350, 250, 180, 130, 90, 65, 55, 45, 40, 28 and 20 nm bulk CMOS technologies and FF in 65, 45, 28 and 20 nm bulk CMOS technologies. After that, this thesis discusses soft error mitigation techniques from Chapter 3 to Chapter 5. In SRAM, ECC is effective for mitigating SBU. However, ECC misses some MCUs resulting in MBU and ECC cannot eliminate SEL. Chapter 3 proposes an MBU mitigation technique for SRAM, and Chapter 4 presents an SEL mitigation technique for SRAM. As mentioned in Section 1.3.2, ECC cannot be applied to logic circuits such as ALU, and algorithmic techniques are used to detect soft errors occurring in logic circuits. However, the algorithmic techniques cannot cover all logic circuits in a microprocessor. Therefore, there is a demand for sequential cells immune to radiation. Chapter 5 discusses MBU mitigation for sequential elements, and Chapter 6 proposes a radiation-hard latch for SBU mitigation.

Finally, SER of SRAM in ultra-low voltage operation is discussed. Achieving low power operation of electron devices is nowadays a social requirement ranging from battery-powered mobile devices to energy-intensive HPC. Power consumption of CMOS circuits strongly depends on the operation voltage, and there is a strong request to decrease the supply voltage for power reduction. Motivated by this, near-threshold and sub-threshold circuits are intensively studied [91]. However, the soft error immunity of these low voltage circuits is hardly discussed. Chapter 7 investigates SRAM SER at a wide range of voltage from 0.19V to 1.6V. Finally, Chapter 8 summarizes the contribution of this thesis and presents a set of soft error mitigation techniques for achieving high reliability of the microprocessors for critical missions.

Chapter 2

Technology trend of SER in bulk CMOS technology

This chapter discusses the scaling trend of SRAM and FF SERs in bulk CMOS technology and their contribution to processor reliability of SPARC V9, which is one of instruction set architectures (ISAs) of SPARC processor family. Neutron and alpha irradiation experiments were performed on SRAMs manufactured in 350, 250, 180, 130, 90, 65, 55, 45, 40, 28 and 20 nm bulk CMOS technologies and FF in 65, 45, 28 and 20 nm bulk CMOS technologies. SRAM SER per bit reached the maximum at 180 nm for neutron and at 250 nm for alpha. In addition, evaluations on various 90 nm SRAMs show that the SER can change by up to 75% due to process conditions and the number of access ports. The FF SER per bit decreased more than SRAM SER in 20 nm bulk CMOS technology. As a result of these facts, the chip-level processor SER has increased in SRAM and has decreased in FF from 65 nm to 20 nm without soft error mitigation techniques on SPARC V9 processors.

2.1 Introduction

SER trend up to 65 nm is reported in a number of literatures [92, 93, 94, 90, 95, 96, 97, 57, 98, 99, 44, 100, 101, 102], and they indicate that the SER per bit was decreasing as the manufacturing technology advanced. While the SER is mainly determined by the amount of Qcrit and the transistor drain size, other phenomena also contribute to the SER considerably, especially PBA, which plays an important role in bulk technologies. Recently, it has been reported that PBA contributes to not only an increase but also a decrease in SER [103, 104, 105, 106, 107], and thus the SER trend depends on a number of complicated factors to be considered. Therefore, a simple extrapolation for SER prediction could be misleading.

This chapter discusses the scaling trend of SRAM and FF SERs and their contributing portions to processor SERs in bulk CMOS technologies. This chapter reviews the trend of SERs through neutron and alpha irradiation tests on SRAMs manufactured in 350, 250, 180, 130, 90, 65, 55, 45, 40, 28 and 20 nm bulk CMOS technologies and FFs manufactured in 65, 45, 28 and 20 nm bulk CMOS technologies. Recently, MOSFET devices are moving to three-dimensional structure, such as FinFET [82] and

tri-gate [108] transistor, and/or FD-SOI devices to mitigate manufacturing variability, short channel effect and leakage current. Beyond 20 nm technology, any fabrication companies do not have a plan to provide conventional bulk CMOS technology, and hence 20 nm bulk CMOS technology is probably the last bulk CMOS technology. Therefore, the trend shown in this chapter covers all the generations of bulk CMOS technology from 350 nm.

This work investigates SER dependence not only on technology generation but also on layout types of the SRAM cell and process conditions through neutron irradiation tests on six variations of 90 nm SRAM. The portions of SRAM and FF were estimated soft errors contributing to chip-level SER on SPARC V9 processors [109] based on neutron irradiation tests on the processor. This chapter also clarifies the impacts of mitigation techniques on SPARC V9 processors: ECC, hardware instruction retry (HIR) [110]. HIR enables the processor to retry instructions when an error is detected by hardware malfunction checkers.

The rest of this chapter is organized as follows. Section 2.2 explains irradiation test procedure. SRAM SER and FF SER are presented in Section 2.3 and Section 2.4, respectively. Chip-level SER on SPARC V9 processors is discussed in Section 2.5. Finally, Section 2.6 concludes this chapter with a brief summary.

2.2 Irradiation test procedure

Alpha and neutron irradiation tests were performed on SRAM and FF. The alpha irradiation tests were carried out with an ^{241}Am alpha source under low pressure atmosphere in a vacuum chamber to reduce the air shielding effect. The distance between the alpha source and the die was less than one millimeter for all the devices under test (DUTs), where DUTs were test chips that included SRAM and/or FF for evaluating SRAM SER and FF SER. Neutron irradiation tests were conducted with spallation neutron beam at RCNP. From four to thirty-two DUTs were irradiated one at a time in a neutron test. All DUTs were assembled with wire bonding package and all tests were performed with front-side irradiation. Note that aluminum was used for the metal layer in 350 nm and 250 nm technologies, and copper was used in 180 nm and finer technologies. All data points of SEU rate on SRAM were derived from more than 10,000 errors in the irradiation tests, on the other hand, data points of SEU rate on FF and MBU rate on SRAM are derived less than 10,000 errors. To show the statistical uncertainty, error bars are included in the following figures for the data points of SEU rate on FF and MBU rate on SRAM.

2.3 SRAM SER

SRAM SER was evaluated with the neutron and alpha irradiation tests. The SRAMs in these tests were manufactured in 350, 250, 180, 130, 90, 65, 55, 45, 40, 28 and 20 nm technologies. These SRAMs consist of ordinary 6T high current cells with conventional layouts unless otherwise specified. The data in this section are from the irradiation test results for SRAM in the DUT manufactured in a double-well process, i.e. without the DNW.

2.3.1 SEU trend on SRAM

Figure 2.1, Figure 2.2 and Figure 2.3 show SRAM SER per cell area, per processor, and per bit, respectively. The SRAM SER per processor was obtained for the products of SRAM SER per bit and the number of SRAM in a processor. The neutron flux was normalized so that it became equal to the alpha flux multiplied by 13,000. For example, when the alpha flux was 0.001 alphas per hour, the neutron flux was 13 neutrons per hour. Note that the neutron flux is 13 neutron per hour in one square centimeter at sea level in New York [4] and the alpha flux is around 0.001 alpha per hour in one square centimeter from ULA level material [56].

Figure 2.1 shows SRAM SERs per area. If the die area size and size ratio of the SRAM area on a processor did not change, SRAM SER per processor both for alpha and neutron increased with technology advance until 55 nm and after 40 nm. Actual SRAM SERs per processor in 130 nm dropped from 250 nm and 180 nm as shown in Figure 2.2. The reason of this drop is the considerably large cache in 250 nm and 180 nm compared to the processor in 130 nm. The large cache in 250 and 180 nm was implemented with off-chip (external die). Except for 250 nm and 180 nm, the size of SRAM cache in a processor increased exponentially as shown in Table 2.1.

Figure 2.3 shows that alpha SERs per bit had a peak at 250 nm technology node and neutron SERs per bit were the highest at 180 nm technology. This trend having a peak around 180 nm in SRAM SER per bit observed in our experimental results is consistent with other predictions [111, 34, 112]. On the other hand, this decreasing trend is hardly observed in neutron SERs per bit at 28 nm and 20 nm technology nodes. In addition, alpha SERs per bit increased at 20 nm technology node. This recent trend on SER per bit and an exponentially increase in the cache size resulted in the increase in SRAM SER per processor in recent 28 nm and 20 nm technologies as shown in Figure 2.2.

SRAM SER per bit (Figure 2.3) is examined further. The neutron SER was the highest at 180 nm technology, and it started to decrease. The alpha SER drastically increased at 250 nm technology, since alpha can cause upsets from 250 nm technology. Up to 350 nm technology, Qcrit could be larger than the maximum charge that an alpha particle can deposit and then alpha was less likely to contribute to soft error occurrence. On the other hand, the alpha SER was decreasing after 250 nm technology from a long-term perspective. Since 180 nm technology, both the alpha and neutron SERs per bit have been decreasing with technology advance. This SER decrease after 180 nm technology is explained by two size factors. The first is a decrease in bit cell area size, and this led to a decrease in the drain size of the soft error sensitive MOS transistor. The drain length in the SRAM cell (Ld in Figure 2.4) shrank as the feature size became finer. Thus, this shrinking contributed to the SER decrease. The second is a decrease in Qcrit. Qcrit decreased with technology advance, and this tendency raised the SER per bit. The Qcirt is determined by the gate size and operational voltage (VDD) [113]. Although VDD was scaled down until 90 nm, the voltage scaling was slowed down after 90 nm as shown in Table 2.2. Besides, the scaling of actual gate length (Lg in Figure 2.4) in SRAM was slowed down in recent technologies to cope with manufacturing variability [3], and consequently the decrease

Table. 2.1 List of evaluated SPARC processors. The instruction set architecture (ISP) are SPARC V9 in all model.

Model name	Process	Cache [MB]
SPARC64 II	350 nm	0.26
SPARC64 GP	250 nm	8.3
SPARC64 GP	180 nm	8.5
SPARC64 V [110]	130 nm	2.3
SPARC64 V+	90 nm	4.4
SPARC64 VI	90 nm	6.4
SPARC64 VII [109]	65 nm	6.3
SPARC64 VIIIfx [114]	45 nm	5.3
SPARC64 IXfx	40 nm	13
SPARC64 X [115, 116]	28 nm	27
SPARC64 XIfx [117]	20 nm	40

Table. 2.2 SRAM supply voltage and cell area normalized by that of 90 nm.

Process	VDD[V]	Normalized SRAM area	Layout type
350 nm	3.3	35	Type 1
250 nm	2.5	15	Type 1
180 nm	1.8	5.4	Type 1
130 nm	1.4	2.7	Type 1
90 nm	1.0	1	Type 4
65 nm	1.0	0.59	Type 4
55 nm	1.0	0.46	Type 4
45 nm	1.0	0.33	Type 4
28 nm	0.85	0.17	Type 4
20 nm	0.90	0.10	Type 4

in Qcrit was also slowed down. As a result, the increase in SRAM SER per bit was slow down.

2.3.2 Cell type dependence on SRAM SER

The SER depends on not only technology generation but also the number of access ports and process conditions. Figure 2.5 shows the SERs of six SRAM variations in 90 nm technology generation, where the SRAM variations are listed in Table 2.3. The six variations were constructed by controlling three factors; layout types of the SRAM cell (Type 1 and Type 4 [3] illustrated in Figure 2.4), number of access ports (1 and 2), and process conditions of ion implantation on channel, well and source-drain diffusion (A, B, and C).

The layout type (Type 1 and Type 4) did not much affect the SER, which was found by comparing A1S and A1V and comparing C1S and C1V. The experimental result did not show the dependence of the layout type in the 90 nm technology although [118] reported that changing the layout type was the reason of the decrease in SRAM SER from 130 nm to 90 nm technologies.

The number of access ports did affect the SER significantly. The SER of C2S is about 75% lower than the SER of C1S and C1V because the two-port SRAM,

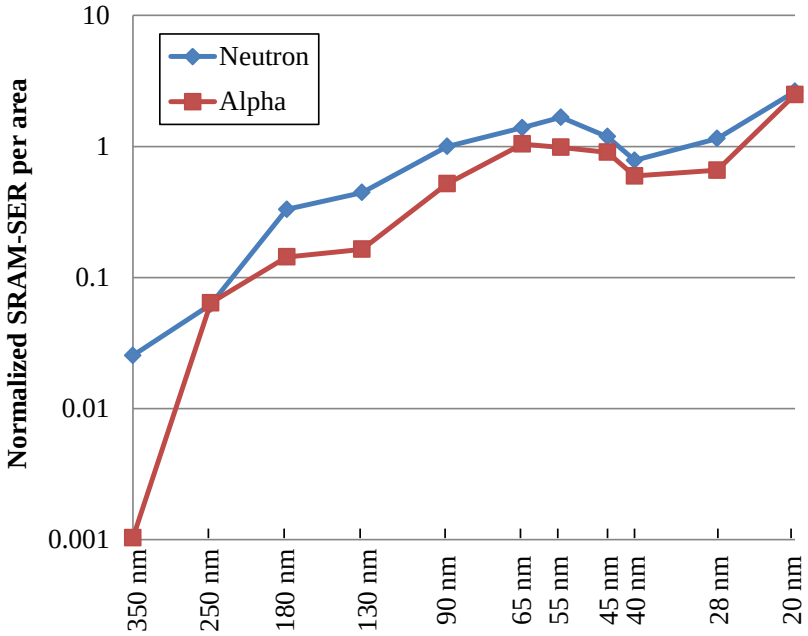


Fig. 2.1 SRAM SER per area normalized with 90 nm neutron SER characterized in neutron and alpha irradiation tests. Neutron flux is 13,000 times higher than alpha flux.

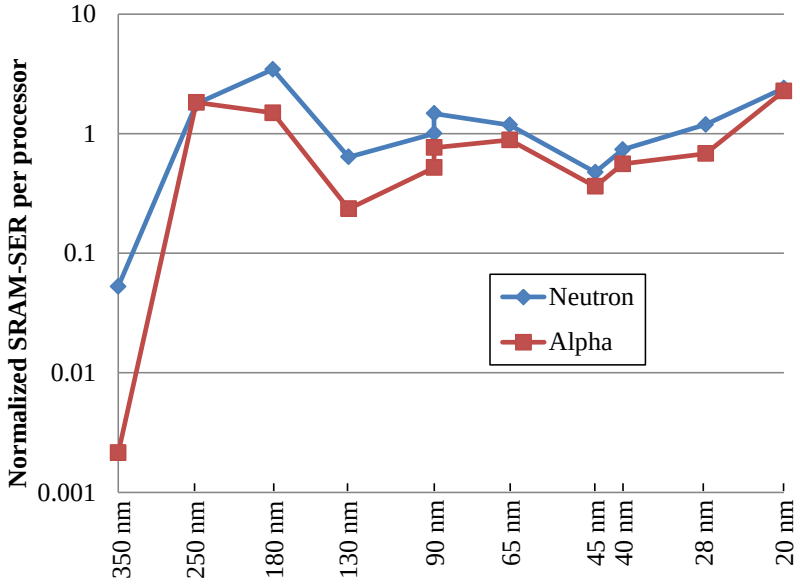


Fig. 2.2 SRAM SER for alpha and neutron in SPARC V9 processor. Neutron flux is 13,000 times as large as alpha flux. These SERs were calculated from the data of Table 2.1 and Figure 2.3. These SERs were normalized with neutron SER in SPARC64 V+ (90 nm).

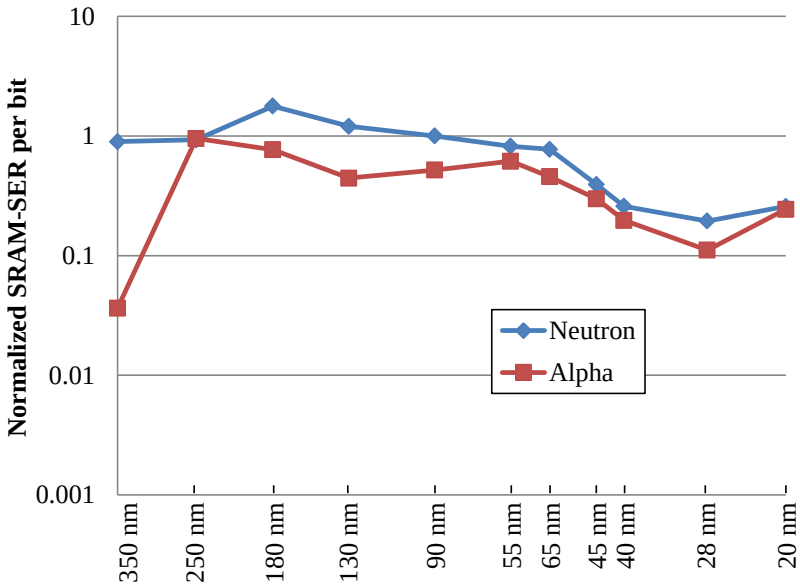


Fig. 2.3 SRAM SER per bit normalized with 90 nm neutron SER characterized in neutron and alpha irradiation tests. Neutron flux is 13,000 times higher than alpha flux. The test conditions and cell size are shown in Table 2.2.

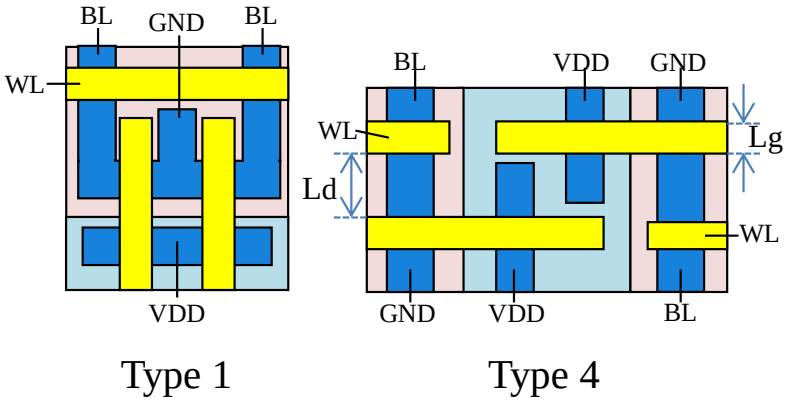


Fig. 2.4 Physical transistor layouts of SRAM cells of Type 1 and 4 [3]. Ld and Lg are the gate length and drain length. BL and WL stand for the bit line and word line.

which consists of eight transistors, has a larger Qcrit than the one-port SRAM. The process conditions of ion implantation also affected the SER, which was observed by comparing A1S, B1S, and C1S. Altering the process conditions changed the SER by 70%.

2.3.3 MBU trend in SRAM

MCU is a serious concern with regard to the reliability of SRAM with ECC as explained in Section 1.3. Although the ECC technique is very effective for mitigating

Table. 2.3 List of SRAM on 90 nm technology generation. SER values at 1.2 V (the last column) in the table were normalized by the average of these six SERs.

Name	Process	#Port	Layout Type	Normalized SER
A1S	A	1	Type 4	0.82
A1V	A	1	Type 1	0.84
B1S	B	1	Type 4	1.02
C2S	C	2	Type 4	0.74
C1S	C	1	Type 4	1.33
C1V	C	1	Type 1	1.26

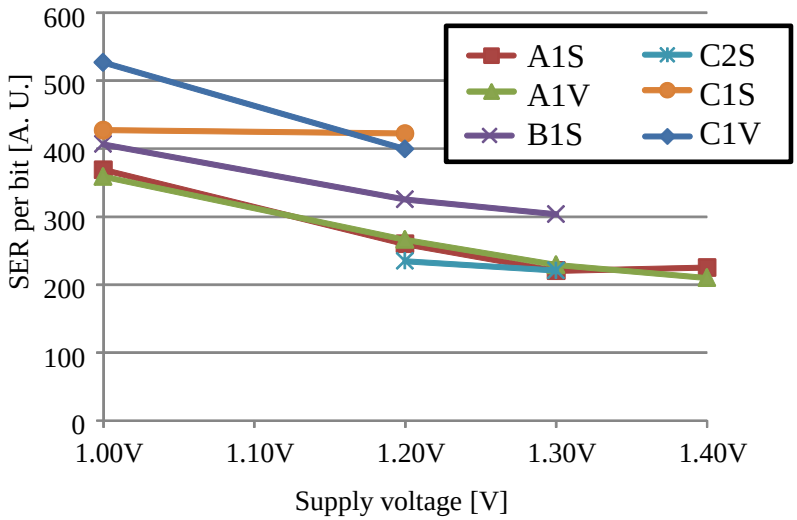


Fig. 2.5 Neutron-induced SERs of 90 nm SRAMs evaluated by irradiation tests, normalized with the average SER at 1.2V.

SBU in SRAM, ECC cannot eliminate MCU in the same word, i.e. flips on the same word line (WL) and on the bit lines (BLs) concurrently selected by column multiplexers (col MUXs). This error, which cannot be corrected by ECC, is called MBU.

Figure 2.6 shows SRAM macro structure with 4 col-MUX. For data reading, one WL is activated by the WL decoder, and the retention data is sent to the sense amplifier through the col-MUX. The col-MUX passes one of input data selected by the column decoder (col-DEC). For example, BL1 data is sent to the sense amplifier when D1 is active in Figure 2.6. This structure provides a mechanism that accessed bits at the same time are located at intervals of four bits. This means that MBU with 4 col-MUX is MCU occurs when bit flips occur in the bits which are four-bit distant.

Figure 2.7 shows the MBU ratio (MBU/SEU) in SRAM with ECC and 4-col MUX. The 4-col MUX were used in SPARC64 processors. Large col-MUX, e.g. 8 or 16 col-MUX, can decrease MBU rate, but, it degrades read and write performance because of increased capacitance of WL. No MBUs were observed in 40 nm and 28 nm SRAMs in our tests. The error bar of MBU in this figure represents a 99.9% statistical confidence level with one(up)-sided estimation. Note that the DUTs did not adopt any MBU mitigation techniques like narrow deep N-well which will be explained in Chapter 3.

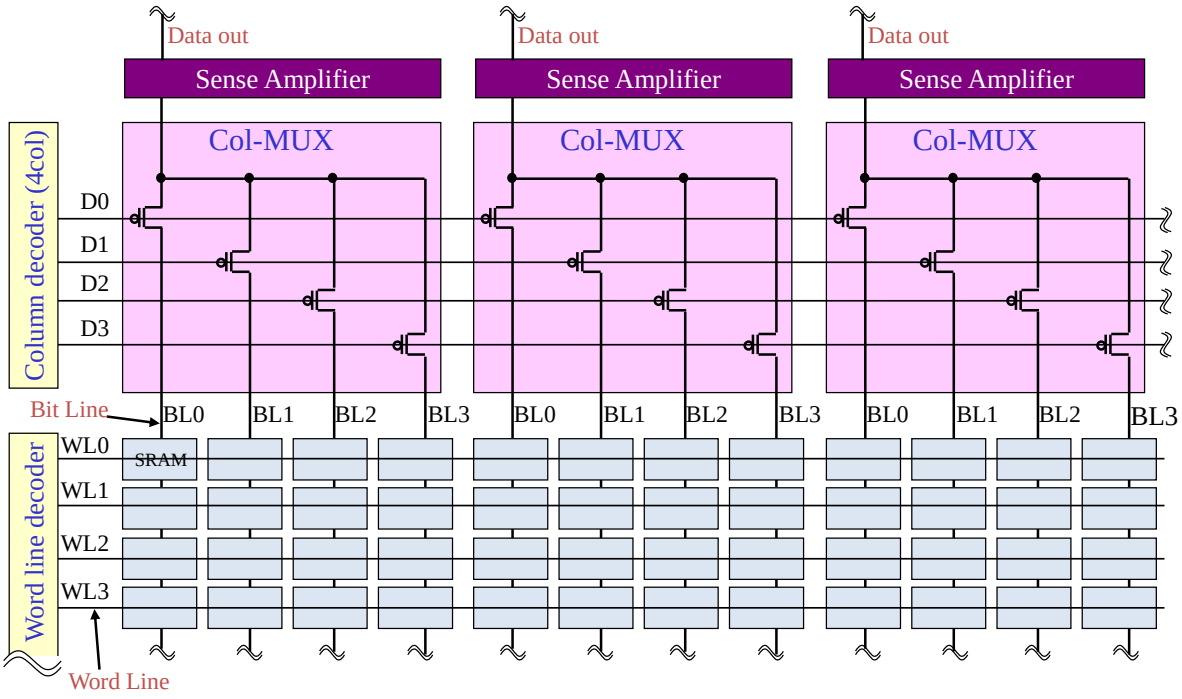


Fig. 2.6 SRAM macro structure with 4col-MUX.

An important observation here is that the MBU ratio is not increasing. The ratio in 20 nm is two orders of magnitude lower than the ratio in 65 nm. This result is opposite to other papers, which show an increasing trend in MBU rate from 65 to 22 nm [112].

A reason for the large drop in this MBU ratio could be a single event upset reversal (SEUR) [105], since [107] reported that the SEUR could contribute to neutron induced SER even in double-well. The deposited charge could be collected into multiple nodes in a bit cell. When the nodes received the charge in such a way that SEUR was invoked, the upset behavior could be canceled out. On the other hand, the nodes receiving charge might cause an MBU. Thus, multi-node charge collection could cause both MBU and SEUR. Interestingly in some cases, even when two nodes related to MBUs received enough charge, either or both of the possible flips could be diminished by SEUR. As a result, MBU was kept at a low level even in a fine technology of 20 nm.

2.4 FF SER

Figure 2.8 shows the trend that neutron-induced FF SER was decreasing with technology advance in the double-well process. Figure 2.9 points out that the decreasing rate was higher than that of SRAM from 45 nm to 28 nm. This trend is explained by SEUR contribution, where the relation between SEUR and PBA is discussed in [107]. PBA can decrease the SER of the FF in these fine technologies by SEUR [105]. In FFs, critical NMOSs locate in the same well, whereas there are critical NMOSs in

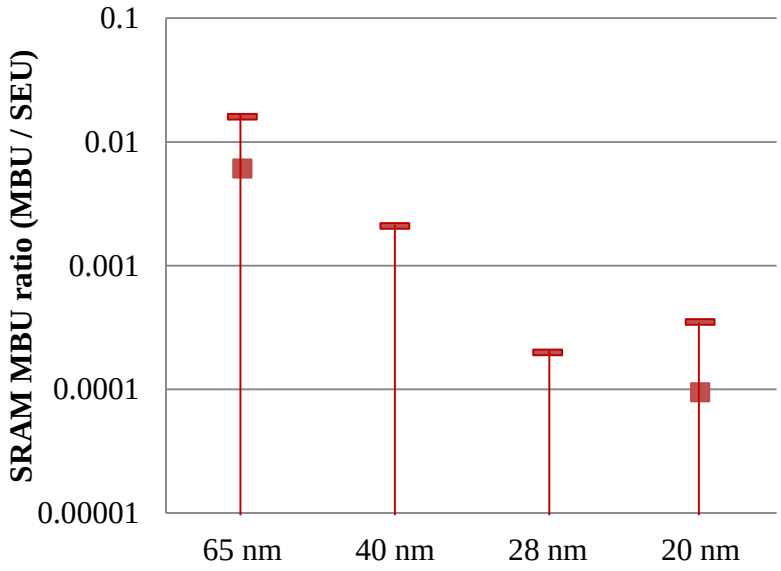


Fig. 2.7 Ratios of SRAM MBU with ECC and 4-col MUX. Error bars represent 99.9% statistical confidence level with one(up)-sided estimation. The up-side estimation can be performed even when no errors are observed, and it is recommended in standards [4, 5].

different wells in SRAM. PBA affects multiple nodes within the same well, and hence SEUR occurs more often in FFs than in SRAMs.

On the other hand, critical PMOSs of both the SRAM and FF locate in the same well, and PBA on PMOS is supposed to induce SEUR as well. However, PBA on PMOS is traditionally much less significant than PBA on NMOS. Furthermore, PBA on PMOS becomes weaker after 65 nm technology because embedded SiGe technology, which is used for the source-drain of PMOS, reduces the current gain of the parasitic bipolar [119, 120]. As a result, PBA on PMOS is less likely to cause SEUR, and hence SER reduction due to SEUR in SRAM is limited. Therefore, the decrease in SRAM SER due to PBA is smaller than that in the SER of FFs.

As mentioned earlier, with regard to the FF in 45 to 28 nm technologies, PBA can decrease the SER by SEUR [105]. In the triple-well process, SEUR affects the SER of FF even in not the latest technology, such as 65 nm technology. Deep N-well, i.e. triple-well, drastically activates PBA and contributes to the SER. The SER of FF in triple-well is lower than in double-well although the SRAM SER in triple-well is higher than that in double-well as shown in Figure 2.10. This result reconfirms that PBA decreases SBU rate of FF only, and PBA does not decrease SRAM SBU rate.

2.5 Chip-level processor SER

This section discusses the portions of SRAM-induced errors and FF-induced errors to the chip-level SER. Table 2.4 lists the processors used for the discussion that were manufactured in 65 and 20 nm technologies, where the SRAM MBU values

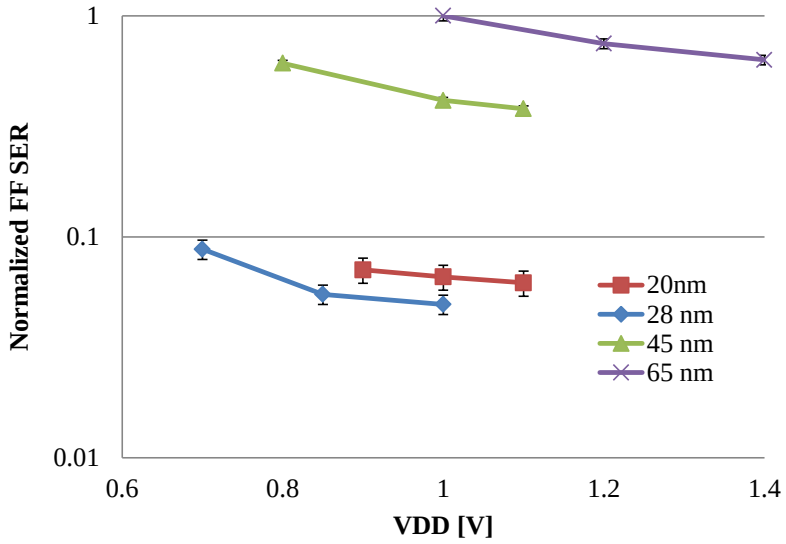


Fig. 2.8 Neutron-induced SER of FFs normalized with SER of FFs manufactured with 65 nm double-well process at 1.0 V. Error bars represent 95% statistical confidence level.

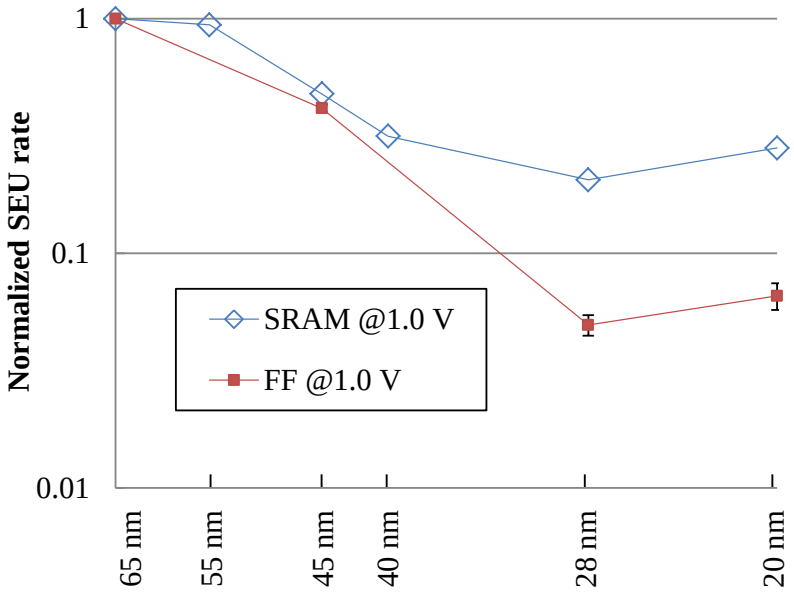


Fig. 2.9 Comparison between neutron-induced SRAM and FF SER. These SERs were evaluated with neutron irradiation test on DUT manufactured with double-well process. Error bars in FF data represent 95% statistical confidence level.

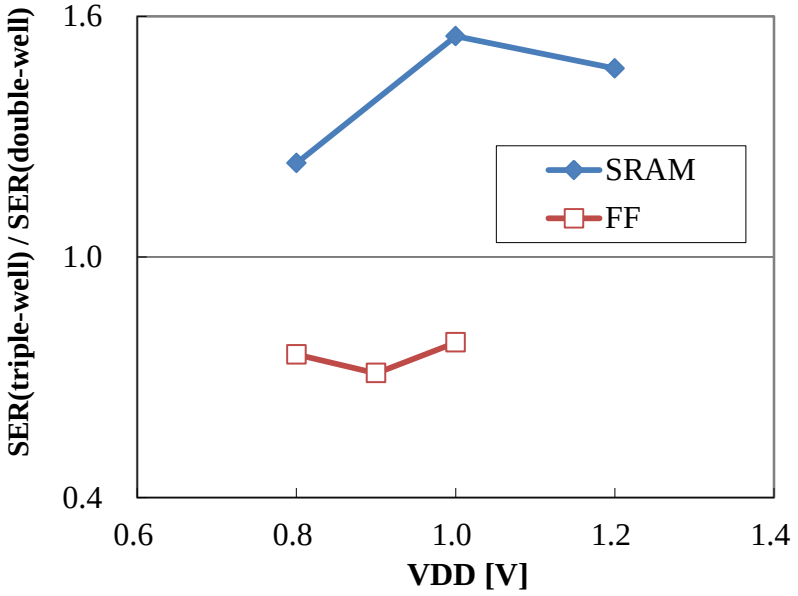


Fig. 2.10 Ratio of SER in triple-well to SER in double-well in 65 nm technology.

Table. 2.4 List of evaluated processors.

Process	Number of Transistors (million)	Number of cores	Die size [mm^2]
65 nm	600	4	445
20 nm	4,500	32	513

are available for these two processors. Note that the chip-level SER is estimated considering the processor operation. On the other hand, SRAM SER per processor was obtained as the simple product of SRAM SER per bit and the number of SRAM in a processor in Section 2.3.1.

The alpha flux of the super ultra-low alpha (SULA) grade Tin-Silver (SnAg) bump, which is used in the SPARC V9 processors, is 0.00025cph/cm^2 [56]. The area ratio of the bumps to the processor die is about 20%. On the other hand, for the alpha flux of 0.001cph/cm^2, the average alpha-induced SER was 70% of the neutron-induced SER in 65 and 20 nm as shown in Figure 2.2. Taking into account the alpha flux difference and the bump area ratio, the alpha-induced SER is estimated to be 3% of the neutron-induced SER in the SPARC processors. This means that alpha contribution is negligibly small. In the following, neutron-induced SERs, which were characterized by the neutron irradiation test mentioned in the previous sections, are used for chip-level SER estimation.

The architectural vulnerability factor (AVF) [121] for SRAM, which is the probability that an upset causes a system error, was calculated from the results of the neutron irradiation test on processors [122] referring to the nominal SER of SRAMs. The AVF corresponds to the processor failure rate divided by the SRAM SER.

The AVF of SRAM ranges from 52.4% to 65.1%, which was observed in the neutron irradiation tests on a SPARC V9 processor executing LINPACK, gee, bzip2, galgel, and sixtrack [122]. The following evaluation of processor SERs uses the average AVF

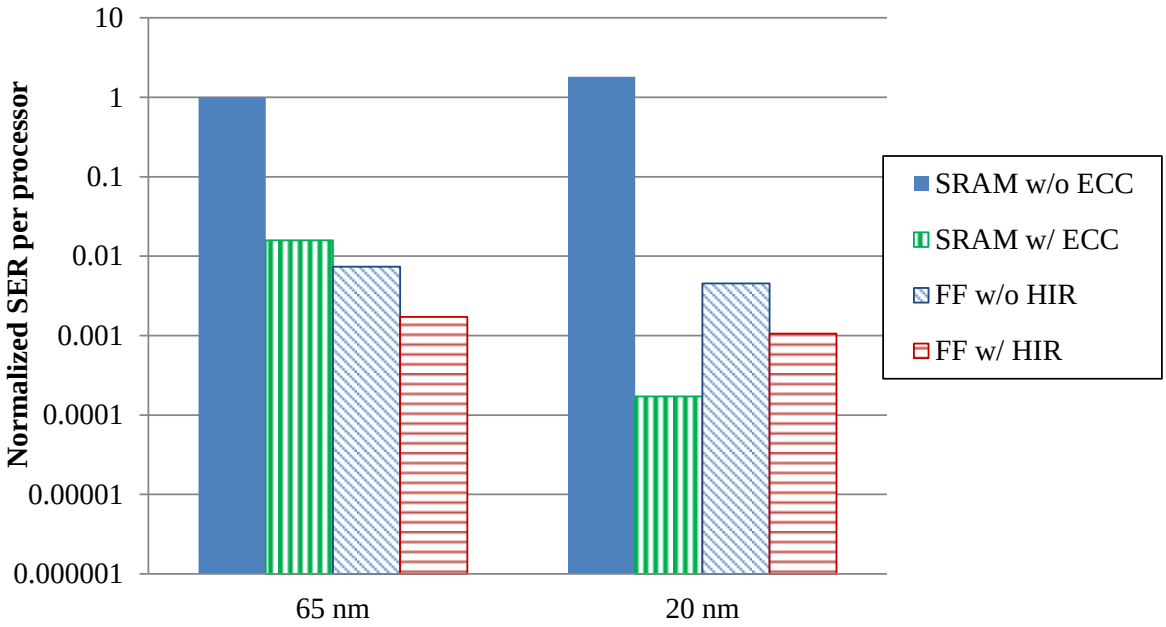


Fig. 2.11 SERs of FF and SRAM contributing to chip-level processor SER. These SERs are normalized with 65 nm SRAM SER without ECC.

of these results for SRAM, which is 60.0%.

Nominal SERs of FF, which does not consider AVF, are also extracted from the neutron irradiation tests mentioned in the previous sections. Similar to SRAM AVF, the FF AVF was calculated based on the neutron irradiation test of processors [122]. This work used the AVF of 6.4% without HIR and 1.5% with HIR. It should be noted that this AVF includes silent data corruptions (SDC), which cannot be detected by the hardware or software. SDC was detected by comparing the data during the irradiation test on the processor. Note that the AVFs can vary depending on the number of cores, but the AVFs in our calculation are assumed constant in all processors in this chapter.

Figure 2.11 summarizes the SER portions of SRAM with and without ECC and FF with and without HIR. This estimation shows that the SRAM and FF SERs are at the same level in 65 nm to 20 nm without ECC or HIR. FF SERs with HIR are comparable in in 65 nm and 20 nm. In 65 nm, SRAM SER with ECC is higher than FF SER with and without HIR. On the other hand, in 20 nm, SRAM with ECC is lower than FF SER with and without HIR.

For sustaining high reliability, ECC cannot be removed in bulk CMOS technology although the ECC mitigation technique has the largest overheads for area, performance, and power consumption. For improving reliability further in 65 nm, further mitigation of SRAM SER is necessary, which means MBU needs to be reduced. For higher reliability both in 20 and 65 nm, further error mitigation in FF is necessary. Reducing SBU in FF is necessary because HIR cannot cover all logic, and Reducing MBU in FF is necessary because algorithm checking for HIR cannot detect MBU.

2.6 Conclusion

This chapter presented the scaling trend of SRAM and FF SERs and their contribution to processor reliability in bulk CMOS technology. All the discussions were based on SRAM and FF SERs obtained through alpha and neutron irradiation tests. SRAM SER per bit reached the maximum at 180 nm for neutron and at 250 nm for alpha. The evaluations on various 90 nm SRAMs show that process conditions and the number of access ports could change SRAM SER by up to 75%. The decrease in FF SER per bit is more significant compared to that of SRAM. Consequently, the chip-level processor SER remains at the same level from 65 to 20 nm both in SRAM and FF without soft error mitigation techniques. This chip level estimation shows that MBU should be mitigated for higher reliability in 65 nm. After that, SBU and MBU in FF should be reduced because HIR cannot protect FFs from MBU and all the SBU. From this observation, this thesis discusses mitigation techniques for MBU in SRAM and SBU and MBU in FF.

Chapter 3

MBU mitigation with narrow deep N-well in SRAM

This chapter studies SRAM structures with the goal of reducing MBU. This chapter first investigates SRAM SER dependence on well depth with and without DNW through neutron and alpha irradiation tests [123]. This chapter then proposes an MBU mitigation technique that uses DNW. While DNW generally raises the SER due to PBA, the proposed technique inserts narrow DNW to increase the distance between cells that are simultaneously selected in the same well. The neutron irradiation test results show that the proposed technique drastically reduces MBU without area overheads.

3.1 Introduction

To mitigate the effects of SEUs in SRAM, ECC is often used as discussed in Chapter 1. Single error correction (SEC)-ECC, which is the most popular ECC for SRAM, is very effective for mitigating the effects of SBU in SRAM. However, SEC-ECC cannot eliminate MCU in the same word, i.e. on the same WL and on the BLs concurrently selected by col-MUXs. Such an uncorrectable MCU in the same word is called a MBU as explained in Section 1.2, and its characterization and mitigation are critical design issues.

In the chip level SER in a processor which was presented in Section 2.5, SER of SRAM with ECC, i.e. MBU rate, can be higher than other SERs such as of FF. Mitigating MBU in SRAM is a critical issue for reliability improvement in processors design.

Triple-well technology with DNW is often adopted for substrate isolation, which enables body biasing, substrate noise suppression for analog circuits, and better isolation for RF signals. On the other hand, DNW increases SEUs, and it has been quantitatively pointed out that the SEU rate of SRAM with DNW is higher than that without DNW [103, 34]. The main reason for the SEU increase due to DNW is that PBA, which changes the well potential under SRAM cells and triggers MCU and SBU occurrence [103], tends to be more active in DNW. In particular, PBA increases MCUs. Thus, well structure significantly affects MCU.

To reduce MBU occurrence, several MBU mitigation techniques have been proposed. However, they involve non-negligible overheads. For example, large col-MUX [115, 116], e.g. 8 or 16 col-MUX, reduces MBUs by increasing the distances between SRAM bit cells that are concurrently selected. This technique, however, degrades the read- and write-speeds because of an increase in the parasitic capacitance of the WLs. Double error correction (DEC)-ECC is another MBU mitigation technique, but it involves considerable overhead in area, access speed and power consumption [124].

In this chapter, to explore SRAM structures with lower MBU rates, first, SRAM SER dependence on well structures is investigated through neutron and alpha irradiation tests. The tests were performed on SRAMs with different well depths with and without DNW. This chapter then proposes an MBU mitigation technique that uses two types of col-MUXs and uses DNW. Here, DNW generally raises the SEU rate as mentioned above. Due to this, the proposed technique might increase ECC-correctable upsets that do not deteriorate chip reliability. However, in exchange for this increase in correctable ECC upsets, the proposed technique can increase the distance between cells that are simultaneously selected and reduce MBUs. The efficiency of this mitigation technique is evaluated with neutron and alpha irradiation tests. Moreover, the manufacturability of narrow DNW is confirmed with a scanning non-linear dielectric microscope (SNDM).

The rest of this chapter is organized as follows. Section 3.2 explains the irradiation test procedures and test chips. Section 3.3 and 3.4 show the impacts of well structures on the SER, and the spatial extent of MBU is investigated. Section 3.5 presents the proposed MBU mitigation technique with narrow DNW, and it shows the mitigation efficiency through neutron irradiation tests. Finally, Section 3.6 concludes this work.

3.2 Experimental procedure

Neutron and alpha irradiation tests were performed on SRAM devices. This section explains the experimental setups. The test procedures of the irradiation tests comply with the JEDEC standard [4]. All the tests were performed with the static test. In this paper, any two upset bits that were three cells or fewer apart were thought to be caused by an event. This classification was applied to all the combinations of upset bits, and the upset bits that were caused by the same event were recognized as an MCU. The distance criterion is applied omnidirectionally.

The neutron irradiation test was carried out with spallation neutron beam in RCNP [125]. The alpha irradiation test was carried out with an ^{241}Am thin alpha source under a low pressure atmosphere in a chamber for suppressing the air shielding effect for alpha rays. The pressure was less than 200 Pa. The test chips were mounted on packages with wire bonding for irradiating the die surface with alpha particles. The package material above the die was removed by using fuming nitric acid. The distance between the alpha source and the die was less than 1 mm. The area of the alpha source is circular with a 15 mm diameter and an activity of 0.1 μCi. The SRAM area on the test chip is less than 12 mm^2. The metal layer thickness of the test chip is approximately 10 μm.

The irradiation tests were performed for three types of test chips: CHIP-A, -B,

Table. 3.1 List of test chips.

Chip type	Macro-well structure	Number of macros
CHIP-A	w/o DNW(deeper well)	16
CHIP-B	w/o DNW	16
CHIP-C	w/ DNW	2
	w/o DNW	2
	w/ narrow DNW	12

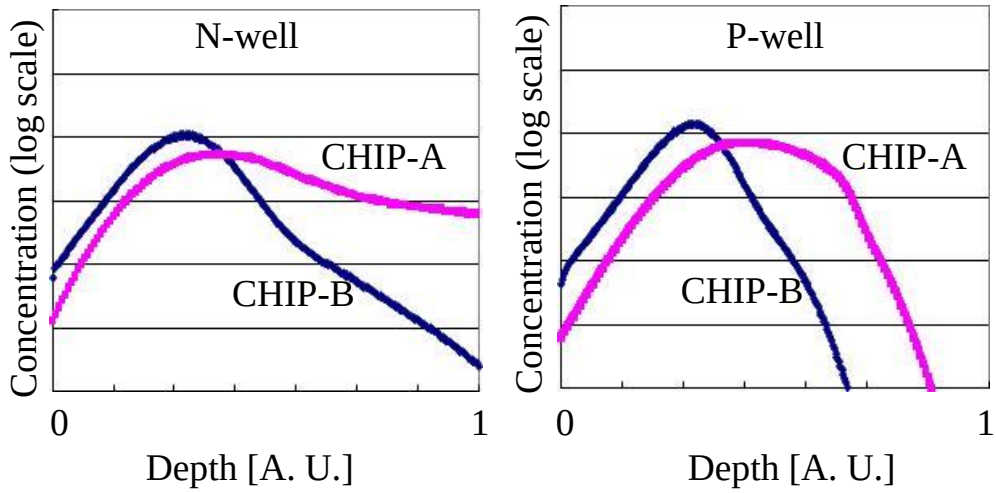


Fig. 3.1 N- and P-well profile in CHIP-A and -B.

and -C listed in Table 3.1. The test chips include about 4 Mbit SRAM consisting of sixteen macros manufactured with 65 nm technology. CHIP-A and -B have sixteen conventional SRAM macros with double-well (i.e. without deep-N-well). The well depth of CHIP-A is intentionally deeper than that of the normal 65 nm technology used for CHIP-B and -C fabrication. Figure 3.1 shows the well profiles for CHIP-A and -B. The difference between CHIP-A and-B is only the well profile. As shown in Table 3.1, CHIP-C has three types of SRAM macros: two macros with DNW, two macros without DNW (double-well), and twelve macros with the proposed MBU mitigation.

The package, wafer thickness, and design masks except DNW are the same for the three test chips. Thus, the density and positions of the well-contacts, which might affect MCU occurrence, are identical in all the chips. This means that the proposed mitigation technique with narrow-DNW as explained in Section 3.5 has no area overheads.

The operation voltage in the tests was 0.6 to 1.4 V, where the nominal VDD of this technology was 1.2 V. The SEU was evaluated with the ALL0/1 pattern in which all bit cells are written with “0” or “1”.

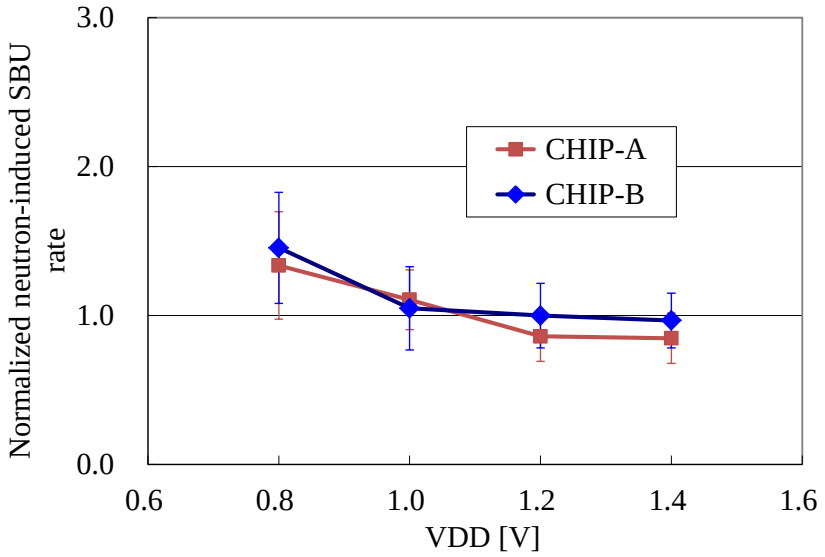


Fig. 3.2 Neutron-induced SBU rates of CHIP-A and -B normalized by SBU rate of CHIP-B at 1.2 V.

3.3 Impact of Well depth on SER

Well depth and volume would affect PBA and SER, but the impact of well profile has not been quantitatively reported in literature. This section evaluates the impact of well depth on SER through neutron and alpha irradiation tests.

Figure 3.2 and Figure 3.3 show comparisons of neutron-induced SBU and MCU rates in terms of two well depths, where the well profile of CHIP-A is deeper than that of CHIP-B as explained by Figure 3.1. The MCU rate in deeper well (CHIP-A) is about 10% higher than CHIP-B at 0.8V, but the difference is not significantly different with statistically 90% confidential level. The SBU rates are also not significant different.

Figure 3.4 and Figure 3.5 present the alpha-induced SBU and MCU rates. Although the MCU rate in CHIP-A is significantly (about 10%) higher than that in CHIP-B only at 1.0V, significant difference were not observed in MCU rates at other voltage condition and SBU rates.

Both for neutron and alpha, the MCU is sensitive to well depth compared with SBU. Well depth can change PBA contribution, and the PBA contribute to MCU more than SBU. The impact of well depth is not significant, and it is less than 10%.

3.4 Impact of deep-N-Well on SER

PBA is generally more active in triple-well (with DNW) than in double-well (without DNW), and hence the SEU rate in triple-well tends to be higher than that in double-well. This section evaluates the impact of DNW on MCU with the irradiation test results of SRAM with double-well in CHIP-B and triple-well SRAM in CHIP-C. The

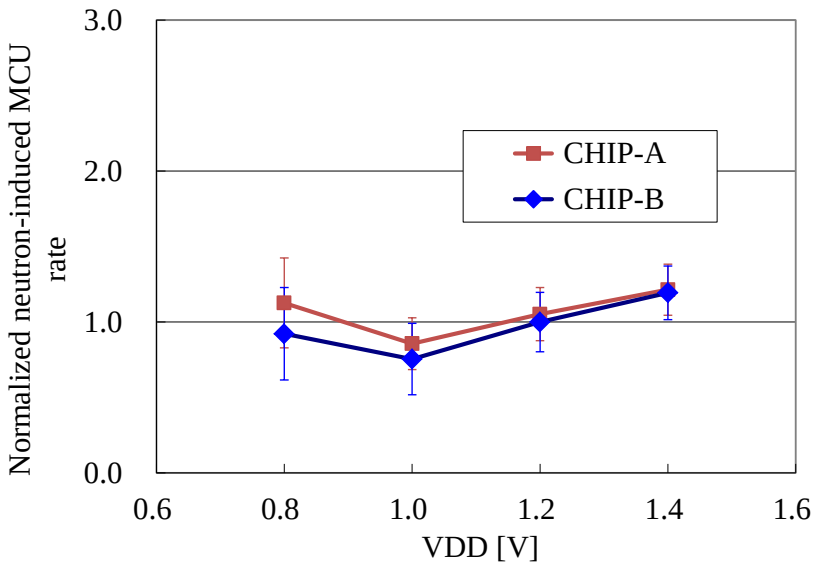


Fig. 3.3 Neutron-induced MCU rates of CHIP-A and -B normalized by MCU rate of CHIP-B at 1.2 V.

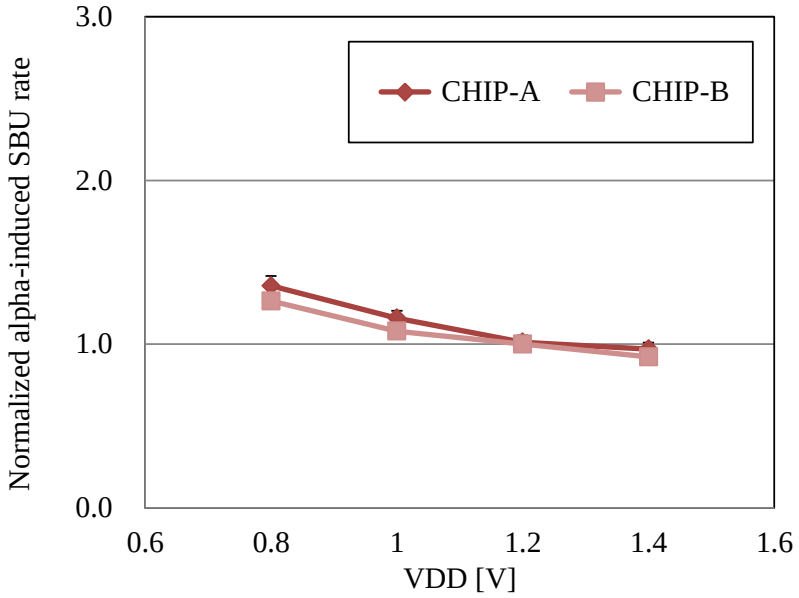


Fig. 3.4 Alpha-induced SBU rates of CHIP-A and -B normalized by SBU rate of CHIP-B at 1.2 V.

observations in this section will be used to propose an MBU mitigation technique with narrow-DNW in the next section.

3.4.1 Neutron test result

Figure 3.6, Figure 3.7, and Figure 3.8 show the results of the neutron irradiation tests. Figure 3.6 shows that the SEU rates at 0.8 V and lower were not much different

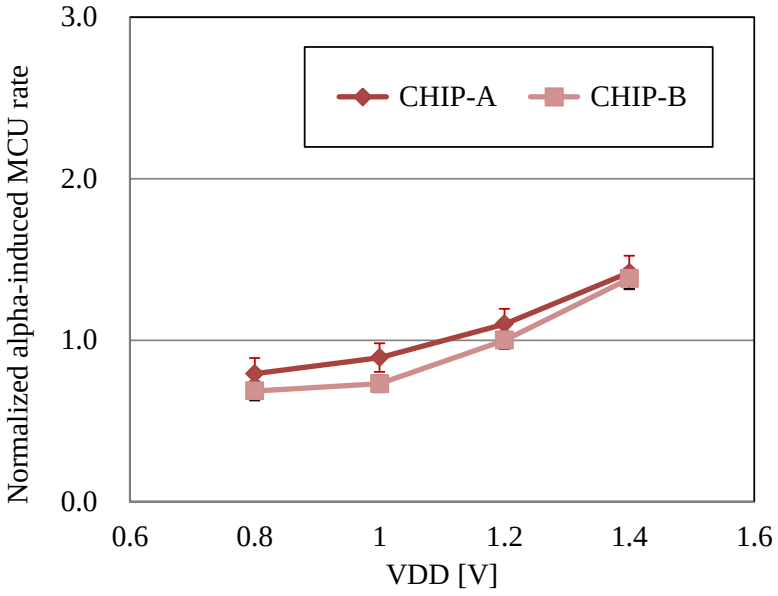


Fig. 3.5 Alpha-induced MCU rates of CHIP-A and -B normalized by MCU rate of CHIP-B at 1.2 V.

between double- and triple-well, whereas the SEU rate at above 0.8 V was higher in triple-well than in double-well. This SEU trend was due to the MCU trend shown in Figure 3.7. The MCU rate in triple-well was much higher than that in double-well, whereas no significant difference was observed in SBU between double- and triple-well in Figure 3.8.

Next, let us examine the MCU rate in Figure 3.7. There was no significant difference in the MCU rate at 0.6 V between double- and triple-well. At low voltages, parasitic bipolar transistor was less likely to be on, and hence it was less active. Due to this, the difference was small (0.6 V).

The MCU rate in triple-well monotonically increased with voltage elevation since PBA became more active at higher voltage. Also, in double-well, the MCU rate increased above 1.0 V. This result indicates that PBA contributed to MCU in double-well, and PBA-induced MCU needs to be taken into account even in double-well. Besides, the MCU rate in double-well has a non-monotonic voltage dependency. This voltage dependency comes from two contrary trends; an increase in voltage makes PBA more active and concurrently makes the Qcrit larger. The increase in Qcrit affects MCU more dominantly than PBA activation up to 1.0 V, while PBA activation elevates the MCU rate overwhelming the Qcrit increase above 1.0 V. On the other hand, the MCU rate in triple-well monotonically increased with voltage increase. This is because the PBA activation is more significant than the Qcrit increase.

3.4.2 Alpha test result

This section discusses alpha-induced upsets. Figure 3.9, Figure 3.10, and Figure 3.11 show the SEU, SBU, and MCU rates. The SEU rate in triple-well is higher than that

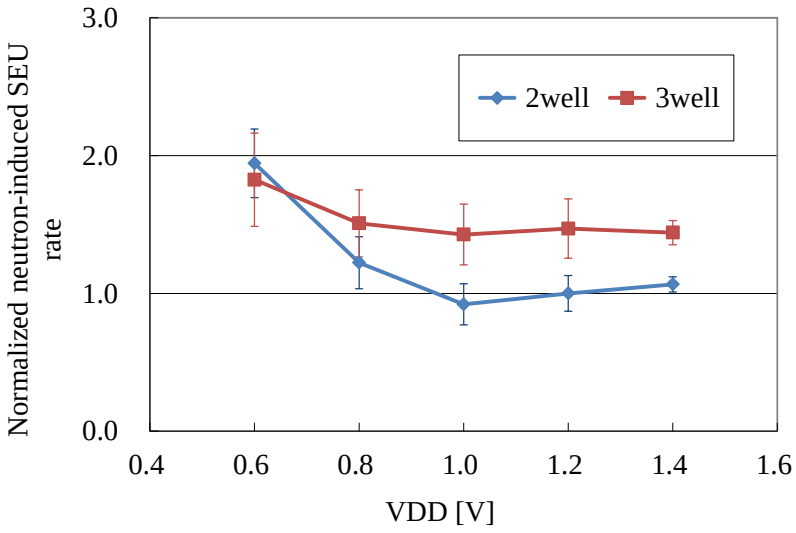


Fig. 3.6 Neutron-induced SEU rates in double-well and triple-well normalized by SEU rate at 1.2 V in double-well.

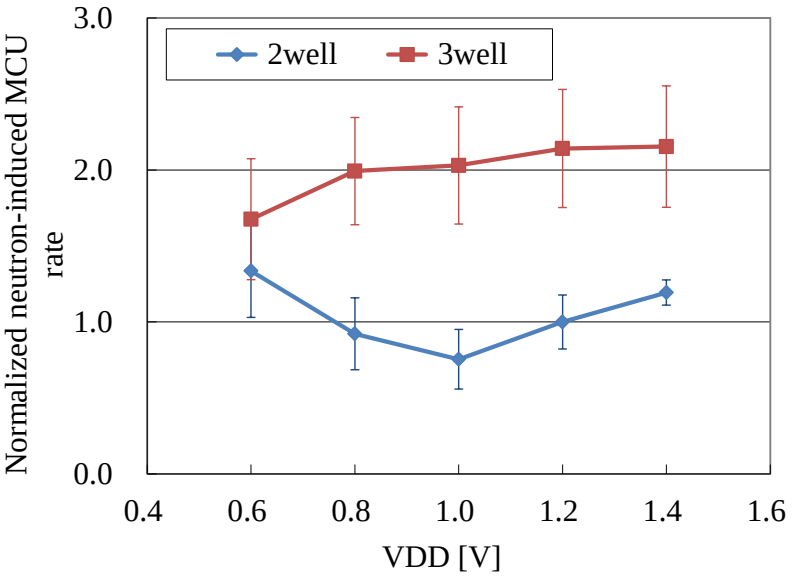


Fig. 3.7 Neutron-induced MCU rates in double-well and triple-well normalized by MCU rate at 1.2 V in double-well.

in double-well at all the voltages as shown in Figure 3.9. This SEU trend originated from the MCU trend shown in Figure 3.10. The MCU rate in triple-well is more than four times higher than that in double-well, while the SBU rates are not much different between double- and triple-well as shown in Figure 3.11. These trends of alpha-induced error rates are similar to those of the neutron-induced error rates.

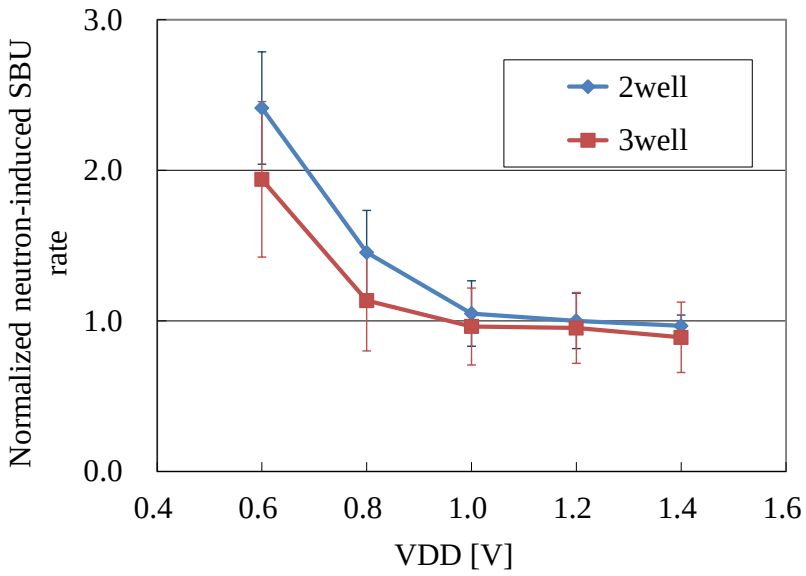


Fig. 3.8 Neutron-induced SBU rates in double-well and triple-well normalized by SBU rate at 1.2 V in double-well.

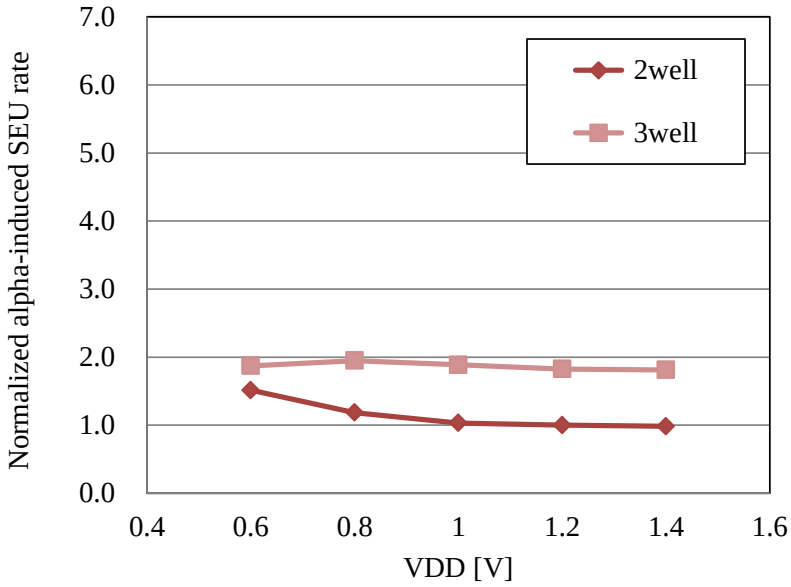


Fig. 3.9 Alpha-induced SEU rates in double-well and triple-well normalized by SEU rate at 1.2 V in double-well.

3.4.3 MBU analysis

The MBU in SRAM with col-MUX is discussed here. Remind that the MBU means the MCU that cannot be corrected by SEC-ECC. Figure 3.12 and Figure 3.13 show neutron- and alpha-induced MBU ratios, respectively. The MBU ratio is defined as the number of MBU events divided by the number of SEU events. In both the figures,

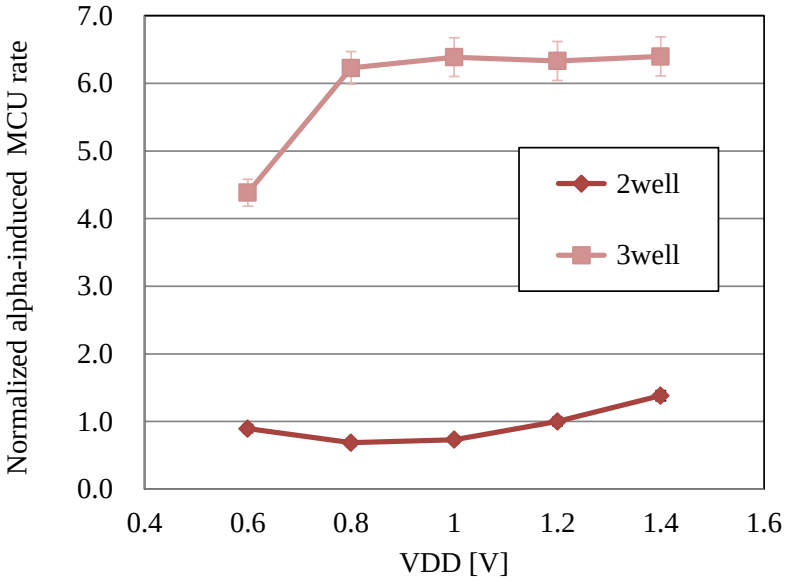


Fig. 3.10 Alpha-induced MCU rates in double-well and triple-well normalized by MCU rate at 1.2 V in double-well.

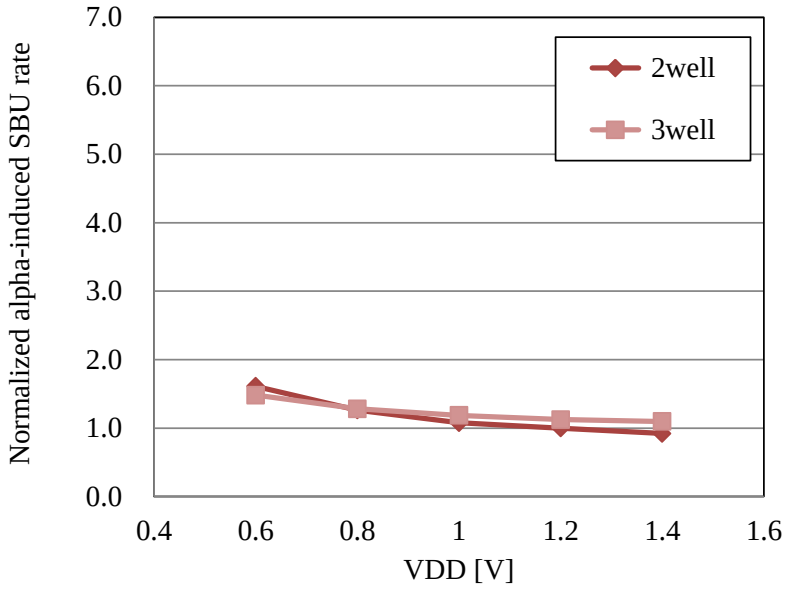


Fig. 3.11 Alpha-induced SBU rates on double-well and triple-well normalized by SBU rate at 1.2 V in double-well.

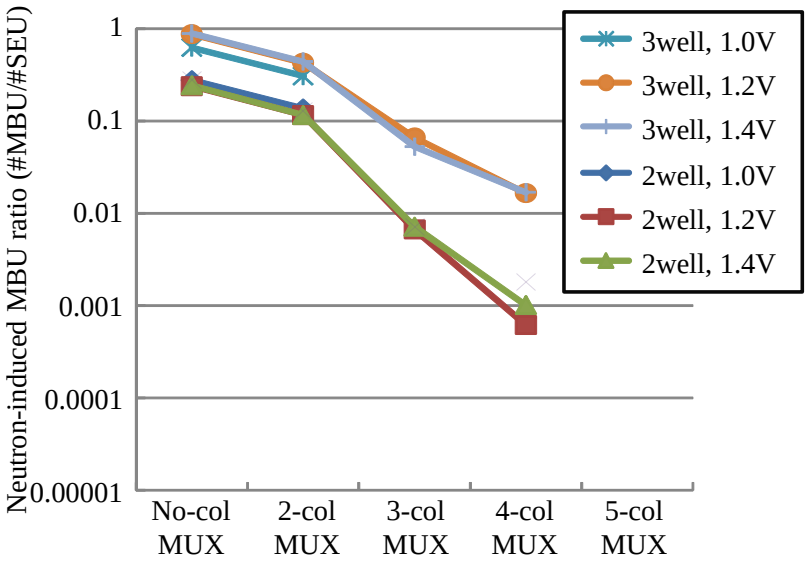


Fig. 3.12 Measured neutron-induced MBU ratio (#MBU/#SEU) in double-well (CHIP-B) and triple-well (CHIP-C).

as the col-MUX becomes larger, the MBU ratio becomes smaller, which confirms that the MBU mitigation efficiency improves with larger col-MUX. In addition, the MBU ratio in triple-well is higher than that in double-well, which is consistent with the results of MCUs.

From these results, it should be noted that, even with 4 col-MUX, MBU occurs not only in triple-well but also in double-well. In the case of 5 col-MUX, no MBUs were observed in both double- and triple-well. These results suggest that, for highly reliable SRAM, it is necessary to adopt still larger col-MUX, such as 8 col-MUX. However, as mentioned in Section 2.3.3, larger col-MUX involves unwanted performance overheads. On the other hand, SEC-ECC with 4 col-MUX is commonly used in high speed RAM macro for the processor cache. This means that an additional MBU mitigation technique applicable to SEC-ECC SRAM with 4 col-MUX with a negligible overhead is higher desirable. This is the motivation for the proposed MBU mitigation technique in the next section.

3.5 MBU mitigation

For mitigating MBU, SRAM cells included in the same word, i.e. on the same WL and on the BLs concurrently selected by col-MUXs, should be placed in different wells since PBA and/or charge diffusion, which can induce MBUs. PBA and charge diffusion both in N- and P-wells can contribute to MBU, and both wells need to be considered. PBA can contribute to MBU both in triple-well and double-well, as shown in the previous section. With triple-well process, N-wells of SRAM bit cells in the same word are connected through DNW. Without the DNW process, i.e. double-well, P-wells of SRAM bit cells in the same word are connected through the P-substrate. In both well structures, bits in the same word are connected to each other through

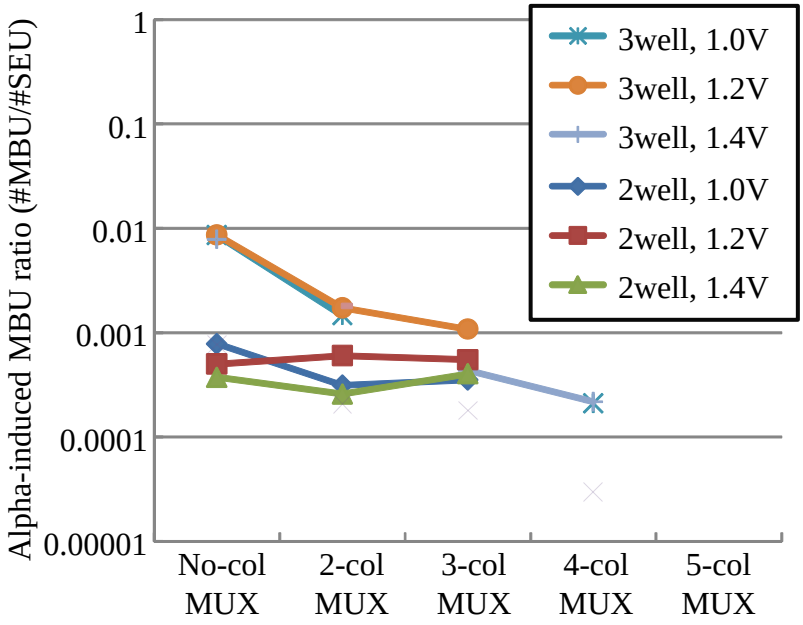


Fig. 3.13 Measured alpha-induced MBU ratio (#MBU/#SEU) in double-well (CHIP-B) and triple-well (CHIP-C).

the shared wells. The proposed technique achieves the well isolation by introducing narrow DNW.

3.5.1 Mitigation technique by narrow DNW

Firstly, this section explains the proposed technique that uses narrow DNW for MBU mitigation. Figure 3.14 illustrates the structure of the proposed MBU mitigation technique. Figure 3.14 (a) shows the conventional cell layout consisting of one N-well and two P-well areas, and the same cell layout was used in the proposed technique. On the other hand, narrow DNWs are placed under every 4 columns for mitigating MBU as shown in Figure 3.14 (b). In addition, the cell positions of columns 1 - 2 and 3 - 4 are exchanged as shown in Figure 3.14 (c).

Let us explain how the technique works. An important feature of the technique is that N-wells (P-wells) in the same word, which share the same WL and the BLs concurrently selected by col-MUXs, are not connected. The P-well of the SRAM cell outside DNW connects with the P-substrate and does not connect with the P-well of the SRAM cell inside DNW as shown in Figure 3.14 (b). On the other hand, this structure horizontally repeats for organizing multi-byte words as shown in Figure 3.14 (c). Strictly speaking, P-wells sharing the same word appear every 8 bit, which indicates that the proposed MBU mitigation technique is expected to attain the MBU mitigation efficiency of 8 col-MUX implementation. Larger values of col-MUX lead to lower MBU rate as discussed in the previous section. Thus, the structure is expected to significantly reduce MBU.

The necessary modifications for the proposed technique are just putting narrow

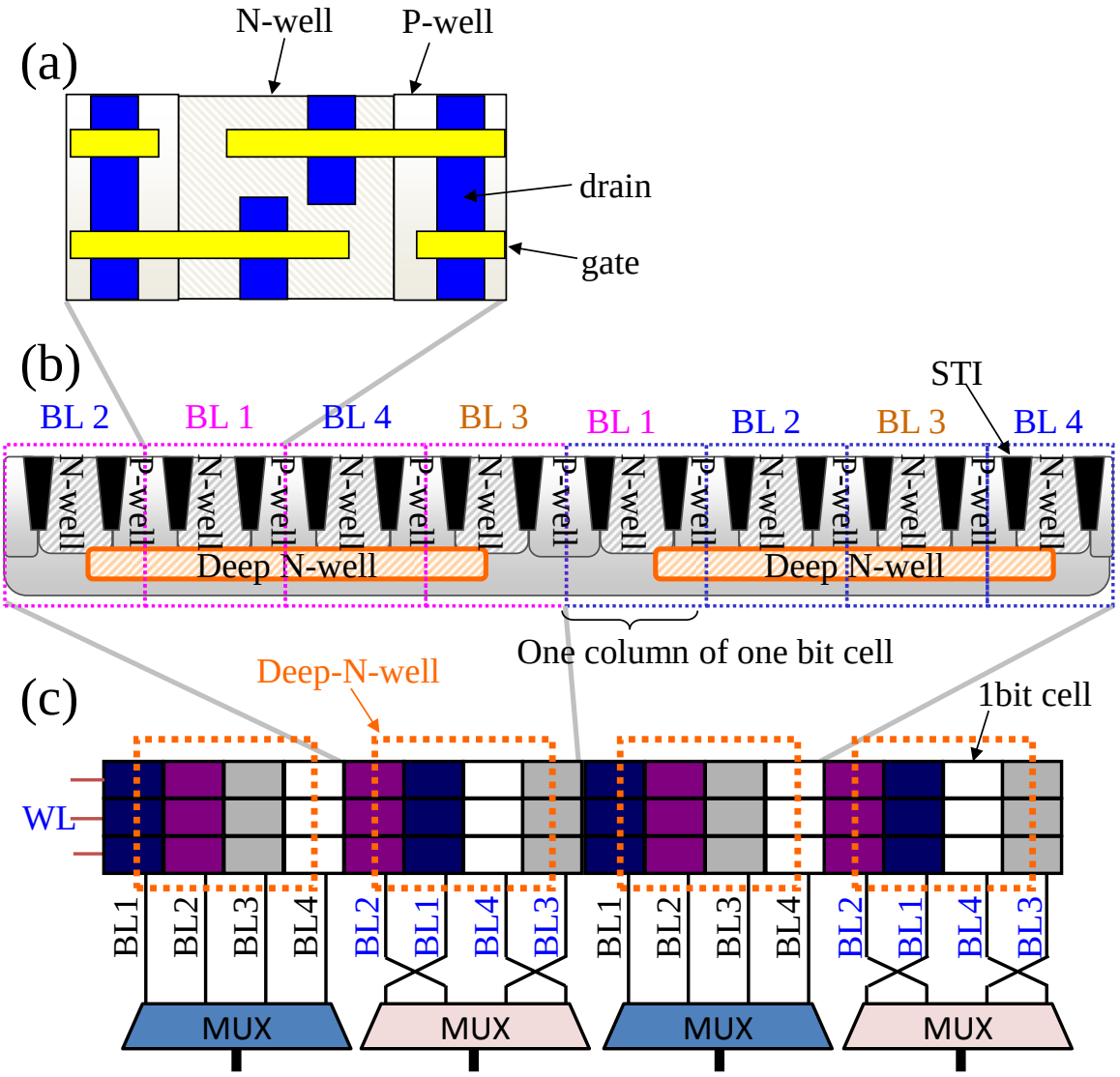


Fig. 3.14 Proposed MBU mitigation technique. (a) layout of one bit SRAM, (b) cross-section of MBU mitigation structure, and (c) interconnection. N-wells (P-wells) of bit cells in the same word (i.e. the same BL number) were not connected.

DNW into normal SRAM macros and altering col-MUX interconnections. A general design rule may not allow us to use the narrow DNW, but there is no fundamental obstacles for the proposed mitigation technique because the design rules on DNW are decided to sustain well-to-well voltage tolerance for enabling body-biasing. On the other hand, the same voltage is given to P-wells in and outside DNW in this mitigation technique, and hence no voltage tolerance issues associated with narrow DNW arise. The manufacturability of the narrow DNW will be confirmed in the next subsection.

An advantage of the proposed technique is that the SRAM macro size is unchanged. The potentials of P-well and N-well are VSS and VDD, respectively, which is similar to the ordinary double-well design. Therefore, well-contacts in the ordinary SRAM

cell also worked well in the proposed SRAM with narrow DNW, which results in the same cell area. In addition, in the case when MOSFET characteristics in double-well are the same as those in triple-well, the proposed technique can be applied without performance or power overheads. This condition is mostly true, since MOSFETs are generally developed so that there is no difference in performance and power consumption between double-well and triple-well. A concern is that an additional mask for DNW could increase the cost. On the other hand, the proposed technique aims to achieve high reliability of processors for mission critical servers. Such processor chips often include high-speed I/O circuits using DNW for noise isolation, and no additional cost is necessary for such chips.

3.5.2 Well structure analysis

To confirm the manufacturability of the narrow DNW, the narrow DNW structures were evaluated with using SNDM [126, 127, 128, 129]. SNDM can perform high spatial resolution measurements of conductive polarization and/or conductive carrier concentration of well structure. SNDM is one of the scanning probe microscope (SPM) techniques to measure electronic properties of semiconductor materials. SNDM was originally developed to measure the polarization direction of ferroelectric materials. Recently, SNDM has been used to observe semiconductor materials, for example, to visualize charges in nonvolatile flash memory [130, 131, 132, 133]. In this work, the conductive polarization distribution of DNWs in SRAM was finely analyzed by SNDM.

Figure 3.15 shows the results obtained from atomic force microscopy (AFM) and SNDM, where AFM was also one of the SPM techniques and was used for observing topographic images. Figure 3.15 (a) shows an AFM topographic image that was observed simultaneously with the SNDM images. In the topographic image, the contacts exposed to the surface are visualized as the white vertical bars. An SNDM image is shown in Figure 3.15 (b). The red region in the SNDM image indicates p-type polarization (carrier), and the blue-color region represents n-type carrier. The region of the DNW is clearly shown. To visualize the spatial distribution of each conductive carrier, the SNDM image was divided into two images depending on the sign, and the absolute intensity images of the n- and p-type carrier are shown in Figure 3.15 (c) and (d), respectively. Furthermore, Figure 3.15 (c) clarifies that the region of DNW does not connect with other regions of DNW, and Figure 3.15 (d) shows that P-wells in DNW were isolated from the P-substrate. Thus, the proposed structure with narrow DNW is manufacturable.

3.5.3 Mitigation efficiency evaluation

The MBU mitigation efficiency of the proposed SRAM with narrow DNW on CHIP-C was evaluated through neutron and alpha irradiation experiments. Figure 3.16 shows the alpha-induced MBU rate of 4 col-MUX ECC. The voltage dependence on MBUs is not statistically significant. Even while the total number of detected errors is 588,322 in the alpha experiment, only one or two MBUs were observed at each voltage. The measurement results show that the MBU mitigation for alpha particles is not drastic.

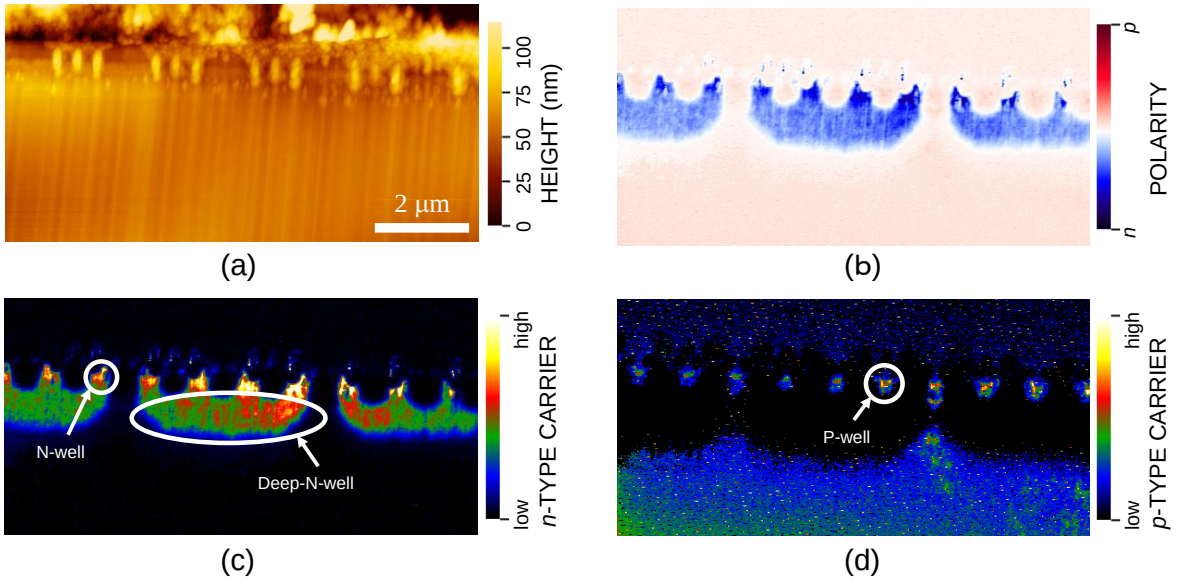


Fig. 3.15 (a) Topographic image obtained by AFM, (b) Observed SNDM image, (c) N-type carrier distribution, (d) P-type carrier distribution.

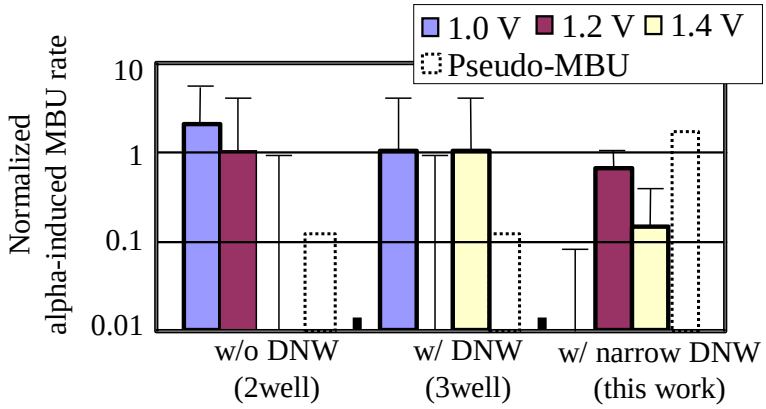


Fig. 3.16 Measured MBU rates in alpha irradiation experiment normalized by MBU rate at 1.2 V in double-well. Pseudo-MBU rates obtained by simulation are also plotted.

To investigate the reason, a Monte Carlo simulation was carried out for calculating the probability that multiple SBUs were recognized as an MBU, which is called a pseudo-MBU. In this simulation, SBUs were injected randomly in time and space assuming the measured SBU rate, performed MCU checking as explained in Section 3.2, and finally picked up the pseudo-MBUs.

Figure 3.16 also shows the pseudo-MBU rate from the simulation results. In the conventional SRAMs with and without DNW, the measured MBU rates were ten times higher than the pseudo-MBU rates, and true MBUs were observed. On the other hand, in the proposed SRAM, the pseudo-MBU rate was comparable with the measured MBU rates, and pseudo-MBUs seem to be included in the measured MBUs.

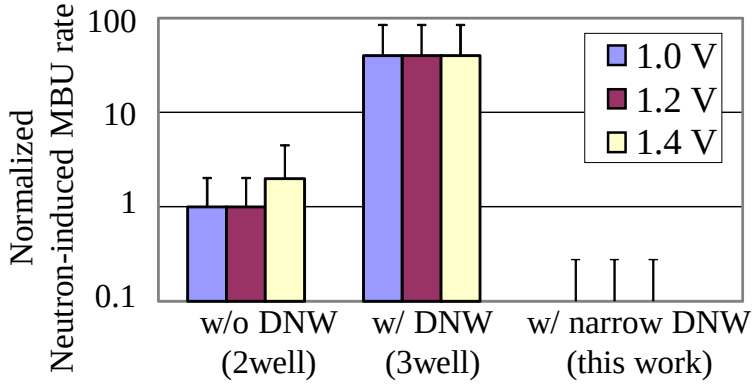


Fig. 3.17 Measured MBU rates in neutron irradiation experiment normalized by MBU rate at 1.2 V in double-well.

Besides, the pseudo-MBU rate of the proposed SRAM was higher than those of conventional SRAMs w/o and w/ DNW. This difference occurs because the probability of pseudo-MBU drastically changes between 3 col-MUX and 4 col-MUX, where the proposed SRAM with narrow DNW consisted of 3 col-MUX and 5 col-MUX due to wire swapping as illustrated in Figure 3.14 (c). The reason for this drastic change is that upset bits within a three-cell distance are thought to be caused by the same event in MCU checking. Therefore, the pseudo-MBU rate for the proposed SRAM was mostly determined by that of 3 col-MUX, and then it was higher than those of conventional SRAMs with 4 col-MUX.

The neutron irradiation test, on the other hand, clearly shows the MBU mitigation effect due to the narrow DNW. Figure 3.17 shows neutron-MBU rates of the conventional 4 col-MUX ECC SRAM with DNW and without DNW and of the proposed SRAM with narrow DNW. No errors were observed in the proposed SRAM in the neutron experiments, while neutron-induced MBU occurred in both the conventional SRAMs with and without DNW. The voltage dependences on MBU were consistent with those on MCU in Figure 3.7. This result shows the excellent mitigation efficiency of the proposed technique with narrow DNW.

3.6 Conclusion

The impact of well structure was investigated through alpha and neutron irradiation tests on SRAM SER. Well depth affected the SEU rate for alpha-induced soft errors at low voltage. PBA contributed to alpha- and neutron-induced MBUs both in triple-well and double-well. MBU was observed in the SEC-ECC SRAMs with 4 or smaller col-MUX both in double- and triple-well.

This chapter proposed an MBU mitigation technique that used DNW in contrast to the common practice that DNW raises the SER. The proposed technique used narrow DNW for isolating the wells of cells that are simultaneously selected. The experimental results showed that the proposed MBU mitigation technique with narrow DNW could reduce neutron-induced MBU. This technique has no area overheads. In

addition, it generally involves no performance or power overheads.

Chapter 4

SEL mitigation with deep P-well in SRAM

This chapter discusses SEL prevention by altering well configurations [134, 135]. The well structures under consideration in this chapter are triple-well structure with deep P-well (DPW), which is newly proposed in this chapter, ordinary double-well structure and triple-well structure with deep N-well (DNW). Doping profiles are also varied in our experiments. Neutron irradiation tests for test chips fabricated in 55 nm and 90 nm bulk Si CMOS processes show that SEL can be suppressed with a DPW or a DNW well configuration and a high-dose implantation in the well.

4.1 Introduction

SEL occurrence in SRAM is one of the most important reliability issues for SRAM based electron devices fabricated in bulk CMOS technology. SEL is an abnormal high-current state in a device triggered by the passage of an energetic particle, and it results in the loss of device functionality [136, 137]. SEL can cause permanent damage to the device [138]. Even if the device is not permanently damaged, the device needs to be turned off to recover from SEL [4]. This means that popular countermeasures for concealing upsets, such as ECC, are helpless to SEL since SEL cannot be terminated. SEL had been regarded as an issue only for the devices used in environment having high energy particles densely, such space environment [139]. On the other hand, SEL is becoming a critical concern even at ground level because terrestrial neutrons can cause SEL in technology nodes below 160 nm [140]. Dodd et al. reported that non-negligible SEL rates were observed in commercial products at terrestrial environment [141].

An abnormal current flows when a parasitic p-n-p-n bipolar, i.e. thyristor, in bulk CMOS devices is activated and power and ground are shorted [142, 143]. Note that there is no p-n-p-n junction in SOI devices and hence SOI devices are immune to SEL [86]. The parasitic p-n-p-n bipolar consists of P-drain, N-well, P-well and N-drain as shown in Figure 4.1. Key parameters which influence SEL occurrence are the resistors (R_{NW} and $R_{PW\&Psub}$ in Figure 4.1) and the current gains of the parasitic bipolar transistors (NPN and PNP in Figure 4.1). $R_{PW\&Psub}$ is determined by the

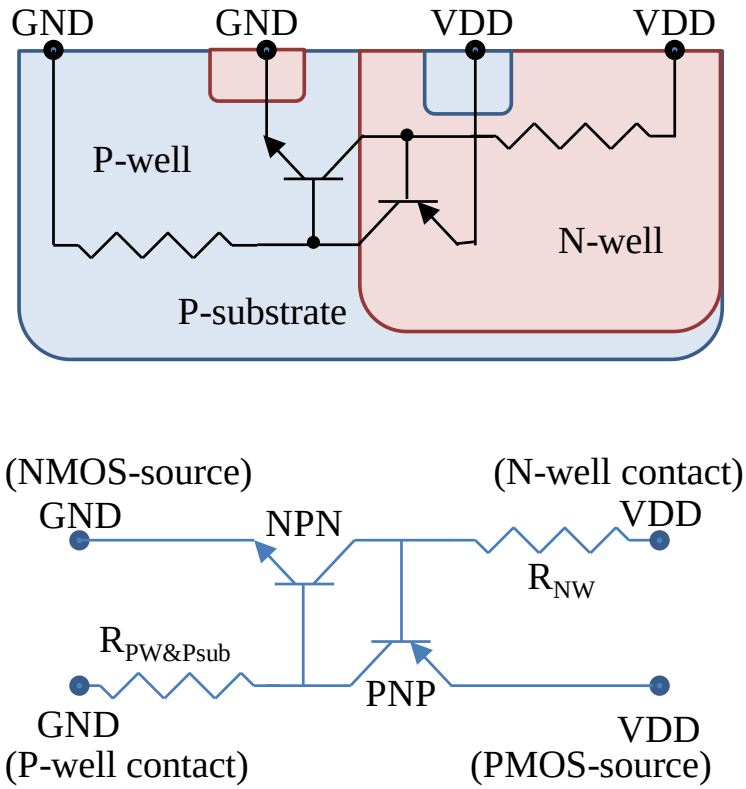


Fig. 4.1 Schematic of parasitic bipolar transistors contributing to SEL in a typical bulk CMOS structure.

resistivity of the P-well and the P-substrate and the distance between the NMOS transistor and P-well-contacts. Similarly, R_{NW} depends on the N-well resistivity and the distance between the PMOS transistor and the N-well-contacts. The current gains are determined by doping concentrations in the well and source regions and the distance between the well-junction and source regions.

To prevent SEL, several design techniques have been proposed. Enlarging the distance from well edge to MOS source regions can suppress SEL [144]. Nicolaidis proposed an SEL mitigation scheme with built-in current sensor [145]. Adding a current-limiting device (CLD) to power line can also mitigate SEL since the reduction of power supply current prevents the parasitic bipolar from being activated [80, 81]. Inserting well-taps, which consists of well-contacts, in SRAM cell area also mitigates SEL [146]. All these techniques increase the circuit area and standard SRAM macro needs to be re-designed.

On the other hand, process modification instead of design modification is an alternative approach. Using epitaxial wafer or thick wafer helps to reduce SEL, but its efficiency is quite limited [88]. It is known that well configuration changes SEL sensitivity. Using DNW prevents SEL effectively [147], where DNW is a popular process option in bulk CMOS manufacturing processes and it is easy to be applied. However, the DNW application accompanies an undesirable side effect that SEU increases, since PBA becomes more likely to occur [34]. Consequently if the increase in SEU rate due

to DNW is not acceptable in products, ECC, which requires SRAM re-design, must be adopted compromising with overheads in speed and area.

This chapter firstly proposes an SEL prevention technique that uses DPW on P-substrate in Section 4.2. After that, Section 4.3 to Section 4.6 comprehensively study well configurations including ordinary double-well without deep-well, triple-well with DNW and triple-well with DPW in terms of SEL tolerance, and give implications on the selection of well configuration taking into account both SEL and SEU. The dependences of SEL rate on well-tap interval in double-well, well dose of double-well, and dose of DPW are also evaluated. In addition, Section 4.6 gives a discussion on the mechanism of DPW for SEL prevention from two aspects; gain of parasitic bipolar transistors and stability of well potential. Well resistivity reduction thanks to DPW, which helps stabilize well potential, is experimentally confirmed. Section 4.7 also shows that DPW is comparable or might be more effective for SEL prevention than CLD both in 55 nm and 90 nm.

The rest of this chapter is organized as follows. Section 4.2 proposes an SEL mitigation technique with DPW. Section 4.3 explains experiments design to explore well configurations for minimizing SEL. Section 4.4 to Section 4.6 show measurement results of neutron irradiation tests. Based on these measurement results, Section 4.7 discusses how well configuration should be selected. Also a comparison between DPW and another technique with current-limiting device is presented there. Finally concluding remarks are given in Section 4.8.

4.2 SEL mitigation by deep P-well

The proposed SEL prevention technique puts DPW under N- and P-wells on P-substrate as shown in Figure 4.2. The DPW can be expected to be easily adopted without changing design rule because DPW does not split any well area, which is different from DNW. The DPW is expected to have three effects contributing to SEL prevention. First, DPW decreases the resistance between SRAM cell and well-contacts ($R_{PW\&Psub}$ in Figure 4.1) and suppresses well potential variation. Second, the gain of parasitic n-p-n bipolar transistor, which consists of NMOS-source, P-well and N-well, decreases due to an increase in effective accepter concentration in the base (Phosphorus). Third, DPW could prevent the electrons which are generated below DPW from being collected to N-well although DPW does not isolate P-substrate and P-well.

4.3 Experiment design

This chapter explores well configurations in terms of SEL and SEU based on experimental results of neutron irradiation tests. To achieve this, it is needed to prepare a comprehensive experiment design consisting of test chip design and irradiation test setup. Our target circuit is SRAM in this chapter.

The first step is test chip design. There are three well configurations under our consideration; double-well without deep-well, triple-well with DNW and triple-well with DPW shown in Figure 4.3, where these three well configurations are hereafter

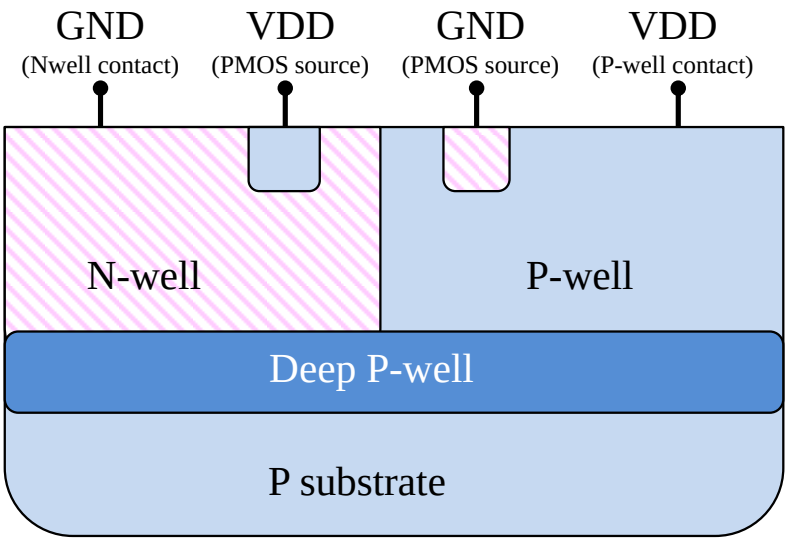


Fig. 4.2 Deep P-well structure.

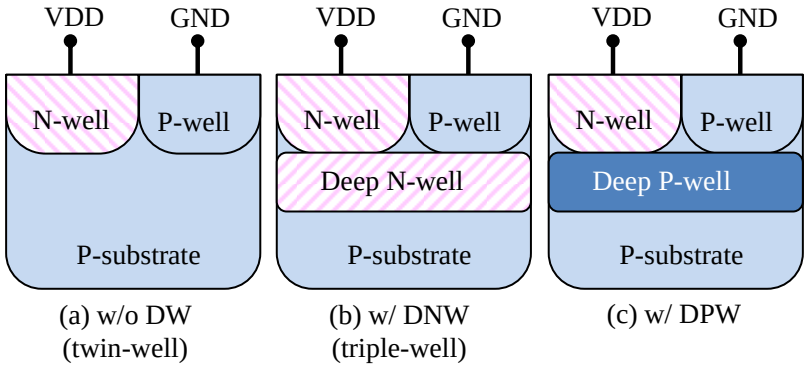


Fig. 4.3 Well configurations; (a) double-well (2W), (b) ordinary triple-well with deep N-well (DNW) and (c) with deep P-well (DPW).

abbreviated to 2W, DNW and DPW. To evaluate the impact of these well configurations on SEL and SEU, test chips should include these well configurations. SEL and SEU are thought to depend on well-tap interval and well dose, and then it is desirable to prepare test chips having different well-tap intervals and well dose. In addition, to assess the dependence of SEL and SEU on technology nodes, test chips fabricated in different technology nodes need to be tested.

To cover these requirements, twelve test chip designs were prepared, and listed in Table 4.1. Each test chip includes SRAM whose SRAM cell consists of conventional 6T cells. Five designs were fabricated in 90 nm process and other seven designs were fabricated in 55 nm process, where all the twelve designs were manufactured with P-substrate epitaxial wafers. DNW or DPW was formed across the whole chip except I/O area. DESIGN-A to -I have various well-tap intervals. DESIGN-J and -K are included to evaluate the effectiveness of SEL prevention with CLD. All the fabricated

Table. 4.1 Summary of test chip designs. The well-tap distances are normalized by that of DESIGN-B. Number in parentheses in well configuration represents the number of variation in dose.

Design	Technology	Well-tap interval	Well-tap area /cell area	CLD	Well configuration
DESIGN-A	90 nm	3.16	3.3%	No	2W(1), DPW(1)
DESIGN-B	90 nm	1.00	104%	No	2W(1)
DESIGN-C	90 nm	2.76	3.8%	No	2W(1)
DESIGN-D	90 nm	3.33	3.1%	No	2W(4), DNW(1), DPW(1)
DESIGN-E	55 nm	0.50	13.6%	No	2W(1)
DESIGN-F	55 nm	1.00	6.8%	No	2W(1)
DESIGN-G	55 nm	1.04	6.7%	No	2W(1), DPW(2)
DESIGN-H	55 nm	1.57	4.4%	No	2W(1)
DESIGN-I	55 nm	2.00	3.4%	No	2W(1)
DESIGN-J	55 nm	1.04	6.7%	Yes (add to DESIGN-G)	2W(1), DPW(1)
DESIGN-K	90 nm	3.16	3.3%	Yes (add to DESIGN-G)	2W(1), DPW(1)

test chips were assembled on plastic packages with wire bonding.

Next, irradiation test setup is examined. When evaluating SEL, data pattern dependence could be observed. In addition, test types, i.e. static and dynamic tests, may show different tendencies.

Using the test chips in Table 4.1, seven tests listed in Table 4.2 were performed. TEST-1 aims to investigate the dependence of SEL and SEU on test type and data pattern using test chips of DESIGN-A(2W). Figure 4.4 illustrates static and dynamic tests. In the static test, all SRAM bits are written, and are read after fifteen minutes passed. In the dynamic test, once the data are written, the data are repeatedly read until one hundred upsets are observed. This result will be presented in Section 4.4.1. Based on this experimental result, test type and data pattern are decided for the successive tests.

Next, TEST-2 and -3 evaluate the impact of well-tap interval on SEL in 55 nm and 90 nm, respectively. DESIGN-E, -F, -G and -I are used for TEST-2, and DESIGN-B, -C, and -D are used for TEST-3, where all the test chips used here were manufactured in double-well process. These results will be presented in Section 4.4.2.

TEST-4 evaluates the impact of 2W, DNW and DPW on SEL and SEU using DESIGN-D in 90 nm. In this test, four 2W test chips having different doses, one DNW test chip and one DPW test chip were irradiated. Using the four 2W test chips, the dependence of SEL on dose can be examined in TEST-4. This result will be discussed in Section 4.5.

SEL in DPW is studied further. TEST-5 studies the relation between DPW dose and SEL prevention efficiency. This result will be discussed in Section 4.6.

Finally, Section 4.7 summarizes the results of TEST-1 to -5 and gives recommendation for selecting the best well configuration for SEL and SEU. In addition, SEL prevention efficiency of DPW will be compared with CLD, where CLD efficiency is evaluated in TEST-6 and -7.

Table. 4.2 Irradiation test list.

TEST	Purpose	Test Chip	Facility	VDD	Temp.
TEST-1	Evaluate dependence on test type and data pattern	DESIGN-A (2W)	ANITA	1.2V	RT*
TEST-2	Evaluate dependence on well-tap interval in 55 nm	DESIGN-E (2W), DESIGN-F (2W), DESIGN-G (2W), DESIGN-H (2W), DESIGN-I (2W)	RCNP	1.2V	RT*
TEST-3	Evaluate dependence on well-tap interval in 90 nm	DESIGN-B (2W), DESIGN-C (2W), DESIGN-D (2W)	RCNP	1.2V	RT*
TEST-4	Evaluate dependence on well configuration (dose & 2W/DNW/DPW)	DESIGN-D (2W with four different dose, DNW, DPW)	RCNP	1.2V	RT*
TEST-5	Evaluate dependence on dose in DPW	DESIGN-G (2W, DPW with two different dose)	RCNP	1.2V 1.4V	RT*
TEST-6	Compare SEL prevention efficiency between CLD and DPW in 55 nm	DESIGN-J (2W, DPW)	ANITA	1.1V 1.2V 1.3V	85C
TEST-7	Compare SEL prevention efficiency between CLD and DPW in 90 nm	DESIGN-A (DPW) DESIGN-K (2W, DPW)	LANSCE	1.2V 1.3V	RT* 85C

* Room temperature

The tests of TEST-1 to TEST-7 were performed with the spallation (board energy) neutron beams of RCNP, LANSCE, and ANITA. These neutron beam energy spectra are similar with the sea level spectrum as shown in Figure 1.13 and suitable for evaluating single event effects for terrestrial neutrons. On the other hand, to exclude a possible beam-dependent difference, the results are compared within those obtained with the same beam.

The occurrence of SEL was counted when unusual current was observed in power supply line, where the unusual current was assumed to be higher than the usual current by ten percent or more. For counting SEL, the current was monitored at five-second interval. The read operation was performed according to the timing chart shown in Figure 4.4, regardless of SEL occurrence. In case that the current in power supply line exceeded a threshold value, on the other hand, the running test was immediately stopped to prevent the test chip from being permanently damaged.

4.4 Dependence on test type, data pattern and well-tap interval

First, the dependence of SEL sensitivity was investigated on test conditions; data pattern stored in SRAM and test types of dynamic and static tests (TEST-1). Also, the dependence on well-tap interval was studied (TEST-2 and -3).

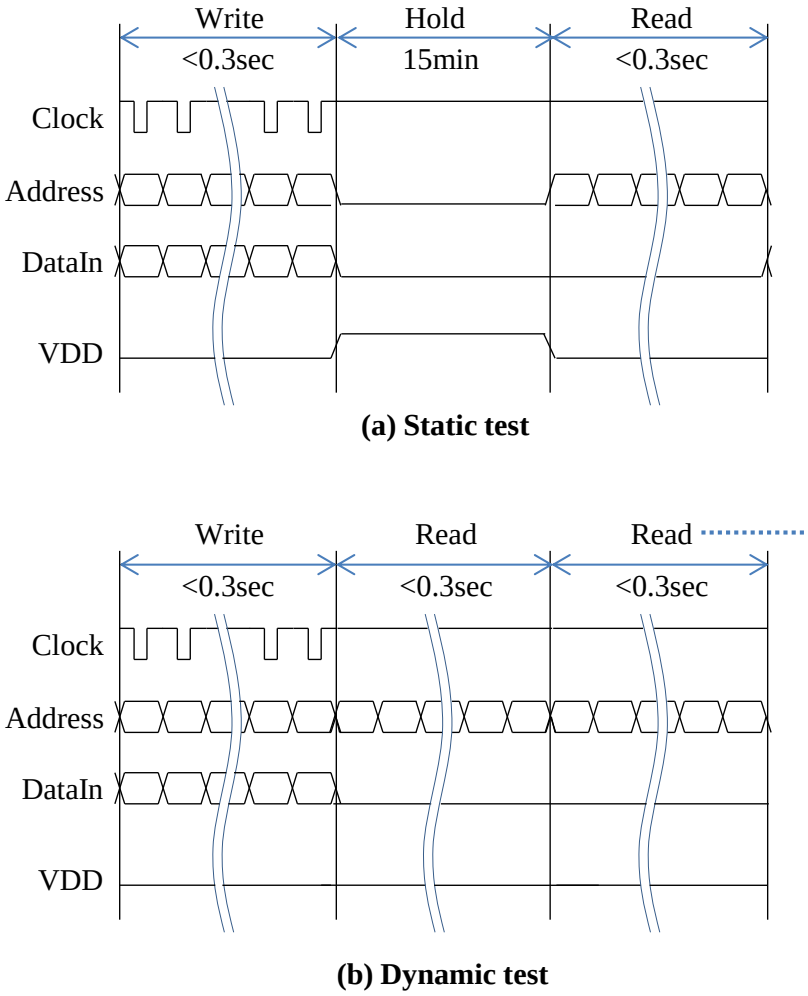


Fig. 4.4 Two types of test; (a) static and (b) dynamic tests.

4.4.1 Dependences on test type and data pattern (TEST-1)

TEST-1 was performed to clarify a test condition in which SEL was more likely to occur. In this test, checker board (CHB) and all same data (ALL0/1) patterns were used. Figure 4.5 shows the test result. Under the static test, the dependence on written data pattern was hardly observed. On the other hand, the test type could affect SEL rate. However, the observed difference was within the error bars of 99% confidential level. This result of TEST-1 turns out that the test type and written data pattern are not critical factors for evaluating SEL in irradiation test. Therefore, SEL was evaluated via static test with CHB pattern in TEST-2 to -5. Besides, SRAM operation could be affected by CLD, and hence dynamic test was selected for TEST-6 and -7.

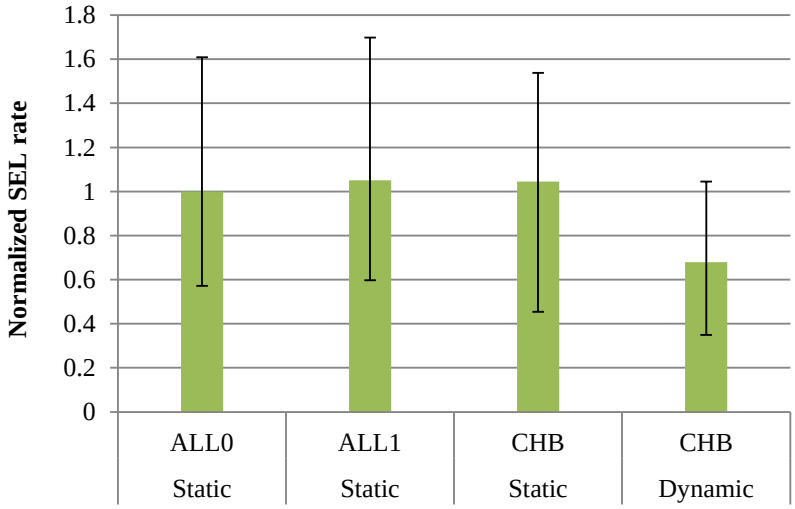


Fig. 4.5 TEST-1 result. SEL rates at 1.2 V on CHIP-A (2W) with error bars at 99% cofidential level. SEL rates are normilized by the SEL rate for static test with ALL0 pattern.

4.4.2 Dependences on well-tap interval (TEST-2 and -3)

Next, TEST-2 and TEST-3 were carried out for investigating the dependence on well-tap interval. As explained in Section 4.1, resistors of R_{NW} and $R_{PW\&Psub}$ in Figure 4.1 are key parameters for SEL sensitivity, and these depend on well-tap interval.

Figure 4.6 shows the measured SEL rates in 55 nm (TEST-2). The result suggests that there is a threshold value of well-tap interval that drastically changes SEL sensitivity. SEL rates were kept low for 0.5 and 1.6 well-tap intervals while SEL rate increased by two orders of magnitude in case of 2.0 well-tap interval. A similar tendency was observed in 90 nm SRAM and this is shown in Figure 4.7. The threshold value was different, but the SEL rate for 3.3 well-tap interval of DESIGN-D was higher than that for 2.8 well-tap interval of DESIGN-C by two orders of magnitude.

These results also indicate that even at room temperature and normal voltage, SEL can be observed especially in SRAM with large well-taps interval. In SRAM design, the well-tap interval should be smaller than such a threshold value. Adding more well-taps leads to shorter well-tap interval and higher SEL tolerance, but the area overhead of the well-tap is not negligible as shown in Table 4.1. Here, the cell area does not include the well-tap area. To minimize the area overhead of the well-tap, it is needed to carefully evaluate the threshold value. On the other hand, when evaluating the SEL prevention efficiency with a limited irradiation beam time, SRAM with large well-tap interval can be a good DUT, since the number of SEL occurrence could be large.

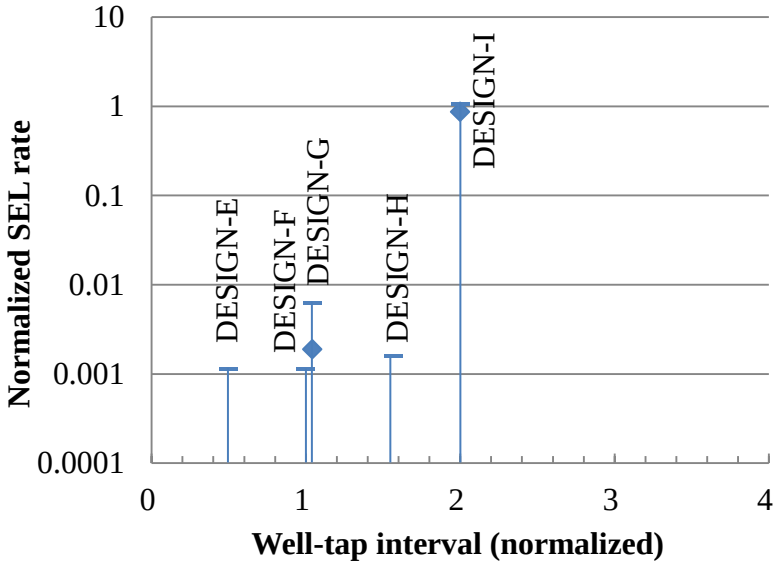


Fig. 4.6 TEST-2 result. SEL rates in 55 nm SRAM at 1.2 V on DESIGN-E (2W), DESIGN-F (2W), DESIGN-G (2W), DESIGN-H (2W) and DESIGN-I (2W) with error bars at 99% confidential level with one(up)-sided estimation as a function of well-tap interval. SEL rates are normalized by the SEL rate of DESIGN-D(2W) shown in Figure 4.7. Note that no SELs were observed in DESIGN-E, -F and -H.

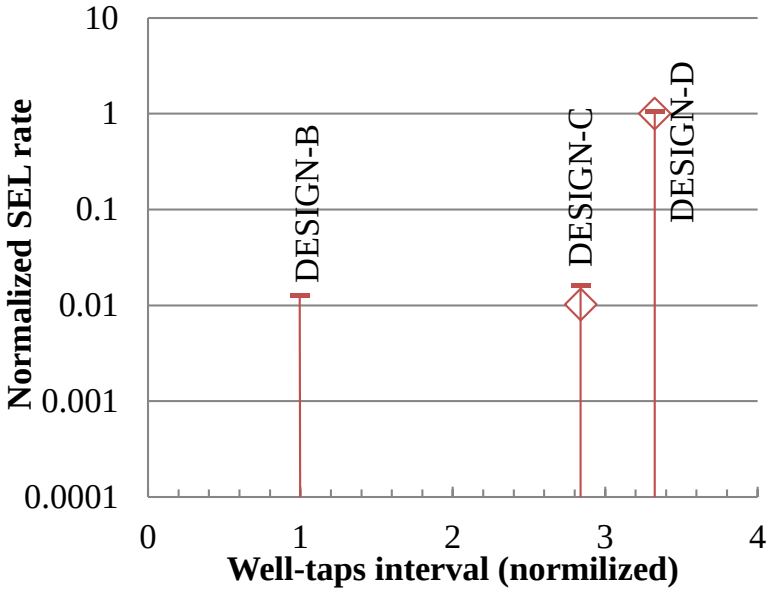


Fig. 4.7 TEST-3 result. SEL rates in 90 nm SRAM at 1.2 V on DESIGN-B (2W), DESIGN-C (2W) and DESIGN-D (2W) with error bars at 99% confidential level with one(up)-sided estimation as a function of well-tap interval. SEL rates are normalized by the SEL rate of DESIGN-D (2W). Note that no SELs were observed in DESIGN-B.

Table. 4.3 Well process conditions for DESIGN-D.

Wafer	Symbol	N-well dose	P-well dose	DNW	DPW
W0	Ref.	1.0 (normalized)	1.0 (normalized)	No	No
W4	NW+	1.0	1.2	No	No
W2	PNW+	1.5	1.5	No	No
W6	PNW++	4.0	4.0	No	No
W3	DNW	1.0	1.0	Yes	No
W1	DPW	1.0	1.0	No	Yes

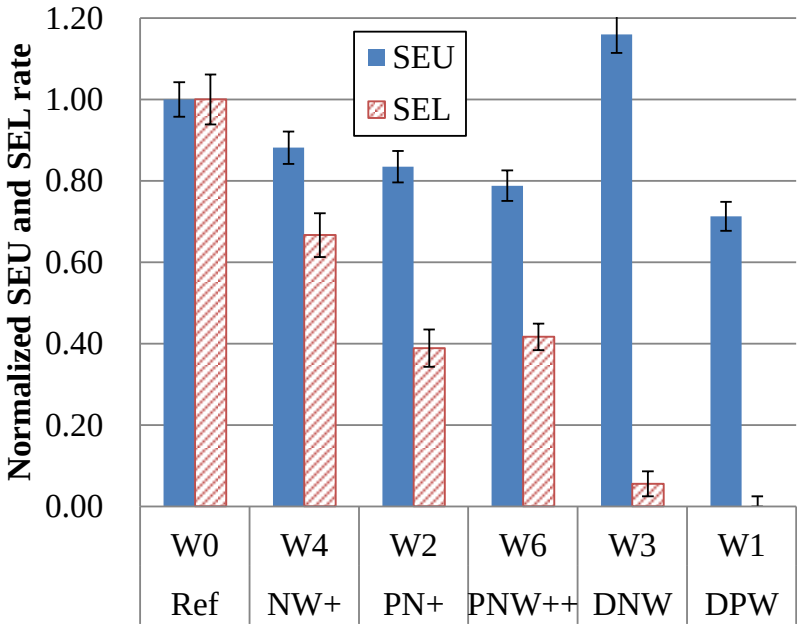


Fig. 4.8 TEST-4 result. SEU and SEL rates in six well process conditions listed in TABLE 4.3. SEU and SEL rates are normalized by SEU and SEL rates of W0 (reference), respectively.

4.5 Dependence of SEL on well configurations (TEST-4)

This section evaluates SEL and SEU dependence on well configurations using DESIGN-D, which was the most SEL sensitive design in TEST-3. Test chips of DESIGN-D was fabricated with six different conditions of well process listed in Table 4.3. Note that all the DESIGN-D test chips were manufactured with the same masks and processes except the well process. The measured neutron-induced SEL rates are shown in Figure 4.8.

First, the dose difference in 2W is discussed. The SEL rate dropped to 70% due to the 20% increase in impurity (Phosphorus) dose of P-well (W0 vs. W4). When both the N- and P-well doses increase by 50%, the SEL rate decreases to 40% (W0 vs. W2). The increase in the well dose lowers the gain of parasitic bipolar transistors, which contributed to SEL reduction. In addition, the gain decrease reduces the SEU rate.

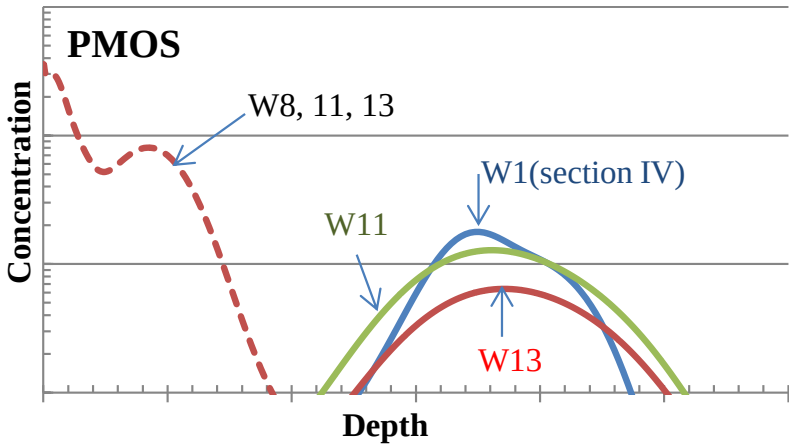


Fig. 4.9 N-well and DPW profiles of wafer of W1 , W8, W11, W13. Right mountain-like curves correspond to DPW.

On the other hand, the 4X increase in the dose did not bring further SEL reduction (W2 vs. W6). The SEL rate reduction by increasing well doping was at most 60%.

The SEL was evaluated also on DNW and DPW SRAM. Figure 4.8 shows that using DNW is more helpful for SEL prevention than the increase in well dose amount (W3 vs. W2). Two SELs were observed in the DNW SRAM (W3) while no SELs occurred in the DPW SRAM (W1) during the same irradiation time. DPW could have higher SEL prevention capability than DNW (W3 vs. W1) with 68% likelihood.

DNW decreased SEL rate, but it increased SEU rate. SEU rate of DNW SRAM (W1) increased by about 20% compared to double-well SRAM (W0). Generally, a 20% increase in SEU is not large enough to change the decision on whether ECC is required, but still an increase in SEU is an undesirable side effect for chip reliability. Reference [103] reported that DNW doubled SEU rate, and it is needed to pay a certain amount of attention to this side effect. On the other hand, DPW contributed to not only SEL prevention but also SEU reduction. Figure 4.8 shows that DPW reduced SEU rate by more than 20%. Among six well configurations in Table 4.3, DPW configuration (W1) was the best in terms of both SEL and SEU. DNW configuration (W3) attained the second lowest SEL while SEU rate increased by 20%. The next section further discusses DPW which attained the highest SEL prevention.

4.6 Prevention efficiency on deep P-well (TEST-5)

This section investigates the dependence of SEL mitigation efficiency on DPW doping profile. Neutron irradiation test was performed on CHIP-G, where test chips were manufactured with three well configurations; 2W and two DPW processes having different DPW dose profiles (W11 and W13 in Figure 4.9). The dose of W11 in DPW region is twice higher than that of W13. W1, which is included in Table 4.3, is also plotted for reference.

Figure 4.10 shows that both the DPW test chips (W11 and W13) achieved high

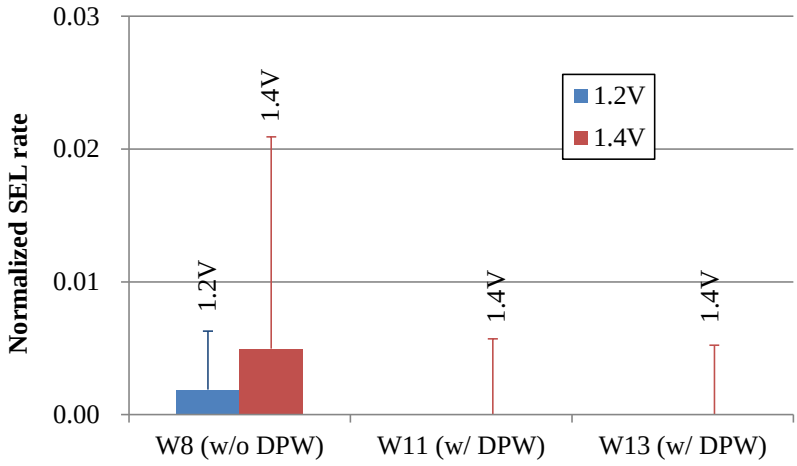


Fig. 4.10 TEST-5 result. SEL rate in W8, W11, W13 of DESIGN-G. SEL rates are normalized by SEL rate of DESIGN-C (2W) with ALL0, static test condition shown in Figure 7. Note that no SELs were observed in W11 and W13.

SEL prevention and no SELs were observed in W11 and W13, where only 1.4V test was performed for W11 and W13. Note that SEL is likely to occur at higher supply voltage, and hence the voltage of 1.4V, which is higher than nominal supply voltage, was selected for the irradiation test. The achievable SEL prevention effects of W11 and W13 were not distinguishable in this test. On the other hand, the SEL rates of W11 and W13 were less than 1 FIT/Mbit for a flux of 13 neutron/hour/cm^2 (the flux at New York) [4] at a 90 % confidence level. For achieving 1 FIT/Mbit SEL rate, the DPW doping profile did not play an important role. This observation is desirable since it makes accurate process control unnecessary in DPW process and makes it easier to apply DPW to SRAM for SEL prevention. It also should be noted that no SELs occurred in all the tests with DPW test chips (W1, W11 and W13), not only in TEST-5 but also TEST-4, -6 and -7 in our irradiation tests, where TEST-6 and -7 will be presented in Section 4.7.

Next, let us discuss how DPW contributes to SEL prevention from two aspects. The first aspect is the gain of parasitic n-p-n bipolar transistor, which consists of N-drain, P-well and N-well, and the gain decreases due to an increase in effective accepter concentration in P-well. This is consistent with a fact that higher doping in double-well also reduced SEL rate in TEST-4 (W0, W2, W4 and W6). The second aspect is the stability of well potential. DPW makes the P-well resistivity lower, which helps suppress well potential variation. To confirm this, well resistance was measured with and without DPW using a test structure to monitor the well resistor shown in Figure 4.11. The resistance between two terminals, which included the resistance of two well-contacts, was measured via wafer probing. P-well resistance with DPW was about 60% lower than that without DPW as shown in Table 4.4. On the other hand, N-well resistances with and without DPW were the same, since the volume of N-well was not changed. The reduction of P-well resistance stabilizes well potential and makes parasitic bipolar transistors less likely to be activated [142].

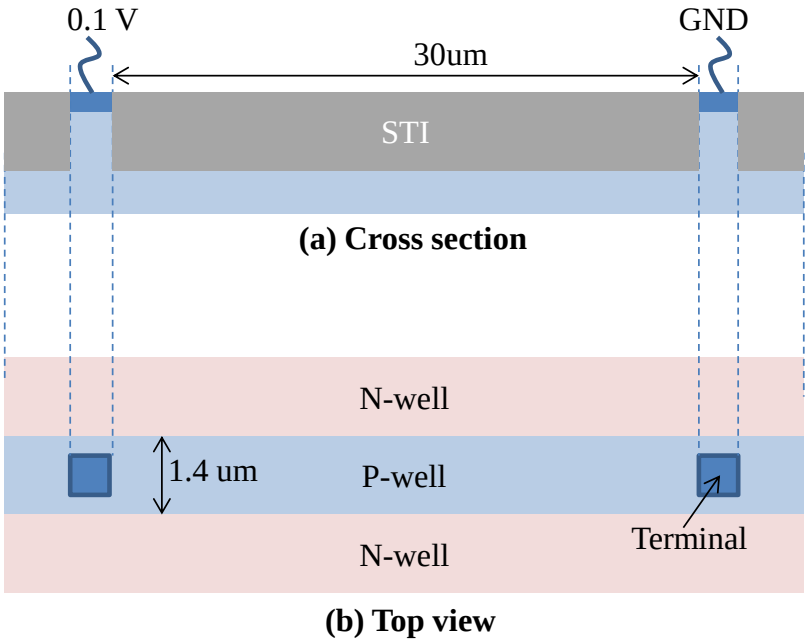


Fig. 4.11 (a) Cross section and (b) top view of P-well resistor monitor.

Table. 4.4 Normalized resistors of well with and without DPW.

	w/o DPW	w/ DPW
N-well	1.0 (normalized)	1.0
P-well	1.0 (normalized)	0.4

4.7 Discussion

The previous section presented the impact of well configurations on SEL, and showed that the following three well configurations were helpful to suppress SEL; (1) highly doped double-well structure, (2) triple-well structure with DNW and (3) triple-well structure with DPW. On the other hand, these configurations have different SEL mitigation efficiencies and different costs for adoption. These differences are discussed in this section.

Increasing well dose in ordinary double-well process reduced SEL occurrence. Although the reduction ratio was moderate (at most 60% in our experiment), this is not accompanied with SEU increase. More importantly, this can be done via process tuning, and no new manufacturing processes need to be developed or added. If the SEL reduction of up to 60% is sufficient for the products, this approach is the most suitable.

DNW attained high prevention efficiency for SEL. DNW is a popular option provided in general bulk CMOS manufacturing processes and it is easy to be applied at a cost of additional masks. However, DNW increased SEU rate. If the SEU rate increase due to DNW is acceptable or ECC is already adopted in the products, DNW

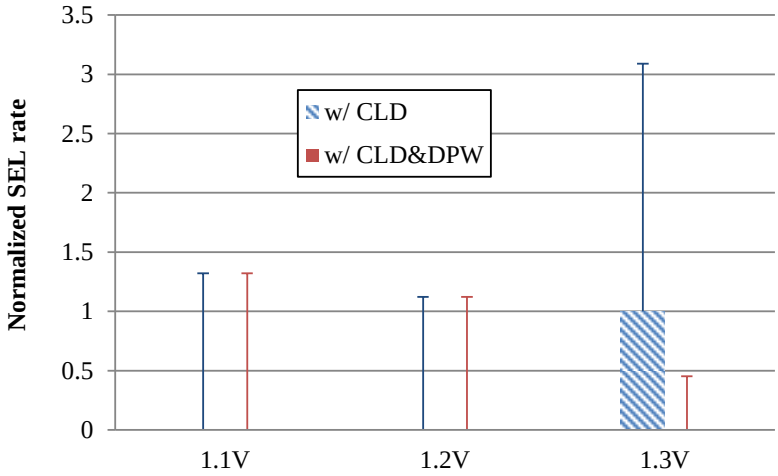


Fig. 4.12 TEST-6 result. SEL rates of DESIGN-J at room temperature (RT) and 85 degree Celsius. SEL rates are normilized by SEL rates at 1.3 V. Note that no SELs were observed with CLD and DPW, and at 1.1V and 1.2V with CLD.

is a good candidate for preventing SEL with a reasonable cost. Especially, this is attractive for fabless design companies since no special requests need to be given to a foundry.

DPW is the most effective for SEL reduction. In addition, SEU is also reduced. For the products in which the device reliability is the primary metric, DPW can be the best option. However, DPW is not a common process option provided by foundries, and hence it takes a cost to newly develop a DPW process. If this cost is cheaper than other solutions, such as circuit-level solutions, one of which will be explained in the next paragraph, DPW can be highly recommended. Here, it should be noted that the development of DPW is not technically difficult since DPW can be constructed by deep Boron ion implantation and this is often available in foundries for power MOS devices and sensor devices [148].

To clarify the advantage of DPW, the SEL prevention efficiency of CLD [80, 81] was evaluated (TEST-6 and -7). TEST-6 was performed on DESIGN-J (2W) and DESIGN-J (DPW). As a CLD, a 5 μm wide PMOS was inserted in series to each line which powered the SRAM cells in a column. The gate of the PMOS was connected to ground (GND). Figure 4.12 shows the test result. SEL was observed even with CLD in the 2W test chip while no SEL was observed in the both DPW test chips with and without CLD.

TEST-7 was performed on DESIGN-A (DPW) and DESIGN-K (2W and DPW). DESIGN-A and DESIGN-K had the same SRAM macros, and only the difference is that CLD was inserted in DESIGN-K. In the test chip without DPW, SEL was observed even with CLD as shown in Figure 4.13, whereas no SEL was observed in the DPW test chips. Note that the SEL rates of the vertical axis in Figure 4.13 are normalized by that of DESIGN-A (2W), which is the SRAM without CLD in ordinary double-well shown in Figure 4.5. This means that the CLD was also helpful for SEL prevention and suppressed by more than 99% SEL. On the other hand, the

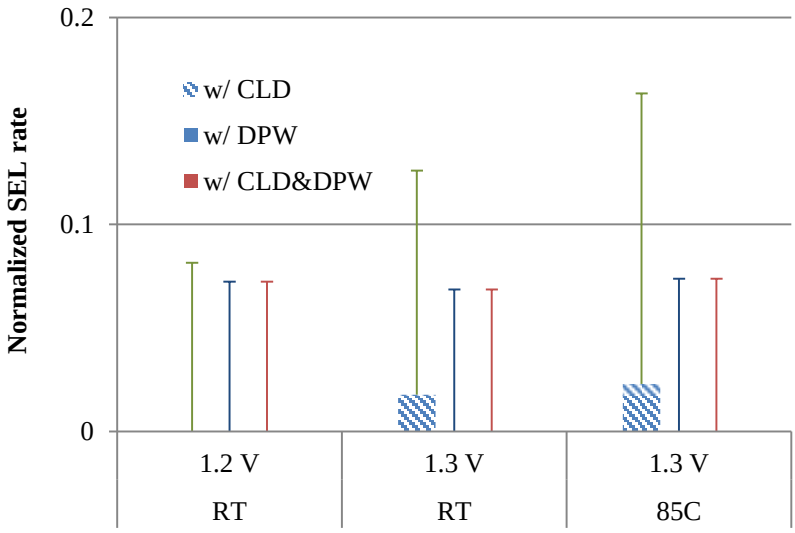


Fig. 4.13 TEST-7 results. SEL rates of DESIGN-A and DESIGN-K at room temperature (RT) and 85 degree Celsius. SEL rates are normalized by SEL rate of DESIGN-A (2W) with ALL0, static test condition. Note that no SELs were observed with CLD at 1.2V and with DPW and with CLD and DPW.

SEL prevention by DPW can be expected to be similar or might be better than that of CLD while the number of observed SELs in this experiment was limited and a significance difference was not observed.

Finally, the performance penalty due to DPW was discussed. One might think that DPW could change the SRAM performances or could increase manufacturing variation by an increase in the number of dopants in the p-substrate since random dopant fluctuation is one of the major sources of manufacturing variation. However, DPW changed the doping profile at a deep region and the doping profile near MOS devices was unchanged as shown in Figure 4.9. The number of dopants in the channel region is the source of manufacturing variation, and the number of dopants in such a deep well is not influential to manufacturing variation. Consequently, the DPW profile (Figure 4.9) should keep MOS performance and variation unchanged. To clarify this, chip level yields were compared in the chips with and without DPW.

Figure 4.14 shows chip level yields evaluated by wafer level tests at 85 and 40 degree Celsius. In the tests, arbitrary data was written into SRAM, and 20 ms later all the data were read and checked. This test procedure was repeated at various supply voltages. To evaluate the SRAM yield, 64 dies on a wafer were tested. If there were some performance differences between SRAMs with and without DPW, such as in read and write access time and drive current balance between PMOS and NMOS, the yield would change. On the other hand, no difference was found in the yield evaluation results shown in Figure 4.14. This result indicates that DPW neither change the performances nor increase manufacturing variation.

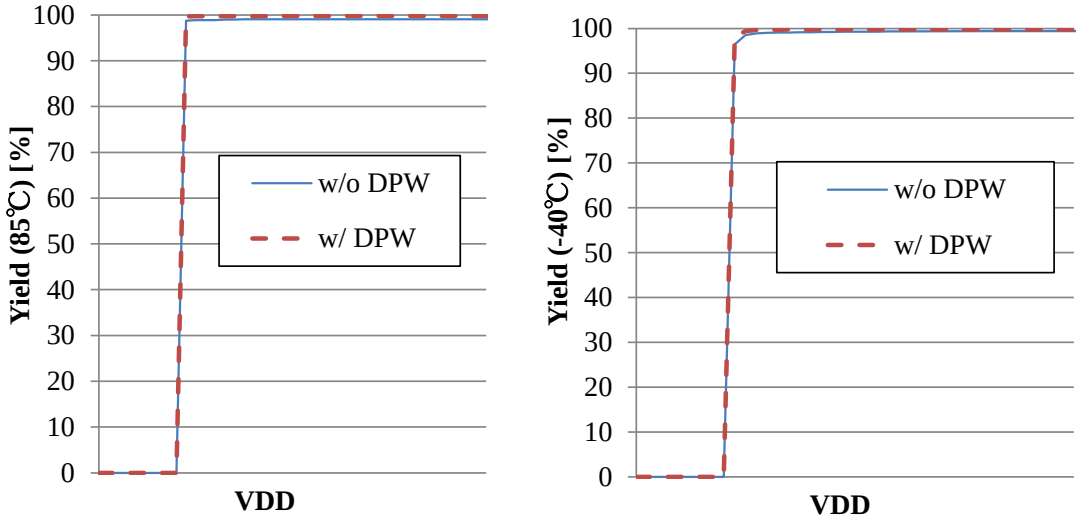


Fig. 4.14 Chip level yields measured by wafer level test in 85 and 40 degree Celsius.

4.8 Conclusion

This chapter experimentally demonstrated through neutron irradiation tests that altering well configuration could improve SEL immunity, and revealed that DPW, DNW and highly doped well reduced SEL rate. These three configurations for SEL prevention have different features. Increasing dose in double-well can mitigate SEL without SEU increase, and at most 60% SEL reduction could be obtained via process tuning. DPW is the most effective solution to eliminate SEL occurrence, and no SEL was observed in our irradiation tests. Furthermore DPW is helpful to reduce SEU as well. While adoption of DPW needs an extra cost to newly construct a DPW process, the DPW process development itself is not technically difficult. The SEL prevention by DPW can be expected to be similar or might be better than that of CLD. An advantage to select DNW for SEL prevention is that DNW is a common process option and can be easily adopted at a cost of additional masks. However, it is needed to pay attention to a fact that DNW increases SEU rate.

Chapter 5

MBU mitigation with well-slits in sequential element

This chapter discusses MBU mitigation by well-slit in sequential elements such as FF and latch. As mentioned in Section 1.3, algorithm checking can detect SBU of sequential elements in ALU. However, multi-bit latch (MBL) is used in the ALU, and MBU cannot be detected by the algorithmic checking. This chapter proposes a technique that mitigates MBU in MBL without performance degradation by applying well-slits [149]. The MBLs with and without well-slit are designed in a test chip, and neutron irradiation test was performed on the test chip. This chapter explains the design of the mitigation technique, and shows test results for clarifying the mitigation efficiency. While 25 errors were observed in the MBL without well-slits, no error was observed in the MBL with well-slits.

5.1 Introduction

As discussed in the previous chapters, SEU in SRAM is often mitigated by ECC in electronic devices for reliability-demanding applications and large-scale applications. On the other hand, in logic circuits, it is generally difficult to apply ECC. Instead, triple modular redundancy (TMR) or double modular redundancy (DMR) is used for mitigating or detecting soft error in logic circuits. These redundant techniques involve large area overhead, and it often exceeds 2×. For mitigating soft error induced failures with low area overhead, hard instruction retry (HIR) with checker and predictor is used for logic circuits in processors [110].

For enabling HIR, checker bits and related circuit components (checker, predictor and comparator) are added to detect errors as illustrated in Figure 5.1. The checker calculates a checker symbol from the output of a unit (e.g. data path and multiplier), and the calculated checker symbol is stored in the checker bits. The predictor predicts the check symbol from the unit input, and the comparator compares the calculated and predicted check symbols. Parity and residue checks are often used for data transmission lines and multipliers, respectively. Once the comparator detects inconsistency, an error flag signal is generated and the running instruction is stopped and retried by HIR. An advantage of HIR is that an error can be detected with simple

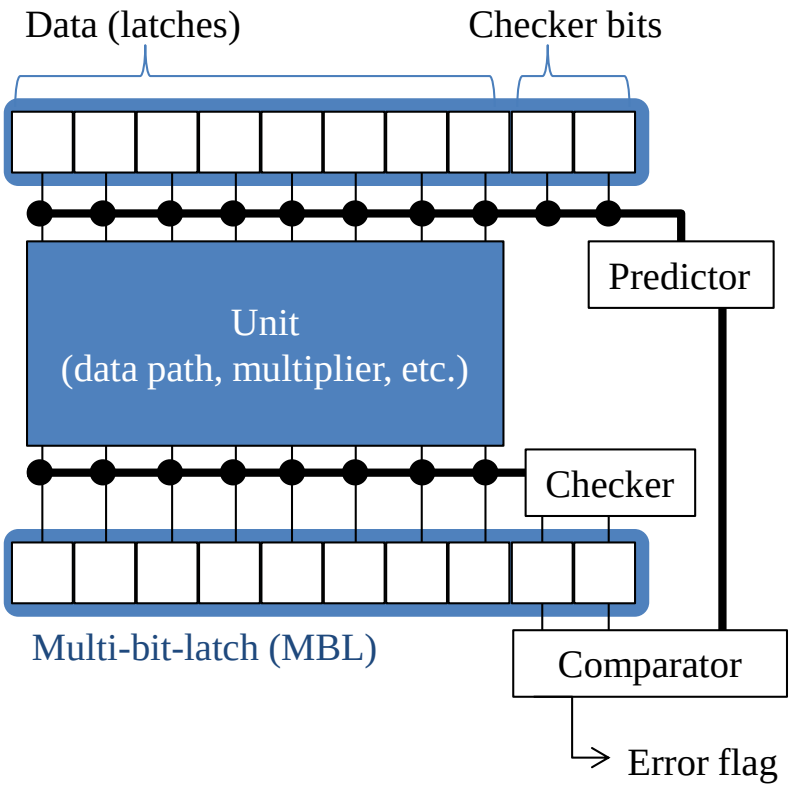


Fig. 5.1 Circuits necessary for HIR.

additional circuits, while other techniques such as TMR often require large overhead. HIR is very effective for mitigating the impact of SEU in sequential elements on the processor operation. In addition, this technique can partially mitigate SET in combinational circuits. Thus, HIR can be applied to reliability-demanding processors with low overheads in area, performance and power consumption.

MBL, which consists of multiple latches, is used for storing a code word including data bits and checker bits. The circuit structure is shown in Figure 5.2. The latches in an MBL share a clock buffer for saving area and power consumption and reducing clock-skew [110]. The predictor and checker in HIR can detect SBU in the MBL. However, these may miss MCU, which is multiple upsets caused by a single neutron strike ranging over one or more MBLs. Similar to SRAM, an MCU that cannot be corrected by HIR in MBL is called MBU in this thesis.

As explained in Section 1.2.2, there are four possible MCU mechanisms, (A) successive hits by one ion, (B) multi hits by multiple ions, (C) charge drift/diffusion and (D) PBA, as shown in Table 1.4. As discussed in Section 3.1, MCU increases with technology scaling, i.e. transistor size shrinking, because of a decrease in distance between bits [34], and hence MCU in MBL is becoming a critical concern for sustaining processor reliability. Furuta et al. [35] reported that in 65 nm FFs, 97% of MCUs occurred in the latches sharing the same P-well, and this suggests that the main reasons of MCU in 65 nm technology are (C) and (D). The MBUs due to (C) and (D) occur in the same well, and hence splitting well areas for each latch is expected to decrease

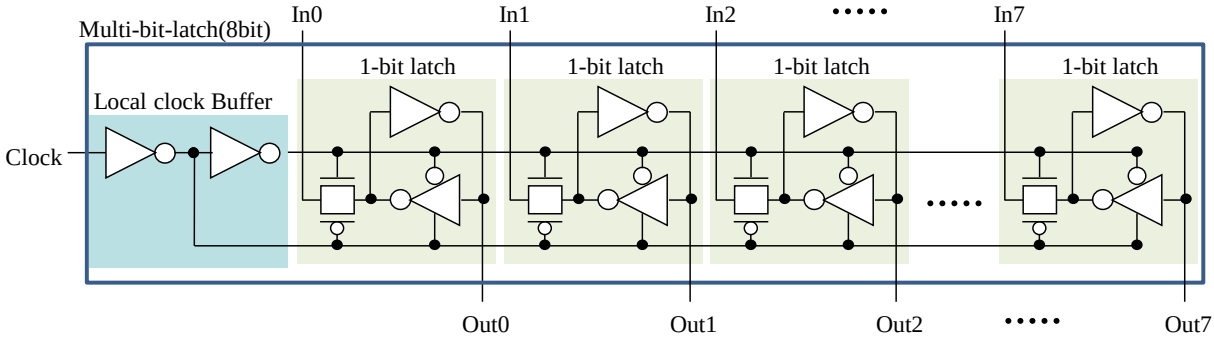


Fig. 5.2 MBL with clock buffer (8-bit).

MBUs that originate from (C) and (D). However, the latches of conventional MBL share a well. Therefore, the conventional MBL has higher MBU rate than SRAM because SRAM adopts interleaving [123]. Meanwhile, a latch-up prevention technique that uses well separation is proposed in [150, 151], while this technique needs a special process option of deep trench (DT) and hence the applicability is limited.

This chapter proposes an MBU mitigation technique for MBL using well-slits. The inserted well-slits isolate wells of each latch for preventing charge diffusion and PBA. This well-slit technique can be applied to any bulk CMOS technologies without process customization, and the MBU mitigation can be achieved only by design modification and consequently with low cost. The area overhead was evaluated in the proposed technique by designing an MBL macro including the predictor, checker and comparator for processors in 28 nm technology. The effectiveness of the proposed mitigation technique is validated through neutron irradiation tests on 28 nm DUTs.

The rest of this chapter is organized as follows. Section 5.2 presents the proposed mitigation technique with well-slits and its overheads. The accelerated test setup is explained in Section 5.3, and Section 5.4 shows test results. Section 5.5 concludes with a brief summary.

5.2 Proposed mitigation technique with well-slit

Figure 5.3 illustrates the proposed MBU mitigation technique that inserts well-slits into MBL. There are two types of well-slits; P-well-slits and N-well-slits. N-well-slits split P-well area and P-well-slits partition N-well area. The well-slits can mitigate MBUs which are caused by PBA and charge diffusion. The well potential fluctuation due to PBA is confined within a well area, resulting in fewer MBUs. The well splitting also prevents electrons and holes from diffusing to adjacent bits.

For preventing latch-ups, Vodman et al. [151] isolated a well from its neighboring wells by deep trenches, which are not included in standard bulk CMOS processes, and the movement of electrons and holes across wells was prevented by the insulator. On the other hand, the proposed technique restricts the drift and diffusion of electrons and holes within a well with reversely-biased PN junctions, and it can be used in any standard bulk CMOS processes. In either case, the charge sharing and well potential fluctuation are confined within the isolated well while their process availabilities are

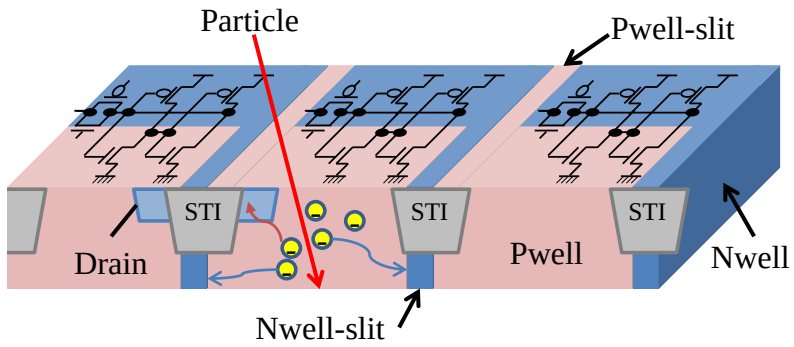


Fig. 5.3 Proposed MBU mitigation technique using well-slit for MBL.

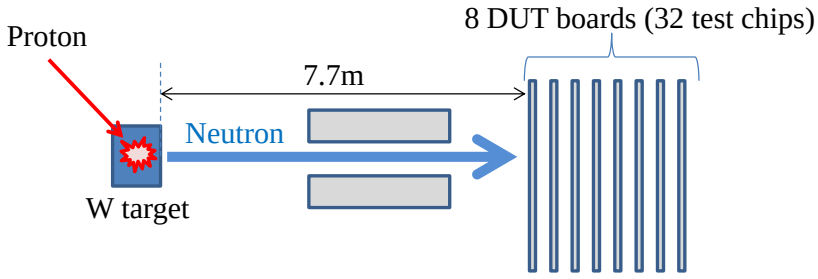


Fig. 5.4 Neutron test configuration at RCNP. This shows only the target, collimator and DUT boards. The other parts are same with other tests shown in Figure 1.15.

different.

An MBL was designed with the proposed MBU mitigation technique in 28 nm technology. The width and length of well-slit are 0.22 μm and 1.52 μm in the MBL with the proposed MBU mitigation technique. As an MBL macro including a clock buffer and a checker, this mitigation technique was implemented with only 5.4% area overhead in an MBL macro for SPARC processors [115, 116].

5.3 Irradiation test setup

A neutron irradiation test was performed on MBLs for evaluating the efficiency of the proposed MBU mitigation technique. The neutron irradiation test was conducted with spallation (white) neutron beam in RCNP at Osaka University. The average flux of neutrons whose energy is higher than 10 MeV is 2.01 billion neutron/hour/cm^2. Eight test boards were irradiated simultaneously as shown in Figure 5.4. The test board has four DUTs and thirty-two DUTs were irradiated simultaneously. The DUT includes latch arrays consisting of latches manufactured with double-well (i.e. without deep N-well) process in 28 nm bulk CMOS technology. The distance between the tungsten target and the first board is 7.7 meter as shown in Figure 5.4. Total irradiation (beam) time is sixty hours, which corresponds to about 1.2 million years in real time. This test aims to measure upset counts during hold operation.

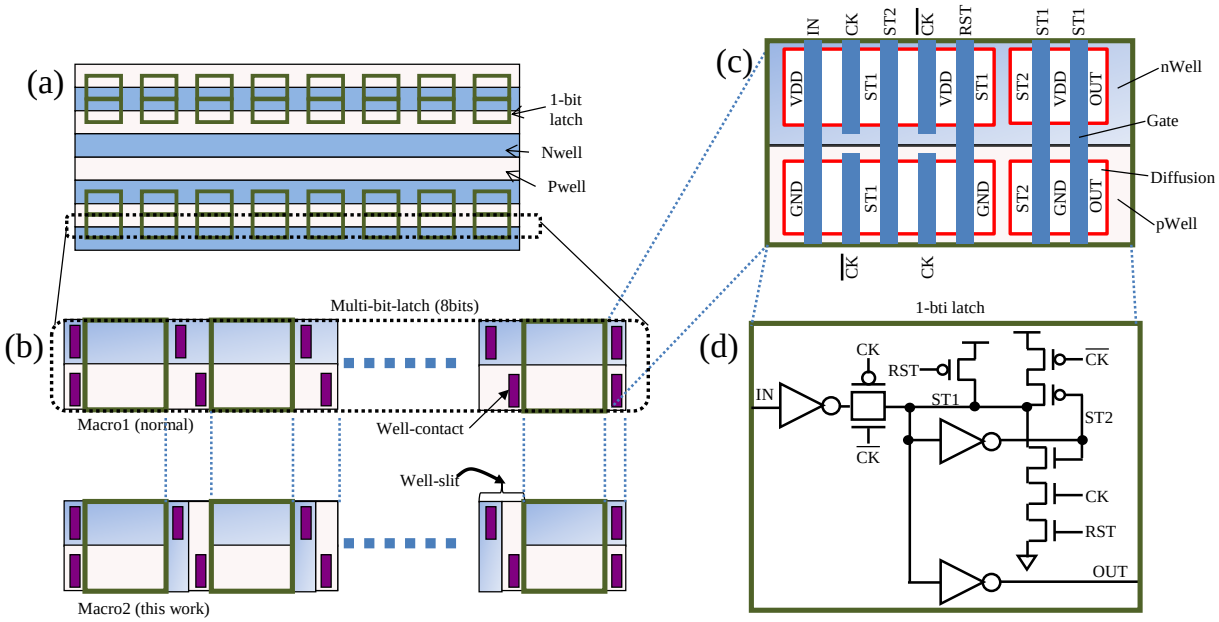


Fig. 5.5 (a) MBL macro placement on the DUT, (a) layout of 8-bit MBL of two madros on DUT, (b) latch layout and (c) schematic of 1-bit latch.

The chip includes two types of MBLs; Macro1 and Macro2 as illustrated in Figure 5.5, and each macro contains about 50k bits. Macro1 is a normal MBL and Macro2 is the MBL to which the proposed mitigation technique is applied. Each MBL consists of eight-bit latches and one clock buffer as shown in Figure 5.2. In Macro2, there are well-slits consisting of N-well and P-well between bit cells as explained in Section 5.2. The spaces between latches inside Macro1 and Macro2 are the same, and for every space well-contacts are placed both in Macro1 and Macro2. Different from conventional MBL, Macro1 is designed having the same spaces and well-contacts between latches so that the impact of well-slit is solely evaluated. For this reason, MBL sizes of Macro1 (normal) and Macro2 (this work) are the same in this DUT. Figure 5.5 (a) illustrates how the MBLs are laid out in the DUT. In this figure, four MBLs are placed, and each of two MBLs shares the well with double-back layout style. For example, the upper two MBLs share the N-well, and the lower MBLs share the P-well. These two MBLs that share the same well are called paired MBLs in the following. Note that this placement is done for the same MBL macro, and Macro1 and Macro2 are not mixedly placed.

MCU was evaluated in two cases that the same and different data were stored in neighboring bits in an MBL, since MCU occurrence depends on test patterns and corresponding positions of sensitive areas [152]. Figure 5.6 (a) and (b) show the node values, and Figure 5.7 (a) and (b) illustrate the sensitive areas when the retention data is “0” and “1”, respectively. During hold operation, the input value of each latch is the same with the stored value through a feedback loop, which will be explained later. The test patterns selected for this evaluation are X-stripe and Y-stripe shown in Figure 5.8. These test patterns include {0, 0}, {0, 1} and {1, 1} neighboring bits, and hence MCU occurrence can be observed against these neighboring bits.

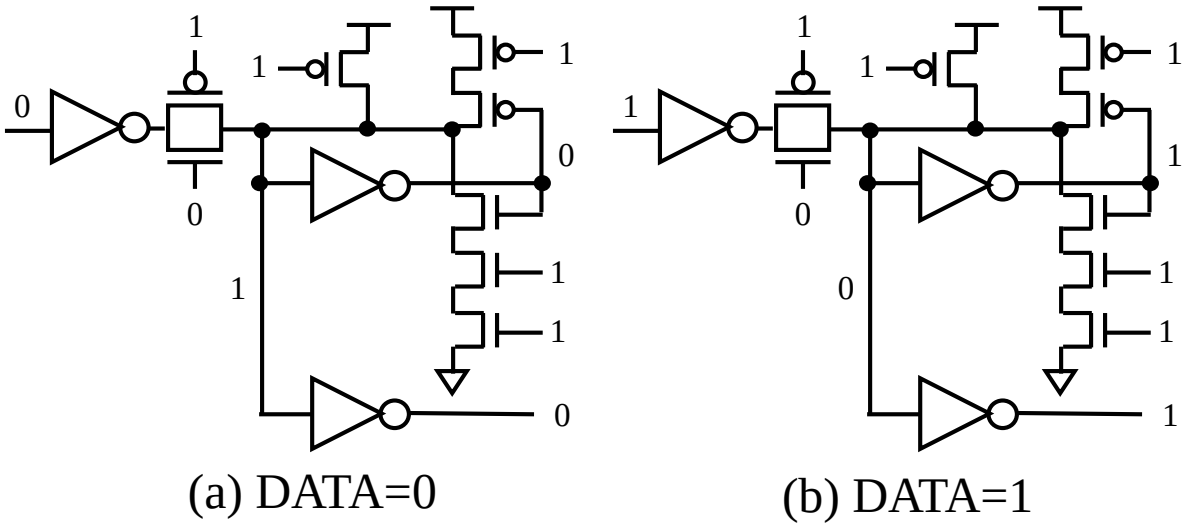


Fig. 5.6 Node values when retention data is (a) 0 and (b) 1. The input data of the latches are the same with the written data during hold operation.

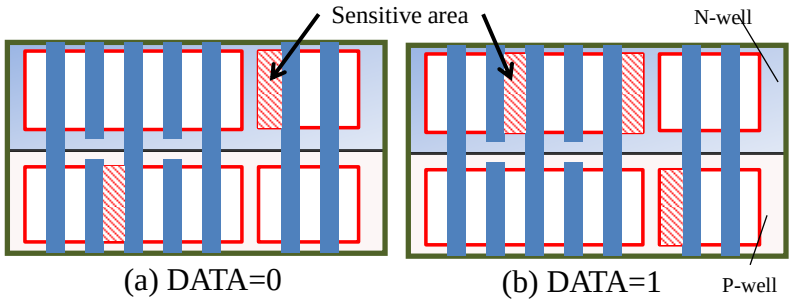


Fig. 5.7 Sensitive area when retention data is (a) 0 and (b) 1.

Figure 5.9 shows the circuit structure in the DUT for enabling tests with X-stripe and Y-stripe patterns. With the column decoder in this control logic, different values can be given to latches in an MBL although a clock buffer controls all the latches in the MBL simultaneously. A latch selected by the column decoder captures 0/1 from DataIn line, and the other latches not selected by the column decoder are overwritten with the current values. By these steps, arbitrary data patterns can be written into the MBL. In addition, in this structure, SET at a local clock buffer arising during the hold operation does not contribute to data upset in the MBL since only overwriting is performed [153].

Figure 5.10 shows the timing chart of the test procedure. In write phase, the data pattern was set to X-stripe or Y-stripe pattern in the MBLs with 10MHz clock signal. Then, the MBLs were kept in hold operation for 15 minutes, and the stored values were read out. The supply voltage was 0.75 V in read/write phases and 0.85 V in hold phase. The hold duration is over 1000 times longer than the read/write durations, and the measured upset counts can be regarded as the upset counts during the hold

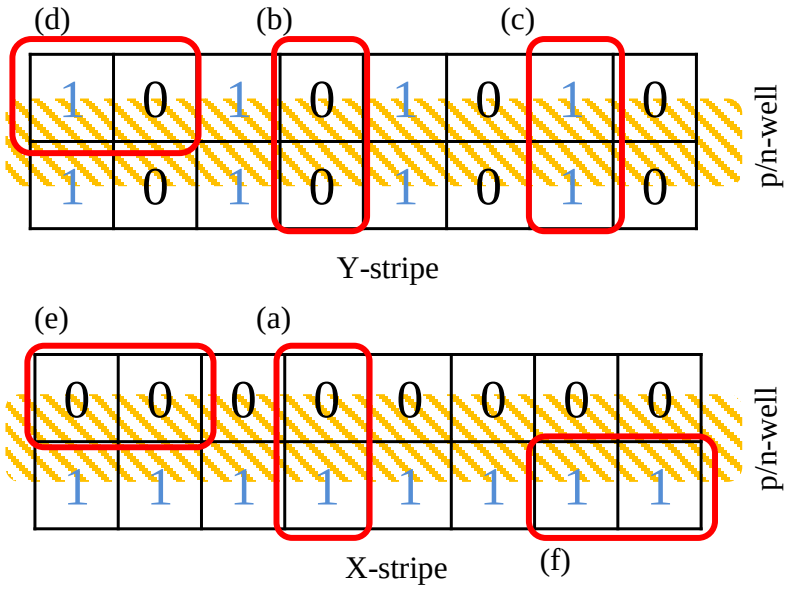


Fig. 5.8 Test patterns of X-stripe and Y-stripe.

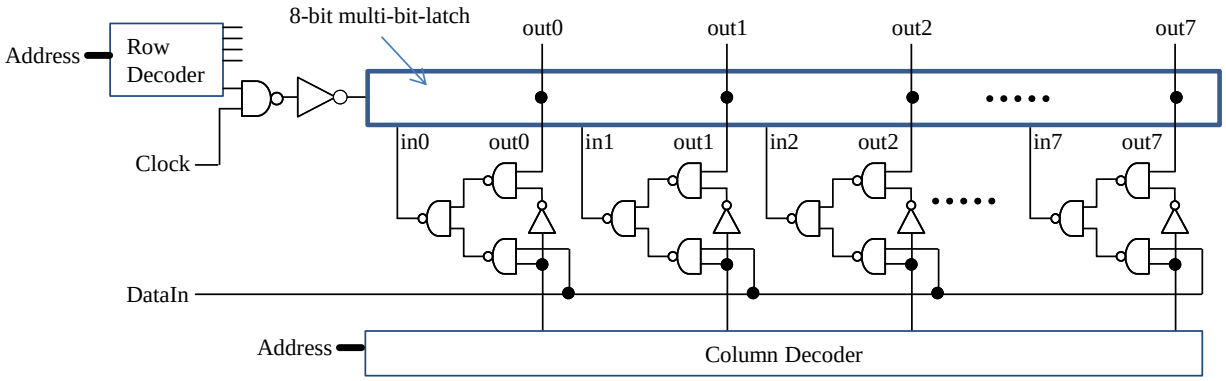


Fig. 5.9 Control logic for 8-bit MBL in the DUT.

operation.

5.4 Experimental results

Table 5.1 lists the error-bit counts of SBU, MCU and MBU. The error-bit counts for DATA0 and DATA1 latches are separately shown, where DATA0/DATA1 latch means a latch whose retention data is "0" / "1" . The proposed MBU mitigation technique does not increase SBU rate as shown in Table 5.1. An increase in SBU rate leads to frequent instruction retries in HIR and consequent performance degradation. This result demonstrates that the proposed mitigation technique does not involve performance overhead.

Twenty-seven MCU events were observed in total in Macro1 (normal) in this irra-

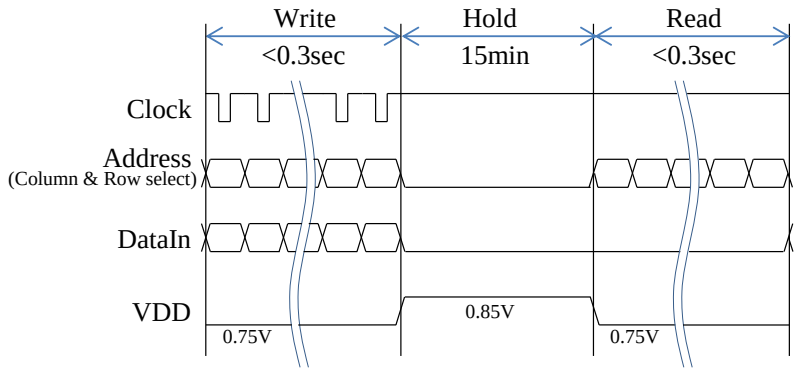


Fig. 5.10 Test timing chart for the 28 nm latch array DUT.

Table. 5.1 SBU, MCU and MBU error-bit counts.

	DATA0	DATA1
SBU in Macro1	676	727
SBU in Macro2	721	655
MCU in Macro1	4	92
MCU in Macro2	0	6
MBU in Macro1	2	86
MBU in Macro2	0	0

diation test. Table 5.1 shows the number of bits flipped in total in the twenty-seven MCU events. There is MCU count difference between DATA0 and DATA1, whereas SBU counts are not much different between DATA0 and 1 as shown in Table 5.1.

A primary factor of soft error in latches is charge collection to NMOS in DATA0 and to PMOS in DATA1 because the latch circuits consist of unbalanced feedback loop circuits [154, 155]. These test results show that PMOS and NMOS equally contribute SBU rate, while PMOS contributes to MCU rate more than NMOS in MBL. A possible reason is that single event upset reversal (SEUR) in NMOS decreased MCU. It is reported that SEUR is more influential in NMOS than in PMOS [105, 156, 103].

Next, MCUs upsetting adjacent two latches are discussed. The number of MCUs is counted separately depending on the stored values ({0, 0}, {0, 1} and {1, 1}) and their spatial direction. Table 5.2 shows the MCU counts, where the spatial pattern classification was performed for the paired the 8 bit-MBLs (Figure 5.5 (a)). Only five MCUs were observed in adjacent two latches, while twenty-seven MCUs were observed in total. The MCU count is quite few, and unfortunately the pattern dependency cannot be discussed further. However, it should be noted here that vertical MCU patterns of (a), (b) and (c) are not MBU and do not result in failures of the processor with HIR, since each MBL includes only a single error. In this case, the error is detected by the checker and predictor, and the processor with HIR can retry the instruction.

The proposed MBU mitigation technique with well-slits perfectly reduced MBU in the MBL. The neutron irradiation test results of Figure 5.11 and Table 5.1 show that no MBU was observed in Macro2, whereas 25 MBU events and consequent 88 bit-

Table. 5.2 MCU counts (events) when stored value in neighboring bits are {0, 0}, {0, 1} and {1, 1} on vertical and horizontal sides.

	Pattern	MCU count on Macro 1	MCU count on Macro 2
Vertical	(a) (b) (c) 0 0 1 1 0 1	1	3
Horizontal	(d) 1 0 (e) 0 0 (f) 1 1	1	0

errors occurred in Macro1 (normal). Here, MCU spatial patterns resulting in MBU depend on the predictor and checker implementation. The residue check whose divisor is three or seven are widely used for the predictor and checker implementation. The parity checking can detect an even number of errors, but cannot detect an uneven number of errors in the MBL. Consequently, when the parity checking is used, 8-HORIZON, 2- HORIZON, 2-STRIPE and 4- STRIPE shown in Figure 5.11 are MBUs, and HIR is not invoked. The residue checking can detect one error, but cannot always detect two or more errors. Accordingly, in case of the residue checking, 3- STRIPE can be MBU and may not invoke HIR. The irradiation results in Figure 5.11 clearly demonstrate that the MBL with the proposed mitigation technique mitigates MBU and contributes to reliability enhancement of electron devices. The error rate of MBL with the mitigation technique is less than 2.3 FIT/Mbit for 13 neutron/hour/cm^2 (sea level in New York) with 90 % statistically confidential level.

5.5 Conclusion

This chapter proposed a technique for mitigating MBU in MBL by inserting well-slits between latch bit cells. The area overhead is only 5.4% as an MBL macro for processors including clock buffer and checker. Neutron irradiation tests clarified that the proposed mitigation technique did not change SBU rate and consequently did not degrade processor performance. It is clearly demonstrated that the proposed mitigation technique can achieve robustness against MBUs, which cannot be detected by the checker and predictor, have not been observed in the proposed MBL even under sixty-hour accelerated irradiation. The MBL with the proposed mitigation technique helps attain excellent reliability of electronic devices.

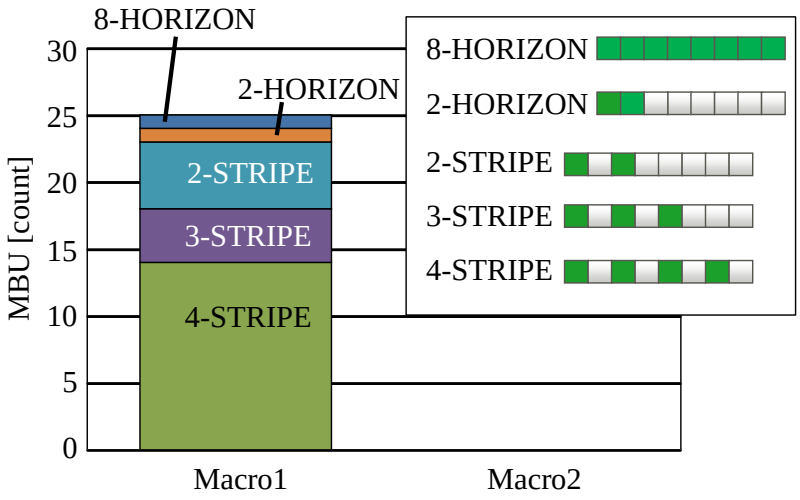


Fig. 5.11 MBU counts in neutron irradiation test on macro1 (normal) and macro2 (with well-slit) of 28 nm latches.

Chapter 6

SBU mitigation in sequential element

This chapter proposes a soft error immune latch called SEILA. SEILA is developed aiming at SBU mitigation in sequential elements. As explained in Section 1.3, ECC or the algorithmic checking cannot be applied to control logic, and hence not only MBU but also SBU must be mitigated for achieving high reliability in microprocessors. SEILAs are designed with 65 nm, 28 nm and 20 nm technologies, and are tested with neutron and alpha irradiations. This chapter describes the structure and SBU mitigation mechanism of SEILA, and shows the irradiation test results.

6.1 Introduction

SEU in sequential elements is critical issues more than in SRAM because it is difficult to apply ECC to the sequential elements in logic circuits. HIR can eliminate SEU in sequential element by retrying the instruction execution after the SEU detection. However, HIR cannot be applied to all logic blocks. Motivated by this, redundancy-based radiation-hard latches having more than two storage nodes are developed for mitigating SEU in sequential elements [157, 158, 77, 159, 160, 161, 78, 79]. The data stored in these latches cannot be corrupted by the charge collection to a single node in those latches. They, however, can be corrupted when the generated charge is collected to multi nodes. There are four possible mechanisms of charge collection to multiple nodes (CCM) as shown in Table 1.4 [34].

Richly placed well contacts can mitigate CCM by attenuating PBA [162, 163]. However, it involves large area overhead. On the other hand, well-tap(tie)-less cell design is now mainstream because larger transistors can be accommodated in short-height cells. The well-tap-less design means no well-contacts in sequential element cells, and it leads to higher CCM. In addition, transistor miniaturization intensifies CCM because the distances between critical nodes become shorter as the transistor size shrinks. Such elevating CCM is degrading the SEU mitigation efficiency of the redundancy-based latches in fine-pitch bulk CMOS technology.

Another data corruption mechanism in the redundancy-based latches is SET occurring at local clock (SETLC). The latch operation is triggered by the clock signal distributed by a clock tree. When SET occurs on a clock buffer in the clock tree, the buffer sends out a hazard signal to the latches. This makes the latches capture the data at an unexpected timing, and an unexpected bit flip may occurs. Besides,

logic cells consisting of small transistors are sensitive to SET [90]. In the clock tree, the final-stage clock buffer, which is included within a latch cell, is relatively small compared to the upstream clock buffers. Therefore, such a clock buffer included in a latch cell is the most vulnerable part in term of SET induced data corruption. However, the conventional radiation-hard latches are not designed to mitigate SETLC. It is reported that the contribution of SETLC increases as technology advances [164]. It is needed to mitigate SETLC in sequential elements for high reliability processors.

This chapter proposes a soft error immune latch named SEILA that reduces SEU due to both CCM and SETLC. For suppressing CCM, SEILA devises and introduces a design guideline on the placement of paired critical transistors and cancelling transistor. SEILA is designed as a multiple height cell to satisfy this design guideline. This multiple-height SEILA cells are compatible with existing standard cell libraries used for commercial products. For mitigating SETLC in SEILA, redundant clock buffers are introduced. Even if a hazard occurs on a clock buffer, the stored data is unchanged. The mitigation efficiency of SEU and SETLC in SEILA is evaluated through irradiation tests.

The rest of this chapter is organized as follows: Section 6.2 explains the experiment procedure for evaluating the efficiency of SEILA. Section 6.3 explains CCM and SETLC mitigation techniques adopted in SEILA. Section 6.4 presents irradiation test results and demonstrates the SBU mitigation efficiency of SEILA. Finally, Section 6.5 concludes this chapter.

6.2 Test procedure

SEU and SETLC in latches were evaluated through neutron and alpha irradiation tests. The neutron test was carried out with the spallation neutron beam at RCNP. The alpha test was performed with an ^{241}Am alpha source in a vacuum chamber. Table 6.1 summarize the latches evaluated in these tests. SEU and SETLC were evaluated with following test conditions:

TEST1: Clock signal (CK1 in Figure 6.1) is kept low after the data is written to the latch. The transmission gate (TM3 in Figure 6.1) between the data retention node and the input terminal of the latch is off-state. The data at Din is kept the same as the retention data during the irradiation. Even when the gate is erroneously opened, the data in the latch is not corrupted. Only SEU at the retention data nodes is observed after irradiation in TEST1.

TEST2: The transmission gate is kept off, and the data at Din is opposite to the retention data in the latch during the neutron irradiation. When the gate is erroneously opened, the data in the latch is corrupted. Upsets both by SEU at the retention data nodes and SETLC are observed after the irradiation in TEST2.

SETLC rate can be evaluated from the difference between upset rates of TEST1 and TEST2.

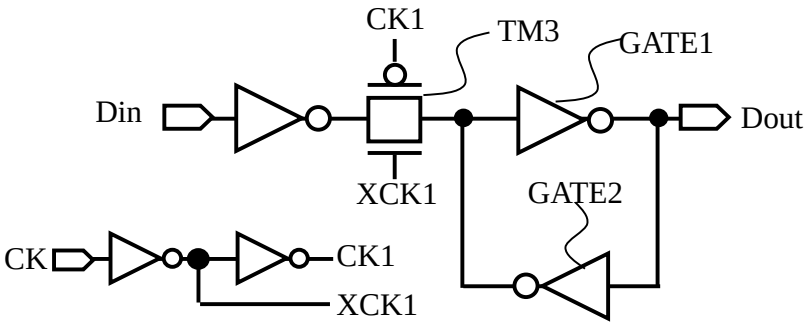


Fig. 6.1 Schematic of normal non-robust latch.

Table. 6.1 List of tested latches.

Name	Technology	Type	Cell height
65 nm SHC-normal latch	65 nm	non-robust	Single
65 nm SHC-DICE	65 nm	DICE type	Single
65 nm DHC-SEILA	65 nm	SEILA	Double
65 nm DHC-SEILA2	65 nm	SEILA	Double
45 nm SHC-normal latch	45 nm	non-robust	Single
28 nm DHC-SEILA	28 nm	SEILA	Double
20 nm THC-SEILA	20 nm	SEILA w/ well-contacts	Triple
20 nm THC-SEILA	20 nm	SEILA w/o well-contacts	Triple

6.3 SEILA

Figure 6.2 shows the schematic of SEILA. SEILA employs dual inter-lock cell (DICE) type circuit for storage in which a voltage variation on one node cannot corrupt storage data [77]. The storage structure, however, cannot protect the retention data from SEU by CCM and SETLC. To overcome these problems, SEILA in the circuit storage, SEILA includes two implementation techniques for enhancing the mitigation efficiency; multi height cell (MHC) and dual clock buffer (DCB). MHC technique, which enables layout optimization, is introduced for suppressing CCM. DCB is applied for mitigating SETLC. This section explains these techniques.

6.3.1 Review of conventional normal and radiation-hard latches

Figure 6.3 and Figure 6.4 show SEU and SETLC rates measured in 65 nm and 45 nm-latches, where these latches are ordinary single height cells (SHC). The error bars in these figures show statistical error variations at 95% confidence level. The SEU and SETLC rates in Figure 6.3, Figure 6.4 and Figure 6.5 are plotted with the same scale. Here, the SEU and SETLC rates are evaluated in two cases; (1) the stored data is one (DATA1) and (2) the stored data is zero (DATA0). The SETLC rate is 10% to 15% of the SEU rate in the 65 nm normal latch. Although, the contribution of SETLC is not so large in the 65 nm latches, it is not negligible in the 45 nm latches

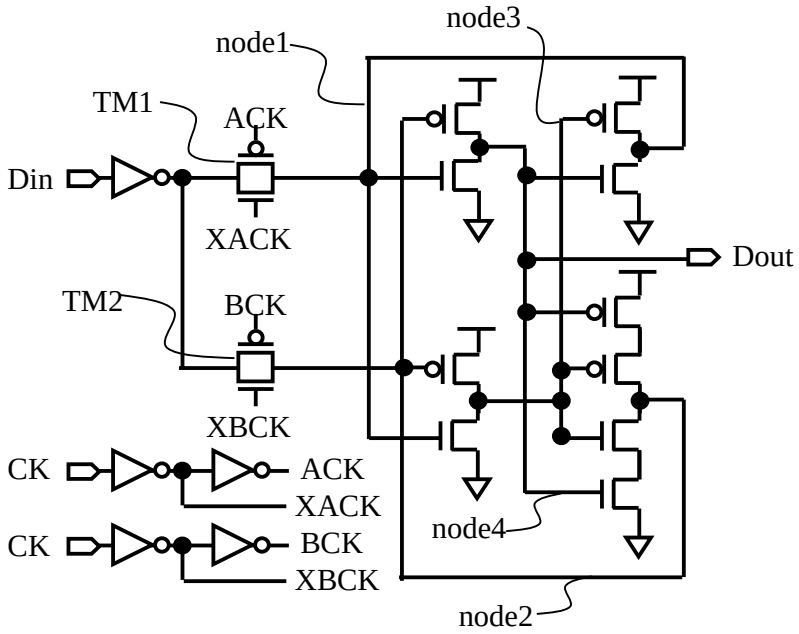


Fig. 6.2 SEILA schematic.

as shown in Figure 6.4. In 45 nm, the SETLC rate is comparable with the SEU rate. Note that the SEU rates are generally different depending on the stored value because PMOS and NMOS have the different charge collection efficiency [165]. In this experiment, the SEU rate difference between DATA0 and DATA1 in the 45 nm normal latch is larger than that in the 65 nm normal latch. A possible reason is that the beta ratio (size ratio of PMOS to NMOS) is much different between the 65 nm and 45 nm latches [120].

The SEU rate decreases as the operation voltage increases because the Qcrit increases. On the other hand, the SETLC rate does not so increased. A possible reason is that increasing operation voltage generally shortens the delay time of input buffer and transfer gate (TM3 in Figure 6.1) and necessary SETLC pulse width for data upset decreases.

Next, the SEU and SETLC rates were evaluated in a conventional radiation-hard latch, where this conventional latch is an DICE type latch which is laid out as a SHC. The circuit structure for data retention is the same with SEILA. The difference in the circuit structure is that the SHC-DICE includes a single local-clock buffer that drives two transmission gates (TM1 and TM2 in Figure 6.2). Figure 6.5 shows the SEU and SETLC rates in the 65 nm SHC-DICE. The SETLC rate in the 65 nm SHC-DICE is comparable to that in the 65 nm SHC-normal latches while the SEU rate of the SHC-DICE decreases. The SHC-DICE can mitigate SEU at the retention data node, but it cannot mitigate SETLC. The contribution of SETLC is no longer negligible in the SHC-DICE. This is the motivation to introduce dual clock buffer, which will be explained in the next subsection.

Another important observation is that even the DICE structure cannot eliminate SEU. The SEU rate reduction is only 90% while the area overhead is 105% compared

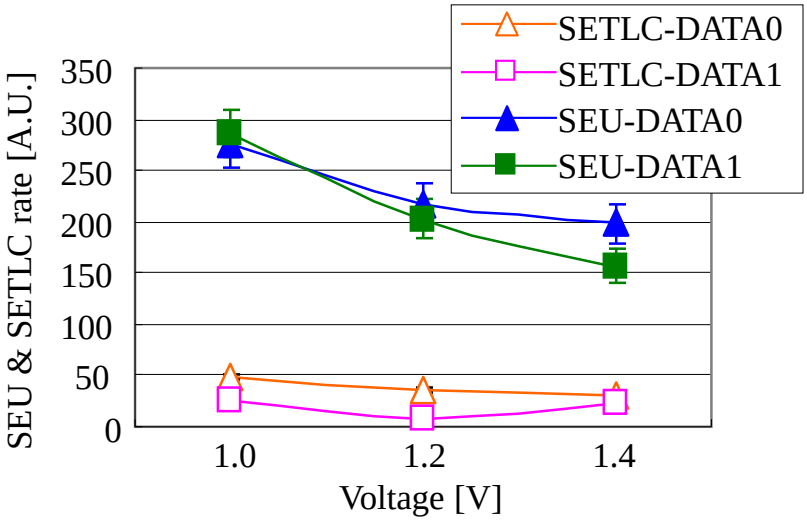


Fig. 6.3 SEU and SETLC rates in case that retention data of all latches are 0 or 1 on 65 nm SHC-normal latch. The error bars show statistical error variations at 95% confidence level.

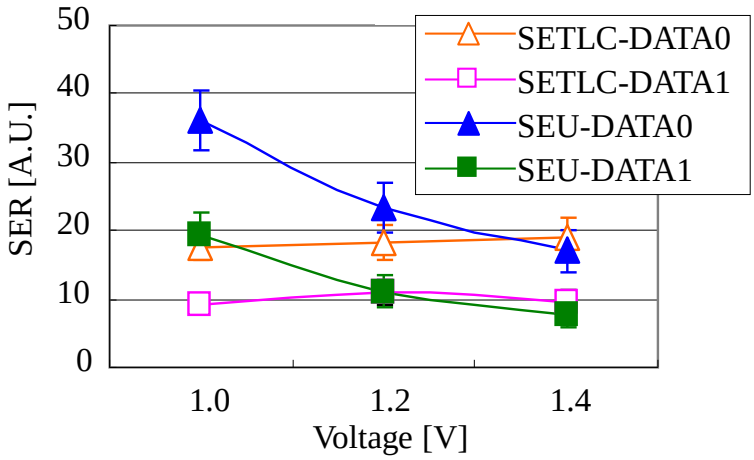


Fig. 6.4 SEU and SETLC rates in case that retention data of all latches are 0 or 1 on 45 nm SHC-normal latch. The error bars show statistical error variations at 95% confidence level.

to the normal latch. This is because CCM is significant in 65 and 45 nm technologies. This CCM issue will be resolved by MHC in Section 6.3.3.

6.3.2 Dual clock buffer (DCB) for SETLC mitigation

This section proposes DCB technique for mitigating SETLC. SEILA, which includes DCB, has two clock-buffers and two transmission gates. There are two storage nodes and they are interlocked. In SEILA, a clock-buffer, a transmission gate and a storage

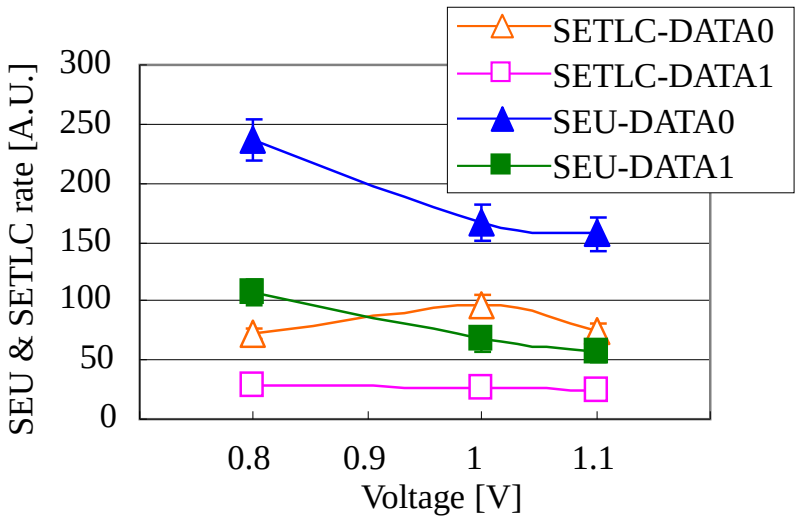


Fig. 6.5 SEU and SETLC rates in case that retention data of all latches are 0 or 1 on 65 nm SHC-DICE. The error bars show statistical error variations at 95% confidence level.

node are grouped. Within the group, a clock-buffer controls a corresponding transmission gate, and the transmission gate transfers the input data to the corresponding storage node, as shown in Figure 6.2. Unless the input data is transferred to the two storage nodes simultaneously, the data stored in the latch is not changed thanks to the interlock mechanism. Therefore, even if a hazard occurs in one of the clock-buffers in SEILA, the stored data does not change. Thus, DCB can prevent the upset from occurring due to SETLC. It should be noted that the overhead of DCB is small and the number of additional transistors is four. When a 2× clock-buffer (consisting of two NMOS and two PMOS) is replaced with two 1× clock-buffers (consisting of a NMOS and a PMOS) in the latch, the cell size is hardly changed.

If a hazard occurs at a clock buffer upstream from the local-clock buffers (i.e. in clock-tree), all the latches connected with the clock buffer can suffer from upset. On the other hand, the size of upstream clock-buffers is larger than that of the local clock-buffers. Additionally, such upstream clock-buffers drive large capacitances. This means that large charge is necessary to cause a hazard at the upstream clock-buffers. As a result, the SET rate of the clock-tree is much smaller than that of the local clock-buffers. In fact, no SET occurring in the clock-tree was observed in the irradiation experiment.

The SETLC rate of the 65 nm DHC-SEILA was evaluated. Figure 6.6 shows the error counts observed in TEST1 and TEST2. The error bars in this figure show statistical error variations at 68% confidence level. There is no significant difference between TEST1 and TEST2 conditions. This result demonstrates that SETLC is not visible in SEILA and DCB eliminates SET-induced upsets as ones expected.

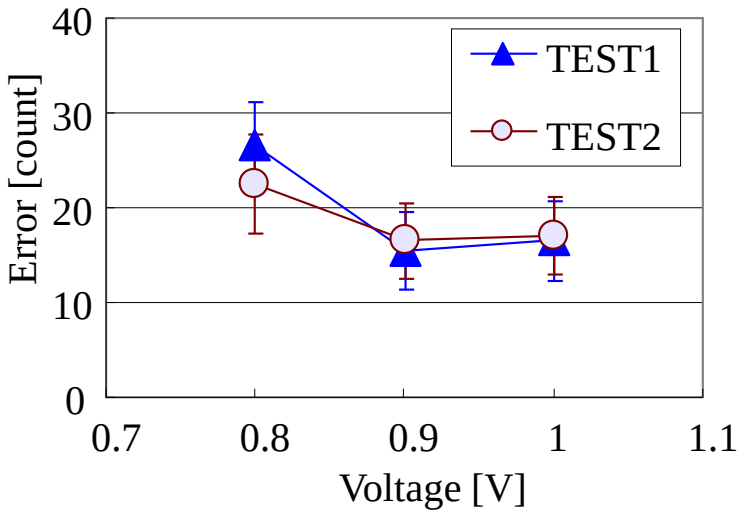


Fig. 6.6 Error count in TEST1 and TEST2 in 65 nm DHC-SEILA2. The error bars show statistical error variations of 68% confidence level.

6.3.3 Multi cell height for CCM mitigation

Charge collection to a single node cannot cause an upset in a redundant latch like SHC-DICE. However, the charge is collected to critical two nodes, the stored data can be corrupted and SEU occurs. This is why the SEU rate reduction of SHC-DICE was not significant as discussed with Figure 6.5.

When the charge is collected to the drain areas of a PMOS and a NMOS which are connected each other, the node voltage does not change much [166]. From the NMOS point of view, the drain of such a PMOS can be regarded as a cancelling area, which is illustrated in Figure 6.7. The PMOS drain and NMOS drain collect holes and electrons, respectively, and the holes and electrons are canceled out due to the connection between the PMOS drain and NMOS drain. On the other hand, from the PMOS point of view, the NMOS drain can be regarded as the cancelling area.

To evaluate the impact of the cancellation, the variation of the node voltage was estimated by device and circuit simulations. When the holes are collected to the PMOS drain connected to node3 and the PMOS drain connected to node4 in Figure 6.2, the stored data flips as shown in Figure 6.8 (a). When the holes are collected to the two drains above mentioned and the electrons are collected to the NMOS drain connected to node4, the stored data is not upset as shown in Figure 6.8 (b).

The impact of CCM due to (A) successive hits by one ion and (C) charge drift/diffusion in Table 1.4 can be suppressed by placing the cancelling area between the two critical areas as shown in Figure 6.7. In this placement, when an ion passes through the two critical areas, the ion must go through the cancelling area as well. In addition, when the charge is shared by the two critical areas, the charge must be also shared by the cancelling area. For enabling such a placement, the layout of SEILA was designed as MHC, i.e. double height cell (DHC) or triple height cell

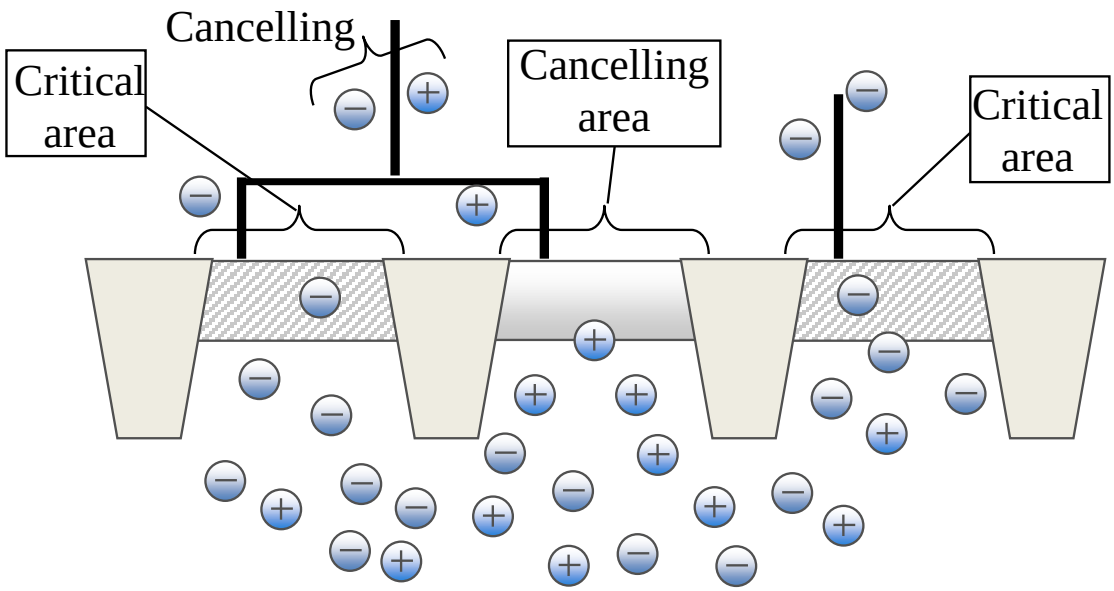


Fig. 6.7 CCM mitigation placement. In this placement, when an ion passes through the two critical areas, the ion must go through the cancelling area as well. In addition, when the charge is shared by the two critical areas, the charge must be also shared by the cancelling area.

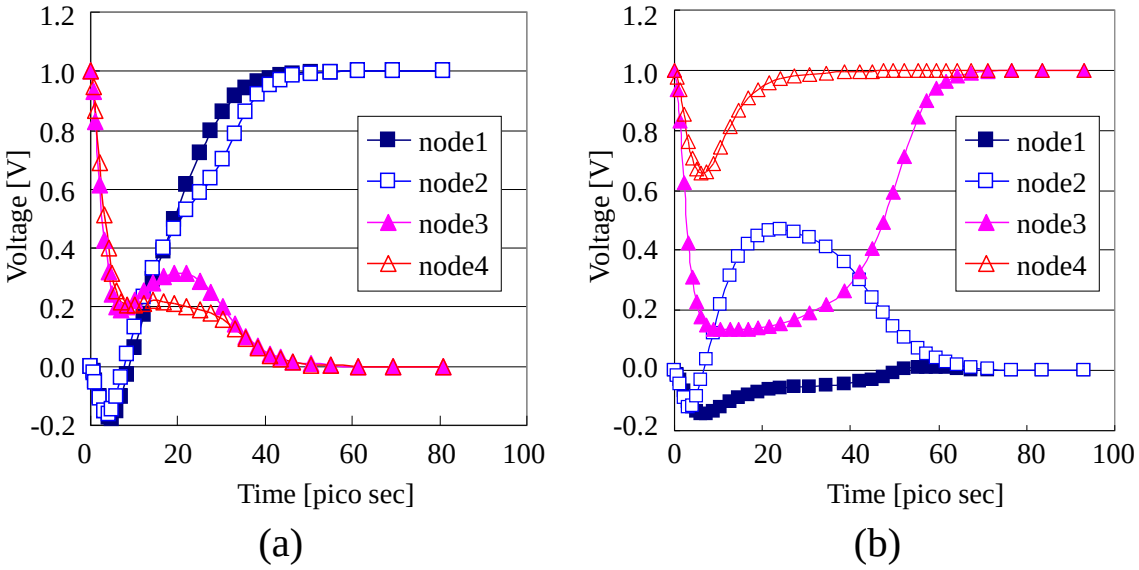


Fig. 6.8 Voltage variation estimated by device and circuit simulations (a) when the holes are collected to the PMOS drain connected to node3 and the PMOS drain connected to node4 in Figure 6.2 and (b) when the holes are collected to the two drains above mentioned and the electrons are collected to the NMOS drain connected to node4.

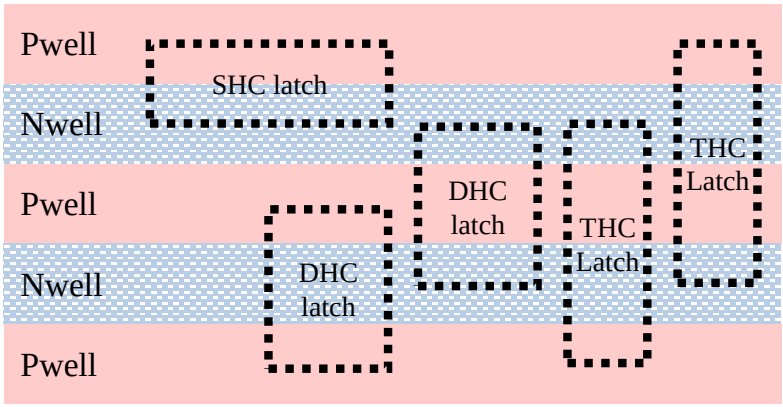


Fig. 6.9 Layouts of SHC, DHC and THC.

(THC) as shown in Figure 6.9. The layout flexibility introduced by the increased cell height makes it possible to exploit the cancelling effect for SEU reduction.

The area for the transistor placement is not different between MHC and SHC, though the aspect ratio is changed as shown in Figure 6.9. First, two SEILA cells were designed with DHC in 65 nm technology (65 nm DHC-SEILA and 65 nm DHC-SEILA2 in Table 6.1). The two SEILAs have different distances between critical areas. The detail of the difference will be explained in Section 6.4.1. In the 65 nm DHC-SEILA, one critical area is put in the upper side, another is put in the lower side, and the cancelling area is put between the two critical areas. Also, two clock-buffers were separately placed in the same way as shown in Figure 6.10 for suppressing not only SET but also CCM in the two clock-buffers. Compared to DHC, THC is expected to attain higher mitigation efficiency. In DHC designed with PMOS center placement, all the PMOSs are included in an N-well area, and NMOS cannot be located between the PMOSs. In DHC designed with NMOS center placement, PMOS cannot be located between the NMOSs. These mean that NMOS/PMOS cancelling area cannot be located between critical areas in the DHC designed with PMOS/NMOS center placement, respectively. However, the routing in the THC cell is difficult because of the narrow width, which may increase the cell area.

6.4 SEU evaluation on SEILA

This section shows the irradiation test results performed for evaluating the SEU mitigation efficiency of SEILA. Section 6.4.1 evaluates the 65 nm DHC-SEILAs. The dependence of the SEU mitigation on the distance between critical areas is also discussed. Section 6.4.2 discusses the SEU mitigation efficiency of the 28 nm DHC-SEILA. From this result of the 28 nm DHC-SEILA, SEILA is improved for 20 nm design. The SEU mitigation efficiency of the improved SEILA is discussed in Section 6.4.3.

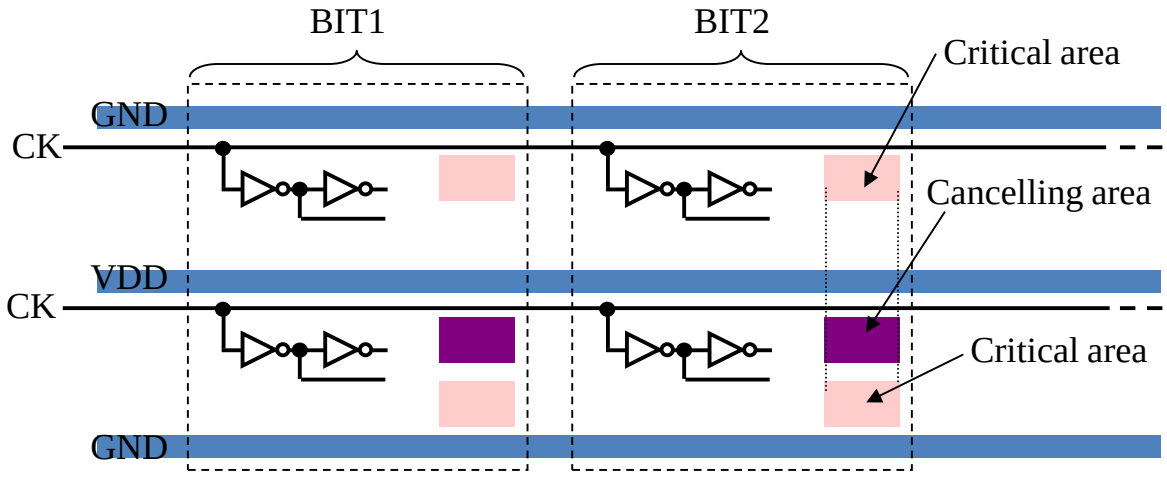


Fig. 6.10 Placement of critical areas and cancelling area. A clock wire is routed in each cell height. Each latch draws clock signal from different two lines for DCB.

6.4.1 SEU mitigation efficiency in 65 nm DHC-SEILA

Neutron irradiation test was performed on a normal latch with SHC, two SEILAs in 65 nm technology (65 nm SHC-normal latch, 65 nm DHC-SEILA, and 65 nm DHC-SEILA2 as shown in Table 6.1). The SEILAs were designed with DHC having different distances between two critical areas (Dp2) (Figure 6.11), where N-well is located at the center in these DHC cells. Distance Dp2 is the distance between the PMOSs of P2 and P4 in Figure 6.11, and it is set to 0.56 μm in 65 nm DHC-SEILA and 0.34 μm in 65 nm DHC-SEILA2. Dp1, which is the distance between the PMOSs of P1 and P3, is 1μm in both the SEILAs.

Figure 6.12 shows SEU rates of the 65 nm DHC-SEILA and 65 nm DHC-SEILA2 in double- and triple-well processes. The DHC technique was effective for the SEU rate reduction. The 65 nm DHC-SEILA2 decreased the SEU rates by 115× and 163× in double- and triple-well at 1.0V, although 65 nm DICE latch, which was designed as SHC, decreased SEU rate by 10× as shown in Figure 6.5. The 65 nm DHC-SEILA2 improved the SEU sensitivity more than 10× from the SHC-DICE latch. The SEU reduction thanks to SEILA is kept both in double- and triple-well. Note that these SEU rates are the average values for DATA0 and DATA1, and they do not include the SETLC rates because these experiments were performed under TEST1 condition.

In the 65 nm DHC-SEILA with shorter Dp2, the SEU reduction is less significant than in the 65 nm DHC-SEILA with longer Dp2. The 65 nm DHC-SEILA decreased the SEU rates by 6.7× and 65× from normal 65 nm latch in double- and triple-well at 1.0V. The reason of the smaller SEU reduction was investigated in terms of the distance from well-contacts and the value stored in the latch. In the test chip, well-tap is placed as shown in Figure 6.13. There are latches which are placed nearly and distantly from the well-taps.

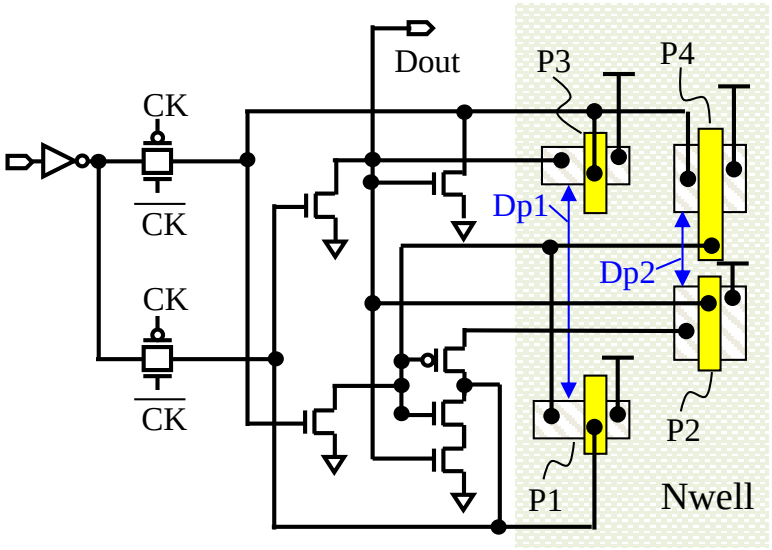


Fig. 6.11 SEILA schematic and layout.

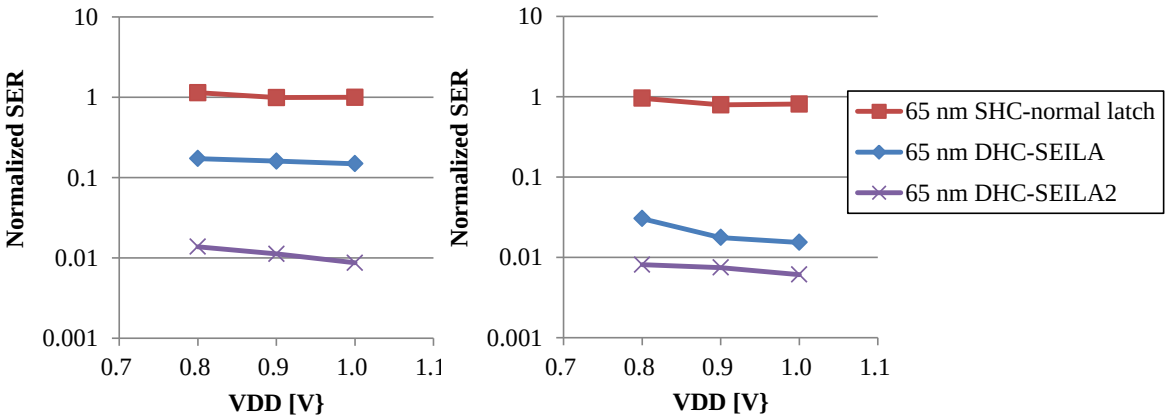


Fig. 6.12 SEU rates of normal latch (65 nm SHC-normal latch), SEILAs (65 nm DHC-SEILA, 65 nm DHC-SEILA2) in (a) double-well (b) triple-well. The SEU rates are normalized with the SEU rate in 65 nm SHC-normal latch at 1.0V in double-well.

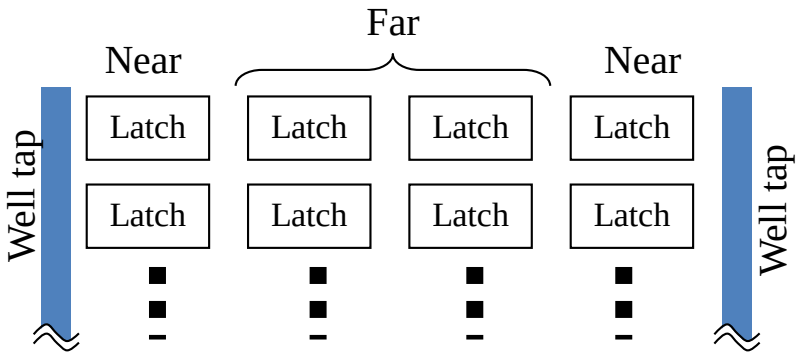


Fig. 6.13 Latch array layout of the test chip for 65 nm latches.

Figure 6.14 shows the SEU rates for DATA0 and DATA1 at the positions near and far from the well-contacts. The SEU rate for DATA0 in the 65 nm DHC-SEILA in double-well is noticeably high, and the SEU rate increases with the distance from the well-contacts. This tendency of the higher SEU rate is due to the charge collection to the drains of P2 and P4 (see Figure 6.11). The PMOSs of P2 and P4 are sensitive in case of DATA0 because PMOS contributes to soft error when the drain node is at low voltage, and the voltages of P2 and P4 drain are low in DATA0. Such significantly high SEU rate was observed only in double-well. PBA on PMOS in double-well is higher than in triple-well because the N-well potential is easy to change in double-well. In addition, PBA becomes more active as the distance from well-contacts increases [103]. This is the reason why the high SEU rate was observed in the 65 nm DHC-SEILA.

The 65 nm DHC-SEILA attained the significant SEU rate reduction by placing the critical areas distantly. However, it is difficult to design the DHC-SEILA layout in more advanced technologies such as 28 nm and 20 nm keeping the amount of SEU reduction, because the absolute distance between the critical areas decreases. The next section discusses the scaling trend of SEU prevention by SEILA.

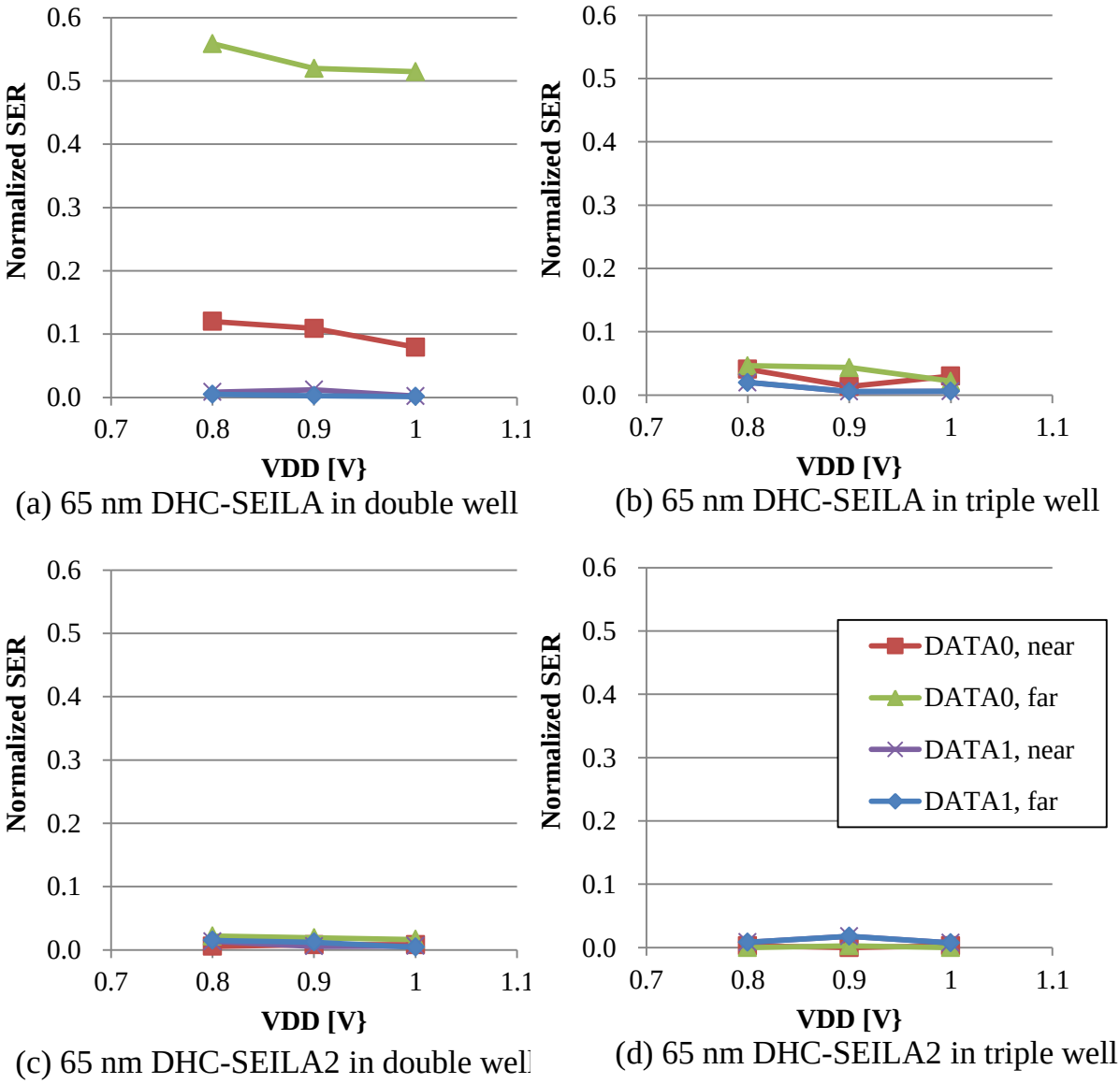
6.4.2 SEU mitigation efficiency on 28 nm DHC-SEILA

A SEILA was designed with DHC in 28 nm technology and its SEU rate was evaluated with neutron irradiation test. The neutron irradiation test was performed on the DUTs including the SEILAs with spallation neutron beam at RCNP. The average flux of neutron beam whose energy was higher than 10 MeV was 2.01 billion neutron/hour/cm^2, and the irradiation time was 60 hours. Figure 6.15 shows the timing chart of the test procedure. During the write phase, a 10MHz clock signal was given to write the data patterns in the latches. Then, the SEILAs were kept in hold operation for 15 minutes, and the stored values were read out. The supply voltage was 0.75 V in read/write phases and 0.7, 0.85 and 0.9V in hold phase. The hold duration is over 1000 times longer than the read/write durations, and hence the measured upset counts can be regarded as the upset counts during the hold operation.

The SEU rate in the 28 nm DHC-SEILA is at the same level with that of the 65 nm DHC-SEILA as show in Figure 6.16. This means that the layout technique using DHC is still active in 28 nm. Naturally, the sensitive area in 28 nm is smaller than in 65 nm, but the distance between the critical areas in 28 nm is shorter than in 65 nm. As a result, the SEU rates are at the same level in the 65 nm and 28 nm DHC-SEILA.

On the other hand, compared to a processor chip fabricated in 65 nm technology, more than 5× transistors are integrated on a microprocessor chip in 28 nm technology [109, 116]. This indicates that the SEU prevention by the DHC-SEILA in 28 nm processors cannot keep the same level of chip-level reliability. If the DHC-SEILA would be used for the next 20 nm processor, further reliability degradation was easily anticipated since CCM would occur more frequently due to transistor shrinking and the number of transistors in a processor would increase.

The result of the 28 nm DHC-SEILA is examined in detail. Figure 6.17 shows the SEU rates in the 28 nm DHC-SEILA for DATA0 and DATA1. SEU was observed only for DATA0 and no SEU was observed for DATA1. On the other hand, the distance between the critical nodes was 0.15 and 0.21 μm for DATA0 and DATA1, respectively.



(a) 65 nm DHC-SEILA in double well

(b) 65 nm DHC-SEILA in triple well

(c) 65 nm DHC-SEILA2 in double well

(d) 65 nm DHC-SEILA2 in triple well

Fig. 6.14 SEU rates of latches located far or near from well-contacts in (a) 65 nm DHC-SEILA in double-well, (b) 65 nm DHC-SEILA in triple-well, (c) 65 nm DHC-SEILA2 in double-well and (d) 65 nm DHC-SEILA2 in triple-well.

This result clarified the importance of the distance on SEU prevention again in 28 nm. Note that the Qcrit is different for DATA0 and DATA1, and this difference can also contribute to the SEU rate difference.

6.4.3 SEU mitigation efficiency on 20 nm DHC-SEILA

To cope with the increase in the number of latches on a chip due to the technology scaling from 28 nm to 20nm, the SEU rate of SEILA must be required to reduce. Otherwise, the microprocessor in 20 nm technology reliability must deteriorate. Motivated by this tendency, 20 nm SEILA was designed with THC. THC is expected

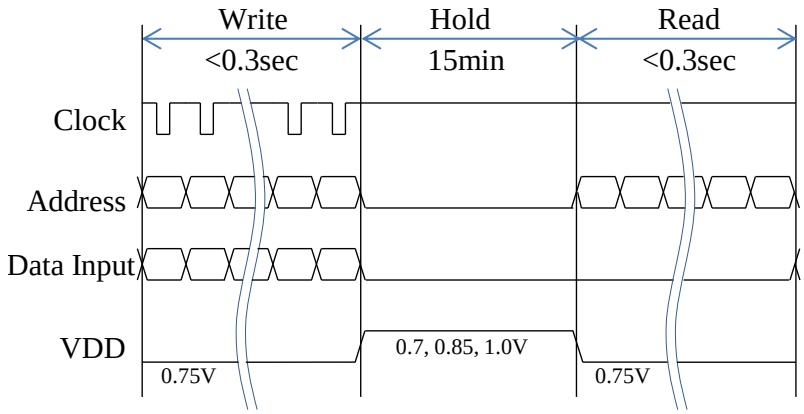


Fig. 6.15 Test timing chart for the 28 nm DUT.

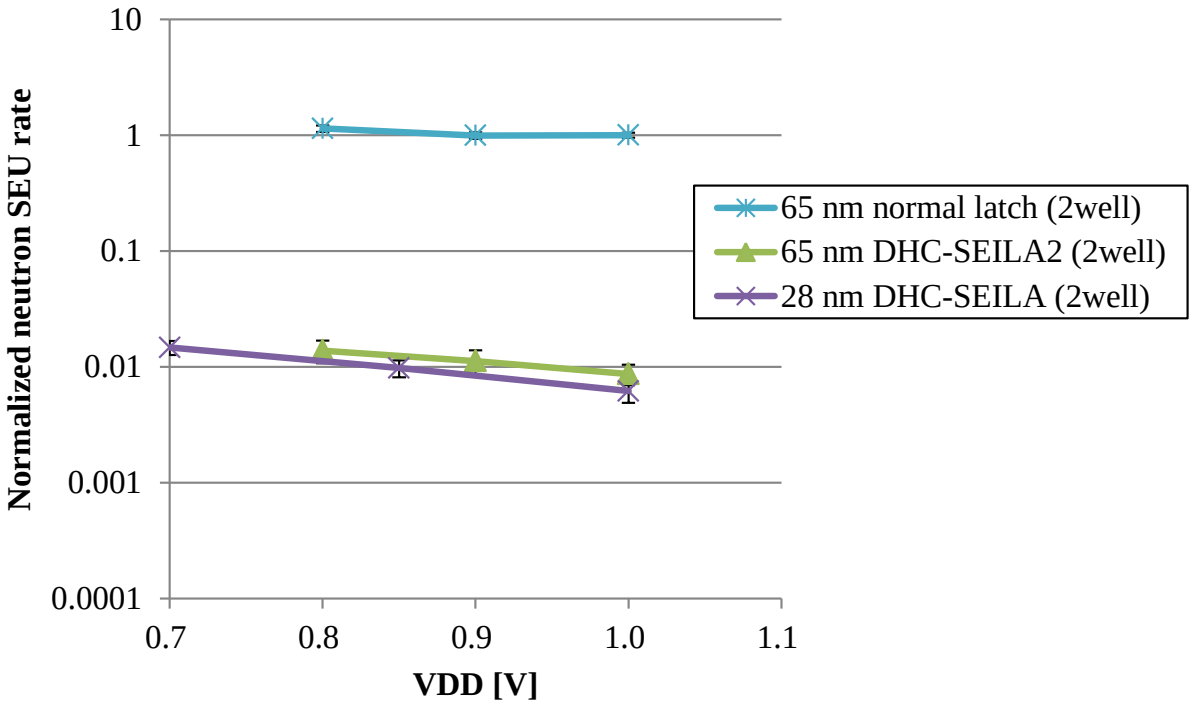


Fig. 6.16 SEU rates in 65 nm normal latch, 65 nm DHC-SEILA2 and 28 nm DHC-SEILA. All latches in this figure are manufactured with double-well process. The SEU rates are normalized with SEU rate in 65 nm normal latch at 1.0V. Error bars represent 90% statistical confidence level.

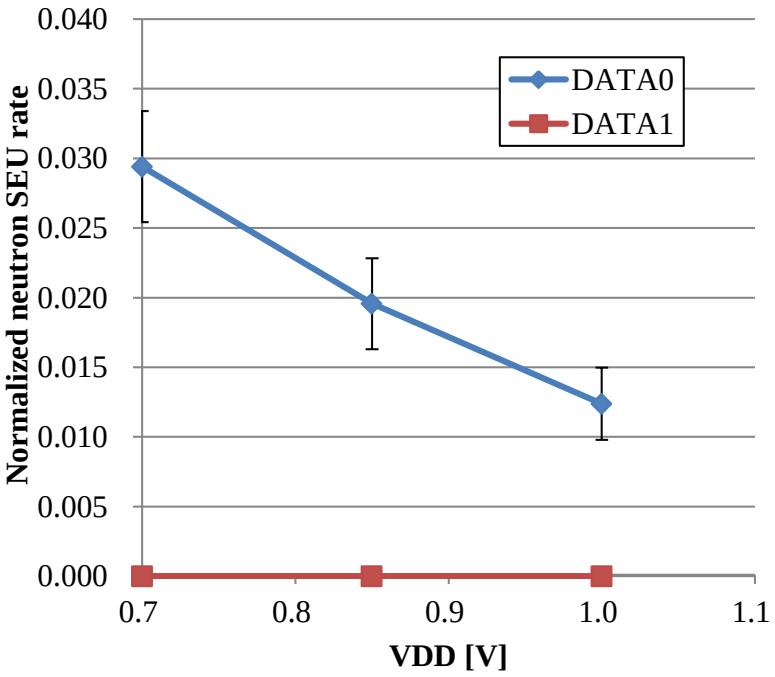


Fig. 6.17 SEU rates in 28 nm DHC-SEILA of double-well for DATA0 and DATA1. The SEU rates are normalized with SEU rate in 65 nm normal latch at 1.0V. Error bars represent 90% statistical confidence level.

to provide higher mitigation efficiency than DHC because 1) larger distance can be obtained, 2) the critical transistor pairs can be located in different wells and 3) the cancelling transistors can be put between the critical transistor pairs. In fact, all the critical pairs of PMOSs and NMOSs are not included in the same well area in the developed THC-SEILA, and the canceling area is located between the paired critical areas. On the other hand, some critical pairs in the DHC-SEILAs are included in the same well, and the cancelling area is not located between the combinations. This transistor location could be one of reasons of SEU occurrence in the DHC-SEILAs. In addition, well-contacts locate in the cell area of the 20 nm THC-SEILA for attenuating PBA induced CCM. The cell size of the designed THC-SEILA is as about 2.4 times large as that of a 20 nm normal latch, and three metal layers are used for interconnection inside the cell, while two metal layers are used in the normal latches.

Neutron irradiation test was performed with the spallation neutron beam at RCNP in 108 hours. The DUT includes two types of 20 nm THC-SEILAs: with and without the well-contact in the cell. About 8 Mb and 6 Mb of the SEILAs with and without well-contacts are included in the DUT. The DUTs were assembled on plastic packages with wire bonding. The five DUT boards were irradiated as shown in Figure 6.15. Each DUT board has three DUTs with DNW and three DUTs without DNW. The DNW is placed under the latches and logic area, not under the I/O area. The N-well and P-well are connected to VDD and GND in the both DUTs with and without DNW. Figure 6.15 shows the timing chart of the test procedure. In the write phase, we set data to all latches in the DUTs with one clock signal. Then, the latches were

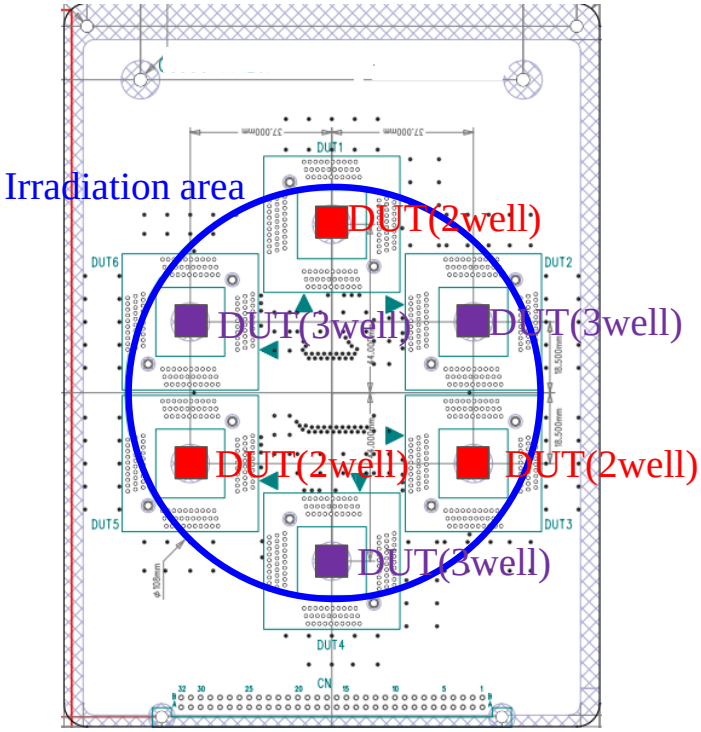


Fig. 6.18 Board configuration for the 20 nm DUT.

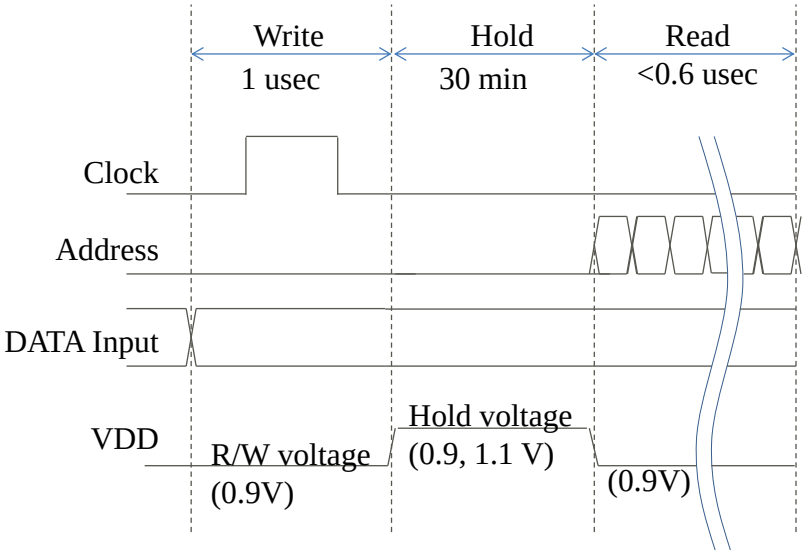


Fig. 6.19 Test timing chart for the 20 nm DUT.

kept in hold operation for 30 minutes, and the stored values were read out. The supply voltage was 0.9V in the read/write phases and 0.9 and 1.1V in the hold phase. The hold duration is over 10,000 times longer than the read/write durations, and hence the measured upset counts can be regarded as the upset counts during the hold operation.

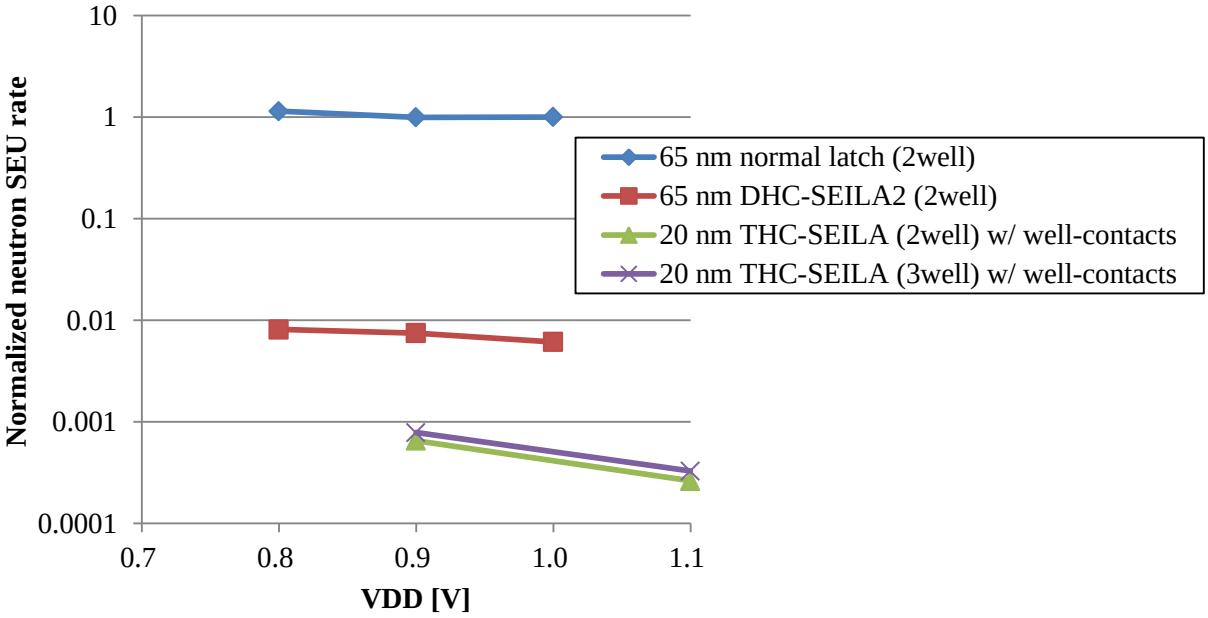


Fig. 6.20 SEU rates of 20 nm THC-SEILA in double- and triple-well. The SEU rates are normalized with SEU rate in 65 nm normal latch at 1.0V. Error bars represent 90% statistical confidence level.

The neutron induced SEU rate of the 20 nm THC-SEILA is 14× lower than that of the 65 nm and 28 nm DHC-SEILA as shown in Figure 6.20. On the other hand, compared to a processor chip fabricated in 65 nm technology, more than 6× transistors are integrated on a microprocessor chip in 20 nm technology [109, 117]. This indicates that the SEU prevention by the THC-SEILA in 20 nm processors improves the chip-level reliability from the 65 nm processors. The SEU rate of the THC-SEILA was kept low in both double- and tipple-well. The SEU rate with triple-well is a little higher than that with double-well.

The result is examined in detail focusing on the difference of the well configuration and the contribution of the well-contacts in the cell. Figure 6.21 shows the SEU rates in the 20 nm THC-SEILA for DATA0 and DATA1 with and without well-contacts in the cell. The error bars in this figure represent 90% statistical confidence level. Changing from double- to triple-well, the SEU rates increases only for DATA0, and no large different was observed for DATA1 in both the 20 nm THC-SEILAs with and without well-contacts. The SEU increase due to the triple-well process is higher in the SEILA without well-contacts than in the SEILA with well-contacts in the cell. The well-contacts contribute to the decrease in the SEU rate in the triple-well.

Also alpha irradiation test was performed using an ^{241}Am alpha source in a vacuum chamber. In the alpha irradiation test at 0.9, 1.0 and 1.1 V, no error was observed in the 20 nm THC-SEILA with and without well-contacts in double- and triple-well, respectively. The SEU rates of all the 20 nm TCH-SEILAs in all conditions are less than 1 FIT/Mbit with 90% statistically probability for 0.001 alpha/hour/cm^2. From these results in the 20 and 28 nm SEILAs, THC design is necessary for achieving high reliability in processors. Adding well-contacts in the cell contributes to the prevention

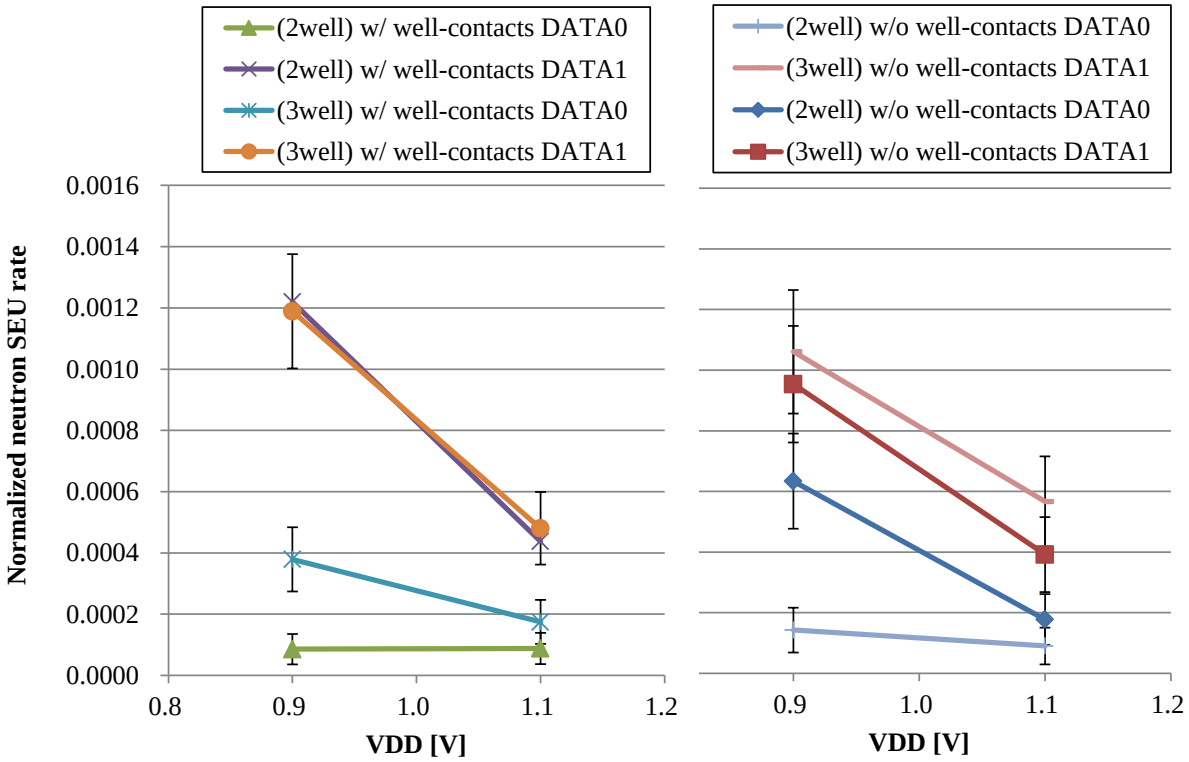


Fig. 6.21 SEU rates in 20 nm THC-SEILA for DATA0 and DATA1 with well-contacts (left) and without well-contacts (right). The error bars represent 90% statistical confidence level.

Table. 6.2 Summary of SEU rates in SEILAs at 1.0V. The SEU rates are normalized with the SEU rate in 65 nm SHC-normal latch. Note that the SEU rates in 20 nm THC-SEILAs have no experimental data and the shown SEU rate is the average of SEU rates at 0.9 V and 1.1 V.

Latch name	SEU rate (2well)	SEU rate (3well)
65 nm DHC-SEILA	0.15	0.015
65 nm DHC-SEILA2	0.0087	0.0061
28 nm DHC-SEILA	0.0062	no data
20 nm THC-SEILA w/ well-contacts	0.00046	0.00056
20 nm THC-SEILA w/o well-contacts	0.00039	0.00061

of SEU occurrence in triple-well.

6.5 Conclusions

This chapter proposed a soft error immune latch called SEILA, which adopted MHC (DHC, THC) design and DCB technique. The MHC design mitigates the SEU occurrence originating from CCM, and the DCB technique prevents SETLC from causing data upset. Table 6.2 summarize the SEU rates of the SEILAs. The 65 nm SEILA designed with DHC and DCB was evaluated with neutron irradiation test. The DCB

eliminated the SEU occurrence due to SETLC, and the DHC reduced the SEU rate by 99.3%. The neutron irradiation test in the SEILAs with different distances between the critical nodes shows that the SEU mitigation efficiency depends on the distance. In 28 nm technology, SEILA was designed with DHC. The SEU rate in the 28 nm DHC-SEILA is comparable with that of the 65 nm DHC-SEILA. The SEU rate in the 28 nm DHC-SEILA is not low enough since more number of latches are used in the 28 nm microprocessor than the 65 nm one. Motivated by this, SEILA was designed in 20 nm technology with THC for achieving higher SEU prevention, and its neutron and alpha SEU rates were evaluated. The neutron induced SEU rate is 14X lower in the 20 nm THC-SEILA than in the 28 nm DHC-SEILA. In the alpha irradiation test, no error was observed and the SEU rate was less than 1 FIT/Mbit with 90% statistically probability for 0.001 alpha/hour/cm^2.

Beyond the 20 nm technology, bulk CMOS technology is predicted not to be used, and FinFET or SOI technologies will be used. Soft error tolerance in FinFET and SOI technology is higher than in bulk CMOS technology [86]. As a result, 20 nm bulk CMOS technology can be the toughest technology for mitigating soft error in SEILA. The results in this chapter confirm that SEILA can be used as a radiation-hard latch in all transistor technologies.

Chapter 7

SEU rate in SRAM at ultra-Low Voltage

This chapter investigates SEU rate in ultra-low voltage operation [167]. Keeping low power consumption in electron devices is a critical issue for current large scale systems, and the further power reduction will be demanded in future processor designs since more processors will be operated in parallel to improve the performance. The most effective approach to reduce power consumption is to lower the supply voltage because the power consumption strongly depends on the operation voltage. To investigate SEU rate of low voltage SRAM for future processor designs, this chapter evaluates and discusses SRAM SEU rate in a wide range of supply voltage. This chapter presents SEU rate measured through neutron and alpha irradiation tests and simulation in SRAM at ultra-low voltages, down to 0.19 V. Measurement results show that SEU rate at 0.19 V is higher than at 1.0 V by two orders of magnitude. This measurement result supported by simulation demonstrates that direct ionization from secondary protons generated by nuclear reaction with neutron collision contribute to a dramatic increase in SRAM soft error-rate at ultra-low voltages in terrestrial environment.

7.1 Introduction

Low power operation is strongly demanded in recent and future highly-integrated electronic devices. An aggressive voltage scaling down to the threshold voltage of MOSFETs can dramatically reduce power consumption of electronic devices. Recently, memory operation at ultra-low voltage down to 0.2 V has been achieved with 9T-SRAM [168]. SRAM operation at such an ultra-low voltage attains low power consumption at the sacrifice of speed performance. Another approach called sleep technology, which scales down supply voltage during data holding as much as memory retention is possible [169], has already been used in SRAM for reducing power consumption. The sleep technology saves power consumption during non-active operations without involving performance penalty for active operations.

Neutrons indirectly induce soft error through nuclear reaction as explained in Section 1.2.2. The nuclear reaction generates charged secondary particles like protons, alpha particles and heavy ions and electron-hole pairs are generated by ionization.

In recent 65 nm to 25 nm technologies, it is reported that direct ionization due to secondary alpha particles is a major contributor to neutron SEU rate in terrestrial environment [65, 64, 70, 69]. On the other hand, in low voltage SRAM, direct ionization from secondary protons can be a major contributor [69, 34, 170], because the low voltage operation reduces Qcrit. Reference [170] demonstrated that low energy protons contribute to SEU rate by direct ionization and the cross-section of low energy protons (< 2 MeV) is three orders of magnitude larger than that of high energy protons (> 10 MeV). The proton impact on SEU rate is also investigated in [171, 172, 173]. Reference [171] reported that direct ionization from protons is a major contributor to the total SEU rate in the international space station (ISS) orbit and geosynchronous (worst day) orbit. Returning to terrestrial environment, [34] demonstrated that the number of generated secondary protons is one or two orders of magnitude larger than the number of alpha particles. The direct ionization from proton could dramatically increase neutron SEU rate of ultra-low voltage SRAM.

SEU rate in 65 nm 10-T sub-threshold SRAM was experimentally studied through neutron irradiation test [174] and alpha irradiation test [175]. The neutron SEU rate at 0.3 V was 7.8 times higher than that at 1.0 V. The alpha SEU rate at 0.3 V was eight times higher than that at 1.0 V, and the increase ratios of neutron and alpha SEU rates were almost the same. On the other hand, the SRAM cell in these works is composed of larger transistors for mitigating Vth variation and achieving ultra-low voltage operation, and the NMOS and PMOS gate areas of cross-coupled inverter are 7.8 and 6.9 times larger than the area of a minimum-sized transistor. Due to this, the Qcrit was not small enough that the secondary proton direct ionization caused upsets [176]. Thus, a drastic increase in neutron SEU rate due to secondary proton direct ionization was not clearly observed [174]. If proton direct ionization starts to contribute to soft error, the increase in neutron SEU rate should be much larger than that in alpha SEU rate [34].

This work evaluates SEU rate on SRAM at ultra-low voltage down to 0.19 V through neutron and alpha irradiation tests manufactured with 90 nm technology. The impact of direct ionization from the secondary protons in terrestrial environment is discussed based on radiation experiments and Monte-Carlo simulations using PHITS [49].

The rest of this chapter is organized as follows. Accelerated test procedure at ultra-low voltage is explained in Section 7.2, and Section 7.3 shows test results. Section 7.4 presents SEU rate calculation by simulation. Section 7.5 concludes this chapter with a brief summary.

7.2 Irradiation test procedure

Alpha and neutron irradiation tests were performed on SRAM devices. This section explains the experimental setups. The alpha irradiation test was carried out with an ^{241}Am alpha source under low pressure atmosphere in a chamber. The distance between the alpha-source and the die is less than one millimeter. The neutron irradiation test was conducted with spallation (wide spectrum) neutron beam at RCNP. The beam and DUT configurations are illustrated in Figure 7.1.

In this chapter, four DUTs mounted on the first board are analyzed to exclude neu-

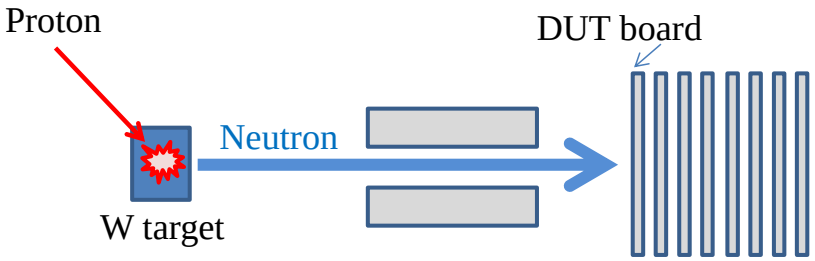


Fig. 7.1 Neutron test configuration at RCNP for 90 nm SRAM. This shows only the target, collimator and DUT boards. The other parts are same with other tests shown in Figure 1.15.

tron scattering and attenuation effects. The DUT includes SRAM arrays consisting of about 4 Mbit SRAM on each DUT with double-well process. This SRAM consists of conventional 6T-SRAM cells with the conventional layout as shown in Figure 7.2. This SRAM was customized for ultra-low voltage operation. The Vth, width and length of transistors were optimized for enabling ultra-low voltage operation in 90 nm technology. The minimum transistor width was selected, whereas the length was enlarged to mitigate random Vth variation by increasing the gate area [177]. Consequently, the SRAM cell size is 1.4 times larger than the normal cell size in the 90 nm technology generation. The power supply to the memory cell areas is separated from other areas.

A quasi-static test was performed for this irradiation experiment. A timing diagram of the SRAM operation and supply voltage is shown in Figure 7.3. The DUTs were irradiated during data read and write as well as data hold. On the other hand, the duration of data hold was 1 minute while the data read and write were completed within 1 second. Therefore, the number of upsets during the data read and write is thought to be negligibly small compared to that during the data hold. The operation voltage for data read/write was 1.2 V. As for data hold, various supply voltages from 0.19 V to 1.6 V were given to the memory cell.

It was supposed that any two upset bits whose distance was three-cell or less were caused by an event. This classification was applied to all the combinations of two upset bits. The upset bits which were caused by the same event were recognized as an MCU event. This distance criterion was applied omnidirectionally.

7.3 Experimental results

First neutron induced SEU rate is discussed. Figure 7.4 shows the measured neutron induced SEU rate. The SEU rate is the minimum at 1.2 V, and it increases as the supply voltage increases and decreases from 1.2 V. The existence of the extremum, which corresponds to the local minimum at 1.2 V, is explained by two different phenomena on soft error as illustrated in Figure 7.5. Qcrit increase according to voltage increase reduces SEU rate. The contribution of PBA, on the other hand, increases and consequently SEU rate increases with voltage increasing. As a result, the SEU rate curve as a function of supply voltage has an extremum as shown in Figure 7.4.

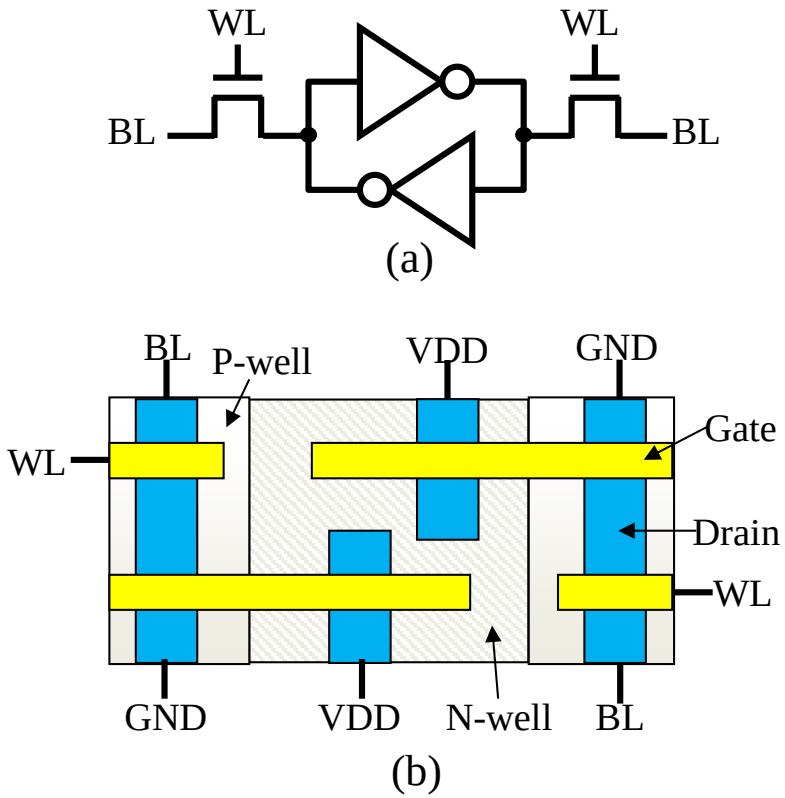


Fig. 7.2 (a) Schematic and (b) layout of SRAM for the irradiation tests.

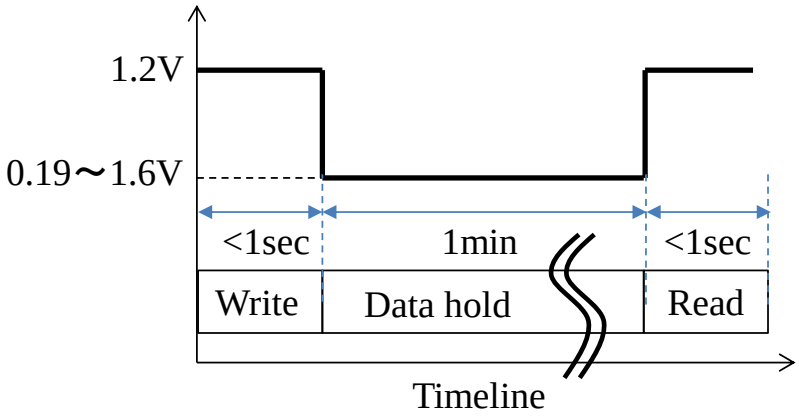


Fig. 7.3 Timeline of the irradiation test.

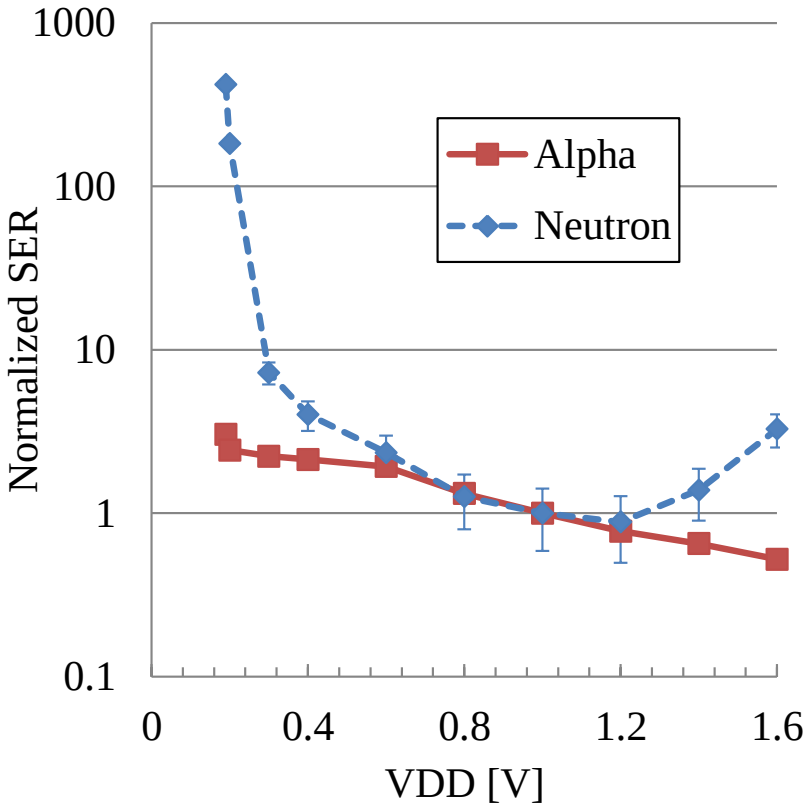


Fig. 7.4 Alpha and neutron SEU rates normalized by alpha and neutron SEU rates at 1.0 V, respectively.

The decreasing trend of SEU rate with voltage increase is consistent with other papers [69, 170, 174, 176, 140, 123]. On the other hand, the SEU rate at voltages higher than the nominal voltage (1.2 V in this process) is not often reported in literature, while it is measured in this chapter. The investigation of the voltage dependency including such high voltages shows that PBA increases in SEU rate at high voltages. Besides, a flat voltage dependency of SEU rate at high voltages is reported in [140]. This flat voltage dependency comes from a fact that the voltage dependencies of PBA and Qcrit are canceled each other at these voltages.

Meanwhile, the alpha induced SEU rate, which is also plotted in Figure 7.4, does not have such an extremum and it monotonically decreases roughly at an exponential rate with voltage increase. Even above 1.2 V, the alpha induced SEU rate decreases in contrast with the neutron induced SEU rate, which suggests PBA is less influential in the alpha induced SEU rate. Reference [175] observed that body voltage and well-tie interval, which affects neutron-induced SEU rate [174], are not related to alpha induced SEU rate and concluded that PBA hardly contributes to alpha induced SEU rate. Our observation in this chapter is consistent with [175].

Next, the difference in SEU rate increase at low voltage is examined. The neutron SEU rate at 0.3 V is about seven times higher than that at 1.0 V, while the increase ratio from 1.0V to 0.3V reported in [174] was 7.8×. The SEU rate increase measured

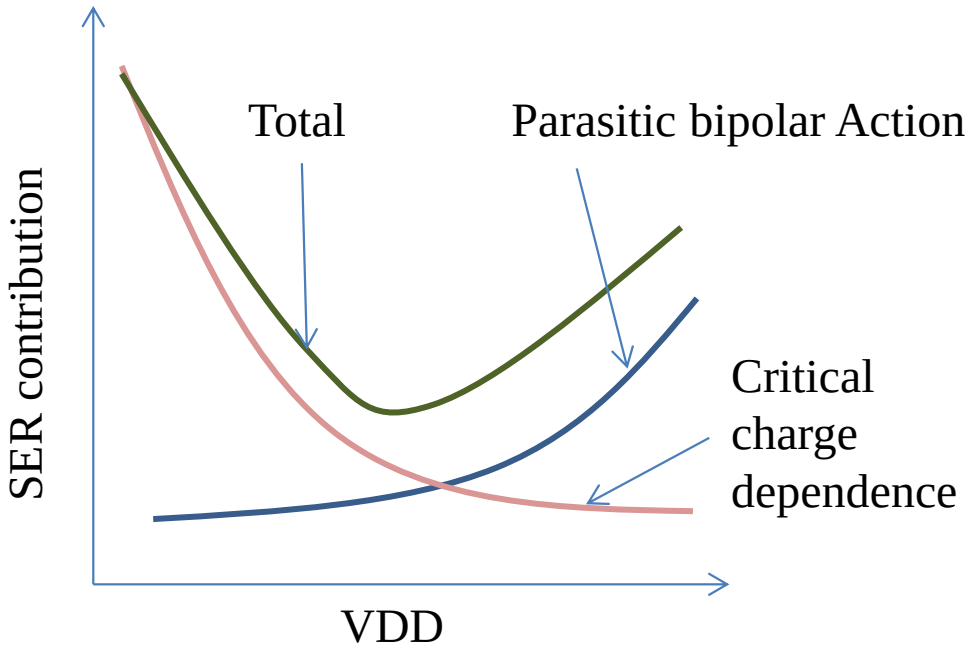


Fig. 7.5 A conceptual illustration of SEU rate contribution.

in this work is consistent with [174]. On the other hand, at ultra-low voltages of 0.19 V and 0.20 V, the neutron SEU rate dramatically increases and its increase at 0.19 V from 1.0V reaches 440×. The SEU rate at such a low voltage has not been reported, and this is the first work that reports such a drastic increase in neutron SEU rate.

In contrast, the alpha SEU rate at these ultra-low voltages increases by only 4× from SEU rate at 1.0 V. This result naturally leads us to conclude that this dramatic increase at ultra-low voltage is caused by proton direct ionization due to secondary protons, since [34] predicted that a drastic increase would be observed once proton direct ionization starts to contribute to SEU rate. The contribution of the proton direct ionization will be further discussed with simulations in the next section.

Lastly, the contribution of PBA is discussed with MCU rate. Figure 7.6 shows that the neutron induced SBU rate increases at above 1.2 V, and the neutron induced MCU rate increases at above 1.0 V. While PBA contributes to both SBU and MCU, the impact on MCU has been more intensively discussed in literature [123, 103] since some of MCUs could not be corrected by ECC and interleaving. Besides, at 1.6 V, the MCU rate is higher than the SBU rate, which means that more than half soft errors are MCU at 1.6 V. This result shows that MCU is more sensitive to PBA, while the contribution ratios of PBA to SBU and MCU rates are different. On the other hand, the alpha induced SBU and MCU rates decrease as voltage increases as shown in Figure 7.7. This result again indicates that the contribution of PBA is not significant in alpha induced soft error, because PBA activation is accompanied with an increase in MCU rate. It can be considered as a cause that high LET particles like heavy ions generated by neutron collision can trigger PBA although low LET particle like alpha

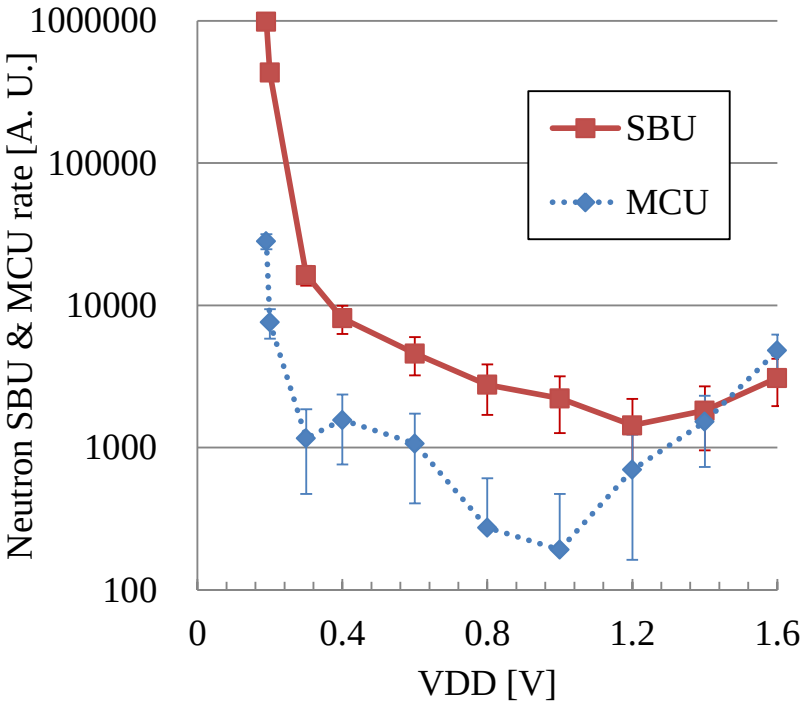


Fig. 7.6 Neutron induced SBU and MCU rates.

cannot trigger PBA in this SRAM. Another possible reason for the trend difference between alpha and neutron induced SBU and MCU could be the angular distribution of ionizing species between alpha irradiation and neutron secondary particles. Further investigations on the impact of the angular distribution with detailed simulations are included in our future work.

7.4 Simulation

To further understand the soft error mechanism at ultra-low voltage, contributions of secondary particles to soft error was calculated. Here, the soft errors are categorized and accumulated depending on the secondary particles (protons, deuterons, tritons, alpha and other heavy ions). In this simulation, Qcrit at each memory cell voltage (0.19 V to 1.6 V) was evaluated by circuit simulation with the conventional double exponential model [178], and a simple linear regression was carried out supposing Qcrit =0 at 0 V. The derived linear function was used for computing Qcrit at each supply voltage including the ranges below 0.19 V and beyond 1.6 V. SEU rate for each Qcrit was calculated by Monte-Carlo simulation using PHITS [49] ver. 2.52 with the sensitive volume method. Note that when Qcrit is 0, every penetration into the sensitive volume is assumed to cause an upset regardless of the deposited charge. The simulation assumed a neutron source whose energy spectrum was the same with the spallation neutron beam at RCNP shown in Figure 1.13, and 1 million neutrons were injected within 0.012 cm^2 whose energy was 1 MeV to 400 MeV. Neutrons below

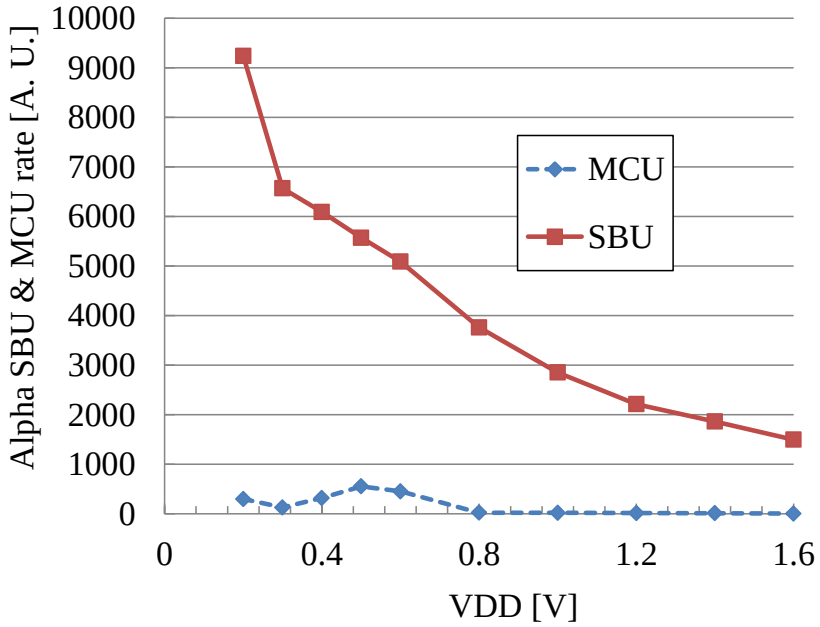


Fig. 7.7 Alpha induced SBU and MCU rates.

1 MeV were not considered.

The simulated structure, which is illustrated in Figure 7.8, reproduces the SRAM structure used in the irradiation tests. The structure consists of a metal layer, which corresponds to interconnect layers, and a Si block. The length, width and depth of the Si block are about 500, 1100 and 500 μm. The structure includes 500 $\times$ 500 bit cells, and the cell array is horizontally surrounded by 50 μm Si. Si substrate is attached below the cells.

In this simulation, two types of sensitive volumes, which correspond to sensitive NMOS and PMOS, are placed. The areas of the sensitive volumes are the same with the drain areas of sensitive NMOS and PMOS, and the depths of the NMOS and the PMOS volumes are 1.24 μm and 0.29 μm, respectively [179]. Besides, SEU rate in this simulation does not include the contribution of PBA. Note that at ultra-low voltage, PBA is less visible as explained with Figure 7.5 and hence this simulation is appropriate to discuss SEU rate at ultra-low voltage.

Figure 7.9 shows the contribution ratio of each secondary particle, and Figure 7.10 presents the calculated SEU rate originating from each secondary particle. As the supply voltage becomes lower, the contribution of proton direct ionization increases, and it becomes larger than that of alpha particles at 0.25 V and below. Below 0.25 V, the Qcrit reaches the point that secondary protons can cause SEU. Consequently, ultra-low voltage SRAM whose supply voltage is lower than 0.25 V is expected to significantly suffer from a drastic increase in SEU rate due to secondary protons. Meanwhile, alpha is dominant in a wide voltage range of 0.25 V to 1.9 V, and other heavy ions become dominant at 1.9 V and higher.

There is a large difference between the simulation and the measurement in terms of the SEU rate increase from 1.0 V to 0.19 V. Figure 7.11 plots the measured and

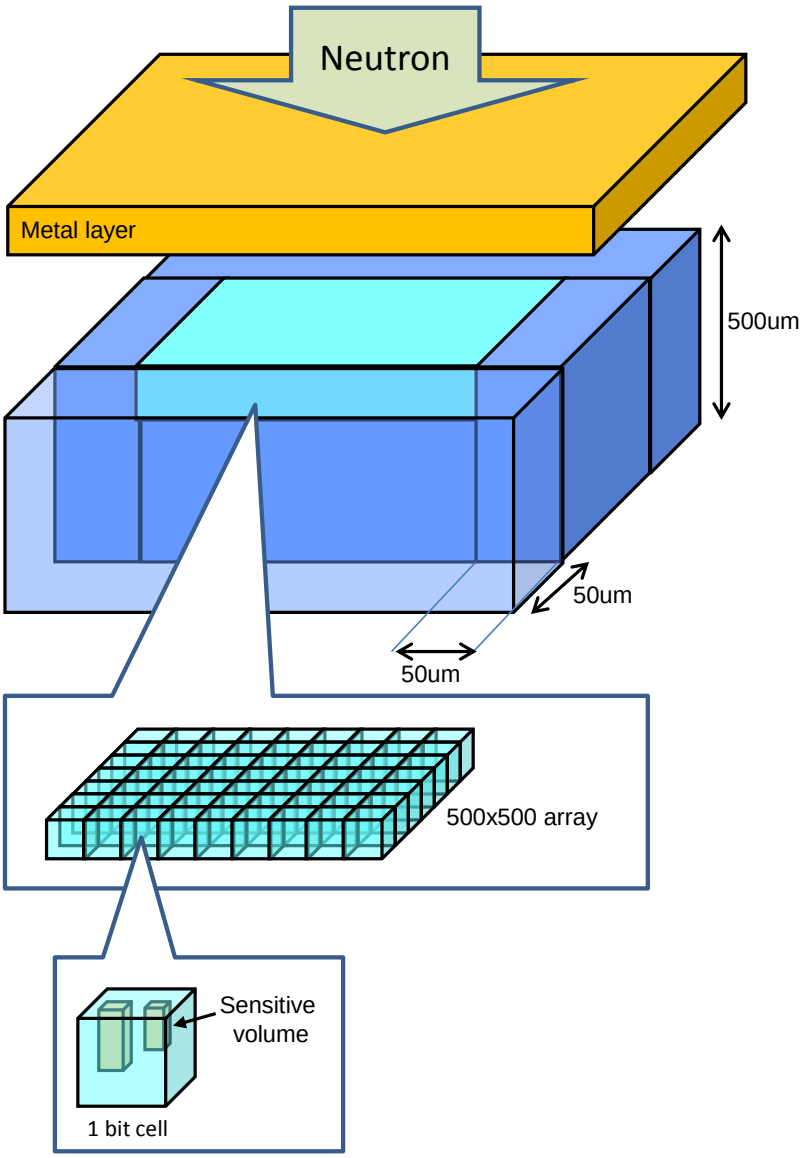


Fig. 7.8 Simulated structure.

simulated SEU rates extracted from Figure 7.4 and Figure 7.10. The SEU rate increase from 1.0 V to 0.19 V in the simulation is 4× whereas that in the measurement is 440×. There are two possible reasons for this underestimation in the simulation,.

The first possible reason is ignoring secondary protons coming from outside of the silicon die modeled in this simulation. Protons can travel a long distance compared to other secondary particles. Figure 7.12 shows the production numbers of proton, alpha, Si and other heavy ions as a function of particle energy, which is calculated with PHITS assuming a neutron beam having RCNP energy spectrum is given to Si substrate. Figure 7.13 shows the production rate as a function of proton travel distance, where it is calculated from the data shown in Figure 7.12 and the relation between proton travel distance in Si and proton energy obtained by SRIM [1]. The distribution has a long right tail, and the portion of protons that travel more than

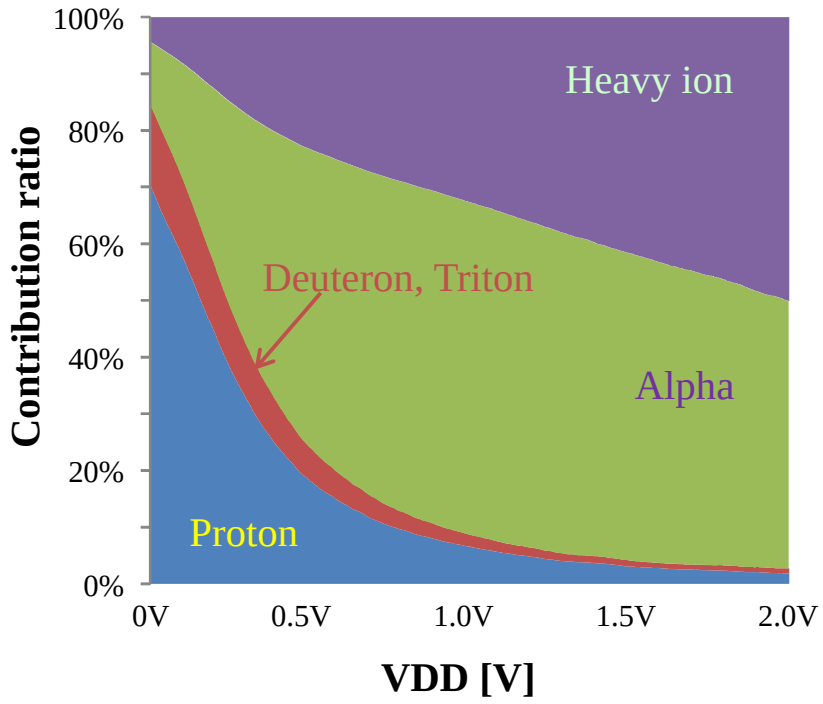


Fig. 7.9 Contribution ratio of each particle in SRAM.

50 μm is more than 90%. On the other hand, the thickness of the metal layer is less than 20 μm, and the width of Si surrounding the SRAM cells is 50 μm in the simulation as shown in Figure 7.8. Meanwhile, the amount of charge deposited increases sharply just before the proton stopping, i.e. following Bragg-Curve, as shown in Figure 7.14. Figure 7.13 and Figure 7.14 indicate that the secondary protons generated even hundreds micrometers to a few millimeters away from the transistor of interest can contribute to SEU rate at ultra-low voltage. Simulating the entire DUT including silicon-die, package and printed circuit board (PCB) is necessary to fully consider such proton contributions.

The second possible reason is the contribution of low-energy neutrons, which was not considered in the simulation. The simulation in this chapter assumed a neutron source that reproduced 1 MeV to 400 MeV RCNP spectrum and neutrons below 1 MeV were not included, because the information on the neutron flux below 1 MeV at RCNP was not available. Further investigations on the possible reasons are included in our future work.

7.5 Conclusions

SEU rate of ultra-low voltage SRAM was evaluated through neutron and alpha irradiation tests and simulations. The measurement results show that neutron induced SEU rate at ultra-low voltage dramatically increases, and SEU rate at around 0.2 V is by two orders of magnitude higher than that at 1.0 V. This result supported by simulation indicates that secondary protons generated by nuclear reaction with neu-

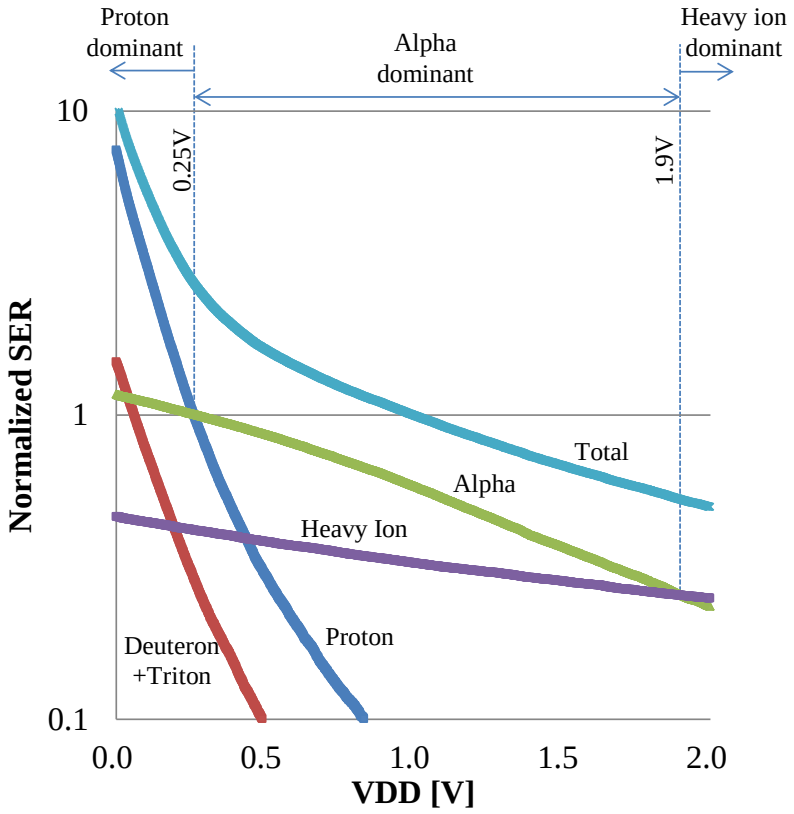


Fig. 7.10 Calculated SEU rate originating from each secondary particle in SRAM. These SEU rates are normalized by the total SEU rate at 1.0 V as 1.

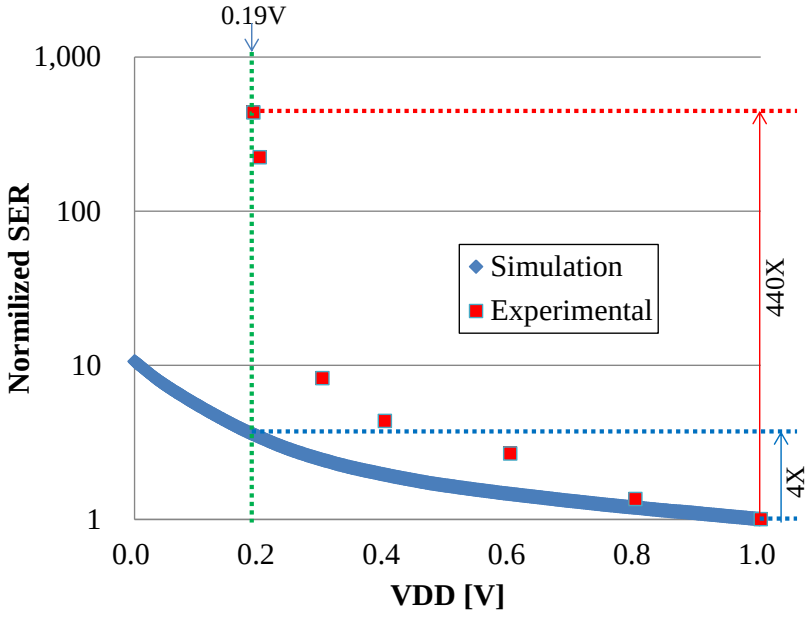


Fig. 7.11 SEU rate comparison between measurement and simulation.

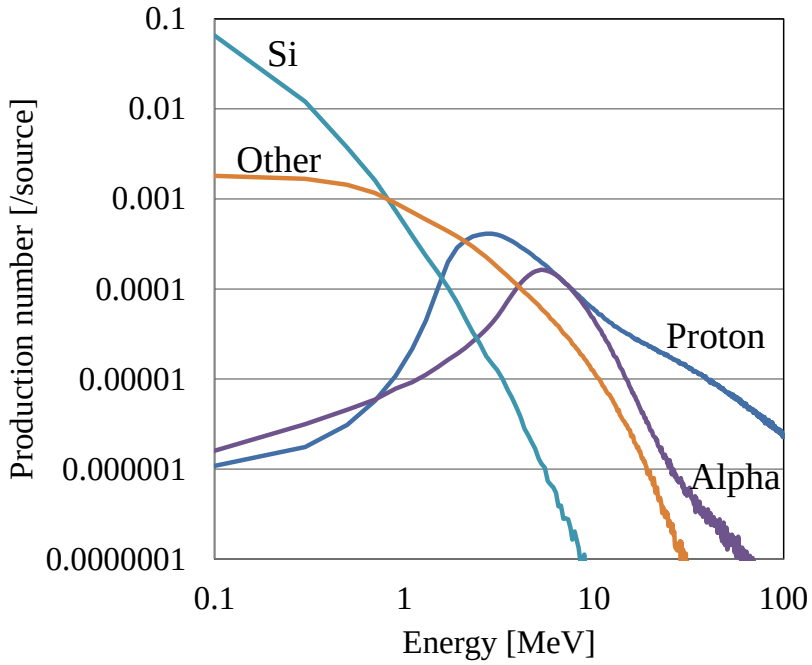


Fig. 7.12 Production numbers of proton, alpha, Si and other heavy ions calculated with PHITS as a function of particle energy. A neutron beam having RCNP energy spectrum is given to Si substrate.

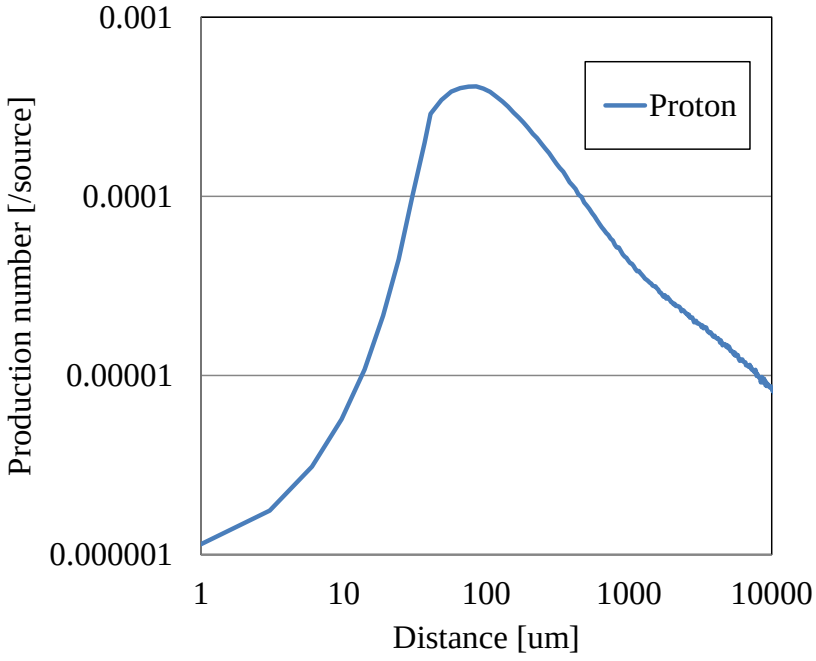


Fig. 7.13 Production probability as a function of proton travel distance calculated from SRIM.

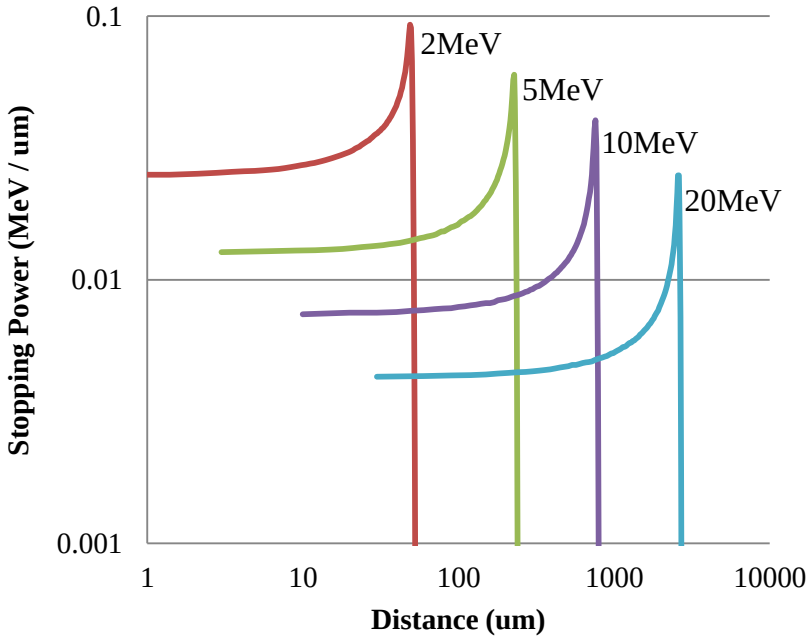


Fig. 7.14 Stopping power of 2.0, 5.0 and 10 MeV protons on silicon, calculated by SRIM. The stopping power and the flight length of proton are lower and shorter than those of alpha, respectively, in comparison with Fig. 1.2.

tron collision are contributing to SEU rate of ultra-low voltage SRAM dominantly in terrestrial environment.

In future technologies, SEU rate could dramatically increase at low voltage since Qcrit also decreases with technology advancing. In SRAMs manufactured with finer lithography such as 16 nm or finer, the contribution of proton direct ionization would be observed even at a voltage much higher than 0.2 V. In this case, soft error can be a primary design concern for both high performance computing based on near-threshold computing [180] and low power consumer and biomedical products.

Chapter 8

Conclusions

Soft error in microprocessors used for mission critical applications and HPC is a crucial issue in terms of both reliability and performance. This thesis focused on soft error occurring in microprocessors manufactured with conventional bulk CMOS technology in terrestrial environment, and discussed how to mitigate soft error for improving the reliability of microprocessors and extending the MTBF of HPC systems. With this motivation, this thesis studied soft error mitigation techniques and clarified their error mitigation efficiency through neutron and alpha irradiation tests.

To identify the key factors that determine the microprocessor reliability, this thesis first discussed the scaling trend of SRAM and FF SERs and their contribution to SPARC V9 processor reliability. For this discussion, neutron and alpha irradiation experiments were performed on SRAMs manufactured in 350, 250, 180, 130, 90, 65, 55, 45, 40, 28 and 20 nm and FF in 65, 45, 28 and 20 nm bulk CMOS technologies. SRAM SER per bit reached the maximum at 180 nm for neutron and at 250 nm for alpha. The evaluations on various 90 nm SRAMs show that process conditions and the number of access ports could change SRAM SER by up to 75%. The decrease in FF SER per bit is more significant compared to that of SRAM. Consequently, the chip-level processor SER remains at the same level from 65 to 20 nm both in SRAM and FF without soft error mitigation techniques. This chip level estimation gave an implication that MBU should be mitigated for higher reliability in 65 nm. Also, SBU and MBU in FF should be reduced because HIR cannot eliminate all the SBU in addition to MBU occurring in FFs. According to these observations, this thesis tackled with MBU in SRAM and SBU and MBU in FF, and developed techniques to mitigate them.

In addition, this thesis investigated SEU rate in ultra-low voltage operation for future processors. Achieving low power operation of electron devices is a vital requirement for large scale systems, and further aggressive power reduction will be demanded in future processor designs. To assess the reliability of such future processors, SEU rate of ultra-low voltage SRAM was evaluated through neutron and alpha irradiation tests and simulations. The test results show that neutron induced SEU rate at ultra-low voltage dramatically increases. The SEU rate at around 0.2 V is by two orders of magnitude higher than that at 1.0 V. This result supported by simulation indicates that secondary protons generated by nuclear reaction with neutron collision are contributing to SEU rate of ultra-low voltage SRAM dominantly in

terrestrial environment.

To mitigate SRAM oriented reliability degradation, techniques for mitigating MBU and SEL in SRAM were developed. Prior to the development of the MBU mitigation technique, the impact of well structure on SRAM SER was investigated through alpha and neutron irradiation tests on SRAM SER. Well depth affected the SEU rate for alpha-induced soft errors at low voltage. PBA contributed to alpha- and neutron-induced MBUs both in triple-well and double-well. MBU was observed in the SEC-ECC SRAMs with 4 or smaller col-MUX both in double- and triple-well. Based on these measurement results, this thesis proposed an MBU mitigation technique that used DNW in contrast to the common practice that DNW raises the SER. The proposed technique used narrow DNW for isolating the wells of cells that were simultaneously selected. The experimental results showed that the proposed MBU mitigation technique with narrow DNW could reduce neutron-induced MBU. This technique has no area overheads. In addition, it generally involves no performance or power overheads.

Next, this thesis discussed SEL immunity of SRAM with various well configurations through neutron irradiation tests, and revealed that DPW, DNW and highly doped well reduced SEL rate, where DPW was newly introduced for SEL mitigation in this thesis. These three configurations for SEL prevention have different features. Increasing well dose in double-well structure can mitigate SEL without SEU increase, and at most 60% SEL reduction could be obtained by process tuning. DNW is an off-the-shelf solution, but it involves an undesirable side effect of SEU increase. DPW is the most effective solution to eliminate SEL occurrence, and no SEL was observed in our irradiation tests. Furthermore DPW is helpful to reduce SEU as well. While adoption of DPW needs an extra cost to newly construct a DPW process, the DPW process development itself is not technically difficult. The SEL prevention by DPW can be expected to be more efficient than that by CLD.

After the discussion on SRAM issues (MBU and SEL), the discussion moved to the soft error in logic circuits, i.e. MBU and SBU in sequential elements. First, this thesis proposed a technique for mitigating MBU in MBL by inserting well-slits between latch bit cells. The area overhead is only 5.4% as an MBL macro. The MBLs with and without well-slit were designed in a test chip, and neutron irradiation test was performed on the test chip. Neutron irradiation tests demonstrated that the proposed mitigation technique did not change SBU rate and consequently rare HIR execution did not degrade processor performance. In this experiment, MBUs, which cannot be detected by the checker and predictor, were not observed in the proposed MBL even under sixty-hour accelerated irradiation. This test result clearly shows that the proposed mitigation technique can contribute to robustness improvement of MBL.

Next, this thesis discussed SBU in sequential elements. SEILA was proposed for SBU mitigation in sequential elements which adopted MHC (DHC, THC) design and DCB technique. SEILAs were designed with 65 nm, 28 nm and 20 nm technologies, and were tested with neutron and alpha irradiations. The rest result on the 65 nm SEILA designed with DHC and DCB showed that the DHC reduced the SEU rate by 99.3% and the DCB could eliminate the SEU occurrence due to SETLC. For 28 nm technology, SEILA was designed with DHC. The SEU rate in the 28 nm DHC-

Table. 8.1 List of countermeasures.

Circuit element	SBU	MBU	SEL
SRAM	• ECC	• Narrow-DNW (Chapter 3	• DPW (Chapter 4)
Sequential element	• Algorithm check and HIR • SEILA (Chapter 6)	• Well-slit (Chapter 5) • FF alternative placement [115]	Negligible

SEILA was comparable with that of the 65 nm DHC-SEILA. The SEU rate in the 28 nm DHC-SEILA was not low enough since more latches were used in the 28 nm microprocessor than in the 65 nm one. SEILA in 20 nm technology was designed with THC for achieving higher SEU prevention than that in 28 nm technology. The neutron induced SEU rate was 14 times lower in the 20 nm THC-SEILA than in the 28 nm DHC-SEILA. In the alpha irradiation test, no error was observed and the SEU rate was less than 1 FIT/Mbit with 90% statistically probability for 0.001 alpha/hour/cm^2.

These investigations on soft error and the proposed soft error mitigation techniques contributed to highly reliable microprocessor design. Table 8.1 summarizes the developed mitigation techniques. In SRAM, narrow DNW mitigates MBU and DPW reduces SEL. In sequential elements, well-slit and SEILA contribute to MBU and SBU reduction, respectively. The proposed mitigation techniques in process and circuit layer accompanied with architectural techniques such as ECC and HIR with algorithmic checking can cover all critical soft error issues in current microprocessor design. Thus, this thesis contributes to highly reliable operations of microprocessors manufactured with bulk CMOS technology.

This thesis discussed the reliability of microprocessors manufactured with bulk CMOS transistor, which is sensitive to soft error compared to FinFET and SOI transistors. Some of soft error mitigation techniques proposed in this thesis are expected to be still helpful to improve the reliability of future microprocessors manufactured with FinFET or SOI. However, the further pursuit of energy efficiency would demand more effort for the soft error mitigation, because drastic power reduction of microprocessors is mandatory for huge super computer system like exa-scale computing. It is getting more and more difficult to achieve the high reliability by traditional mono-layer approach. Cross-layer reliability consideration and improvement covering from device-level, transistor-level, circuit-level, architecture-level, and software-level techniques will be crucially important, and the cross-layer optimization for reliability enhancement is the direction of our future works.

Appendix A

Geometry factor calculation for alpha irradiation test

TThis appendix explains how to calculate geometry factor (GF) for alpha irradiation tests. Geometry factor is defined as the ratio of the dose flux on a test die to the alpha source flux as introduced in Section 1.2.4. Section A.1 explains the derivation of the GF for alpha irradiation tests. Section A.2 exemplifies a Perl code for calculating the GF, and Section A.3 gives examples of GF calculation.

A.1 Geometry factor derivation

The computation of the GF is explained using Figure A.1. Let us assume there is a single-side alpha source whose radiation dosage density is A_1 and area is S_1 (marked by "1" in Figure A.1). In this case, the number of alpha particles emitted from the source is $2S_1A_1$. In alpha irradiation tests, the alpha source and the DUT chip

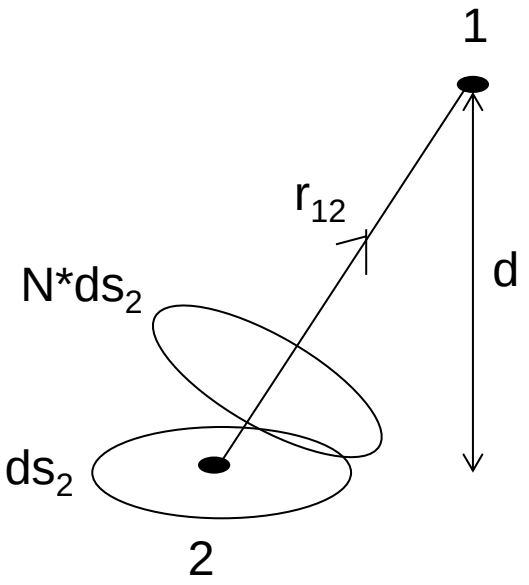


Fig. A.1 Locations of alpha source ("1") and DUT chip ("2").

(marked by "2" in Figure A.1) face each other, and their surfaces are in parallel. The minimum distance between the surfaces is d. Let us denote arbitrary positions on the alpha source and the chip as $\mathbf{r}_1$ and $\mathbf{r}_2$, respectively. In this configuration, if the chip is located distantly from the alpha source, the number of alpha particles that arrive at the chip decreases. In addition, the number of injected alpha particles varies depending on the location within the chip. From now, the density of radiation dosage at $\mathbf{r}_2$ is denoted as $dA_2(\mathbf{r}_2)$. The radiation dosage that arrives at tiny area, dS_2, on the chip is given by

$$dA_2(\mathbf{r}_2)dS_2 = \frac{ndS_2}{4\pi {r_{21}}^2} 2A_1 dS_1 \quad , \tag{A.1}$$

where $2A_1 dS_1$ represents the radiation dosage emitted from the tiny area, S_1, on the alpha source. r_{21} is $|\mathbf{r}_2 - \mathbf{r}_1|$, and n is d/r_{21}. In this equation, ndS_2 represents the area normal to the vector of $\mathbf{r}_2 - \mathbf{r}_1$, and $\frac{ndS_2}{4\pi {r_{21}}^2}$ is the surface area of a sphere whose diameter is r_{21}. Here, let us define the axes of the three-dimensional space to satisfy $\mathbf{r}_1 = (x_1, y_1, 0)$ and $\mathbf{r}_2 = (x_2, y_2, d)$. In this case, Eq. (A.1) can be rewritten as

$$dA_2(x_2, y_2) = \frac{A_1}{2\pi} \frac{d}{{r_{21}}^3} dx_1 dy_1 \quad . \tag{A.2}$$

In order to obtain the density of radiation dosage that is irradiated from the entire area of the alpha source, Eq. (A.2) is integrated over the total area of the alpha source.

$$\begin{aligned} A_2(x_2, y_2) &= A_1 \left[\frac{d}{2\pi} \int dx_1 \int dy_1 \frac{1}{{r_{21}}^3} \right] \\ &\equiv A_1 g(x_2, y_2) \quad , \end{aligned} \tag{A.3}$$

where $g(x_2, y_2)$ is defined as geometry factor. The average value of geometry factor over the chip is given by

$$\bar{g} = \frac{1}{S_2} \int dx_1 \int dy_1 g(x_2, y_2) \quad ,$$

where S_2 is the area of the chip. If the alpha source is assumed to have a square shape, the integration of the geometry factor can be performed.

$$g(x_2, y_2) = \frac{d}{2\pi} \int_{-L_x}^{L_x} dx_1 \int_{-L_y}^{L_y} dy_1 \left[(x_2 - x_1)^2 + (y_2 - y_1)^2 + d^2 \right]^{-3/2} \quad , \tag{A.4}$$

where $2L_x$ and $2L_y$ are the lengths of respective sides of the chip along the horizontal and longitudinal axes, respectively. On the other hand, if the radiation source has a round shape, the integration of the geometric factor is solved using polar coordinates of which the center of DUT chip is the origin.

$$g(x_2, y_2) = \frac{d}{2\pi} \int_0^{r_{\max}} dr \int_0^{2\pi} d\theta \left[(x_2 - r\cos\theta)^2 + (y_2 - r\sin\theta)^2 + d^2 \right]^{-3/2} r \quad , \tag{A.5}$$

where r and θ are valuables in the polar coordinates, and $r_{\max}$ is the radius of the radiation source. Using Eqs. (A.4) and (A.5), the radiation dosage at each observation point on the chip can be computed.

A.2 Perl code for GF calculation

This section gives a Perl code for calculating the geometry factor. This code can be used for using square and round shape alpha sources.

```
#! /usr/bin/perl
##########################################################3
$mesh1 =100; #for source
$mesh2 = 50; #for chip
$shape = 1; #1:round  2:square
$pi = 3.14159265358979323846264338327950288419 72;
$total_charge=0;
#distance between source and chip
$dd = 1.5;
########round########
$r1min = 0.00; #radius for round shape
$r1max = 4.0;
$theta1min = 0.0*$pi; # angle for round shape
$theta1max = 2.0*$pi;
########square########
$x1min = -10;# coodinate for square
$y1min = -10;
$x1max = 10;
$y1max = 10;
########shape of chip########
$x2min = -1.0; #square
$y2min = -1.0;
$x2max = 3.0;
$y2max = 3.0;
############################################################
# set fundamental
############################################################
$dr1 = ($r1max - $r1min)/$mesh1;
$dtheta1 = ($theta1max - $theta1min)/$mesh1;
#
$dx1 = ($x1max - $x1min)/$mesh1;
$dy1 = ($y1max - $y1min)/$mesh1;
#
$dx2 = ($x2max - $x2min)/$mesh2;
$dy2 = ($y2max - $y2min)/$mesh2;
############################################################
# main loop
############################################################
for(my $ii=0; $ii < $mesh2; $ii++){
$x2 = $x2min + $ii*$dx2;
for(my $jj=0; $jj < $mesh2; $jj++){
$y2 = $y2min + $jj*$dy2;
$integral = 0;
```

```
############
if($shape == 1){&ROUND;}
elsif($shape == 2){&SQUARE;}
print "$x2 $y2 $integral\n";
$total_charge += $integral;
}
print "\n";
}
$total_charge /= ($mesh2*$mesh2);
print "\#$total_charge\n";
############################################################
sub ROUND{
for(my $mm=0; $mm < $mesh1; $mm++){
$r1 = $r1min + $mm*$dr1;
for(my $nn=0; $nn < $mesh1; $nn++){
$theta1 = $theta1min + $nn*$dtheta1;
$x1 = $r1*cos($theta1);
$y1 = $r1*sin($theta1);
$integral = $integral + (($x1-$x2)**2 + ($y1-$y2)**2 + $dd**2)**(-3/2)*$r1;
}
}
$integral = 2*$dd/(4.0*$pi)*$integral*$dr1*$dtheta1;
}
############################################################
sub SQUARE{
for(my $mm=0; $mm < $mesh1; $mm++){
$x1 = $x1min + $mm*$dx1;
for(my $nn=0; $nn < $mesh1; $nn++){
$y1 = $y1min + $nn * $dy1;
$integral = $integral +  (($x1-$x2)**2 + ($y1-$y2)**2 + $dd**2)**(-3/2);
}
}
$integral = 2*$dd/(4.0*$pi)*$integral*$dx1*$dy1;
}
############################################################-
```

A.3 Calculation example

This section gives examples of the GF calculation.

First example of Figure A.2 shows GF profiles when the shape and size of the alpha source is changed. GFs are calculated for the following four alpha sources: (a) 5 mm $\times$ 5 mm square, (b) 20 mm $\times$ 20 mm square, (c) 5 mm ϕ round, and (d) 20 mm ϕ round shapes. The distance between the alpha source and the die is 1 mm. The minimum and maximum GFs are 0.2 and 0.7 with (a), and 0.903 and 0.911 with (b), and the difference between the minimum and maximum is much different. The similar tendency is found in (c) and (d). These calculation results indicate that larger source is better to obtain uniform radiation dosage in alpha irradiation test.

Second example of Figure A.2 shows GF profiles when the centers of the die and the

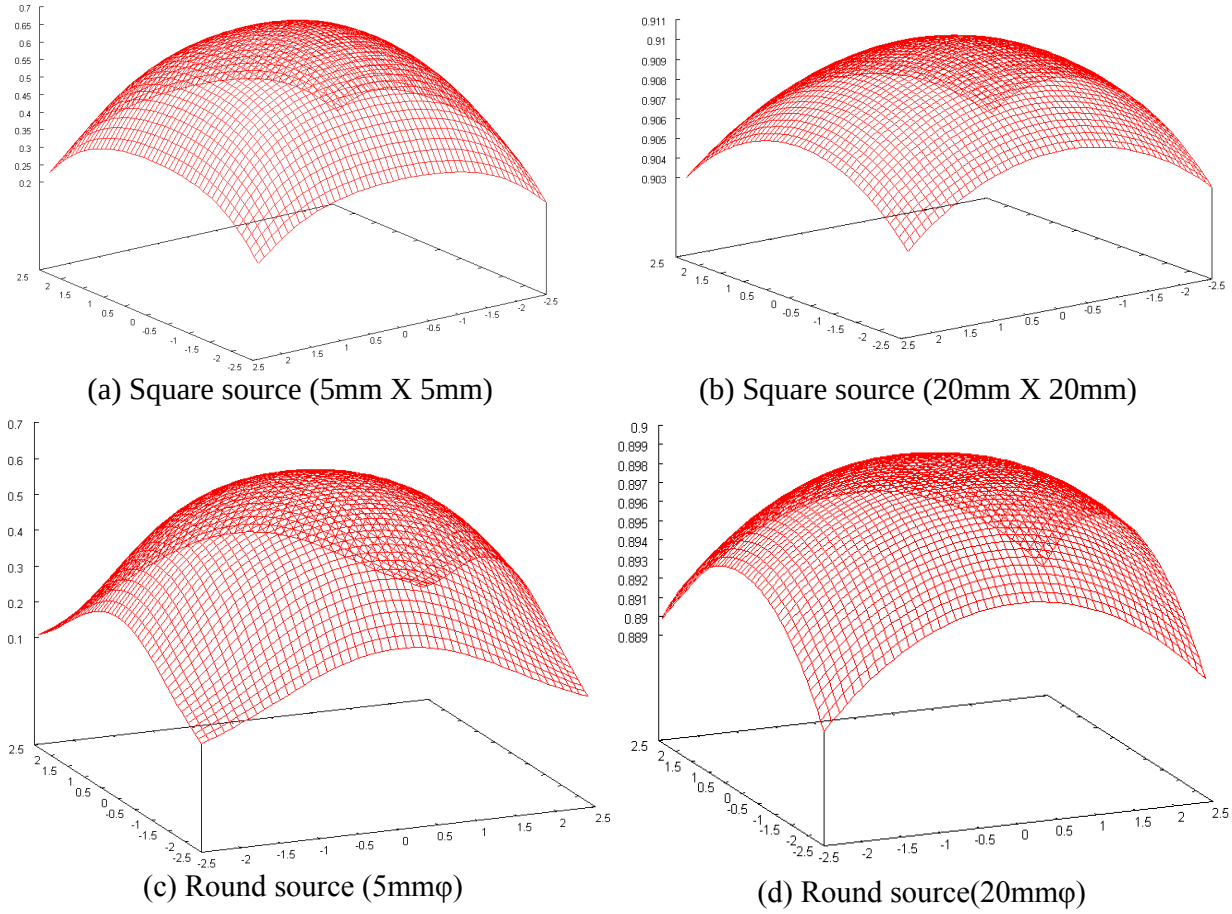
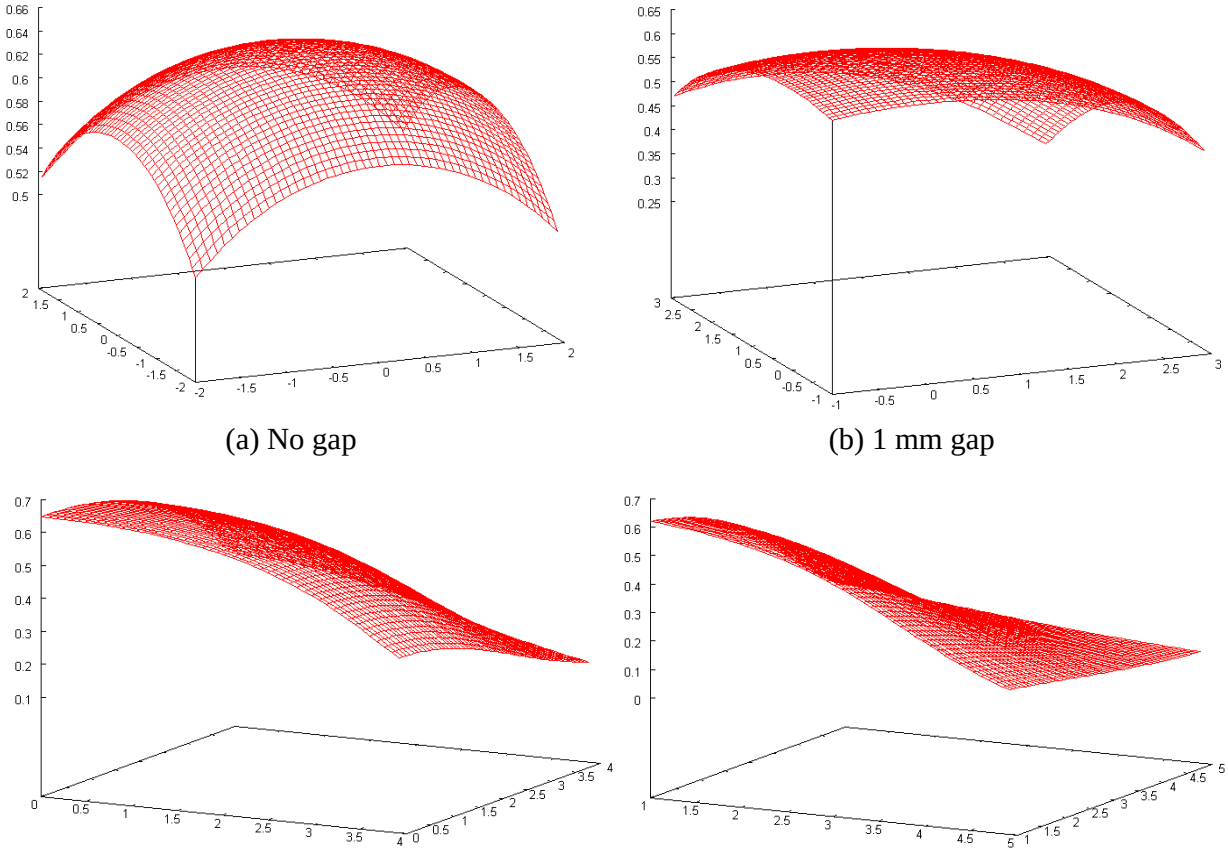


Fig. A.2 Alpha dosage profiles on the die (5 mm × 5 mm) when using alpha sources of (a) 5 mm × 5 mm square, (b) 20 mm × 20 mm square, (c) 5 mm ϕ round, (d) 20 mm ϕ round shapes. The distance between the alpha source and the die is 1 mm. The scale of X and Y axes are millimeter, and the Z axis represents GF (non-dimension).

source are misaligned. The misalignment distance between the centers of the alpha source and die is (a) 0 mm, (b) 1 mm, (c) 2 mm and (d) 3 mm. The die size is 4 mm × 4 mm square and the alpha source has 8 mm ϕ round shape. The distance between the alpha source and the die is 1.5 mm. These calculation results indicate that the accurate alignment of the alpha source and the die is important when using a small alpha source in alpha irradiation tests.



(a) No gap (b) 1 mm gap

(c) 2 mm gap (d) 3 mm gap

Fig. A.3 Alpha dosage profiles on the die (4 mm × 4 mm) when using a 8 mm ϕ alpha source. The centers of the source and die are misaligned, and the distance between the centers is (a) 0 mm, (b) 1 mm, (c) 2 mm and (d) 3 mm. The distance between the alpha source and the die is 1.5 mm. The scale of X and Y axes are millimeter and the Z axis represents GF (non-dimension).

Bibliography

[1] J. F. Ziegler and J. P. Biersack, *Treatise on Heavy-Ion Science*. Boston, MA: Springer US, Jan. 1985.

[2] "JANIS 4.0 (http://www.oecd-nea.org/janis/)."

[3] "International Technology Roadmap for Semiconductors (ITRS) 2011 edition," 2011.

[4] JEDEC, "Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray Induced Soft Error in Semiconductor Devices: JESD89A," *JEDEC Sold State Technol. Assoc.*, pp. 1–85, 2006.

[5] ISO, "ISO26262: Road vehicles - Functional safety," tech. rep., 2011.

[6] N. Kimizuka, K. Yamaguchi, K. Imai, T. Iizuka, C. Liu, R. Keller, and T. Horiuchi, "NBTI enhancement by nitrogen incorporation into ultrathin gate oxide for 0.10-μm gate CMOS generation," in *2000 Symp. VLSI Technol. Dig. Tech. Pap. (Cat. No.00CH37104)*, pp. 92–93, IEEE, 2000.

[7] H. Mori, Y. Ikeda, T. Kato, T. Uemura, and H. Matsuyama, "Lifetime evaluation on AC stress in High-K / Metal-Gate with Using Dual-Pulsed-Test-System," in *Int. Conf. Solid State Devices Mater.*, pp. 122–123, 2012.

[8] V. Huard, F. Monsieur, G. Ribes, and S. Bruyere, "Evidence for hydrogen-related defects during NBTl stress in p-MOSFETs," in *2003 IEEE Int. Reliab. Phys. Symp. Proceedings, 2003. 41st Annu.*, pp. 178–182, IEEE, 2003.

[9] Y. Ikeda, H. Mori, T. Kato, T. Uemura, M. Yoshida, M. Onoda, and H. Matsuyama, "Investigation of BTI degradation in LDMOS transistors," in *Int. Conf. Solid State Devices Mater.*, pp. 454–455, 2012.

[10] E. Takeda, K. Ikuzaki, H. Katto, Y. Ohji, K. Hinode, A. Hamada, T. Sakuta, T. Funabiki, and T. Sasaki, "VLSI reliability challenges: from device physics to wafer scale systems," *Proc. IEEE*, vol. 81, pp. 653–674, May 1993.

[11] E. Li, E. Rosenbaum, L. Register, J. Tao, and P. Fang, "Hot carrier induced degradation in deep submicron MOSFETs at 100° C," in *2000 IEEE Int. Reliab. Phys. Symp. Proceedings. 38th Annu. (Cat. No.00CH37059)*, pp. 103–107, IEEE, 2000.

[12] E. Wu, J. Aitken, E. Nowak, A. Vayshenker, P. Varekamp, G. Hueckel, J. McKenna, D. Harmon, L.-K. Han, C. Montrose, and R. Dufresne, "Voltage-dependent voltage-acceleration of oxide breakdown for ultra-thin oxides," in *Int. Electron Devices Meet. 2000. Tech. Dig. IEDM (Cat. No.00CH37138)*, pp. 541–544, IEEE, 2000.

[13] J. McPherson and H. Mogul, "Disturbed bonding states in SiO/sub 2/ thin-films and their impact on time-dependent dielectric breakdown," in *1998 IEEE Int. Reliab. Phys. Symp. Proc. 36th Annu. (Cat No 98CH36173) RELPHY-98*,

pp. 47–56, IEEE, 1998.

[14] J. W. McPherson, "A model for stress-induced metal notching and voiding in very large-scale-integrated Al-Si (1%) metallization," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 5, p. 1321, Sept. 1987.

[15] E. Ogawa, J. McPherson, J. Rosal, K. Dickerson, T.-C. Chiu, L. Tsung, M. Jain, T. Bonifield, J. Ondrusek, and W. McKee, "Stress-induced voiding under vias connected to wide Cu metal leads," in *2002 IEEE Int. Reliab. Phys. Symp. Proceedings. 40th Annu. (Cat. No.02CH37320)*, pp. 312–321, IEEE, 2002.

[16] P. Ho, K.-D. Lee, E. Ogawa, X. Lu, H. Matsuhashi, V. Blaschke, and R. Augur, "Electromigration reliability of Cu interconnects and effects of low K dielectrics," in *Dig. Int. Electron Devices Meet.*, pp. 741–744, IEEE, 2002.

[17] J. R. Black, "Mass Transport of Aluminum by Momentum Exchange with Conducting Electrons," in *6th Annu. Reliab. Phys. Symp.*, pp. 148–159, IEEE, Nov. 1967.

[18] F. Chen, F. Ungar, A. Fischer, J. Gill, A. Chinthakindi, T. Goebel, M. Shinosky, D. Coolbaugh, V. Ramachandran, Y. Siew, E. Kaltalioglu, S. Kim, and K. Park, "Reliability Characterization of BEOL Vertical Natural Capacitor using Copper and Low-k SiCOH Dielectric for 65nm RF and Mixed-Signal Applications," in *2006 IEEE Int. Reliab. Phys. Symp. Proc.*, pp. 490–495, IEEE, 2006.

[19] N. Suzumura, S. Yamamoto, D. Kodama, K. Makabe, J. Komori, E. Murakami, S. Maegawa, and K. Kubota, "A New TDDB Degradation Model Based on Cu Ion Drift in Cu Interconnect Dielectrics," in *2006 IEEE Int. Reliab. Phys. Symp. Proc.*, pp. 484–489, IEEE, 2006.

[20] JEITA, "JEITA SER Testing Guideline," tech. rep., Tokyo, 2005.

[21] IEC, "Part: 38 Soft Error Test Method for Semiconductor Devicewith Memory," tech. rep., 2008.

[22] IEC, "Process management for avionics - Atmospheric radiation effects - Part 1: Accommodation of atmospheric radiation effects via single event effects within avionics electronic equipment — IEC Webstore — Publication Abstract, Preview," tech. rep., 2012.

[23] Automotive Electronics Council, "Failure Mechanism Based Stress Test Qualification for Integrated Circuits," tech. rep., 2007.

[24] E. Ibe, T. Toba, K. Shimbo, and H. Taniguchi, "Fault-based reliable design-on-upper-bound of electronic systems for terrestrial radiation including muons, electrons, protons and low energy neutrons," in *2012 IEEE 18th Int. On-Line Test. Symp.*, pp. 49–54, IEEE, June 2012.

[25] S. R. Messenger, G. P. Summers, E. A. Burke, R. J. Walters, and M. A. Xapsos, "Modeling solar cell degradation in space: A comparison of the NRL displacement damage dose and the JPL equivalent fluence approaches," *Prog. Photovoltaics Res. Appl.*, vol. 9, pp. 103–121, Mar. 2001.

[26] P. Ma, T.P. and Dressendorfer, *Ionizing Radiation Effects in MOS Devices and Circuits.* John Wiley & Sons, 1989.

[27] T. R. Oldham, *Ionizing Radiation Effects in MOS Oxides.* Singapore: World Scientific, 1999.

[28] T. Oldham and F. McLean, "Total ionizing dose effects in MOS oxides and devices," *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 483–499, June 2003.

[29] H. J. Barnaby, "Total-Ionizing-Dose Effects in Modern CMOS Technologies," *IEEE Trans. Nucl. Sci.*, vol. 53, pp. 3103–3121, Dec. 2006.
[30] T. Uemura and M. Hashimoto, "Investigation of Single Event Upset and Total Ionizing Dose in FeRAM for Medical Electronic Tag," in *2015 IEEE Int. Reliab. Phys. Symp.*, p. (in press), 2015.
[31] T. May and M. Woods, "Alpha-particle-induced soft errors in dynamic memories," *IEEE Trans. Electron Devices*, vol. 26, pp. 2–9, Jan. 1979.
[32] Y. Tosaka and S. Satoh, "Simulation of multiple-bit soft errors induced by cosmic ray neutrons in DRAMs," in *2000 Int. Conf. Simul. Semicond. Process. Devices (Cat. No.00TH8502)*, pp. 265–268, IEEE, 2000.
[33] B. Schroeder, E. Pinheiro, and W. Weber, "DRAM errors in the wild: a large-scale field study," *ACM SIGMETRICS Perform. Eval. Rev.*, vol. 37, pp. 193–193–204–204, June 2009.
[34] E. Ibe, S. Chung, S. Wen, H. Yamaguchi, Y. Yahagi, H. Kameyama, S. Yamamoto, and T. Akioka, "Spreading Diversity in Multi-cell Neutron-Induced Upsets with Device Scaling," in *IEEE Cust. Integr. Circuits Conf. 2006*, pp. 437–444, IEEE, Sept. 2006.
[35] J. Furuta, K. Kobayashi, and H. Onodera, "Impact of cell distance and well-contact density on neutron-induced Multiple Cell Upsets," in *2013 IEEE Int. Reliab. Phys. Symp.*, pp. 6C.3.1–6C.3.4, IEEE, Apr. 2013.
[36] J. N. Bradford, "Single Event Error Generation by 14 MeV Neutrons Reactions in Silicon," *IEEE Trans. Nucl. Sci.*, vol. 27, no. 6, pp. 1479–1484, 1980.
[37] H. Kobayashi, K. Shiraishi, H. Tsuchiya, M. Motoyoshi, H. Usuki, Y. Nagai, K. Takahisa, T. Yoshiie, Y. Sakurai, and T. Ishizaki, "Soft errors in SRAM devices induced by high energy neutrons, thermal neutrons and alpha particles," in *Dig. Int. Electron Devices Meet.*, pp. 337–340, IEEE, 2002.
[38] M. Olmos, R. Gaillard, A. Overberghe, J. Beaucour, S. Wen, and S. Chung, "Investigation of Thermal Neutron Induced Soft Error Rates in Commercial Srams with 0.35 μm to 90 nm Technologies," in *2006 IEEE Int. Reliab. Phys. Symp. Proc.*, pp. 212–216, IEEE, 2006.
[39] S. Wen, R. Wong, M. Romain, and N. Tam, "Thermal neutron soft error rate for SRAMS in the 90NM-45NM technology range," in *2010 IEEE Int. Reliab. Phys. Symp.*, pp. 1036–1039, IEEE, 2010.
[40] Y. Fang and A. S. Oates, "Thermal Neutron-Induced Soft Errors in Advanced Memory and Logic Devices," *IEEE Trans. Device Mater. Reliab.*, vol. 14, pp. 583–586, Mar. 2014.
[41] J. Park, G. Kim, M. Zhang, K. Park, M. Lee, I. Kim, J. Bae, S. Pae, J. Choi, D. Shin, N.-I. Lee, and K. Kim, "Development of Thermal Neutron SER-Resilient High-K/Metal Gate Technology," in *2013 IEEE Int. Reliab. Phys. Symp. Proc.*, 2014.
[42] T. Sato and K. Niita, "Analytical Functions to Predict Cosmic-Ray Neutron Spectra in the Atmosphere," July 2009.
[43] T. Sato, H. Yasuda, K. Niita, A. Endo, and L. Sihver, "Development of PARMA: PHITS-based Analytical Radiation Model in the Atmosphere," Oct. 2009.
[44] Y. Tosaka, R. Takasu, T. Uemura, H. Ehara, H. Matsuyama, S. Satoh, A. Kawai, and M. Hayashi, "Simultaneous measurement of soft error rate of 90 nm CMOS

SRAM and cosmic ray neutron spectra at the summit of Mauna Kea," in *2008 IEEE Int. Reliab. Phys. Symp.*, pp. 727–728, IEEE, Apr. 2008.

[45] R. Takasu, Y. Tosaka, H. Matsuyama, H. Ehara, Y. Kataoka, A. Kawai, M. Hayashi, and Y. Murai, "Measurement of Cosmic Ray Neutron Spectra in the Energy Region of 20-200 MeV at the Summit of Mauna Kea and Several Different Altitudes," in *Proc. 30th Int. Cosm. Ray Conf. July 3 - 11*, vol. 1, 2008.

[46] R. L. Bramblett, R. I. Ewing, and T. Bonner, "A new type of neutron spectrometer," *Nucl. Instruments Methods*, vol. 9, pp. 1–12, Oct. 1960.

[47] T. Kato, R. Akano, T. Uemura, Y. Watanabe, and H. Matsuyama, "Neutron Shielding Effect of Stacked Servers and Its Impact on Reduction of Soft Error Rate," *IEEE Trans. Nucl. Sci.*, vol. 61, pp. 3408–3415, Dec. 2014.

[48] M. Reginatto and P. Goldhagen, "MAXED, a computer code for maximum entropy deconvolution of multisphere neutron spectrometer data," *Health Phys.*, vol. 77, no. 5, pp. 579–583, 1999.

[49] T. Sato, K. Niita, N. Matsuda, S. Hashimoto, Y. Iwamoto, S. Noda, T. Ogawa, H. Iwase, H. Nakashima, T. Fukahori, K. Okumura, T. Kai, S. Chiba, T. Furuta, and L. Sihver, "Particle and Heavy Ion Transport code System, PHITS, version 2.52," *J. Nucl. Sci. Technol.*, vol. 50, pp. 913–923, Sept. 2013.

[50] W. H. Bragg and R. Kleeman, "XXXIX. On the α particles of radium, and their loss of range in passing through various atoms and molecules," *Philos. Mag. Ser. 6*, vol. 10, pp. 318–340, Sept. 1905.

[51] EUR, "DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment," tech. rep., 2003.

[52] A. Masuda, M. Ishikawa, M. Kohinata, M. Mashima, K. Tsuji, and T. Shinkawa, "Development of immersion sn plating process for low-alpha bump formation," in *2008 58th Electron. Components Technol. Conf.*, pp. 1654–1658, IEEE, May 2008.

[53] M. S. Gordon, K. P. Rodbell, H. H. K. Tang, P. Ronsheim, Z. Zhu, S. E. Rauch, B. D. McNally, and S. Coleman, "Ultra-Low Emissivity Alpha-Particle Detection," *IEEE Trans. Nucl. Sci.*, vol. 59, pp. 3101–3109, Dec. 2012.

[54] M. S. Gordon, D. F. Heidel, K. P. Rodbell, B. Dwyer-McNally, and W. K. Warburton, "An Evaluation of An Ultralow Background Alpha-Particle Detector," *IEEE Trans. Nucl. Sci.*, vol. 56, pp. 3381–3386, Dec. 2009.

[55] R. Takasu, Y. Tosaka, H. Fukuda, and Y. Karaoka, "A novel method for accurately estimating alpha-induced soft error rates," in *2005 IEEE Int. Reliab. Phys. Symp. 2005. Proceedings. 43rd Annu.*, pp. 230–233, IEEE, 2005.

[56] H. Mori, T. Uemura, H. Matusyama, T. Yamazaki, and T. Soeda, "Detection Technique with Alpha-tracking and Emissivity Comparison," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3438–3442, 2014.

[57] Y. Tosaka, R. Takasu, H. Ehara, T. Uemura, H. Oka, S. Satoh, N. Matsuoka, and K. Hatanaka, "Technological Trends of Soft Error Estimation Based on Accurate Estimation Method," *Jpn. J. Appl. Phys.*, vol. 45, pp. 3185–3188, Apr. 2006.

[58] W. K. Warburton and B. Dwyer-McNally, "Electronic background rejection in a

new ultra-low background alpha-particle counter," *Nucl. Instruments Methods Phys. Res. Sect. B Beam Interact. with Mater. Atoms*, vol. 263, no. 1, pp. 221–224, 2007.

[59] B. G. Cartwright and E. K. Shirk, "A Nuclear-track-recording Polymer of Unique Sensitivity and Resolution," *Nucl. Instruments Methods*, vol. 153, no. 2-3, pp. 457–460, 1978.

[60] M. S. Gordon, K. P. Rodbell, D. F. Heidel, C. Cabral, E. H. Cannon, and D. D. Reinhardt, "Single-event-upset and alpha-particle emission rate measurement techniques," *IBM J. Res. Dev.*, vol. 52, pp. 265–273, May 2008.

[61] A. V. Prokofiev, E. Passoth, A. Hjalmarsson, and M. Majerle, "CUP-A New High-Flux Irradiation Position at the ANITA Neutron Facility at TSL," *IEEE Trans. Nucl. Sci.*, vol. 61, pp. 1929–1936, Aug. 2014.

[62] N. B. Patel and H. Puchner, "Correlation of soft error rates between mono-energetic and full spectrum beams on a 90nm SRAM technology," in *2009 IEEE Int. Reliab. Phys. Symp.*, pp. 948–951, IEEE, Apr. 2009.

[63] A. V. Prokofiev, J. Blomgren, S. P. Platt, R. Nolte, S. Rottger, and A. N. Smirnov, "ANITA-a new neutron facility for accelerated SEE testing at the svedberg laboratory," in *2009 IEEE Int. Reliab. Phys. Symp.*, pp. 929–935, IEEE, Apr. 2009.

[64] S. Abe, Y. Watanabe, N. Shibano, N. Sano, H. Furuta, M. Tsutsui, T. Uemura, and T. Arakawa, "Multi-scale Monte Carlo simulation of soft errors using PHITS-HyENEXSS code system," in *2011 12th Eur. Conf. Radiat. Its Eff. Components Syst.*, pp. 390–395, IEEE, Sept. 2011.

[65] S. Abe, Y. Watanabe, N. Shibano, N. Sano, T. Arakawa, H. Furuta, M. Tsutsui, and T. Uemura, "Simulation of Cosmic-ray Neutron Induced Soft Errors Using PHITS and HyENEXSS," in *Int. Radiat. Eff. Semicond. Devices Sp. Appl.*, 2010.

[66] J. F. Ziegler and J. P. Biersack, "Treatise on Heavy-Ion Science (SRIM)," 2008.

[67] J. F. Ziegler, J. P. Biersack, and U. Littmark, "The Stopping and Range of Ions in Mtter," 1985.

[68] T. Kato, T. Uemura, and H. Matsuyama, "High-Accuracy Estimation of Soft Error Rate using PHYSERD with Circuit Simulation," in *2014 Int. Conf. Simul. Semicond. Process. Devices*, pp. 345–348, 2014.

[69] S. Abe, Y. Watanabe, N. Shibano, N. Sano, H. Furuta, M. Tsutsui, T. Uemura, and T. Arakawa, "Neutron-induced soft error analysis in MOSFETs from a 65nm to a 25 nm design rule using multi-scale Monte Carlo simulation method," in *2012 IEEE Int. Reliab. Phys. Symp.*, pp. SE.3.1–SE.3.6, IEEE, Apr. 2012.

[70] S. Abe, Y. Watanabe, N. Shibano, N. Sano, H. Furuta, M. Tsutsui, T. Uemura, and T. Arakawa, "Multi-Scale Monte Carlo Simulation of Soft Errors Using PHITS-HyENEXSS Code System," *IEEE Trans. Nucl. Sci.*, vol. 59, pp. 965–970, Aug. 2012.

[71] "Azure: Microsoft's Cloud Platform."

[72] D. Skarin, M. Sanfridson, and J. Karlsson, "Impact of Soft Errors in a Brake-by-Wire System," *Proc. 2007 IEEE Work. Silicon Errors Log. - Syst. Eff. (SELSE 3)*.

[73] H. Miyazaki, Y. Kusano, H. Okano, T. Nakada, K. Seki, T. Shimizu, N. Shinjo,

F. Shoji, A. Uno, and M. Kurokawa, "K computer: 8.162 PetaFLOPS massively parallel scalar supercomputer built with over 548k cores," in *2012 IEEE Int. Solid-State Circuits Conf.*, pp. 192–194, IEEE, Feb. 2012.

[74] J. von Neumann, "First draft of a report on the EDVAC," *IEEE Ann. Hist. Comput.*, vol. 15, no. 4, pp. 27–75, 1993.

[75] C. L. Chen and M. Y. Hsiao, "Error-Correcting Codes for Semiconductor Memory Applications: A State-of-the-Art Review," *IBM J. Res. Dev.*, vol. 28, pp. 124–134, Mar. 1984.

[76] T. Rao, "A generalization of the single b-Bit byte error correcting and double bit error detecting codes for high-speed memory systems," *IEEE Trans. Comput.*, vol. 45, pp. 508–511, Apr. 1996.

[77] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2874–2878, 1996.

[78] P. Hazucha, T. Karnik, S. Walstra, B. Bloechel, J. Tschanz, J. Maiz, K. Soumyanath, G. Dermer, S. Narendra, V. De, and S. Borkar, "Measurements and analysis of SER-tolerant latch in a 90-nm dual-V/sub T/ CMOS process," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1536–1543, Sept. 2004.

[79] M. Zhang, S. Mitra, T. M. Mak, N. Seifert, N. J. Wang, Q. Shi, K. S. Kim, N. R. Shanbhag, and S. J. Patel, "Sequential Element Design With Built-In Soft Error Resilience," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 14, pp. 1368–1378, Dec. 2006.

[80] H. Puchner, R. Kapre, S. Sharifzadeh, J. Majjiga, R. Chao, D. Radaelli, and S. Wong, "Elimination of Single Event Latchup in 90nm SRAM Technologies," in *2006 IEEE Int. Reliab. Phys. Symp. Proc.*, pp. 721–722, IEEE, 2006.

[81] P. Layton, D. Czajkowski, J. Marshall, H. Anthony, and R. Boss, "Single event latchup protection of integrated circuits," in *RADECS 97. Fourth Eur. Conf. Radiat. its Eff. Components Syst. (Cat. No.97TH8294)*, pp. 327–331, IEEE, 1997.

[82] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," in *Int. Electron Devices Meet. 1999. Tech. Dig. (Cat. No.99CH36318)*, pp. 67–70, IEEE, 1999.

[83] D. Hisamoto, T. Kaga, and E. Takeda, "Impact of the vertical SOI 'DELTA' structure on planar device technology," *IEEE Trans. Electron Devices*, vol. 38, pp. 1419–1424, June 1991.

[84] M. Gaillardin, M. Raine, P. Paillet, M. Martinez, C. Marcandella, S. Girard, O. Duhamel, N. Richard, F. Andrieu, S. Barraud, and O. Faynot, "Radiation effects in advanced SOI devices: New insights into Total Ionizing Dose and Single-Event Effects," in *2013 IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf.*, pp. 1–2, IEEE, Oct. 2013.

[85] M. R. Shaneyfelt, J. R. Schwank, P. E. Dodd, J. Stevens, G. Vizkelethy, S. E. Swanson, and S. M. Dalton, "SOI Substrate Removal for SEE Characterization: Techniques and Applications," *IEEE Trans. Nucl. Sci.*, vol. 59, pp. 1142–1148, Aug. 2012.

[86] J. Schwank, V. Ferlet-Cavrois, M. Shaneyfelt, P. Paillet, and P. Dodd, "Radia-

tion effects in SOI technologies," *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 522–538, June 2003.

[87] M. L. Alles, R. D. Schrimpf, R. A. Reed, L. W. Massengill, R. A. Weller, M. H. Mendenhall, D. R. Ball, K. M. Warren, T. D. Loveless, J. S. Kauppila, and B. D. Sierawski, "Radiation hardness of FDSOI and FinFET technologies," in *IEEE 2011 Int. SOI Conf.*, pp. 1–2, IEEE, Oct. 2011.

[88] P. Dodd, M. Shaneyfelt, E. Fuller, J. Pickel, F. Sexton, and P. Winokur, "Impact of substrate thickness on single-event effects in integrated circuits," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 1865–1871, 2001.

[89] Y. Fang and A. S. Oates, "Neutron-Induced Charge Collection Simulation of Bulk FinFET SRAMs Compared With Conventional Planar SRAMs," *IEEE Trans. Device Mater. Reliab.*, vol. 11, pp. 551–554, Dec. 2011.

[90] H. Nakamura, T. Uemura, K. Takeuchi, T. Fukuda, S. Kumashiro, and T. Mogami, "Scaling effect and circuit type dependence of neutron induced single event transient," in *2012 IEEE Int. Reliab. Phys. Symp.*, pp. 3C.3.1–3C.3.7, IEEE, Apr. 2012.

[91] B. Zhai, R. G. Dreslinski, D. Blaauw, T. Mudge, and D. Sylvester, "Energy efficient near-threshold chip multi-processing," in *Proc. 2007 Int. Symp. Low power Electron. Des. - ISLPED '07*, (New York, New York, USA), pp. 32–37, ACM Press, 2007.

[92] P. Shivakumar, M. Kistler, S. Keckler, D. Burger, and L. Alvisi, "Modeling the effect of technology trends on the soft error rate of combinational logic," in *Proc. Int. Conf. Dependable Syst. Networks*, pp. 389–398, IEEE Comput. Soc, 2002.

[93] K. Tanaka, H. Nakamura, T. Uemura, K. Takeuchi, T. Fukuda, and S. Kumashiro, "Study on Influence of Device Structure Dimensions and Profiles on Charge Collection Current Causing SET Pulse Leading to Soft Errors in Logic Circuits," in *2009 Int. Conf. Simul. Semicond. Process. Devices*, pp. 1–4, IEEE, Sept. 2009.

[94] H. Nakamura, K. Tanaka, T. Uemura, K. Takeuchi, T. Fukuda, and S. Kumashiro, "Measurement of neutron-induced single event transient pulse width narrower than 100ps," in *2010 IEEE Int. Reliab. Phys. Symp.*, pp. 694–697, IEEE, 2010.

[95] Y. Tosaka, H. Ehara, M. Igeta, T. Uemura, H. Oka, N. Matsuoka, and K. Hatanaka, "Comprehensive study of soft errors in advanced CMOS circuits with 90/130 nm technology," in *IEDM Tech. Dig. IEEE Int. Electron Devices Meet. 2004.*, pp. 941–944, IEEE, 2004.

[96] Y. Tosaka, R. Takasu, H. Ehara, T. Uemura, H. Oka, S. Satoh, N. Matsuoka, and K. Hatanaka, "Technology Trend of Soft Errors based on Accurate Estimation Method," in *Int. Conf. Solid State Devices Mater.*, pp. 442–443, 2005.

[97] T. Uemura, Y. Tosaka, and S. Satoh, "Neutron-induced Soft-Error Simulation Technology for Logic Circuits," in *Int. Conf. Solid State Devices Mater.*, pp. 942–943, 2005.

[98] T. Uemura, Y. Tosaka, S. Satoh, K. Takahisa, and K. Hatanaka, "Scaling Trends and Mitigation Techniques for Soft Errors in Flip-Flops," in *Int. Conf. Solid State Devices Mater.*, pp. 284–285, 2006.

[99] T. Uemura, Y. Tosaka, and S. Satoh, "Neutron-Induced Soft-Error Simulation Technology for Logic Circuits," *Jpn. J. Appl. Phys.*, vol. 45, pp. 3256–3259, Apr. 2006.

[100] Y. Tosaka, T. Uemura, H. Ando, H. Matsuyama, K. Shono, K. Takahisa, M. Fukuda, and K. Hatanaka, "Neutron-Accelerated Test of Soft Error in Logic Element and System," in *Int. Work. Radiat. Eff. Semicond. Devices Sp. Radiat.*, pp. 85–90, 2008.

[101] R. Baumann, "The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction," in *Dig. Int. Electron Devices Meet.*, pp. 329–332, IEEE, 2002.

[102] N. Seifert, P. Slankard, M. Kirsch, B. Narasimham, V. Zia, C. Brookreson, A. Vo, S. Mitra, B. Gill, and J. Maiz, "Radiation-Induced Soft Error Rates of Advanced CMOS Bulk Devices," in *2006 IEEE Int. Reliab. Phys. Symp. Proc.*, pp. 217–225, IEEE, 2006.

[103] G. Gasiot, D. Giot, and P. Roche, "Multiple Cell Upsets as the Key Contribution to the Total SER of 65 nm CMOS SRAMs and Its Dependence on Well Engineering," *IEEE Trans. Nucl. Sci.*, vol. 54, pp. 2468–2473, Dec. 2007.

[104] J. Maiz, S. Hareland, K. Zhang, and P. Armstrong, "Characterization of multi-bit soft error events in advanced SRAMs," in *IEEE Int. Electron Devices Meet. 2003*, pp. 21.4.1–21.4.4, IEEE, 2003.

[105] I. Chatterjee, B. Narasimham, N. N. Mahatme, B. L. Bhuva, R. D. Schrimpf, J. K. Wang, B. Bartz, E. Pitta, and M. Buer, "Single-Event Charge Collection and Upset in 40-nm Dual- and Triple-Well Bulk CMOS SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 58, pp. 2761–2767, Dec. 2011.

[106] A. D. Tipton, J. A. Pellish, J. M. Hutson, R. Baumann, X. Deng, A. Marshall, M. A. Xapsos, H. S. Kim, M. R. Friendlich, M. J. Campola, C. M. Seidleck, K. A. LaBel, M. H. Mendenhall, R. A. Reed, R. D. Schrimpf, R. A. Weller, and J. D. Black, "Device-Orientation Effects on Multiple-Bit Upset in 65 nm SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 55, pp. 2880–2885, Dec. 2008.

[107] T. Uemura, T. Kato, and H. Matsuyama, "Impact of parasitic bipolar action and soft-error trend in bulk CMOS at terrestrial environment," in *2013 IEEE Int. Reliab. Phys. Symp.*, pp. 6C.4.1–6C.4.6, IEEE, Apr. 2013.

[108] D. James, "Intel Ivy Bridge unveiled — The first commercial tri-gate, high-k, metal-gate CPU," in *Proc. IEEE 2012 Cust. Integr. Circuits Conf.*, pp. 1–4, IEEE, Sept. 2012.

[109] T. Maruyama, "Fujitsu's Next Generation Quad-Core Processor," in *Hot chips*, 2008.

[110] H. Ando, Y. Yoshida, A. Inoue, I. Sugiyama, T. Asakawa, K. Morita, T. Muta, T. Motokurumada, S. Okada, H. Yamashita, Y. Satsukawa, A. Konmoto, R. Yamashita, and H. Sugiyama, "A 1.3 GHz fifth generation SPARC64 microprocessor," in *2003 IEEE Int. Solid-State Circuits Conf. 2003. Dig. Tech. Pap. ISSCC.*, vol. 1, pp. 246–491, IEEE, 2003.

[111] E. Ibe, Y. Yahagi, F. Kataoka, Y. Saito, A. Eto, and M. Sato, "A self-Consistent Integrated System for Terrestrial-Neutron Induced Sungle Event Upset of Semiconductor Devices at the Ground," in *Proc. Int. Conf. Inf. Technol. Appl.*, 2002.

[112] E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, "Impact of Scaling

on Neutron-Induced Soft Error in SRAMs From a 250 nm to a 22 nm Design Rule," *IEEE Trans. Electron Devices*, vol. 57, pp. 1527–1538, July 2010.

[113] M. Nicolaidis, *Soft Errors in Modern Electronic Systems*. Springer US, 2011.

[114] T. Maruyama, T. Yoshida, R. Kan, I. Yamazaki, S. Ymamura, N. Takahashi, M. Hondou, and H. Okano, "Sparc64 VIIIfx: A New-Generation Octocore Processor for Petascale Computing," in *Hot chips*, pp. 30–40, 2010.

[115] R. Kan, T. Tanaka, G. Sugizaki, K. Ishizaka, R. Nishiyama, S. Sakabayashi, Y. Koyanagi, R. Iwatsuki, K. Hayasaka, T. Uemura, G. Ito, Y. Ozeki, H. Adachi, K. Furuya, and T. Motokurumada, "The 10th Generation 16-Core SPARC64 Processor for Mission Critical UNIX Server," *IEEE J. Solid-State Circuits*, vol. 49, pp. 32–40, Jan. 2014.

[116] R. Kan, T. Tanaka, G. Sugizaki, R. Nishiyama, S. Sakabayashi, Y. Koyanagi, R. Iwatsuki, K. Hayasaka, T. Uemura, G. Ito, Y. Ozeki, H. Adachi, K. Furuya, and T. Motokurumada, "A 10th generation 16-core SPARC64 processor for mission-critical UNIX server," in *2013 IEEE Int. Solid-State Circuits Conf. Dig. Tech. Pap.*, pp. 60–61, IEEE, Feb. 2013.

[117] T. Yoshida, "SPARC64 XIfx: Fujitsu's next generation processor for HPC," in *Hot chips 26*, 2014.

[118] A. Dixit, R. Heald, and A. Wood, "Trends from Ten Years of Soft Error Experimentation," in *Proc. Silicon Errors Log. Syst. Eff.*, 2009.

[119] T. Kato, T. Uemura, H. Mori, Y. Ikeda, K. Suzuki, S. Satoh, and H. Matsuyama, "Radiation-Induced Parasitic Bipolar Effect in PMOS with Embedded SiGe," in *Int. Conf. Solid State Devices Mater.*, pp. 847–848, 2012.

[120] T. Kato, T. Uemura, H. Mori, Y. Ikeda, K. Suzuki, S. Satoh, and H. Matsuyama, "Impact of Parasitic Bipolar Effect on Single-Event Upset in p-Type MetalOxideSemiconductor Field Effect Transistor with Embedded SiGe," *Jpn. J. Appl. Phys.*, vol. 52, p. 04CC15, Apr. 2013.

[121] A. Biswas, P. Racunas, R. Cheveresan, J. Emer, S. Mukherjee, and R. Rangan, "Computing Architectural Vulnerability Factors for Address-Based Structures," in *32nd Int. Symp. Comput. Archit.*, pp. 532–543, IEEE, 2005.

[122] H. Ando, R. Kan, Y. Tosaka, K. Takahisa, and K. Hatanaka, "Validation of hardware error recovery mechanisms for the SPARC64 V microprocessor," in *2008 IEEE Int. Conf. Dependable Syst. Networks With FTCS DCC*, pp. 62–69, IEEE, 2008.

[123] T. Uemura, R. Tanabe, and H. Matusyama, "Mitigation technique against multi-bit-upset without area, performance and power overhead," in *2012 IEEE Int. Reliab. Phys. Symp.*, pp. 5B.4.1–5B.4.6, IEEE, Apr. 2012.

[124] J. Chang, S. Chen, W. Chen, S. Chiu, R. Faber, R. Ganesan, M. Grgek, V. Lukka, W. W. Mar, J. Vash, S. Rusu, and K. Zhang, "A 45nm 24MB on-die L3 cache for the 8-core multi-threaded Xeon Processor," 2009.

[125] Y. Iwamoto, M. Fukuda, Y. Sakamoto, A. Tamii, K. Hatanaka, K. Takahisa, K. Nagayama, H. Asai, K. Sugimoto, and I. Nashiyama, "Evaluation of the White Neutron Beam Spectrum for Single-Event Effects Testing at the RCNP Cyclotron Facility," *Nucl. Technol.*, vol. 173, no. 2, pp. 210–217, 2011.

[126] Y. Cho, S. Atsumi, and K. Nakamura, "Scanning Nonlinear Dielectric Microscope Using a Lumped Constant Resonator Probe and Its Application to Inves-

tigation of Ferroelectric Polarization Distributions," *Jpn. J. Appl. Phys.*, vol. 36, pp. 3152–3156, May 1997.

[127] Y. Cho, S. Kazuta, and K. Matsuura, "Scanning nonlinear dielectric microscopy with nanometer resolution," *Appl. Phys. Lett.*, vol. 75, p. 2833, Nov. 1999.

[128] Y. Cho, A. Kirihara, and T. Saeki, "Scanning nonlinear dielectric microscope," *Rev. Sci. Instrum.*, vol. 67, p. 2297, June 1996.

[129] H. Odagawa and Y. Cho, "Theoretical and Experimental Study on Nanoscale Ferroelectric Domain Measurement Using Scanning Nonlinear Dielectric Microscopy," *Jpn. J. Appl. Phys.*, vol. 39, pp. 5719–5722, Sept. 2000.

[130] K. Honda and Y. Cho, "Visualization using scanning nonlinear dielectric microscopy of electrons and holes localized in the thin gate film of a metal-SiO2-Si3N4-SiO2-semiconductor flash memory," *Appl. Phys. Lett.*, vol. 86, p. 013501, Dec. 2005.

[131] K. Honda, S. Hashimoto, and Y. Cho, "Visualization of charges stored in the floating gate of flash memory by scanning nonlinear dielectric microscopy," *Nanotechnology*, vol. 17, pp. S185–S188, Apr. 2006.

[132] K. Honda, S. Hashimoto, and Y. Cho, "Visualization of electrons and holes localized in gate thin film of metal SiO[sub 2]Si[sub 3]N[sub 4]SiO[sub 2] semiconductor-type flash memory using scanning nonlinear dielectric microscopy after writing-erasing cycling," *Appl. Phys. Lett.*, vol. 86, p. 063515, Feb. 2005.

[133] K. Ishikawa, K. Honda, and Y. Cho, "Resolution enhancement in contact-type scanning nonlinear dielectric microscopy using a conductive carbon nanotube probe tip," *Nanotechnology*, vol. 18, p. 084015, Feb. 2007.

[134] T. Uemura, T. Kato, R. Tanabe, H. Iwata, H. Matsuyama, M. Hashimoto, K. Takahisa, M. Fukuda, and K. Hatanaka, "Preventing single event latchup with deep P-well on P-substrate," in *2014 IEEE Int. Reliab. Phys. Symp.*, pp. SE.3.1–SE.3.4, IEEE, June 2014.

[135] T. Uemura, T. Kato, R. Tanabe, H. Iwata, J. Ariyoshi, H. Matsuyama, and M. Hashimoto, "Exploring Well-Configurations for Minimizing Single Event Latchup," *IEEE Trans. Nucl. Sci.*, vol. 61, pp. 3282–3289, Dec. 2014.

[136] T. Aoki, "Dynamics of heavy-ion-induced latchup in CMOS structures," *IEEE Trans. Electron Devices*, vol. 35, no. 11, pp. 1885–1891, 1988.

[137] K. Soliman and D. K. Nichols, "Latchup in CMOS Devices from Heavy Ions," *IEEE Trans. Nucl. Sci.*, vol. 30, no. 6, pp. 4514–4519, 1983.

[138] H. Becker, T. Miyahira, and A. Johnston, "Latent damage in CMOS devices from single-event latchup," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 3009–3015, Dec. 2002.

[139] A. Johnston, "The influence of VLSI technology evolution on radiation-induced latchup in space systems," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 505–521, Apr. 1996.

[140] P. Dodd, M. Shaneyfelt, J. Schwank, and G. Hash, "Neutron-induced soft errors, latchup, and comparison of SER test methods for SRAM technologies," in *Dig. Int. Electron Devices Meet.*, pp. 333–336, IEEE, 2002.

[141] P. Dodd, M. Shaneyfelt, J. Schwank, and G. Hash, "Neutron-induced latchup in SRAMs at ground level," in *2003 IEEE Int. Reliab. Phys. Symp. Proceedings,*

2003. 41st Annu., pp. 51–55, IEEE, 2003.

[142] G. Bruguier and J.-M. Palau, "Single particle-induced latchup," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 522–532, Apr. 1996.

[143] R. G. Useinc, "Analytical Model of Radiation Induced or Single Event Latchup in CMOS Integrated Circuits," in *2005 8th Eur. Conf. Radiat. Its Eff. Components Syst.*, pp. PC21–1–PC21–4, IEEE, Sept. 2005.

[144] J. Spratt, J. Pickel, R. Leadon, R. Lacoe, S. Moss, and S. LaLumondiere, "A single event latchup suppression technique for COTS CMOS ICs," *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 2219–2224, Dec. 2003.

[145] M. Nicolaidis, "A Low-Cost Single-Event Latchup Mitigation Sscheme," in *12th IEEE Int. On-Line Test. Symp.*, pp. 111–118, IEEE, 2006.

[146] N. A. Dodds, J. M. Hutson, J. A. Pellish, R. A. Reed, H. S. Kim, M. D. Berg, M. R. Friendlich, A. M. Phan, C. M. Seidleck, M. A. Xapsos, X. Deng, R. C. Baumann, R. D. Schrimpf, M. P. King, L. W. Massengill, and R. A. Weller, "Selection of Well Contact Densities for Latchup-Immune Minimal-Area ICs," *IEEE Trans. Nucl. Sci.*, vol. 57, pp. 3575–3581, Dec. 2010.

[147] S. Voldman, E. Gebreselasic, M. Zierak, D. Hershberger, D. Collins, N. Feilchenfeld, S. St. Onge, and J. Dunn, "Latchup in merged triple well structure," in *2005 IEEE Int. Reliab. Phys. Symp. 2005. Proceedings. 43rd Annu.*, pp. 129–136, IEEE, 2005.

[148] J.-E. Yeon, M.-Y. Park, K.-M. Cho, and H.-J. Kim, "A new high voltage shorted-anode IGBT with intrinsic body diode improves performance of single-ended induction cooker," in *2013 15th Eur. Conf. Power Electron. Appl.*, pp. 1–9, IEEE, Sept. 2013.

[149] T. Uemura, T. Kato, H. Matsuyama, and M. Hashimoto, "Mitigating Multi-Bit-Upset With Well-Slits in 28 nm Multi-Bit-Latch," *IEEE Trans. Nucl. Sci.*, vol. 60, pp. 4362–4367, Dec. 2013.

[150] A. Watson and S. Voldman, "The effect of deep trench and sub-collector on the latchup robustness in BiCMOS silicon germanium technology," in *Bipolar/BiCMOS Circuits Technol. 2004. Proc. 2004 Meet.*, pp. 172–175, IEEE, 2004.

[151] S. Voldman, "The Influence of a Novel Contacted Polysilicon-Filled Deep Trench (DT) Biased Structure and Its Voltage Bias State on CMOS Latchup," in *2006 IEEE Int. Reliab. Phys. Symp. Proc.*, pp. 151–158, IEEE, 2006.

[152] S. Yoshimoto, T. Amashita, S. Okumura, K. Nii, H. Kawaguchi, and M. Yoshimoto, "NMOS-inside 6T SRAM layout reducing neutron-induced multiple cell upsets," in *2012 IEEE Int. Reliab. Phys. Symp.*, pp. 5B.5.1–5B.5.5, IEEE, Apr. 2012.

[153] T. Uemura, Y. Tosaka, H. Matsuyama, K. Shono, C. J. Uchibori, K. Takahisa, M. Fukuda, and K. Hatanaka, "SEILA: Soft error immune latch for mitigating multi-node-SEU and local-clock-SET," in *2010 IEEE Int. Reliab. Phys. Symp.*, pp. 218–223, IEEE, 2010.

[154] T. Uemura, T. Kato, H. Matsuyama, K. Takahisa, M. Fukuda, and K. Hatanaka, "Investigation of multi cell upset in sequential logic and validity of redundancy technique," in *2011 IEEE 17th Int. On-Line Test. Symp.*, pp. 7–12, IEEE, July 2011.

[155] T. Uemura, T. Sakoda, and H. Matsuyama, "Layout optimization to maximize tolerance in SEILA: Soft error immune latch," in *2011 IEEE Int. Conf. IC Des. Technol.*, pp. 1–4, IEEE, May 2011.

[156] I. Chatterjee, S. Jagannathan, D. Loveless, B. L. Bhuva, S. Wen, R. Wong, and M. Sachdev, "Impact of well contacts on the single event response of radiation-hardened 40-nm flip-flops," in *2012 IEEE Int. Reliab. Phys. Symp.*, pp. SE.4.1–SE.4.6, IEEE, Apr. 2012.

[157] T. Uemura, R. Tanabe, Y. Tosaka, and S. Satoh, "Novel Soft Error Hardened Latches and Flip-Flop," in *Int. Conf. Solid State Devices Mater.*, pp. 84–85, 2007.

[158] T. Uemura, R. Tanabe, Y. Tosaka, and S. Satoh, "Soft Error Hardened Latch and Its Estimation Method," *Jpn. J. Appl. Phys.*, vol. 47, pp. 2736–2741, Apr. 2008.

[159] T. Uemura, R. Tanabe, Y. Tosaka, and S. Satoh, "Using Low Pass Filters in Mitigation Techniques against Single-Event Transients in 45nm Technology LSIs," in *2008 14th IEEE Int. On-Line Test. Symp.*, pp. 117–122, IEEE, July 2008.

[160] T. Uemura, Y. Tosaka, H. Matsuyama, K. Takahisa, and K. Hatanaka, "Robust Flip-Flop against Soft Errors for Combinational and Sequential Logic Circuits," in *Int. Conf. Solid State Devices Mater.*, pp. 88–89, 2008.

[161] T. Uemura, Y. Tosaka, H. Matsuyama, K. Takahisa, M. Fukuda, and K. Hatanaka, "Robust Flip-Flop Circuit against Soft Errors for Combinational and Sequential Logic Circuits," *Jpn. J. Appl. Phys.*, vol. 48, p. 04C070, Apr. 2009.

[162] B. D. Olson, O. A. Amusan, S. Dasgupta, L. W. Massengill, A. F. Witulski, B. L. Bhuva, M. L. Alles, K. M. Warren, and D. R. Ball, "Analysis of Parasitic PNP Bipolar Transistor Mitigation Using Well Contacts in 130 nm and 90 nm CMOS Technology," *IEEE Trans. Nucl. Sci.*, vol. 54, pp. 894–897, Aug. 2007.

[163] O. Amusan, L. Massengill, M. Baze, B. Bhuva, A. Witulski, J. Black, A. Balasubramanian, M. Casey, D. Black, J. Ahlbin, R. Reed, and M. McCurdy, "Mitigation Techniques for Single-Event-Induced Charge Sharing in a 90-nm Bulk CMOS Process," *IEEE Trans. Device Mater. Reliab.*, vol. 9, pp. 311–317, June 2009.

[164] N. Seifert, B. Gill, V. Zia, M. Zhang, and V. Ambrose, "On the Scalability of Redundancy based SER Mitigation Schemes," in *2007 IEEE Int. Conf. Integr. Circuit Des. Technol.*, pp. 1–9, IEEE, May 2007.

[165] T. Heijmen, P. Roche, G. Gasiot, and K. Forbes, "A Comparative Study on the Soft-Error Rate of Flip-Flops from 90-nm Production Libraries," in *2006 IEEE Int. Reliab. Phys. Symp. Proc.*, pp. 204–211, IEEE, 2006.

[166] M. H. Yukiya Kawakami, "Investigation of soft error rate including multi-bit upsets in advanced SRAM using neutron irradiation test and 3D mixed-mode device simulation," in *IEDM Tech. Dig. IEEE Int. Electron Devices Meet. 2004.*, pp. 945–948, IEEE, 2004.

[167] T. Uemura, T. Kato, H. Matsuyama, and M. Hashimoto, "Soft-Error in SRAM at Ultra-Low Voltage and Impact of Secondary Proton in Terrestrial Environment," *IEEE Trans. Nucl. Sci.*, vol. 60, pp. 4232–4237, Dec. 2013.

[168] B. Wang, T. Q. Nguyen, A. T. Do, J. Zhou, M. Je, and T. T. Kim, "A 0.2V 16Kb 9T SRAM with bitline leakage equalization and CAM-assisted write performance boosting for improving energy efficiency," in *2012 IEEE Asian Solid State Circuits Conf.*, pp. 73–76, IEEE, Dec. 2012.

[169] K. Sarfraz, "Comparison of two SRAM matrix leakage reduction techniques in 45nm technology," in *2010 Int. Conf. Microelectron.*, pp. 367–370, IEEE, Dec. 2010.

[170] B. D. Sierawski, K. M. Warren, R. A. Reed, R. A. Weller, M. M. Mendenhall, R. D. Schrimpf, R. C. Baumann, and V. Zhu, "Contribution of low-energy ($\ll$ 10 MeV) neutrons to upset rate in a 65 nm SRAM," in *2010 IEEE Int. Reliab. Phys. Symp.*, pp. 395–399, IEEE, 2010.

[171] B. D. Sierawski, J. A. Pellish, R. A. Reed, R. D. Schrimpf, K. M. Warren, R. A. Weller, M. H. Mendenhall, J. D. Black, A. D. Tipton, M. A. Xapsos, R. C. Baumann, X. Deng, M. J. Campola, M. R. Friendlich, H. S. Kim, A. M. Phan, and C. M. Seidleck, "Impact of Low-Energy Proton Induced Upsets on Test Methods and Rate Predictions," *IEEE Trans. Nucl. Sci.*, vol. 56, pp. 3085–3092, Dec. 2009.

[172] K. P. Rodbell, D. F. Heidel, H. K. Tang, M. S. Gordon, P. Oldiges, and C. E. Murray, "Low-Energy Proton-Induced Single-Event-Upsets in 65 nm Node, Silicon-on-Insulator, Latches and Memory Cells," *IEEE Trans. Nucl. Sci.*, vol. 54, pp. 2474–2479, Dec. 2007.

[173] D. F. Heidel, P. W. Marshall, K. A. LaBel, J. R. Schwank, K. P. Rodbell, M. C. Hakey, M. D. Berg, P. E. Dodd, M. R. Friendlich, A. D. Phan, C. M. Seidleck, M. R. Shaneyfelt, and M. A. Xapsos, "Low Energy Proton Single-Event-Upset Test Results on 65 nm SOI SRAM," *IEEE Trans. Nucl. Sci.*, vol. 55, pp. 3394–3400, Dec. 2008.

[174] H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Neutron-Induced Soft Errors and Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM," *IEEE Trans. Nucl. Sci.*, vol. 58, pp. 2097–2102, Aug. 2011.

[175] H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Alpha-particle-induced soft errors and multiple cell upsets in 65-nm 10T subthreshold SRAM," in *2010 IEEE Int. Reliab. Phys. Symp.*, pp. 213–217, IEEE, 2010.

[176] R. Harada, S. Abe, H. Fuketa, T. Uemura, M. Hashimoto, and Y. Watanabe, "Angular Dependency of Neutron-Induced Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM," *IEEE Trans. Nucl. Sci.*, vol. 59, pp. 2791–2795, Dec. 2012.

[177] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1439, Oct. 1989.

[178] S. Satoh, R. Sudo, H. Tashiro, N. Higaki, S. Yamaguchi, and N. Nakayama, "CMOS-SRAM soft-error simulation system," in *Proc. Int. Work. Numer. Model. Process. Devices Integr. Circuits NUPAD V*, pp. 181–184, IEEE, 1994.

[179] Y. Tosaka, S. Satoh, and H. Oka, *An Accurate and Comprehensive Soft Error Simulator NISES II.* Vienna: Springer Vienna, Jan. 2004.

[180] S. Borkar, "Exascale computing - A fact or a fiction?," in *2013 IEEE 27th Int. Symp. Parallel Distrib. Process.*, pp. 3–3, IEEE, May 2013.