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A CAPACITOR-LESS TRANSIENT-RESPONSE-IMPROVED CMOS LOW-DROPOUT REGULATOR

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Abstract

A 1.7V 100mA capacitor-less CMOS low-dropout (LDO) regulator for system-on-chip applications which can both reduce board space and external pins is presented. By using a combination of fast transient improvement and frequency compensation method, the proposed LDO regulator provides a fast transient response, as well as good stability during the whole variation of load current. The proposed LDO regulator has been implemented in a 0.18μm CMOS process, and the active chip area is $0.15mm^2$. The voltage derivation is less than 30mV for the load current change between 0 and 100mA. The dropout voltage is about 300mV at 100mA load current.

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1. Introduction

Power management is a very important issue in portable electronic applications. Although linear regulators have a better transient response and less noise than the switching regulators, they are relatively inefficient. So the low-dropout regulators (LDOs) which are able to provide effective stabilization of the output voltage even when the difference between input and output voltage is less than 0.3V, are used more and more in electric equipments especially in communication systems.

The LDO regulators usually use a large-size PMOS transistor as the power transistor to drive high load current while achieving low dropout voltage. If we use a large off-chip load capacitor, then the large gate capacitance of the PMOS power transistor creates a low-frequency non-dominant pole while the large off-chip load capacitor generates the low-frequency dominant pole. So the uncompensated LDO regulator is unstable. The conventional compensation techniques usually use the zero generated by the load capacitor and its equivalent series resistance (ESR) to achieve the frequency compensation. So it has a narrow bandwidth and requires a huge load capacitor and ESR. Furthermore, we should carefully choose the value of the load capacitor and its ESR to ensure the stability of the LDO regulator, otherwise the LDO regulator will oscillate when the zero locates at too low (e.g., beyond the dominant pole) or too high frequency (e.g., far behind the unity-gain frequency). Different approaches have been reported to achieve the frequency compensation [1-5]. The simple and effective approach is adding a voltage buffer between the error amplifier and the power transistor. For example, in [1], an emitter-follower has been adopted as a voltage buffer to drive the PMOS power transistor. The low output resistance of the emitter-follower allows the pole at the gate of the power transistor to be moved to higher frequency. The work in [2] proposed an LDO regulator which uses a current feedback amplifier to achieve the fast transient response and high slew rate. The work in [3] proposed a current buffer with dynamically-biased shunt feedback which only dissipates low quiescent current at no-load condition. The method can greatly improve the efficiency of the LDO regulator when the load current is low, while it can achieve the frequency

compensation and good transient response. The work in [4] proposed another frequency compensation method which generated the low-frequency zero with a voltage-controlled current source instead of using the huge load capacitor and its ESR.

Traditional off-chip LDO regulator needs an up-to-μF output capacitor which will occupy huge area in the present integrated circuit process, so it is hard to meet the demands of system-on-chip (SoC) solutions. On-chip and local LDO regulators are utilized to power up sub-blocks of a system individually, so this can significantly reduce crosstalk and improve the voltage regulation. In addition, SoC designs with on-chip and local LDO regulators can reduce both board space and external pins significantly. In [5], a high slew-rate amplifier with push-pull output stage is proposed to enable an ultra-low quiescent current LDO regulator with improved transient response. The proposed amplifier helps to improve stability of LDO regulator without using any on-chip compensation capacitors. The work in [6] proposed an LDO regulator which can improve the transient response using a current sensing capacitor and a current amplifier as a differentiator.

In this paper, we introduce a discharge current path and a charge current path into the LDO regulator, which can both greatly improve the transient response of the LDO regulator and achieve the frequency compensation. With the proposed compensation method, the transient response performance of the LDO regulator can be greatly improved.

2. Stability and Transient Analysis of Capacitor-less LDO Regulator

2.1. Stability analysis of conventional LDO regulator

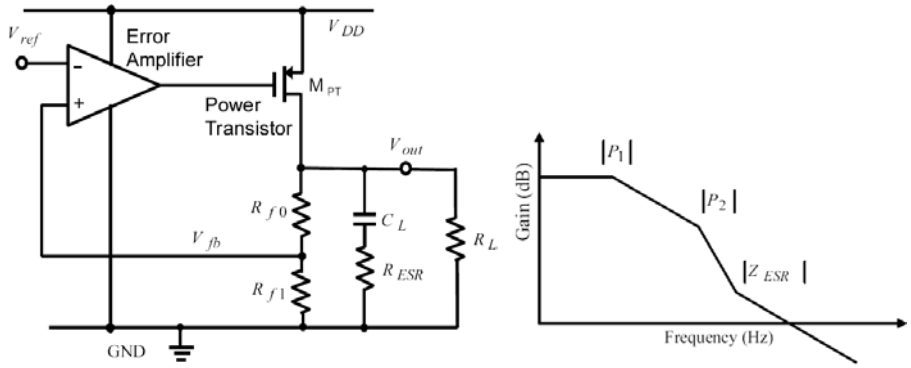
The structure of a classical CMOS LDO regulator shown in Figure 1 is composed of an error amplifier, a PMOS power transistor, a feedback-resistors network, a voltage reference and a load capacitor C_L with ESR, R_{ESR}. Generally, the feedback resistors R_{f0} and R_{f1} are much higher than the resistor R_L. There are two poles and one zero in the LDO regulator:

$$P_1 = -\frac{1}{C_L(R_L + R_{ESR})}, \tag{1}$$

$$P_2 = -\frac{1}{C_p R_1}, \tag{2}$$

$$Z_{ESR} = -\frac{1}{C_L R_{ESR}}. \tag{3}$$

Here C_p is the gate capacitance of the power transistor M_{PT}, and R_1 is the output resistance of the error amplifier. The conventional frequency compensation techniques usually use the zero generated by the load capacitor and its ESR. So it has a narrow bandwidth and requires a huge load capacitor and ESR. Furthermore, if the ESR is too large or too small, then the LDO regulator will be unstable.



(a) (b)

Figure 1. (a) Circuit topology of the conventional LDO regulator and (b) frequency compensation scheme for it.

2.2. Stability analysis of capacitor-less LDO regulator

Compared with the conventional LDO regulator, the capacitor-less LDO regulator does not use the large load capacitor. So we cannot use the zero generated by the large load capacitor and its ESR to compensate the LDO regulator. There are two poles of the LDO regulator which locate at the

output of the error amplifier and the LDO regulator output. Figure 2 shows the structure and the small-signal scheme of the capacitor-less LDO regulator. The poles P_1 and P_2 can be expressed as:

$$P_1 = -\frac{1}{R_1(C_a + C_{GS} + A_{pass}C_{GD})}, \tag{4}$$

$$P_2 = -\frac{1}{[R_{out}//(R_{f0} + R_{f1})//R_L]C_{INT}}. \tag{5}$$

As the power transistor M_{PT} is very large in order to drive large load current, its gate-source and gate-drain capacitances, C_{GS} and C_{GD}, are extremely large, in the range of tens of picofarads. C_{GD} also forms a Miller capacitor which increases the effective input capacitance of the power transistor M_{PT} by its voltage gain A_{pass} upto a few hundreds of picofarads. Thus, the output pole of the error amplifier P_1 locates at low frequency of typically a few kilohertz. The voltage gain A_{pass} changes with varying load current. P_1 is therefore load dependent, but less sensitive than the pole P_2. The second pole P_2 is located at the LDO regulator's output as shown in Figure 2(b) and is directly proportional to the load current. When the load current increases, the output resistance decreases and the pole P_2 moves to higher frequency. So the capacitor-less LDO regulator is usually stable when the load current is high. At low currents, the effective load resistance increases significantly. P_2 is then pushed to lower frequency in close proximity to the pole P_1. Stability cannot be guaranteed due to the decreased phase margin. The uncompensated capacitor-less LDO regulator is not stable at low currents, especially at the no-load condition.

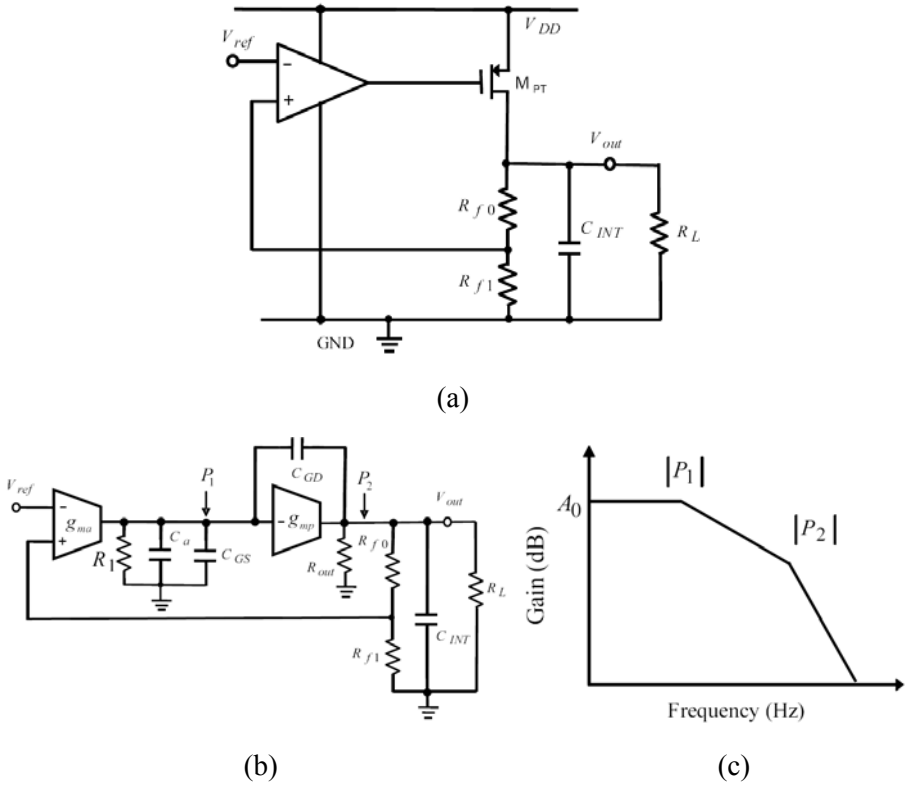


Figure 2. (a) Circuit topology of uncompensated capacitor-less LDO regulator, (b) its small-signal equivalent circuit and (c) frequency compensation scheme for it.

The Miller compensation method [6], which is shown in Figure 3, is the most direct and effective capacitor-less LDO regulator compensation method. After adding the frequency compensation capacitor and resistor C_m and R_c, the pole P_2 can be re-expressed as:

$$P_2 = -\frac{g_{mp}}{C_{INT}}. \tag{6}$$

A zero is generated as follows:

$$Z_1 = \frac{g_{mp}}{(1 - g_{mp}R_c)C_m}. \tag{7}$$

Based on the above analysis, the compensated capacitor-less LDO regulator is more stable when the load current increases, which is opposite with the conventional LDO regulators.

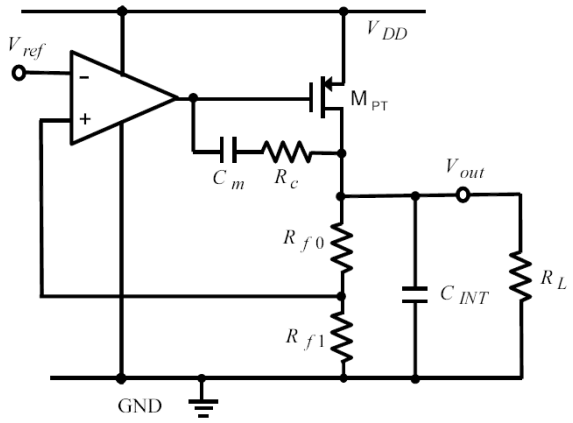


Figure 3. Miller-compensated capacitor-less LDO.

2.3. Transient analysis of conventional LDO regulator

In general, conventional LDO regulators in Figure 1 use the large external capacitor to improve the transient load regulation [2]. The output capacitor stores potential energy equivalent to the output voltage. Thus, the change in output voltage is inversely proportional to the output capacitance. The output voltage ripple for a given load transient is reduced by increasing the output capacitance. This relationship becomes much more apparent when the load transients are much faster than the gain-bandwidth product, which is usually the case.

When the load current significantly increases from zero upto $I_{load,max}$, the power transistor cannot respond immediately, so the load will sink current from the large external capacitor. The maximum of output transient voltage $\Delta V_{out,max}$ is given by

$$\Delta V_{out,max} \approx \frac{I_{load,max} t_p}{C_L} + \Delta V_{ESR}, \tag{8}$$

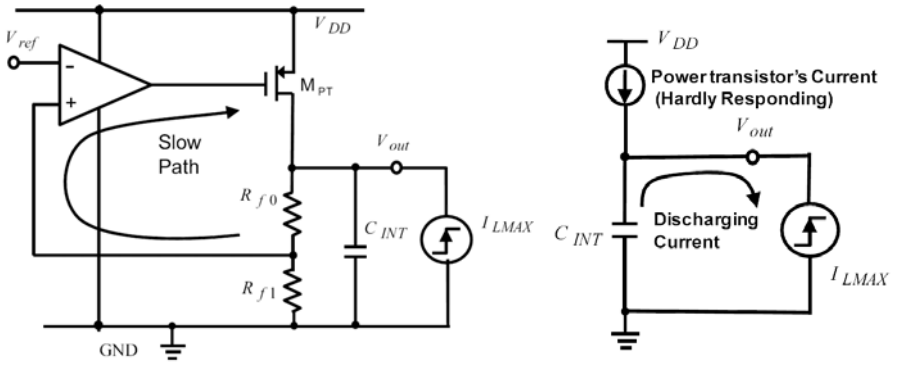
$$t_p \approx \frac{1}{BW_{cl}} + \frac{C_p \Delta V_p}{I_{sr}}, \tag{9}$$

where BW_{cl} is the closed-loop bandwidth of the system, ΔV_p is the voltage variation at the power transistor's gate capacitance C_p, I_{sr} is the output slew-rate current of the error amplifier, and $\Delta V_{ESR} \approx R_{ESR} I_{load,max}$. When $C_L = 4.7\mu\text{F}$, $C_p = 20\text{pF}$, $\Delta V_p = 1\text{V}$, $I_{sr} = 20\mu\text{A}$, $I_{load,max} = 100\text{mA}$, the transition time is 1μs, and BW_{cl} and ΔV_{ESR} are negligible, $\Delta V_{out,max}$ is estimated to about 20mV. However, when the external capacitor is reduced by several orders of magnitude, the transient response is greatly affected. If $C_L = 1\text{nF}$, then the output of the capacitor-less LDO regulator changes about 200V! A large output capacitor and large closed-loop bandwidth improve the load regulation. Conventional LDO regulators inherently have large output capacitors and therefore will have better load regulation versus capacitor-less LDO regulators. So a transient-improvement circuit must be studied in the capacitor-less LDO regulator.

2.4. Transient analysis of capacitor-less LDO regulator

The power transistor comprises the most important element in the LDO regulator transient response. It supplies current to the load impedance to develop the desired output voltage. The extremely large effective gate capacitance contributes the most devastating propagation delay owing to its slewing. The power transistor can only supply the desired current to the load when the gate voltage V_G reaches steady-state after some time delay t_p. The speed of the capacitor-less LDO regulator is mainly determined by the power transistor propagation delay t_p, and the gain-bandwidth product of the error amplifier loop. As shown in Figure 4, when the load current significantly increases from 0mA to I_{LMAX} in 1μs, the power transistor cannot respond immediately and essentially acts as a constant current source. At this time, the output voltage change only affects the drain-source voltage V_{DS} of the power transistor, while the gate-source voltage V_{GS} of the power transistor

still keeps unchanged. So the transient response can be improved greatly only if the output voltage changes can be sensed and the V_{GS} of the power transistor can be controlled accordingly as soon as possible.



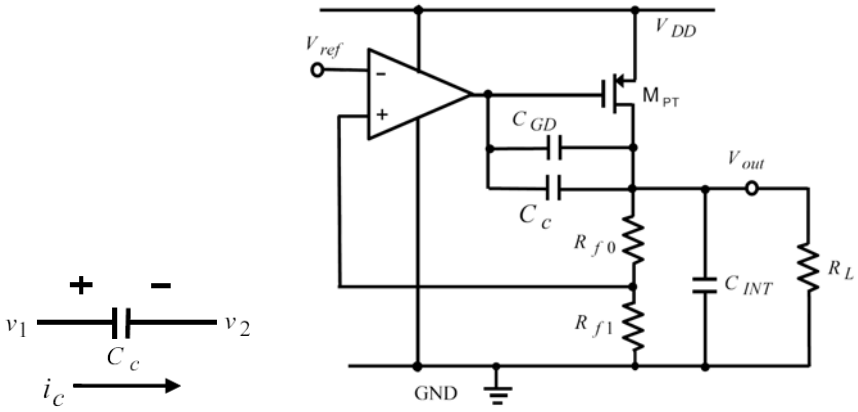
(a) (b)

Figure 4. (a) Transient response of the capacitor-less LDO regulator when the load current rises from 0mA to 100mA and (b) its simple model.

The capacitor-less LDO regulator output voltage sags due to the slow response of the control circuit and the power transistor gate capacitance. The ideal sensing network would relay the output voltage information to the V_G to change V_{GS} without consuming any power or changing the DC operating points of the power transistor. A differentiator sensing network realizes such a function. A basic capacitor differentiator shown in Figure 5(a) has the following characteristics:

$$i_c = C_c \frac{d}{dt}(v_1 - v_2). \tag{10}$$

When one end of the differentiator capacitor is attached to the output voltage node and the other end is attached to the power transistor gate, the output voltage change would induce a gate current proportional to the output voltage change. So the simplest way of capacitor coupling is formed as shown in Figure 5(b), and at the same time, the Miller compensation is formed from the perspective of frequency compensation.



(a) (b)

Figure 5. (a) Basic capacitive differentiator and (b) simplest way of coupling.

However, it is not the best way to improve the transient response. When the load current changes from 0mA to 100mA, the output voltage drops through the power transistor gate voltage change. At the same time, the sensing role of the differentiator capacitor based on equation (10) declines as the voltage across it reduces. In order to enhance the sensing role of the differentiator capacitor C_c must be far greater than the gate-drain capacitance C_{GD} of the power transistor so that the kind of coupling can play a fast pathway. On the other hand, from the perspective of frequency compensation, the differentiator capacitor C_c decreases the frequency of the right-half-plane zero as follows:

$$Z_1 = \frac{g_{mp}}{C_{GD} + C_c}. \tag{11}$$

This results in loop stability degradation. Based on the above analysis, the coupling circuit must be designed to pass only the sensed output signal to the power transistor gate, while also to shield the influence of power transistor gate signal on the LDO regulator output. So a unilateral transient compensation path from the LDO regulator's output to the power transistor gate is required and the minimum delay must be ensured.

In the work in [6], a fast pathway is added to pass the LDO regulator's output change to the power transistor gate, as shown in Figure 6. It uses a capacitor C_f to sense the output voltage transients and the OTA as a unilateral coupling circuit. In this circuit, the current signal through the sensing capacitance C_f is converted to voltage signal by a transimpedance amplifier, and then the voltage signal can be inputted to the OTA, which inadvertently increases the response time of the transient compensation path.

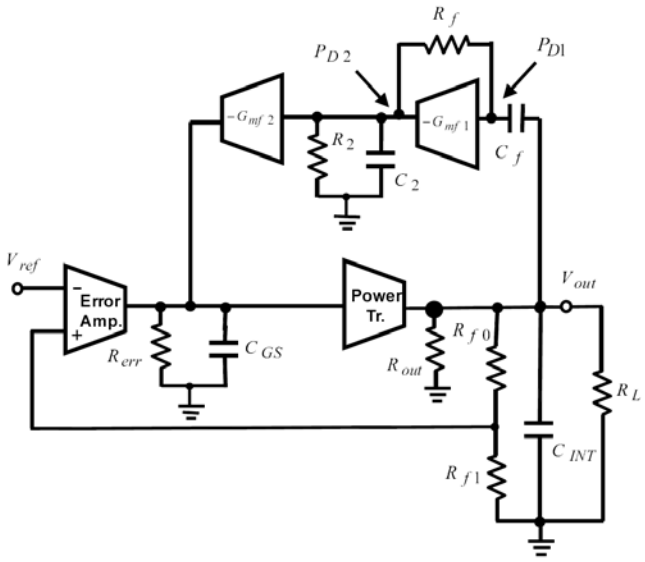
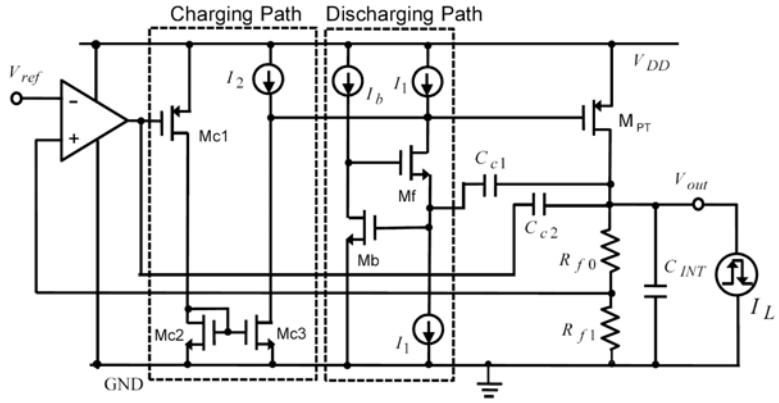


Figure 6. The way of transient response improvement proposed in the literature [6].

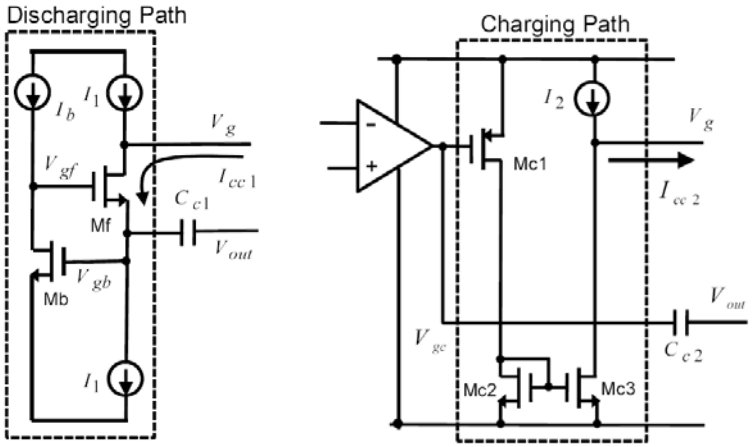
3. Proposed Transient Compensation and Frequency Compensation

The paper aims to improve transient response of the capacitor-less LDO regulator by establishing a new fast transient response path which completes the frequency compensation purposes at the same time. As shown in Figure 7, this paper uses a transient improving path for load current rising from 0mA to 100mA. One end of the sensing capacitance C_{c1} is connected to the end of the LDO regulator output, the other end is connected to the source of a common-gate connected MOS transistor (*Mf*). As the source of *Mf* is an input

node with a very low impedance, the current signal from the sensing capacitor C_{c1} can be entirely passed to the power transistor gate, while the feed-forward path from the gate to the output of LDO regulator is not formed. The sensing capacitor C_{c1} samples the decrease in the output voltage of LDO regulator, and then the source voltage of *Mf* decreases, resulting in a large instantaneous discharge current to the power transistor gate through *Mf*. This unilateral feedback path has very small total delay.



(a)



(b) (c)

Figure 7. (a) The structure of the proposed capacitor-less LDO regulator, (b) the proposed discharging and (c) charging paths in it.

In order to further increase the transient current, a negative feedback is used in this paper, as shown in Figure 7(b). When the sensing capacitor C_{c1} samples the decrease in output voltage, the MOS transistor *Mb* increases the gate voltage of *Mf*, enhancing an instantaneous discharging current to the power transistor gate. On the other hand, negative feedback increases the effective transconductance of *Mf*, reducing equivalent input impedance of the node V_{gb}, thereby speeding up the transient response.

When the load current decreases from 100mA to 0mA, the output voltage rises, the sensing capacitor C_{c1} increases the source voltage of *Mf*, the negative feedback decreases the gate voltage of *Mf*, and then *Mf* becomes off-state. At this time, the bias current I_1 charges the gate capacitor of the power transistor. In order to further increase the transient charging current, this paper designs a charging current path as shown in Figure 7(c): the current signal from the sensing capacitor C_{c2} reflects the rise of the output voltage, and the current signal is amplified by the current mirror [7], resulting in a larger instantaneous charging current to the power transistor gate and thereby speeding up the transient response.

From the perspective of frequency compensation, the small-signal analysis of the proposed discharging and charging path is shown in Figure 7(b), (c).

$$V_{gc} = \frac{sC_{c2}R_1}{1 + sC_{c2}R_1} V_{out}, \tag{12}$$

$$I_{cc1} = g_{mf}(V_{gf} - V_{gb}) = -G_{mfb}V_{gb}, \tag{13}$$

$$I_{cc2} = sC_{c2}R_1(V_{out} - V_{gc})g_{mc1}K_c = \frac{sC_{c2}g_{mc1}K_cR_1}{1 + sC_{c2}R_1} V_{out}. \tag{14}$$

Here $G_{mfb} = (1 + g_{mb}R_b)g_{mf}$, $K_c = g_{mc3}/g_{mc2}$, R_1 is the equivalent output resistance of the op-amp, R_b is the equivalent output resistance of the common-source amplifier with the transistor *Mb* and the current source I_b,

and g_{mc1}, g_{mc2}, g_{mc3}, g_{mf} and g_{mb} are the transconductances of $Mc1$, $Mc2$, $Mc3$, Mf and Mb, respectively. At the same time, equation (15) is obtained

$$I_{cc1} = sC_{c1}(V_{gb} - V_{out}) \tag{15}$$

with equations (13) and (15), I_{cc1} is given by

$$V_{gb} = \frac{sC_{c1}}{G_{mfb} + sC_{c1}} V_{out}, \tag{16}$$

$$I_{cc1} = -\frac{sC_{c1}G_{mfb}}{G_{mfb} + sC_{c1}} V_{out}. \tag{17}$$

With equations (13) and (17), the simple small-signal equivalent circuit of the proposed capacitor-less LDO regulator is shown in Figure 8(a), where g_{mp} is the transconductance of the power transistor, R_{out} is the equivalent resistance of output node, C_{INT} is the equivalent output capacitor of the proposed LDO regulator, R_2 is the equivalent output resistance of the common-source amplifier with the transistor $Mc3$ and the current source I_2, I_{in} is the output current of the op-amp output. With Norton-equivalent-current-equation, equations (18) and (19) are obtained

$$\frac{V_g}{R_2} + sC_{GD}(V_g - V_{out}) + I_{cc1} - I_{cc2} = g_{mc1}R_1K_cI_{in}, \tag{18}$$

$$\frac{V_{out}}{R_{out}} + sC_{INT}V_{out} - sC_{GD}(V_g - V_{out}) = I_{cc1} - g_{mp}V_g. \tag{19}$$

Thus, the transfer function is given by:

$$\frac{V_{out}}{I_{in}} = -g_{mp}g_{mc1}K_cR_1R_2R_{out}\left(1 - \frac{sC_{GD}}{g_{mp}}\right)\frac{\left(1 + \frac{sC_{c1}}{G_{mfb}}\right)(1 + sC_{c2}R_1)}{1 + As + Bs^2 + Cs^3 + Ds^4}, \tag{20}$$

$$A \approx g_{mp}R_2R_{out}(C_{c1} + C_{c2}g_{mc1}K_cR_1), \tag{21}$$

$$B \approx g_{mp}R_1R_2R_{out}C_{c1}C_{c2}\left(1+\frac{g_{mc1}K_c}{G_{mfb}}\right), \tag{22}$$

$$C \approx \frac{g_{mp}R_1R_2R_{out}C_{GD}C_{c1}C_{c2}}{G_{mfb}} \approx 0, \tag{23}$$

$$D \approx \frac{R_1R_2R_{out}C_{GD}C_{INT}C_{c1}C_{c2}}{G_{mfb}} \approx 0, \tag{24}$$

where $C_{GD} \ll C_{c1}, C_{c2}$. So the two poles and three zeros are given by:

$$P_1 \approx -\frac{1}{g_{mp}R_2R_{out}(C_{c1}+C_{c2}g_{mc1}K_cR_1)}, \tag{25}$$

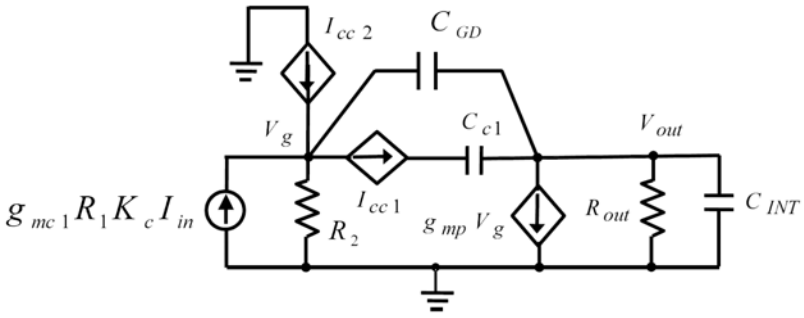
$$P_2 = \frac{1}{BP_1} \approx -\frac{1}{R_1C_{c2}}\frac{1+\frac{g_{mc1}K_cR_1C_{c2}}{C_{c1}}}{1+\frac{g_{mc1}K_c}{G_{mfb}}}, \tag{26}$$

$$Z_1 = -\frac{1}{C_{c2}R_1}, \tag{27}$$

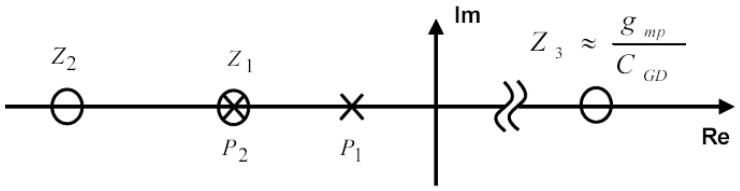
$$Z_2 = -\frac{G_{mfb}}{C_{c1}}, \tag{28}$$

$$Z_3 = \frac{g_{mp}}{C_{GD}}. \tag{29}$$

From equations (25)-(29), with multiplied capacitance and Miller compensation, P_1 and P_2 are effectively split, P_2 are far away from P_1, and the effect of P_2 can be cancelled by Z_1 locating near P_2 when $G_{mfb} \gg g_{mc1}K_c$ and $C_{c1} \gg g_{mc1}K_cR_1C_{c2}$. Considering the effect of C_{GD}, the right-half-plane zero Z_3 appears far away from these poles and zeros. Figure 8(b) shows the poles and zeros of the proposed capacitor-less LDO regulator.



(a)



(b)

Figure 8. (a) Small-signal equivalent circuit and (b) its poles and zeros of the proposed capacitor-less LDO regulator.

By using a combination of fast transient compensation and frequency compensation, the proposed LDO regulator provides a fast transient response, as well as good stability during the whole variation of load current.

4. Circuit Design and Experimental Results

The proposed LDO regulator is designed and fabricated in a 0.18μm CMOS process. Figure 9 shows the complete schematic of the proposed LDO regulator. R_f is connected in series to C_{c2} for additional zero cancellation. Note that *Mc*1, *Mc*2 and *Mc*3 in Figure 9 realize the additional gain-stage with Miller capacitor C_{c2}. C_0 is also connected in parallel to *Mb* for more stable frequency response. The simulated results of the loop gain of the designed LDO regulator show that the phase margin is better than 70° for all cases, as shown in Figure 10.

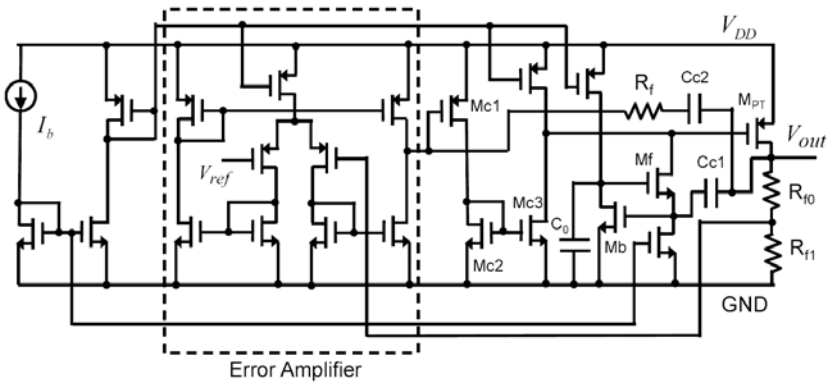


Figure 9. Schematic of the designed capacitor-less LDO regulator.

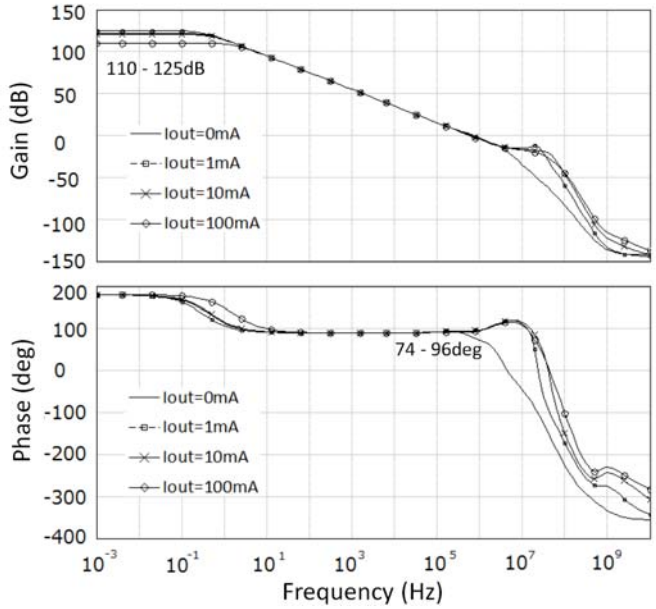


Figure 10. AC simulation results of loop gain of the designed capacitor-less LDO regulator (V_{DD} = 2.6V, C_L = 100pF).

The micrograph of the fabricated LDO regulator is shown in Figure 11 and the core area occupation is 0.15mm^2 including the bandgap reference circuitry. From the experimental results, we can see that the proposed LDO regulator keeps good stability without using any load capacitors.

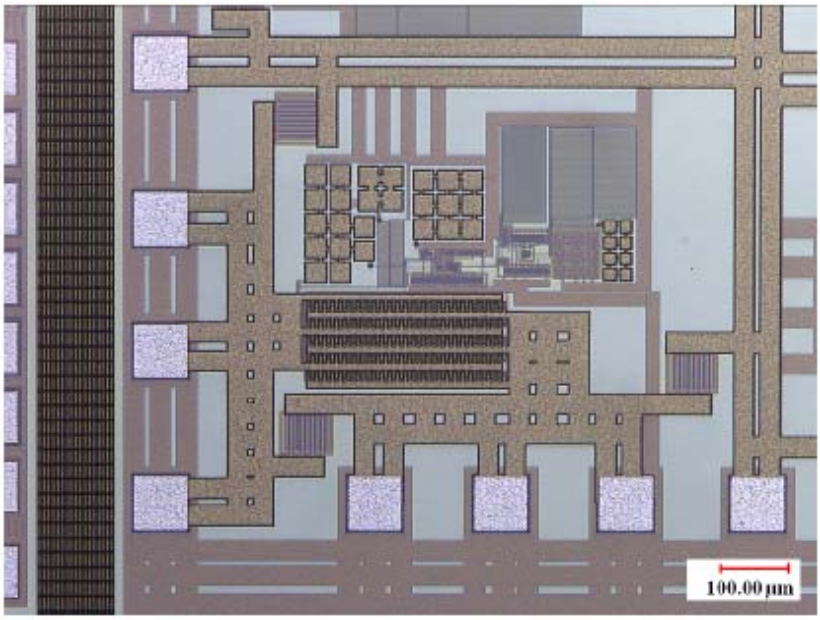


Figure 11. Micrograph of the fabricated capacitor-less LDO regulator.

The measured supply current of the proposed LDO regulator (I_q) is 54μA at 2.6V supply at room temperature, in which about 10μA is estimated to be consumed by the bandgap reference circuit. The input voltage range of the LDO regulator is design from 1.7V to 3V and the LDO regulator can deliver up to 100mA with a dropout voltage of 300mV.

Figure 12 shows the measured PSRR response of the proposed LDO regulator at different load currents. The PSRR at 10kHz are about −36dB, −35dB and −29dB at 1mA, 10mA and 100mA load currents, respectively. As seen from the results, the proposed LDO regulator attains about –20dB PSRR up to 100kHz. The equivalent output noise was measured for different load currents, as shown in Figure 13. The worst case spot noise at 10kHz was roughly $1.0\mu V/\sqrt{Hz}$ and was mainly due to $1/f$ noise.

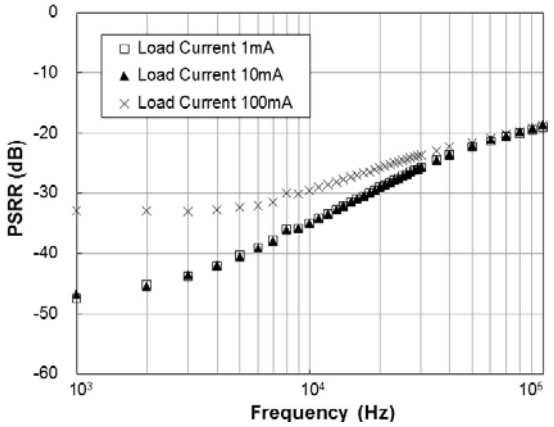


Figure 12. Measured PSRR response of the fabricated capacitor-less LDO regulator (V_{DD} = 2.6V).

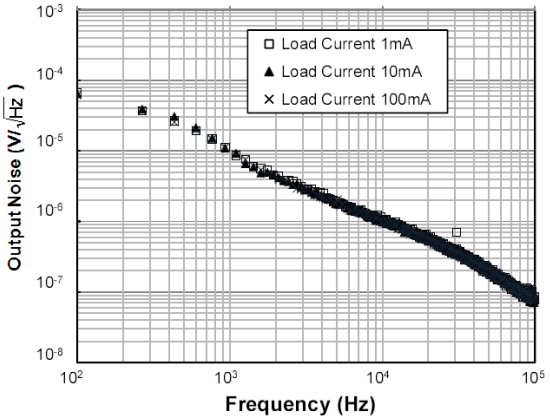


Figure 13. Measured equivalent output noise of the fabricated capacitor-less LDO regulator (V_{DD} = 2.6V).

Figure 14 shows the measured line regulation at different load currents (e.g., 1mA, 10mA and 100mA). The measured line regulation is 7.5mV/V at 1mA load current and 4.3mV/V at 100mA load current. The load regulation at 2.6V supply is measured to be about 330μV/mA.

Figure 15 shows the load transient response of the proposed LDO regulator, where DC-cut output voltage waveform is used. The load current is

switched between 0mA and 100mA within 10μs. Thanks to both the charge and discharge paths to improve the transient response, the fabricated LDO regulator can respond quickly accurately even under this large load transient situation. The LDO regulator can recover the output voltage within 15μs for this large load current change and the voltage derivation is less than 30mV, which includes output under/overshoots and load regulation variations.

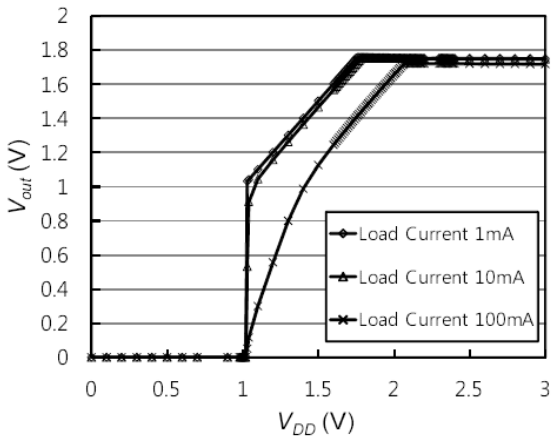


Figure 14. Measured line regulation of the fabricated capacitor-less LDO regulator.

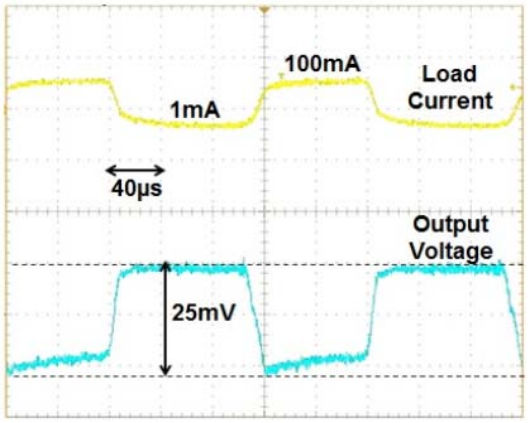


Figure 15. Load transient response of the fabricated capacitor-less LDO regulator (load current frequency: 5kHz, V_{DD} = 2.6V).

Table 1 shows a performance comparison of some previously reported LDO regulators with the proposed one. It is noted that the proposed LDO regulator has comparatively small load transient deviations and response time, attributed to the charge and discharge paths in the circuit.

Table 1. Performance comparison of some previously reported LDO regulators with the proposed one

	[6]	[7]	[8]	This work
Technology (μm)	0.35	0.35	0.6	0.18
$I_{load,max}$ (mA)	50	150	100	100
V_{out} (V)	2.8	1.8	1.3	1.7
V_{drop} (mV)	200	200	200	300
I_q (μA)	65	27	38	54
C_L (F)	100p	1μ	0	0
Area (mm^2)	0.12	0.409	0.307	0.15
ΔV_{out} (mV) (full load transient)	<90	<70	<150	<30
Settling time (μs)	≈15	≈5	≈2	≈15
PSRR@1kHz (dB)	−57	−40	< −60	−33
Loop gain (dB)	55-62	58-87	90-110	110-125

5. Conclusion

In this paper, an LDO regulator based on the proposed fast discharge and charge current paths has been presented. The proposed topology cannot only improve the transient response but also achieve the frequency compensation. The experimental results show that the recovery time of the LDO regulator is less than 15μs and the variation voltage is less than 30mV when the load current changes between 1mA and 100mA. The line and the load regulations

are 4.3mV/V at 100mA load current and 330μV/mA at 2.6V supply. The reduced board real estate, pin count, and good transient response will greatly benefit the SoC designs.

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