論 文 内 容 の 要 旨

氏 名 (福田 大輔)	
論文題名	A Study on Modeling and Mitigating Wire Shape Variation with Measurement Data Analysis (測定データを用いた配線形状ばらつきのモデル化および抑制手法に関する研究)

論文内容の要旨

This thesis discusses prediction and mitigation methods of wire shape variation. Wire shape variations have a large impact on chip performance and yield, but they are found after manufacturing process. Once unacceptable wire shape variation is detected from fabricated chips, process or chip layout tunings are launched. Hence, this conventional countermeasure costs a huge amount of time and money. In addition, this conventional countermeasure may be applied iteratively in trial-and-error manner because the effect of tunings cannot be estimated correctly before fabrication. In the worst case, the iteration does not converge and acceptable shape cannot be obtained.
In nano-scale processes, copper interconnect is mainly adopted and formed with damascene fabrication process. Wire shape variations of copper interconnect consist of wire width variation and wire height variation. Additionally, in recent advanced technologies, irregular open / short error called Edge-over-Erosion error (EoE-error) occurs frequently. This error is hardly predicted in conventional simulation models. The purpose of this thesis is to predict wire shape variations accurately and to mitigate its impact before manufacturing for improving yield and productivity. For this purpose, the main causes of each variation need to be identified first. Then, an accurate prediction model for each variation is constructed with analysis of measurement data obtained from manufacturing process and chip layout characteristics extracted from chip design data.

This thesis firstly presents a prediction model of wire width variation. The main cause of unexpected wire width variations originates from etching process. The analysis of measurement data and chip layout characteristics reveals that wire width variation heavily depends on the chip layout even distant from a wire of interest. From this fact and qualitative properties of etching process, this thesis proposes a prediction model. This thesis also proposes a wire width adjustment method that tunes the etching process on the fly using the proposed prediction model. Experimental results show that the proposed wire width adjustment method reduces the gap between target value and real value by 68.9% in a test case.

This thesis secondly presents a mitigation method of wire height variation with ECP (Electro-Chemical Plating) and CMP (Chemical Mechanical Planarization) prediction models. ECP is a copper deposition process to fill up wire trenches and CMP is a technique to remove redundant copper after ECP.

In this thesis, three problems which the mitigation method faces for the practical use are discussed: how to efficiently handle huge chip data, insufficient accuracy of ECP model, and how to predict hard-to-detect errors effectively. To solve these problems, this thesis develops an efficient data extraction tool from GDSII data format. In addition, this tool extracts necessary data quickly from the information on dummy fill modification without updating GDSII file. Therefore, this tool can reduce large processing cost of layout characteristics extraction and dummy fill modification. This study then improves an ECP process prediction model. Although ECP process strongly affects the final chip surface topography, the accuracy of existing ECP prediction model is not sufficient. The improved model can reduce the error of initial copper shape by 51.1% - 68.2%. Based on these methods, an effective hot-spot detection method considering die-to-die variations is devised, where a hot-spot is defined as the point which may degrade timing or manufacturing yield due to the wire height variations occurred in ECP and CMP processes. Die-to-die variations have a great impact on final wire height variations, but ECP and CMP prediction models cannot take care of die-to-die variations directly. Thus, this work defines corner conditions of ECP and CMP process variations, and finds the short-error in those corner conditions. By performing the model-guided layout modification to eliminate these error, wire height variations of chip surface is reduced by 84.4% and these short-errors are avoided before manufacturing.

Finally, this thesis proposes an EoE-error prediction method in CMP process with a novel multi-level machine learning technique. EoE-errors occur at copper removal stage of CMP process at which multiple materials are polished simultaneously. The cause of this error is unexpected over-polishing with more than ten times larger removal rate of copper than ordinary rate, which leads to open errors. On the other hand, the mechanism of EoE-error occurrence is complicated and is not understood well enough. Therefore, to find parameters which affect EoE-error, data analysis is executed with error measurement data of a test chip and its layout characteristics. An EoE-error prediction model is constructed from these parameters using the proposed multi-level machine learning method. Experimental results show that the proposed method can predict EoE-errors with 89.6-89.7% accuracy.

With utilizing these proposed methods, wire shape variations occurred in manufacturing process can be estimated before fabrication, and the risk of chip performance reduction and yield loss can be mitigated in design time.

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論文審査の結果の要旨及び担当者

氏　名	（　福田　大輔　）

	（職）	氏　名
論文審査担当者	主 査　教授	尾上 孝雄
	副 査　教授	中前 幸治
	副 査　准教授	橋本 昌宜

論文審査の結果の要旨

本論文は、測定データを活用したVLSI製造工程における配線形状ばらつきの見積もりと低減に関する研究の成果をまとめたものであり、以下の主要な結果を得ている。

1. 配線幅ばらつきの見積もりと低減

エッチング工程に起因する配線幅ばらつきの低減手法について議論している。チップの測定データと設計レイアウトの解析により、遠く離れたレイアウトも配線幅に影響を与えることを確認している。この解析結果に基づき、配線幅ばらつきの見積もりモデルを提案している。さらに、配線幅ばらつきの見積もり結果を用いて即座にエッチング工程を調整し、配線幅ばらつきを低減する手法を提案している。提案手法を適用することにより、配線幅のずれを68.9%、ばらつきを40.9%低減できることを実験的に示している。

2. 配線高さばらつきの見積もりと低減

ECP (Electro-Chemical Plating)とCMP (Chemical Mechanical Planarization)の見積もりモデルに基づく配線高さ低減手法を提案している。巨大な設計データの効率的な取り扱い、ECPモデルの精度改善、ならびにチップ間ばらつきの考慮により、レイアウト修正による配線高さばらつきの低減を実用化している。実験により、ECPモデルの精度が51.1%から68.2%改善したことを確認している。チップ間ばらつきの考慮により、これまで発見することができなかったショート故障の発見を可能としている。提案手法を適用により、配線高さばらつきを84.4%削減し、ショート故障を製造前に取り除くことが出来ることを実験的に示している。

3. EoE (Edge-over-Erosion)故障の見積もり

近年の先端プロセスで顕在化しつつあるEoE故障の見積もり手法を提案している。EoE故障は複数の材料をCMP工程で研磨しているときに発生するが、その発生条件は十分に解明されていない。本論文では、チップの測定結果の解析によりEoE故障に影響を与えるパラメータを特定し、機械学習を複数段に適用することにより、EoE故障の発生を予期する見積もりモデルを構築している。実験により、見積もりモデルの精度が89.6%から89.7%の精度であることを示し、製造前にEoE故障の発生の見積もりが可能であることを確認している。

以上のように、VLSI製造工程における配線形状ばらつきの見積もりと低減に関する研究は、微細製造プロセスで製造されるVLSIの歩留まり向上という点において非常に有用である。特に発生条件やメカニズムが解明されていない現象についても測定データを有効に活用した見積もり手法を提示しており、本論文は先端VLSIの製造歩留まりに寄与するものと期待できる。従って、博士（情報科学）の学位論文として価値のあるものと認める。