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Title	A Study on Modeling and Mitigating Wire Shape Variation with Measurement Data Analysis
Author(s)	福田, 大輔
Citation	大阪大学, 2015, 博士論文
Version Type	VoR
URL	https://doi.org/10.18910/53944
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A Study on Modeling and Mitigating Wire Shape Variation with Measurement Data Analysis

Submitted to
Graduate School of Information Science and Technology
Osaka University

July 2015

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Publication list

Journal papers

1. D. Fukuda, K. Watanabe, N. Idani, Y. Kanazawa, and M. Hashimoto, “Edge-over-Erosion Error Prediction Method Based on Multi-Level Machine Learning Algorithm,” *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E97-A, no. 12, pp. 2373-2382, Dec. 2014.
2. D. Fukuda, K. Watanabe, Y. Kanazawa, and M. Hashimoto, “Modeling the Effect of Global Layout Pattern on Wire Width Variation for On-the-Fly Etching Process Modification,” *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E98-A, no. 07, pp. 1467-1474, Jul. 2015.

Conference papers with referee

1. D. Fukuda, T. Shibuya, N. Idani, and T. Karasawa, “Full-Chip CMP Simulation System,” In *International Conference on Planarization/CMP Technology (ICPT)*, pp. 187-194, Oct. 2007.

Conference papers without referee

1. D. Fukuda, I. Nitta, Y. Kanazawa, T. Shibuya, N. Idani, T. Karasawa, O. Yamasaki, and M. Ito, “Yield Enhance Technique Using CMP Simulation in Design and Manufacturing Process,” In *Proceedings of IPSJ DA Symposium*, pp. 271-276, Aug. 2008 (in Japanese)
2. D. Fukuda, H. Matsuoka, and T. Shibuya, “Modeling of Layout Dependent Copper Electrochemical Plating,” In *IEICE Technical Report*, VLD2006-15, vol. 106, no. 113, pp.7-12, Jun. 2006 (in Japanese)

Abstract

This thesis discusses prediction and mitigation methods of wire shape variation. Wire shape variations have a large impact on chip performance and yield, but they are found after manufacturing process. Once unacceptable wire shape variation is detected from fabricated chips, process or chip layout tunings are launched. Hence, this conventional countermeasure costs a huge amount of time and money. In addition, this conventional countermeasure may be applied iteratively in trial-and-error manner because the effect of tunings cannot be estimated correctly before fabrication. In the worst case, the iteration does not converge and acceptable shape cannot be obtained.

In nano-scale processes, copper interconnect is mainly adopted and formed with damascene fabrication process. Wire shape variations of copper interconnect consist of wire width variation and wire height variation. Additionally, in recent advanced technologies, irregular open / short error called Edge-over-Erosion error (EoE-error) occurs frequently. This error is hardly predicted in conventional simulation models. The purpose of this thesis is to predict wire shape variations accurately and to mitigate its impact before manufacturing for improving yield and productivity. For this purpose, the main causes of each variation need to be identified first. Then, an accurate prediction model for each variation is constructed with analysis of measurement data obtained from manufacturing process and chip layout characteristics extracted from chip design data.

This thesis firstly presents a prediction model of wire width variation. The main cause of unexpected wire width variations originates from etching process. The analysis of measurement data and chip layout characteristics reveals that wire width variation heavily depends on the chip layout even distant from a wire of interest. From this fact and qualitative properties of etching process, this thesis proposes a prediction model. This thesis also proposes a wire width adjustment method that tunes the etching process on the fly using the proposed prediction model. Experimental results show that the proposed wire width adjustment method reduces the gap between target value and real value by 68.9% in a test case.

This thesis secondly presents a mitigation method of wire height variation with ECP (Electro-Chemical Plating) and CMP (Chemical Mechanical Planarization) prediction models. ECP is a copper deposition process to fill up wire trenches and CMP is a technique to remove redundant copper after ECP process. In this thesis, three problems which the mitigation method faces for the practical use are discussed: how to efficiently handle huge chip data, insufficient accuracy of ECP model, and how to predict hard-to-detect errors effectively. To solve these problems, this thesis develops an efficient data extraction tool from GDSII data format. In addition, this tool extracts necessary data quickly from the information on dummy fill modification without updating GDSII file. Therefore, this tool can reduce large processing cost of layout characteristics extraction and dummy fill modification. This study then improves an ECP process prediction model. Although ECP process strongly affects the final chip surface topography, the accuracy of existing ECP prediction model is not sufficient.

The improved model can reduce the error of initial copper shape by 51.1% - 68.2%. Based on these methods, an effective hot-spot detection method considering die-to-die variations is devised, where a hot-spot is defined as the point which may degrade timing or manufacturing yield due to the wire height variations occurred in ECP and CMP processes. Die-to-die variations have a great impact on final wire height variations, but ECP and CMP prediction models cannot take care of die-to-die variations directly. Thus, this work defines corner conditions of ECP and CMP process variations, and finds the short-error in those corner conditions. By performing the model-guided layout modification to eliminate these error, wire height variations of chip surface is reduced by 84.4% and these short-errors are avoided before manufacturing.

Finally, this thesis proposes an EoE-error prediction method in CMP process with a novel multi-level machine learning technique. EoE-errors occur at copper removal stage of CMP process at which multiple materials are polished simultaneously. The cause of this error is unexpected over-polishing with more than ten times larger removal rate of copper than ordinary rate, which leads to open errors. On the other hand, the mechanism of EoE-error occurrence is complicated and is not understood well enough. Therefore, to find parameters which affect EoE-error, data analysis is executed with error measurement data of a test chip and its layout characteristics. An EoE-error prediction model is constructed from these parameters using the proposed multi-level machine learning method. Experimental results show that the proposed method can predict EoE-errors with 89.6-89.7% accuracy.

With utilizing these proposed methods, wire shape variations occurred in manufacturing process can be estimated before fabrication, and the risk of chip performance reduction and yield loss can be mitigated in design time.

Acknowledgments

First of all, I would like to express my deepest gratitude to Professor Takao Onoye in Osaka University for providing me a precious opportunity and an excellent environment to study as a doctoral student in his laboratory.

I have no adequate words to express my heartfelt appreciation to Associate Professor Masanori Hashimoto in Osaka University. All of my productive researches are credited to none other than him. His advanced perspective and thoughtful advises led me to successful achievements.

I would like to express my appreciation to Professor Kouji Nakamae in Osaka University for detailed review and insightful suggestions.

I am deeply grateful to Professor Masaharu Imai, Professor Tatsuhiro Tsuchiya, Professor Haruo Takemura, Professor Makoto Nakamura, Professor Akihisa Yamada, and Professor Yasuhiro Yoshida in Osaka University for useful advices.

I would like to express my sincere appreciation to Professor Hidetoshi Onodera in Kyoto University, Professor Kazutoshi Kobayashi in Kyoto Institute of Technology, for their valuable lectures of VLSI design.

I would like to express my sincere appreciation to Mr. Shinichi Wakana, Mr. Kaoru Kawamura, and Mr. Toshiyuki Shibuya in Fujitsu Laboratories LTD. for providing me an opportunity to go to Osaka University for a doctoral course. Without their guidance and encouragement this thesis would not have been possible.

I would like to express my gratitude to Mr. Naoki Idani in Mie Fujitsu Semiconductor LTD., Mr. Kenichi Watanabe in Fujitsu Semiconductor LTD., Mr. Toshiyuki Karasawa in Fujitsu Ltd., Ms. Izumi Nitta, Mr. Yuji Kanazawa in Fujitsu Laboratories LTD., for their helpful advices, discussion, feedback, and guidance that allowed this research to progress.

I owe my deepest gratitude to Mr. Hidetoshi Matsuoka, Dr. Takahide Yoshikawa, Dr. Rafael Kazumiti Morizawa, Mr. Tatsuru Matsuo, Mr. Tsutomu, Ishida, Mr. Toshiro Uchida, Mr. Ryo Endo in Fujitsu Laboratories LTD., Mr. Masaru Ito, Mr. Osamu Yamasaki, Mr. Eizi Kondo in Socionext Inc., for their insightful comments and suggestions.

This work is supported by Fujitsu Laboratories LTD. I thank for permission to study in Osaka University. The integrated chips in this thesis has been fabricated and measured in Mie Fujitsu Semiconductor LTD.

I would like to thank Ms. Yuki Yoshida, and Ms. Tomomi Kondo for their various supports throughout my student life.

Finally I would like to thank my wife Ayumi and my son Michiyuki for their encouragements and assistance throughout my career. For their support, I dedicate this thesis to them.

Contents

Chapter 1 Introduction 1
1.1 Sources of wire shape variations 1
1.1.1 Lithography 2
1.1.2 Etching 3
1.1.3 ECP and CMP 3
1.1.4 Effects of each process on wire shape variation 5
1.2 Problems in manufacturing processes 6
1.2.1 Wire width variation 7
1.2.2 Wire height variation 7
1.2.3 EOE-error 7
1.3 Objective of this thesis 8

Chapter 2 Modeling the effect of global layout pattern on wire width Variation for On-the-Fly Etching Process Modification 13
2.1 Introduction 13
2.2 Overview of etching process 15
2.3 Prediction and mitigation of wire width variation 17
2.3.1 Definitions 17
2.3.2 Proposed prediction model 19
2.3.3 On-the-fly wire width adjustment via etching process modification 20
2.4 Experimental results 22
2.5 Conclusion 25

Chapter 3 A practical wire height mitigation method with ECP and CMP simulation 27
3.1 Introduction 27
3.2 Overview of proposed method for mitigating wire height variation . . . 30
3.2.1 Extraction 30
3.2.2 ECP simulation 31
3.2.3 CMP simulation 31
3.2.4 Hot-spot detection and layout modification 32
3.2.5 Calibration 32
3.3 Issues to be solved for practical use of the proposed method 32
3.3.1 Handling huge chip data 32
3.3.2 Accuracy of ECP model 33
3.3.3 Effective methods for analysis of the results 33
3.4 Proposed approach 33

3.4.1 Chip data extraction with virtual dummy filling method 33
3.4.2 Refined ECP model 34
3.4.3 Effective hot-spot detection method 38
3.5 Experimental results 40
3.6 Conclusion 43

Chapter 4 Edge-over-Erosion error prediction based on multi-level machine learning 45
4.1 Introduction 45
4.2 Concept and overview 47
4.2.1 Concept of EoE-error prediction method 47
4.2.2 Overview of EoE-error prediction method 47
4.3 Error analysis and parameter extraction stages 49
4.4 Model construction and prediction stage 54
4.4.1 Machine learning algorithms 55
4.4.2 Multi-level machine learning algorithm 56
4.4.3 Model construction and prediction flow 58
4.5 Experimental results 59
4.6 Conclusion 63

Chapter 5 Conclusion 65

Bibliography 67

List of tables

2.1 Details of calibration / validation chip designs. 22
2.2 CD loss value of validation chips. 25

3.1 Comparison with commercial tool in extraction process. 42

4.1 Confusion matrix. 54
4.2 Details of calibration / validation chips. 60
4.3 Prediction performance comparison. 60

List of figures

1.1 Manufacturing flow of wire forming. 2
1.2 CMP process apparatus. 4
1.3 Multi stage CMP process. 5
1.4 Cross sectional view of interconnect layer. 8
1.5 General structure of this thesis. 9

2.1 Common test structure on a wafer. 14
2.2 Overview of RIE system. 16
2.3 Anisotropic and isotropic etching. 16
2.4 Sidewall protection. 17
2.5 Relationship between DICD, FICD, and target wire width. 18
2.6 Region for parameter $\overline{m}$ calculation. 20
2.7 Procedure of on-the-fly wire width adjustment via etching process modification. 21
2.8 Estimated etching vs. measured etching bias for calibration data. 23
2.9 Model calibration results with various effective lengths. 23
2.10 Estimated etching vs. measured etching bias for validation data. 25
2.11 CD loss distribution of validation chips. 26

3.1 Definition of dishing and erosion. 28
3.2 Flow for mitigating wire height variation. 29
3.3 Parameters extracted from a mesh. 30
3.4 Definition of height and step height. 31
3.5 Definition of dummy-filling area. 34
3.6 3 patterns of ECP topography. 36
3.7 Relationship between parameter T_e and line width / space. 37
3.8 Relationship between parameter δ_s, δ_e and line width / space. 38
3.9 Relationship between ECP topography and final surface topography. 39
3.10 Wafer-to-wafer variation of copper thickness range within a wafer. 39
3.11 Simulation vs. experimental results of ECP process. 41
3.12 Chip surfaces with effective hot-spot detection method and a modification result. 42

4.1 Cross sectional view of interconnect layer. 46
4.2 Overview of proposed EoE-error prediction method. 48
4.3 Test chip structure. 49
4.4 Relationship between EoE and metal density of module area. 51

4.5 Relationship between EoE and module size. 52
4.6 Definition of effective length. 52
4.7 region for effective density computation. 53
4.8 Density deviation vs. EoE-error occurrence in a 65 nm process. 53
4.9 Detailed shapes of EoE cross section. 54
4.10 Model complexity of SVM method. 57
4.11 Comparison of Accuracy rate of (a) combinations of learning method and (b) number of multi-level. 58
4.12 Detailed flow of construction and prediction stages with multi-level machine learning method. 59
4.13 P_{err}, P_{ok}, and g-mean with various sampling ratio in SVM. 61
4.14 Details of EoE-errors in chip V1a. 62

Chapter 1

Introduction

This chapter describes the background and the objectives of this thesis. This thesis focuses on the modeling of wire shape variations using measurement data and chip layout characteristics. The following sections describe the background of the wire shape variation problems, explain sources of the variations, and present the objective of this thesis.

1.1 Sources of wire shape variations

As the technology of VLSI manufacturing process continues to shrink, it becomes a challenging problem to generate layout patterns that can satisfy performance and manufacturability requirements since design rule sets have become increasingly more complex. Technology scaling also leads interconnect delay to dominate circuit delay [1, 2]. This is because that wire resistance and capacitance increase significantly [2–4] due to the decrease in wire cross sectional area and wire pitch in advanced technologies. Furthermore, coupling capacitance of wires becomes dominant because of high aspect ratio of wire shape [5–7]. Therefore, nowadays the wire geometry has a strong impact on the wire resistance and capacitance, and consequently affects the interconnect delay significantly. On the other hand, in advanced technologies, it is getting difficult to manufacture wires as designed, and wire shape variation is inevitable. As a result, the variation of total wire capacitance can be more than 10% and the variation of wire resistance due to wire shape variation can be over 30%, which results in more than 35% delay variation on long interconnect and may cause yield loss [9–11]. Thus, the wire shape variation is one of the serious issues that degrade chip performance and yield.

Let us review the interconnect fabrication process. Copper (Cu) interconnect is widely applied to 130 nm and below technologies, because of its smaller resistance as compared to aluminum. In the aluminum process, interconnect is patterned by dry etch process. On the other hand, copper interconnect is constructed by damascene fabrication process [12–14]. Figure 1.1 shows the manufacturing flow of copper wire forming with the damascene fabrication process. Lithography, etching, electro-chemical plating (ECP), and chemical mechanical planarization (CMP) are main processes of shaping copper metal wires. In the damascene fabrication process, interconnect trenches and via holes are printed and etched after inter-layer dielectric (ILD) material deposition. Then, a thin barrier metal layer, which facilitates copper film generation, is deposited as a seed layer [14]. Next, copper is deposited to fill up the trenches and holes on the whole wafer surface by ECP process. Finally, copper outside the trenches is removed to generate interconnect patterns. CMP process is a technique to remove redundant copper and to planarize the wafer surface. These processes iterate over layers. This

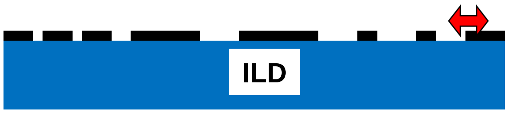
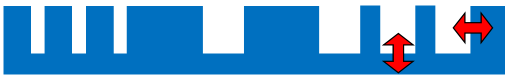
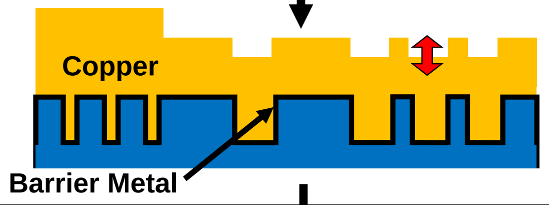
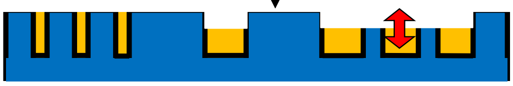
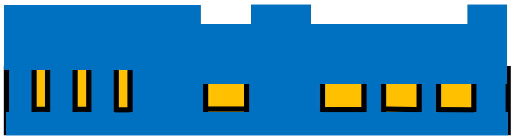
Process		Variation	
		Height	Width
Lithography			✓
Etching		✓	✓
ECP		✓	
CMP		✓	
Continue to upper layer			

Fig. 1.1 Manufacturing flow of wire forming.

section surveys each process of interconnect manufacturing.

1.1.1 Lithography

Lithography is a process to print an image of chip layout pattern on a wafer. Minimum feature size of advanced process technology has become much smaller than the lithographic wavelength (193nm), which results in unavoidable wire shape distortion and consequent wire width variations due to optical diffraction and interference. For enabling the sub-wavelength feature size manufacturing, resolution enhancement technologies (RET) have been developed, such as optical proximity correction (OPC), sub-resolution assist features (SRAF), phase-shift mask (PSM), off-axis illumination (OAI), and double patterning technology (DPT) [8, 15–25]. OPC is the most popular method, and it adds and/or subtracts features to/from the mask patterns to improve the wire shape printed on a wafer. SRAF is a feature introduced to improve the process margin of a resulting wafer pattern, where SRAF itself is not printed on a wafer. PSM controls the phase of the light between adjacent apertures. This method reduces the sensitivity to defocus conditions and achieves high-resolution imaging with good depth of focus (DOF). Here, DOF means the range of distance between the lens and the wafer that appears acceptably sharp in an image. Large DOF value mitigates the distortion in the projected image on unflat wafer surface, where the wafer surface is not perfectly flat throughout the manufacturing process. OAI is an optical system that brings light to the mask at an oblique angle, which enables pattern printing with higher resolution. DPT decomposes a single mask pattern into two masks to increase the pitch size within each mask and improve DOF for higher resolution and better printability. The primal goal of RET techniques is to keep the feature shape printed on a wafer as close to the layout in design time as possible.

1.1.2 Etching

Etching process forms interconnect trenches by removing the material from the wafer surface. Wafers are covered with photoresist except the interconnect pattern [26, 27, 29]. In the etching process, reactive-ion etching (RIE) is a popular technique, and it is a dry etching technique using plasma. Key specifications demanded in this process are high etch rate, high aspect ratio, and straight cross sectional trench sidewall profile. In RIE, free radicals and positive ions react with the wafer surface. Free radicals are electrically activated neutral species. They diffuse over the wafer and react with the surface materials. The positive ions are other reactive species in RIE. The positive ions are accelerated toward the wafer surface by electric field, and they cause both chemical and sputter etching of the surface materials.

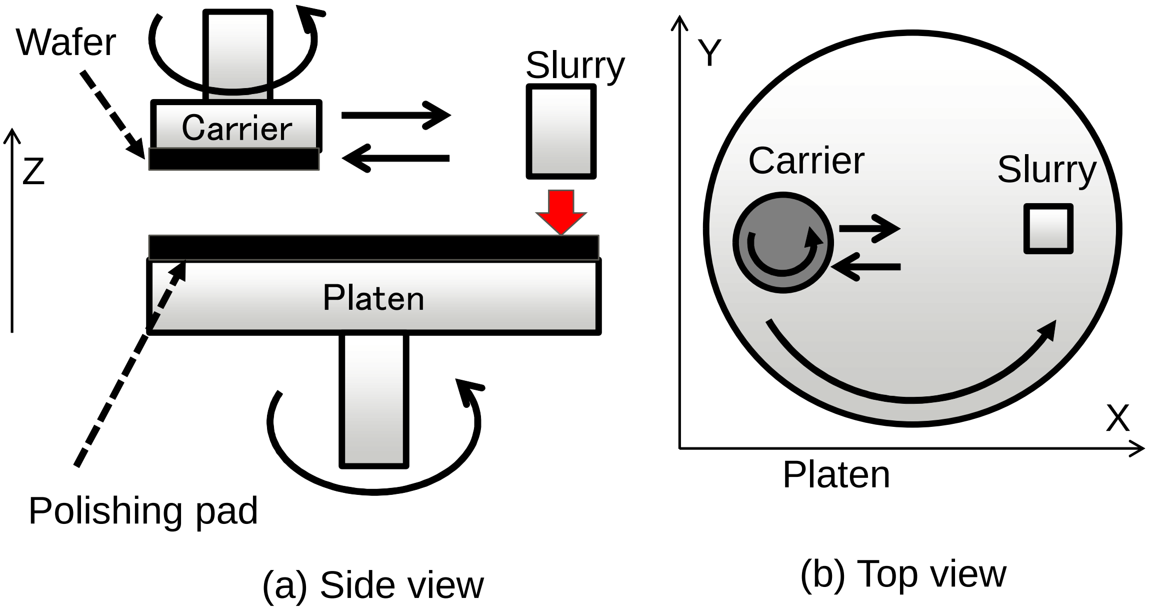
One of the main advantages of RIE method is a high etching rate, which is achieved by the synergy between chemical reaction due to free radicals and ion bombardment due to positive ions [28]. The ion bombardment removes the reaction product on the wafer surface, which helps free radicals react with the wafer surface. The etching rate of the wafer surface using both the species simultaneously is much higher than the rate using individual species separately.

In RIE method, high selectivity and anisotropy are demanded to achieve proper wire trench shape. Selectivity is the ratio of reaction rate between the target material and the others. In etching process, wafer surface is covered with photoresist materials. To dig the trench pattern properly, high selectivity to wafer surface material compared to photoresist is required. Free radicals have high selectivity, but positive ions have low selectivity. Anisotropy is the directional dependence of etching ability. Anisotropic etching can dig the wire trench along the photoresist pattern without undercut, and mitigate wire width variations. Here, undercut means the sidewall material removal under the photoresist pattern. Positive ion drifts toward the wafer surface vertically and its etching process becomes anisotropic. On the other hand, etching mechanism of free radical is an isotropic process which has no directional dependency in etching property.

Sidewall protection mechanism also contributes to the reduction of wire width variation [29–31]. The reaction materials from the surface by etching process is deposited on the sidewall and protected from isotropic etching.

1.1.3 ECP and CMP

ECP is a process to deposit the copper material onto the whole wafer to fill up the trenches after barrier metal deposition, and CMP is a process to remove the copper that overflows the interconnect trenches. ECP and CMP processes have become essential techniques for enabling many-layer damascene process interconnection.



(a) Side view (b) Top view

Fig. 1.2 CMP process apparatus.

ECP is the most popular method for copper deposition. Copper ions in a solution react with the wafer surface and they are deposited [32]. To achieve excellent trench filling capability, chemical additives (accelerator, suppressor, and leveler) in the plating solution play an important role [33–39]. The improvement of overall copper layer planarization benefits the subsequent copper CMP process.

Figure 1.2 shows the CMP process apparatus. In CMP process, wafer is attached to the carrier and pushed down to the platen table which is covered with the polishing pad. The wafer carrier and platen rotate in X-Y plane and the carrier is reciprocated in the radial direction of the platen. The wafer surface is polished with polishing pad in conjunction with CMP slurries. The slurries containing chemicals, fluids, and abrasives are fed on the polishing pad during polishing process. A softened surface layer is formed on a wafer thanks to chemical reactions between the wafer surface materials and slurry chemicals, and the softened layer is then removed by abrasives and polishing pad.

Generally, CMP process consists of multi stage polishing process because the target material in the first half is copper and that in the latter half is copper, ILD, and barrier metal [40–43, 45–47]. These two stages are called copper removal stage, and barrier removal stage, respectively (figure1.3).

The mechanism of CMP process is complicated, and hence CMP process is difficult to tune. CMP process has many parameters, such as polishing pressure, rotating speed of platen and wafer, slurry flow rate, polishing time, and consumable (polishing pad, slurry) characteristics. They all affect the wafer surface topology, and these parameters have different values in each stage. Especially barrier removal stage is very complex because multiple materials that have different polishing rate should be simultaneously polished to achieve high uniformity of wafer surface. Due to this, layout patterns affect the uniformity of wafer surface. Layout patterns include not only wire density / shape of target location but also those of its surrounding layout.

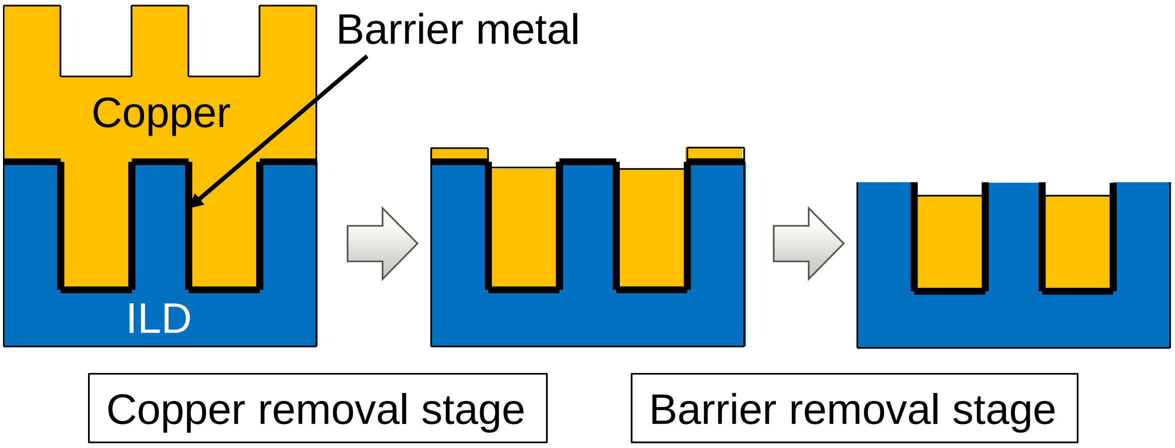


Fig. 1.3 Multi stage CMP process.

The detail of each stage of multi-stage CMP process is described in the following.

1. **Copper removal stage**
   In this stage, copper is mainly polished to reduce ECP induced height variation. To achieve good planarity, it is crucially important when the copper removal stage ends and the successive barrier removal stage starts. This stage transition is performed once barrier metal is detected at a specified wafer point by a sensor in the platen table. This barrier metal detection is called endpoint detection. After the endpoint detection, the removal process continues for a certain time to clearly remove the copper on the barrier metal across a wafer. This duration is called overpolishing time, and it adjusts the amount of copper removal to achieve the target height. In this stage, high etching rate of copper and high selectivity of copper to barrier metal are required for achieving high throughput and small surface height variation.
2. **Barrier removal stage**
   After the copper removal, the copper in the wire trench, the barrier metal on the sidewall of the wire trench and on the surface between the trenches, and the ILD below the barrier metal between the trenches are polished simultaneously. The CMP process parameters and removal selectivity between these materials are carefully selected to achieve the target height without sacrifice of surface uniformity.

1.1.4 Effects of each process on wire shape variation

Wire shape variation consists of wire height variation and wire width variation. In addition, wire open / short error originating from the wire manufacturing flow is often observed in advanced technology [48]. Open / short error causes malfunctions of circuits. This phenomenon can be regarded as a result of severe wire shape variation.

Wire height variation mainly depends on ECP / CMP and etching process. Trench depth variation in etching process causes non-uniformity of the bottom of interconnect trenches, but an etch stop layer (ESL) technique provides good control of the trench depth variation. This ESL technique exploits large selectivity difference between wafer material and ESL [49].

Non-uniformity of the upper surface of wire metal is affected by the initial height of metal deposited in ECP and the amount of metal removed in CMP. To reduce the upper surface variation, several methods are proposed that restrict the acceptable metal density in a small range, where the range of acceptable metal density is one of the most effective parameter to reduce the ECP / CMP wire height variation [50–56].

Wire width variation occurs in lithography, etching, and CMP process. Wire pattern printed on a wafer in lithography process is affected by its surrounding patterns because of the diffraction effects of optical sub-wavelength lithography. Therefore, several RET, which are introduced in section 1.1.1, are adopted to reduce process variation. On the other hand, the DOF requirements of the lithography process become stringent in advanced process technology. The nonplanarity of lower layer according to CMP variation propagates to upper layer, which consumes the DOF budget and makes wire pattern printed in lithography process ambiguous [10, 51]. This printed pattern degradation results in wire width variation. Etching also influences the wire width variation because of the variation of horizontal etching performance. Both lithography and etching process are influential in wire width variation, but etching process is more influential. It is because it finalizes the variation while the variation in lithography process can be mitigated in successive etching process.

Conventional wire open / short error occurs in lithography process. Wire shape distortion in subwavelength lithography process causes bridging between wires and wire disconnection. To prevent these errors, RET techniques are widely used [8, 15–25]. On the other hand, CMP is another major factor of open / short error occurrence in advanced technologies. Improper polishing process causes over-polishing and consequent disconnection, or copper residue between wires and consequent short error. Furthermore, wafer height variation propagates to upper layer and it increases the occurrence of open / short error at upper layer [2, 32]. Recently, Edge-over-Erosion error (EoE-error), which was hardly observed in aluminum interconnect technology, occurs frequently. This is a wire defect caused by irregular over-polishing in CMP process. The detail of this error will be explained in section 1.2.3.

1.2 Problems in manufacturing processes

As discussed in the previous section, wire shape variation has a large impact on chip performance. In practical manufacturing process, various countermeasures against the variation are taken.

RET techniques are adopted to reduce variation in lithography process. The wire thickness non-uniformity in CMP process is dependent on variations of layout characteristics, such as wire width and density, and hence dummy fill technique is applied [50–56], where dummy fill is a non-functional feature inserted to the layout for reducing variations in layout characteristics.

In CMP process, many process parameters and physical or chemical property values of consumable materials affect the chip surface topography [57–63, 65], and their mutual relation to the surface uniformity is complicated. Therefore, predicting thickness variations before manufacturing with CMP prediction model is becoming essential to appropriately tune the CMP process. However, it is impractical to consider all the process parameters in the prediction model because of the model complexity and exorbitant runtime. Due to this fact, CMP prediction model is often constructed with a small number of parameters which can be changed dynamically during CMP process and have a large influence on the results. CMP prediction model also includes a few model parameters which are adjusted to improve prediction accuracy. Calibration process is executed for adjusting those model parameters with experimental data. It should be noted that the obtained CMP prediction model is effective only when other parameters that are not included in the prediction model are unchanged from the experimental data used for calibration. Hence, another calibration process using different experimental data is required once the parameters that are not included in the prediction model are changed.

In spite of these efforts against variation, there are problems in an actual wire manufacturing process. This section briefly summarizes the problems.

1.2.1 Wire width variation

In actual manufacturing, unexpected large variation in wire width that has an impact on chip yield is observed. More specifically, such a large variation mainly originates from etching process, and hence the chip layout variation is a key contributor to the variation. Generally, common test structures to monitor the manufacturing process are placed on a wafer and wire width in these structures are measured and monitored. Reference [83] reported that the surrounding area which affected the etching process was smaller than the test structure size, and hence it was expected that the chip layout could not affect the etching process at the test structure location. However, in reality, a systematic wire width variation originating from the chip layout is observed. A prediction model of wire width variation which takes into account the surrounding layout pattern in a wider range around the test structure is needed.

1.2.2 Wire height variation

Although several ECP and CMP prediction models are proposed to estimate the surface planarity of the chip, the prediction accuracy is not high enough especially in ECP prediction in practical manufacturing process, which results in a large estimation error of wire height. In addition, large variations occur only in specific regions of wafer and it is difficult to predict these errors without considering die-to-die variations in ECP and CMP processes. An effective method to identify the region of large variations in design time should be developed.

1.2.3 EOE-error

As mentioned in section 1.1.4, EoE-errors have arose in advanced technologies. Figure1.4 shows the cross sectional view of EoE-error. Dishing is defined as the height difference between copper and ILD, and erosion is defined as the difference between initial and final ILD heights. EoE-error is the localized over-polishing error which is often seen near pattern edges. Copper metal is removed more than ten times faster than its ordinary removal rate at the place where EoE-error occurs. Empirically, EoE-error occurs under the following condition. 1) The CMP process is removing multiple materials simultaneously. 2) The removal rate of copper is much higher than other materials.

EoE-error causes not only open errors but also short errors at the upper layer due to the propagation of the surface irregularities, but its detail mechanism is still unclear. It is demanded to develop an EoE-error prediction method that can be used in design time to avoid unexpected yield loss.

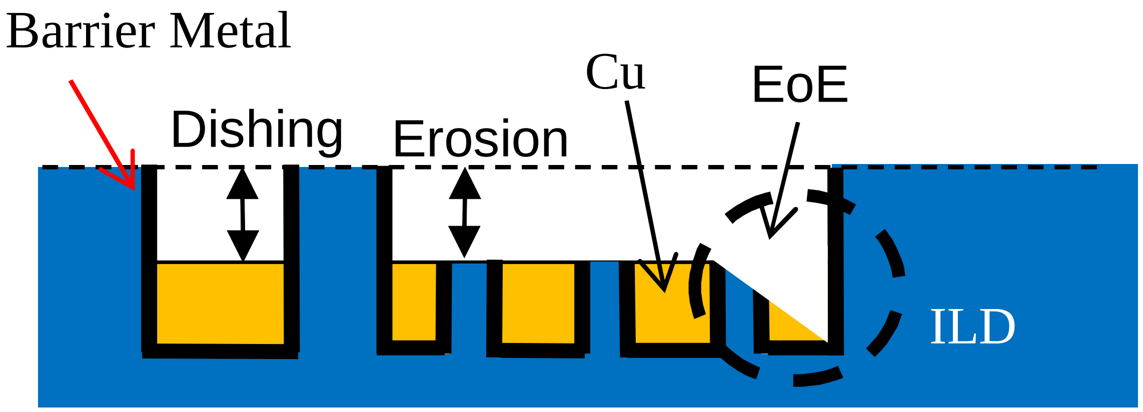


Fig. 1.4 Cross sectional view of interconnect layer.

1.3 Objective of this thesis

Conventionally, these problems are found after fabrication. The conventional countermeasure to these problems is illustrated in the top of figure1.5. Once they are found, process and/or chip layout are modified to avoid the problems. However, this countermeasure to the problems is too costly and deteriorates productivity. In fact, mask set modification in nano-meter technology costs over 1 million dollars [64]. To make matters worse, this modification is often repeated through trial and error until the problems are solved, because the effect of modification cannot be estimated accurately. Therefore, to avoid such inefficient trial-and-error modification, a prediction model that reasonably reproduces these variations with acceptable modeling effort is highly demanded.

Actual manufacturing processes are usually difficult to model with “white-box” model, which is fully derived from physical laws. This is because manufacturing process may include unknown noises, unseen dynamics, and immeasurable parameters [66]. To solve this problem, “gray-box” modeling approach is widely used [67,68]. This approach combines available physical knowledge with statistical methods. This approach enables the model to take into account any unclear factors using calibration parameters, and these calibration parameters are adjusted with experimental data. In contrast, “black-box” modeling approach extracts a relation among given numerical data without understanding physical phenomenon [69–72]. This approach is effective in case that the mechanism of the target phenomenon is complicated and is not understood enough to build a physical model. Regardless of the modeling approach used to model wire shape variation, the derived model should be usable for analyzing the relationship between the target phenomenon and the characteristics of the chip layout and it should be able to guide process and chip layout modification for the problem avoidance.

The goal of this thesis is to establish a virtualization framework of wire manufacturing process with highly precise prediction models for improving yield and productivity. The contribution of this thesis is illustrated in the bottom of figure 1.5. The developed models are used to tune process parameters and modify chip layout for avoiding the problems without fabrication, which considerably reduces the turn-around-time of the process tuning and saves the

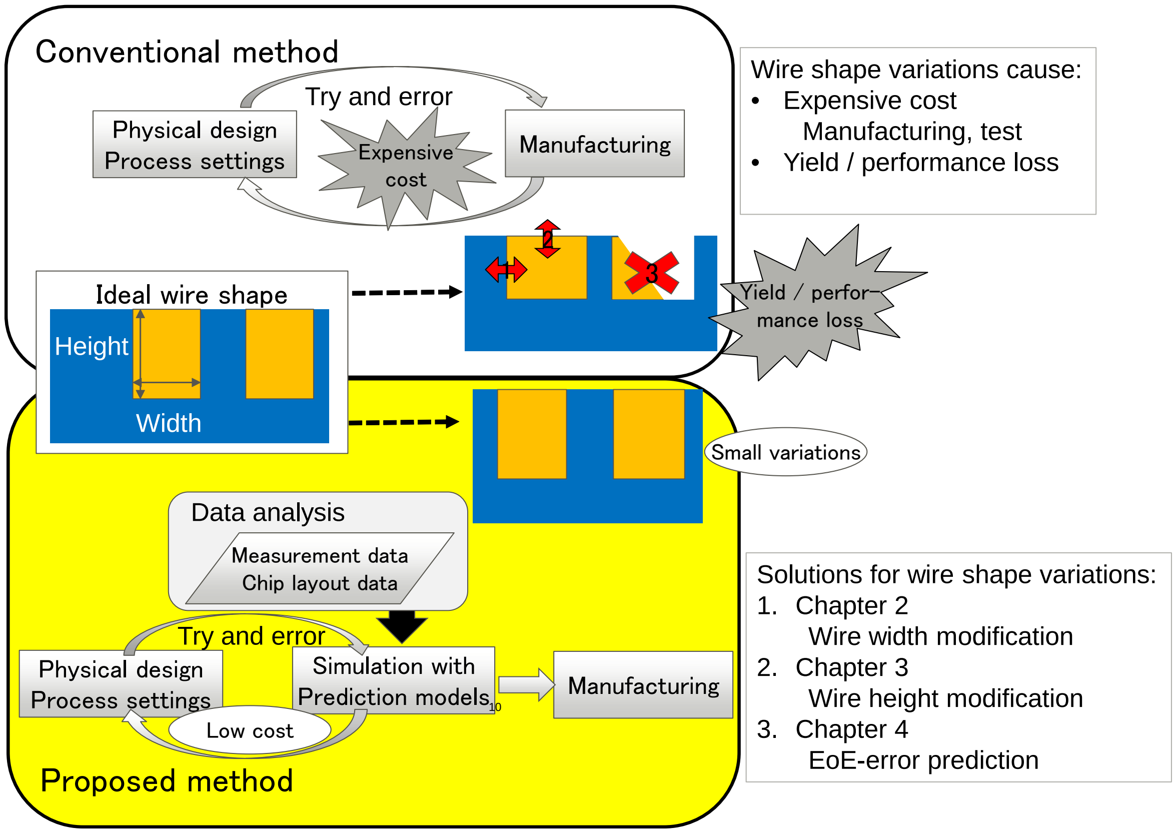

Conventional method
Try and error
Physical design
Process settings
Expensive cost
Manufacturing
Wire shape variations cause:
• Expensive cost
Manufacturing, test
• Yield / performance loss
2
3
Ideal wire shape
Height
Width
Yield / performance loss
Small variations
Data analysis
Measurement data
Chip layout data
Try and error
Physical design
Process settings
Simulation with
Prediction models
Low cost
Manufacturing
Solutions for wire shape variations:
1. Chapter 2
Wire width modification
2. Chapter 3
Wire height modification
3. Chapter 4
EoE-error prediction
Proposed method

Fig. 1.5 General structure of this thesis.

mask cost. As discussed in section 1.2, there are three major variation problems in actual wire manufacturing process and they all have a serious impact on yield and productivity [73, 80]. This thesis presents accurate prediction methods for each variation problem. To achieve the goal, this thesis utilizes not only measurement data obtained in manufacturing process but also various characteristics extracted from chip layout data, and analyzes the relationship between the problems and layout characteristics. In the modeling, depending on the complexity of the target phenomenon, this thesis employs gray-box and black-box modeling approaches to build accurate prediction models that include parameters relevant to wire shape variations.

For accomplishing the goal mentioned above, the following subjects are studied in this thesis.

- To develop a prediction model of wire width variation and a wire width adjustment method that tunes the etching process.
- To develop a method to mitigate wire height variation considering die-to-die variations.
- To develop an EoE-error prediction model with machine learning techniques.

Firstly, chapter 2 proposes a prediction model of etching induced wire width variation accounting for global layout pattern variation. According to the measurement results, wire width variation heavily depends on the chip layout pattern which is far from the wire width measurement spot as well as local chip layout pattern. A prediction model is constructed from physical properties and hypotheses of etching process with data analysis of the measurement data from many industrial chips and its layout characteristics abstracted from chip design data. This thesis then proposes a wire width adjustment method which tunes the etching process with the proposed prediction model. Then experiments verify the accuracy of the prediction model and estimates how much wire width variation can be potentially reduced with other industrial chips.

Secondly, chapter 3 discusses wire height variation and its mitigation method with ECP and CMP prediction models. In implementing the mitigation method and applying it to practical design, it is found that there are three problems to solve. The first problem is the computational time to process layout data, since layout characteristics information, wire density, perimeter length, wire width, etc. is necessary for ECP and CMP prediction models. It is too costly to handle each wire shape of the entire chip accurately. Therefore, the chip data is divided into small 10μm $-$ 40μm square meshes and average characteristic values of each mesh are stored in the database from original GDSII or OASIS format data. In addition, virtual dummy filling method is developed, which roughly calculates the wire characteristics of dummy metal without considering the exact shape and location of an enormous number of dummy fills. The reasons are as follows. 1) The amount of dummy fill features is much larger than that of other functional wires and dummy fill consumes large extraction time and data size. 2) During dummy fill optimization, dummy properties such as size and space is repeatedly varied for finding better manufacturability because dummy fill optimization does not affect the logic function and wire topology. Therefore, the virtual dummy filling method reduces the cost of iterative extraction and dummy modification drastically. The second problem is the large prediction errors of chip surface topography, and it comes from the inaccuracy of the existing ECP prediction model. This thesis then proposes a refined ECP prediction model which employs additional parameters on the basis of data analysis of measurement data and layout characteristics. The third problem is the difficulty in finding errors that occur only in a specific variation condition. To find such errors, this chapter proposes an effective hot-spot detection method which can deal with die-to-die variations, where hot-spot is defined as the point which may degrade timing or manufacturing yield. After ECP and CMP are processed, hot-spots are found in some chips on a wafer whereas other chips on the same wafer are manufactured normally. This is because die-to-die variations of ECP and CMP processes exist. The analysis of measurement data reveals that die-to-die variation heavily depends on the variations of initial copper thickness after ECP process and over-polishing time in copper removal stage of CMP process. Thus, this work solves the three problems that prevent the mitigation of wire height variation. Using these solutions, this chapter implements the proposed mitigation method that can detect hot-spots before manufacturing, and demonstrates a case study showing its efficiency.

Thirdly, chapter 4 proposes an EoE-error prediction model which can recognize unexpected yield loss before manufacturing. Though CMP process tuning, such as slurry selection, polishing pressure, etc. is an effective solution of EoE-error reduction, it may results in a significant change in chip surface topography because of complicated CMP process mechanism. It is practical to predict EoE-errors under the fixed CMP process condition with the proposed model and then to modify the chip layout using the method such as dummy fill optimization techniques. EoE occurrence mechanism is too complicated to build a physical model, and therefore the relationship between EoE-errors and chip layout characteristics is firstly analyzed with measurement data of real chips and its chip layout data. After identifying the layout characteristics that affect EoE-errors from data analysis, this chapter introduces a black-box prediction model which judges whether EoE-error occurs or not using machine learning algorithms. Machine learning algorithms are capable of finding regularities from large data statistically, but measurement data of EoE-errors includes large amount of noise and it may cause overfitting problem. Therefore, this thesis proposes a multi-level machine learning method which can achieve high accuracy and avoid overfitting problem. The effectiveness of the proposed method is validated with industrial chips.

The rest of this thesis is organized as follows. Chapter 2 proposes a prediction model of wire width variation according to global layout pattern variation. Chapter 3 describes the issues in constructing a mitigation method of wire height variation and gives solutions to these issues. Chapter 4 proposes the EoE-error prediction method with multi-level machine learning algorithm. Finally chapter 5 concludes this thesis.

Chapter 2

Modeling the effect of global layout pattern on wire width Variation for On-the-Fly Etching Process Modification

This chapter describes a prediction model of etching induced wire width variation which takes into account global layout pattern variation. This chapter also presents a wire width adjustment method that modifies etching process on the fly according to the critical dimension loss estimated by the proposed prediction model and wire space measurement just before etching process.

Experimental results show that the proposed model achieved good performance in prediction, and demonstrated that the potential reduction of the gap between the target wire width and actual wire width thanks to the proposed on-the-fly etching process modification was 68.9% on an average.

2.1 Introduction

Wire width and wire height control is a key factor to achieve high performance and yield enhancement as discussed in section 1.1. Chip fabrication includes manufacturing test which judges whether a chip has defects or not, and the manufacturing test occupies a considerable portion of chip fabrication cost [78]. To reduce the test cost, wafer level screening is often used in manufacturing test [79]. In this screening, a common test structure is placed on scribe lines in a wafer (figure 2.1) and electrical characteristics of the test structure are measured before all individual chips on the wafer are tested. If an outlier value is found in the measurement of the common test structure, the wafer is discarded. It is because the number of faulty chips on such a wafer is empirically much larger than those on other wafers.

For checking the result of wiring processes, wire resistance is often measured in the wafer level screening. If the systematic variation of wire resistance originated from only process conditions and local test structure layout, there should be no resistance difference regardless of the chip layout on a wafer. However, a certain difference in wire resistance value is observed in the measurement data of the test structure with various chip layouts. This means

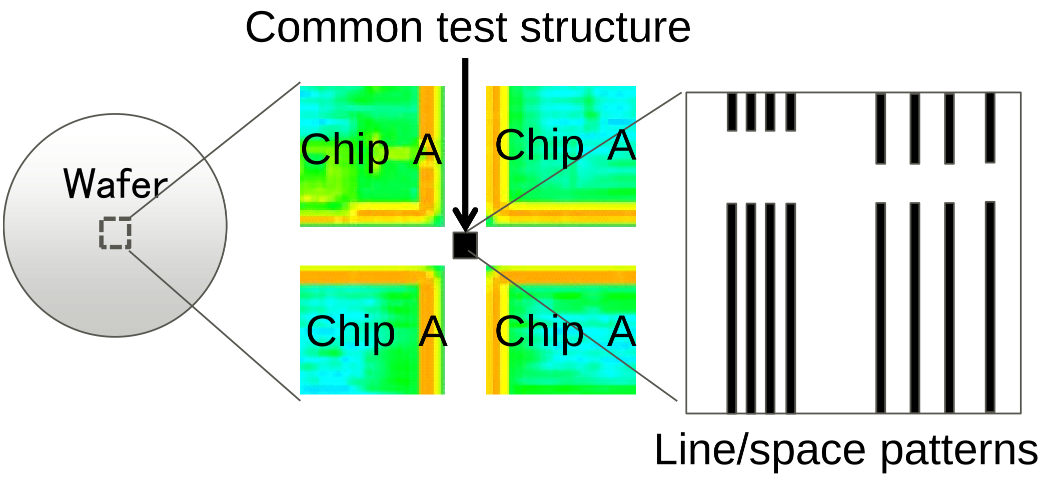


Fig. 2.1 Common test structure on a wafer.

that the process forming wire metal pattern is affected by global layout which consists of the surrounding layout in a certain range around the test structure.

Section 1.1 described that the main processes of shaping copper metal wire were lithography, etching, electro-chemical plating (ECP), and chemical mechanical planarization (CMP). Wire height variation heavily depends on ECP and CMP processes, and chapter 3 proposed a method to mitigate wire height variation.

On the other hand, wire width variation depends on lithography and etching processes. Both the processes are affected by global layout pattern as well as local test pattern [16,29,81]. Here, local layout pattern is defined as a wire of interest and its adjacent objects, and global layout pattern is defined as features abstracted from a wire of interest and its surrounding layout within a certain range. Lithography simulation can predict the shape of interconnect accurately, but it is too costly for full chip analysis. Thus, several heuristic prediction methods whose execution time is acceptable are proposed [81–83].

To achieve desired wire widths in fabrication, etching process prediction is more important than lithography process prediction. This is because the variation occurred in lithography process can be compensated by adjusting successive etching process parameters, such as gas flow, wafer temperature, and etching time as long as etching process can be correctly simulated. For such a purpose, there are some methods that predict etching induced wire width variation in consideration of local layout pattern [84–89]. However, these do not take into account global layout pattern. Another approach is a feedback control through an iteration of fabrication, measurement and process modification [90, 91], but it takes a longer time and costs wafer loss before the process is stabilized.

Aiming to mitigate wire width variation, this chapter shows a prediction model of etching induced wire width variation that considers global layout variation. In addition, this chapter propose a method that adjusts wire width through on-the-fly etching process modification [77]. Contributions of this work include the followings.

- This is the first work to develop a model that predicts etching induced wire width variation taking into account an effect of global layout pattern variation with gray-box modeling approach. To achieve high accuracy, model parameters are calibrated with measured data of industrial chips.

- A wire width adjustment method with the prediction model is proposed. This adjustment method can reduce the wire width variation by compensating lithography and prospective etching induced variations with instant etching process alternation.
- The accuracy of the prediction model and the effectiveness of the proposed adjustment method is assessed with industrial chips.

The rest of this chapter is organized as follows. Section 2.2 reviews etching process and defines the wire width variation problem occurring in etching process. Section 2.3 introduces a prediction model for wire width variation and explain how to adjust wire width using the prediction model. Section 2.4 presents experimental results. Finally, section 2.5 concludes this chapter.

2.2 Overview of etching process

This section reviews etching process and its mechanism briefly. In the fabrication process of ultra large integrated circuits, reactive-ion etching (RIE) is widely used [26, 29] as discussed in section 1.1.2. Figure 2.2 illustrates an RIE system. RIE is a kind of dry etching method using gas glow discharge plasma, where the plasma is maintained with RF power. The plasma dissociates and ionizes feed gases (e.g. CxFy for SiO2 etching) in a vacuum system and generates free radicals and positive ions as etch species, which react with the material of the wafer surface.

Free radicals are main reactive species of etching process. Radicals, which are electrically activated neutral species, are diffused and adsorbed on the wafer surface, and they finally react with the wafer surface materials.

Energetic gas ions are other key species of etching mechanism. A wafer is located on a cathode electrode and acquires negative charge because electron mobility is higher than ion mobility. Positive ions drift toward the wafer and they collide with materials on the wafer surface. Some ions react with the materials chemically, and others cause physical sputtering.

Synergism of ion bombardment and chemical reaction gives a high etching rate [28], which is an advantage of RIE process. The etching rate of the wafer exposed to ion and radical fluxes simultaneously is much higher than that of the wafer exposed to each flux separately. Ion bombardment helps to remove reaction product of wafer surface and accelerates another surface reaction of free radicals, which results in the higher etching rate.

In etching process, there are two important factors to control wire trench profile. The first is selectivity, which is the etching rate ratio of a target material to other materials. In chip fabrication, wafer surface is covered by photoresist pattern, and ESL at the bottom of trench prevents over-etching. To remove only the exposed potions of SiO2 properly, high selectivity to both photoresist and ESL materials is required. Radical etching is generally more selective than ion etching because physical sputtering in ion etching process is less dependent on the materials. Secondly, anisotropy determines the shape of wire trench. Anisotropy is the directionality of etching process, and it is opposed to isotropy. Anisotropic and isotropic etching is illustrated in figure 2.3. Ion etching process is highly anisotropic because ion flux has a direction vertical to the wafer surface. Radical etching, on the other hand, is an isotropic process because free radical is electrically neutral and has the same etching rate in every direction.

In RIE process, highly anisotropic etching is accomplished thanks to sidewall protection

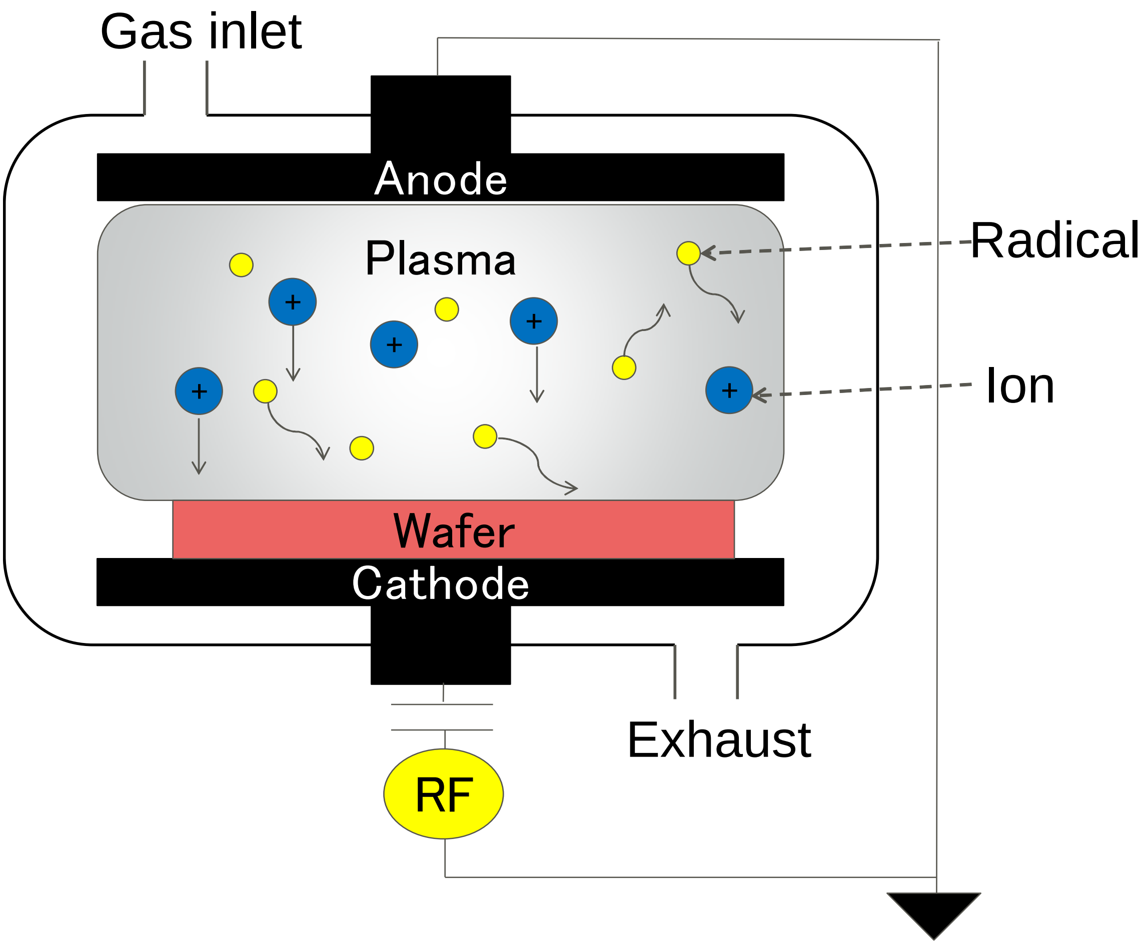

Gas inlet
Anode
Plasma
Radical
Ion
Wafer
Cathode
Exhaust
RF

Fig. 2.2 Overview of RIE system.

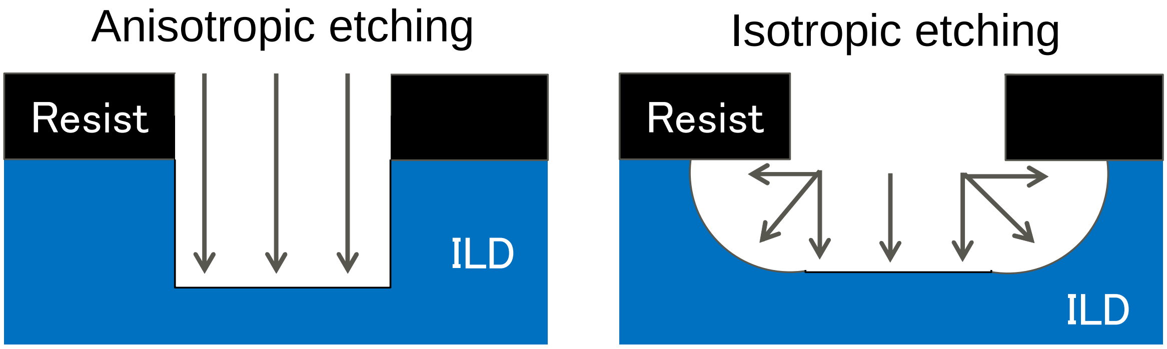

Anisotropic etching
Resist
ILD
Isotropic etching
Resist
ILD

Fig. 2.3 Anisotropic and isotropic etching.

mechanism (figure 2.4) [29,30]. SiO2 and photoresist materials output both volatile gaseous reaction products and solid polymer reaction products. The polymer products redeposit on the surface and form a polymer film layer. This polymer film plays an important role as an inhibitor to protect the surface from radical etching. Note that only sidewalls of the trench

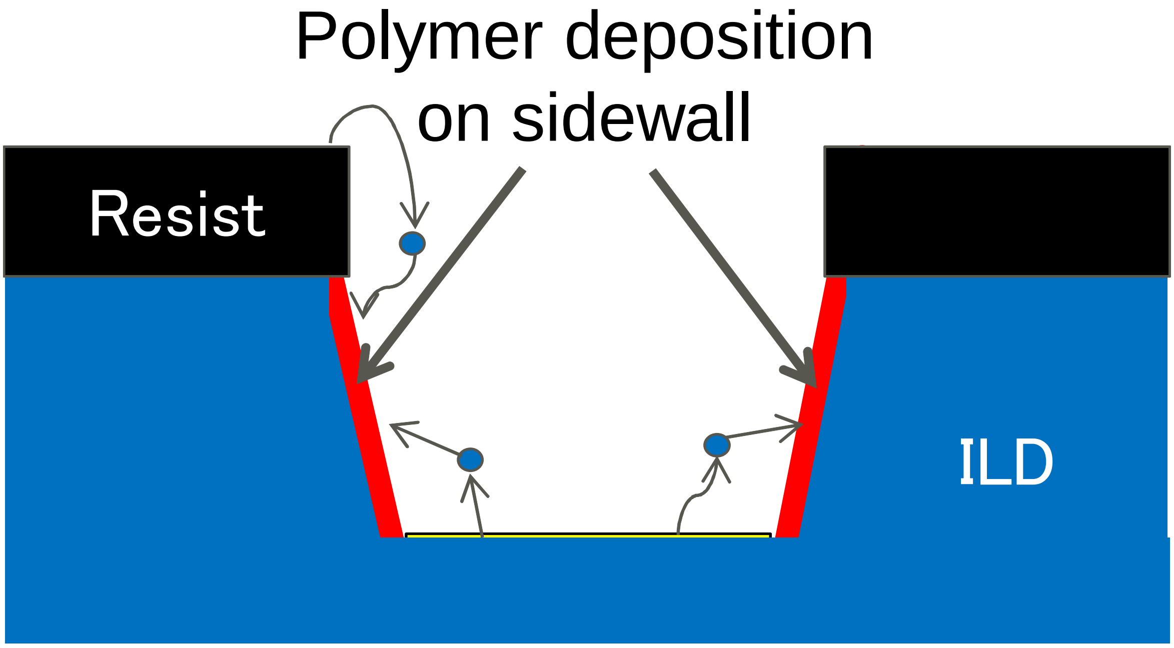


Fig. 2.4 Sidewall protection.

are covered by the polymer film because they are not exposed to ion bombardment which can remove the polymer deposition. Thus, sidewalls are protected from etching, and RIE process becomes more anisotropic.

The sidewall protection mechanism has a great effect on the wire width variation because the horizontal etching rate heavily depends on the thickness of the sidewall polymer film. This mechanism can be related to many parameters, such as the amount of free radicals, the ratio of etchable area and photoresist area, and etching rate. An important point here is that those parameters are affected by global layout variation [27, 29]. This work focuses on the sidewall protection mechanism as a major factor of wire width variation in etching process and studies the modeling of wire width variation originating from this mechanism.

2.3 Prediction and mitigation of wire width variation

This section proposes a prediction model of wire width variation, which can be applicable to a variety of chip layouts on a wafer. To achieve high accuracy of the model, the proposed model calibrates its model parameters using the measured data of various industrial chips. This section also describes a method to mitigate wire width variation with on-the-fly etching process modification.

2.3.1 Definitions

In the manufacturing process used in this study, a common test structure is placed at a fixed location on a wafer for monitoring wire width variation. Wire widths of test patterns in the structure are measured twice: before and after etching process. The former measured value is called development inspection critical dimension (DICD) and the latter is called final

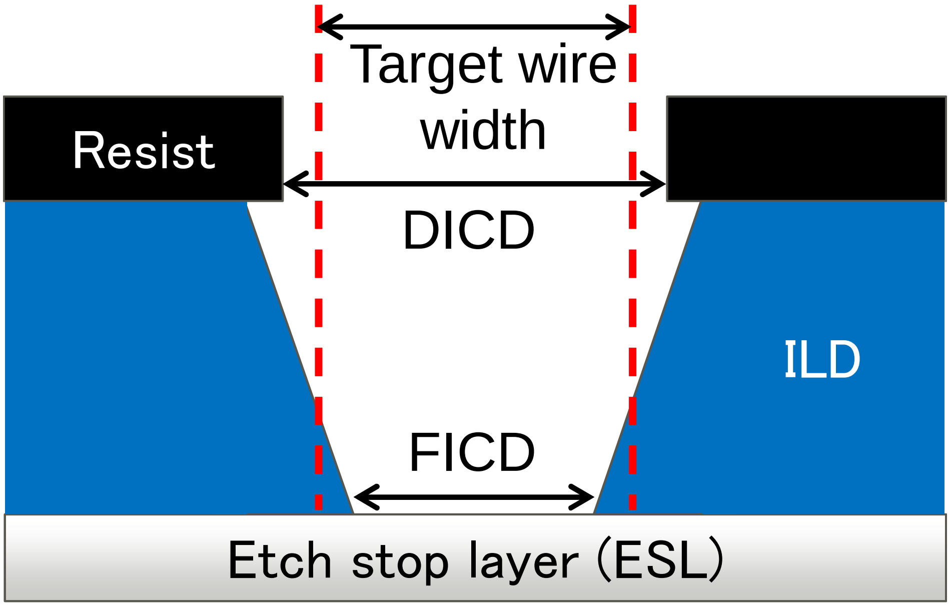


Fig. 2.5 Relationship between DICD, FICD, and target wire width.

inspection critical dimension (FICD). Here, it is defined that a parameter "etching bias" Δw as the difference between DICD and FICD, and a parameter "Critical Dimension (CD) loss" g as the difference between target wire width w_t and FICD.

$$\Delta w = FICD - DICD, \tag{2.1}$$

$$g = FICD - w_t. \tag{2.2}$$

CD loss g can be positive and negative according to the relationship of sizes between FICD and w_t.

Figure 2.5 shows the relationship between DICD, FICD and target wire width. To obtain a wire profile with no CD loss ($g = 0$), etching bias Δw should be equal to the difference between target wire width and DICD ($\Delta w = w_t - DICD$). On the other hand, DICD varies wafer by wafer due to lithography process. If the etching process can be tuned to satisfy $\Delta w = w_t - DICD$ for every wafer, the CD loss can be minimized.

The proposed wire width adjustment method, which will be explained in section 2.3.3, alters etching process to satisfy $\Delta w = w_t - DICD$ aiming at $g = 0$. Here, DICD can be obtained by measuring the common test structure on the wafer before the etching process. The target wire width w_t is also available. On the other hand, it is difficult to obtain the tuned etching process that satisfies $\Delta w = w_t - DICD$ directly. Therefore, the CD loss is firstly estimated if normal etching process is performed. Then, the etching process is slightly modified to eliminate the estimated CD loss, and the modified process is applied to the wafer. Note that every manufacturer empirically knows how much trench width would change when the etching process is modified. However, there are no models that estimate the absolute value of Δw that varies depending on global layout pattern. This is the motivation to develop a model for estimating Δw in case of normal etching process. This developed model will be explained in the next subsection.

2.3.2 Proposed prediction model

The proposed model predicts etching bias Δw that occurs depending on global layout pattern. The proposed model is derived from four qualitative properties below.

a. **Etching bias is proportional to the thickness of sidewall polymer film.**
The polymer film deposited on sidewalls prevents the sidewalls from being etched by isotropic free radical etching. Therefore, the thicker the film grows, the smaller the trench width, i.e. the wire width, becomes.

b. **Thickness of sidewall polymer film is affected by the wire area density.**
The sidewall polymer is composed of the products from substrate material (e.g. SixHyFz) and from photoresist material (e.g. CxHyFz) [29]. On the other hand, the redeposition rate to the surface and etching prevention strength are different between these materials [31]. Due to that, the etchable wire area (substrate material) to the total area (substrate and photoresist materials) has an influence on the thickness of the sidewall polymer film and the consequent etching prevention ability. The ratio of the etchable wire area to the total area is synonymous with the wire area density.

c. **Thickness of sidewall polymer film is also affected by the total edge length.**
Here, edge length is defined as the wire perimeter. Supposing the amount of generated polymer materials is fixed, the polymer film becomes thicker when the total sidewall area in which the polymer materials are redeposited is small. Besides, the sidewall area is the product of the edge length and the trench depth, and hence to the sidewall area is proportional to the edge length.

d. **Parameters are calculated in the area within the range of effective length.**
It is assumed that reaction products scattered from a certain point are redeposited within a fixed range from that point. This is reasonable since the reaction products tend to be redeposited before they are diffused distantly. As a result, the reaction products and the sidewall area out of the range have little effect on the redeposition process at the point of interest. To deal with this assumption, a parameter called “effective length” is introduced [92]. According to our preliminary evaluation, this parameter is hardly dependent on process technology size. This parameter could depend on etching process parameters, but in this chapter the etching process is assumed to be fixed.

According to the above qualitative properties, a prediction model is proposed as follows.

$$\Delta w = \alpha \cdot \overline{m}, \tag{2.3}$$

$$\overline{m} = d^{\beta} \cdot e^{\gamma}, \tag{2.4}$$

where Δw is the etching bias at a point of interest and $\overline{m}$ is the average of multiplication parameter m within the effective length L. d is wire area density in a mesh, e is total edge length in a mesh, and α, β, and γ are calibration parameters. Parameter α, β, γ, and effective length L are calibrated using etching bias data of industrial chips measurement. This model employs gray-box modeling approach to integrate the both kinds of information: above physical properties and statistical information from the measurement data.

The average computation in equation 2.3 includes numerical integration. To efficiently compute equation 2.3, a whole chip is discretized into small meshes and related parameters are extracted and recorded for each mesh, which helps reduce the size of database and calcu-

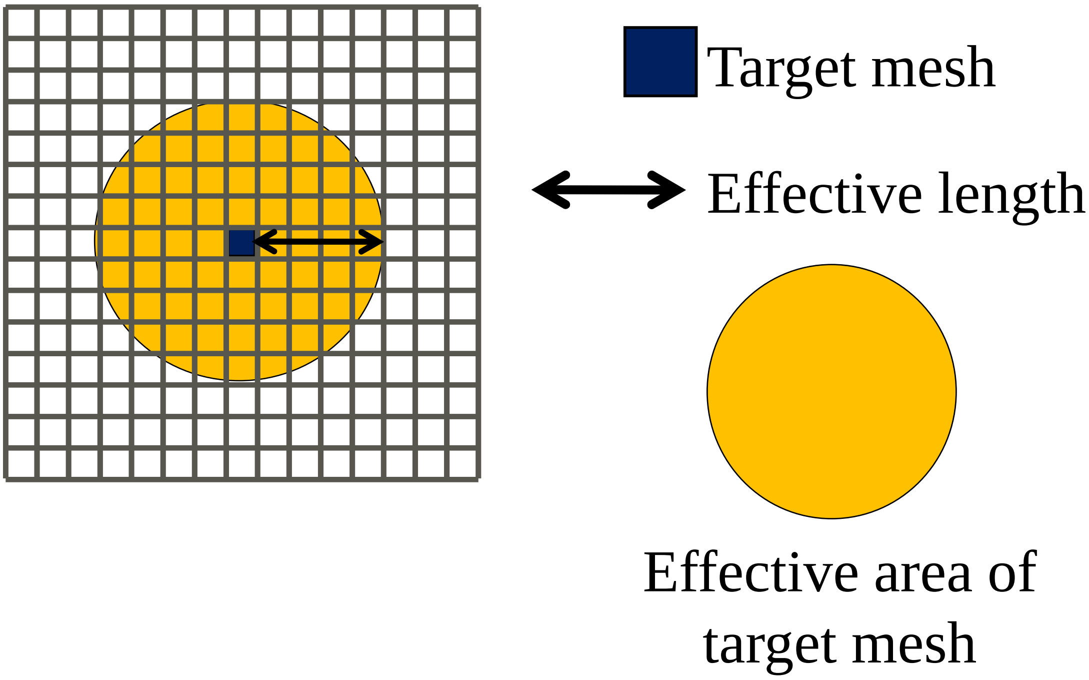


Fig. 2.6 Region for parameter $\overline{m}$ calculation.

lation cost. Namely, layout parameters necessary for the prediction of wire width variation, i.e. d and e, are extracted for every mesh from the original chip data. Consequently, wire width variation is predicted for each mesh.

Figure 2.6 illustrates $\overline{m}$ calculation with discretized meshes. Using effective length L, the proposed model compute $\overline{m}$ of the target mesh as an average of parameters m of the meshes within the range of effective length from the target mesh.

2.3.3 On-the-fly wire width adjustment via etching process modification

Given the prediction model presented in the previous subsection, wire width variation that occurs depending on global layout pattern can be estimated now. This subsection explains how CD loss can be mitigated using the prediction model.

Figure 2.7 shows the procedure of wire width modification. Now, a new wafer is prepared whose lithography process is completed but whose successive etching process is not completed. This successive etching process is modified based on the CD loss estimated by the proposed prediction model of etching bias and measured DICD of the common test structure on the wafer after lithography process. This etching process modification is performed for every wire layer.

Firstly, parameters d and e are extracted from the layout data. Here, the target mesh is the mesh in which the common test structure is located, and layout parameters of each mesh within the range of effective length are extracted using layout data of chip, wafer and common test structure. Then, etching bias Δw is calculated with these parameters and the proposed prediction model of equations 2.3 and 2.4. Note that the prediction model has been already calibrated with calibration data. Next, CD loss g of target mesh is calculated with this pre-

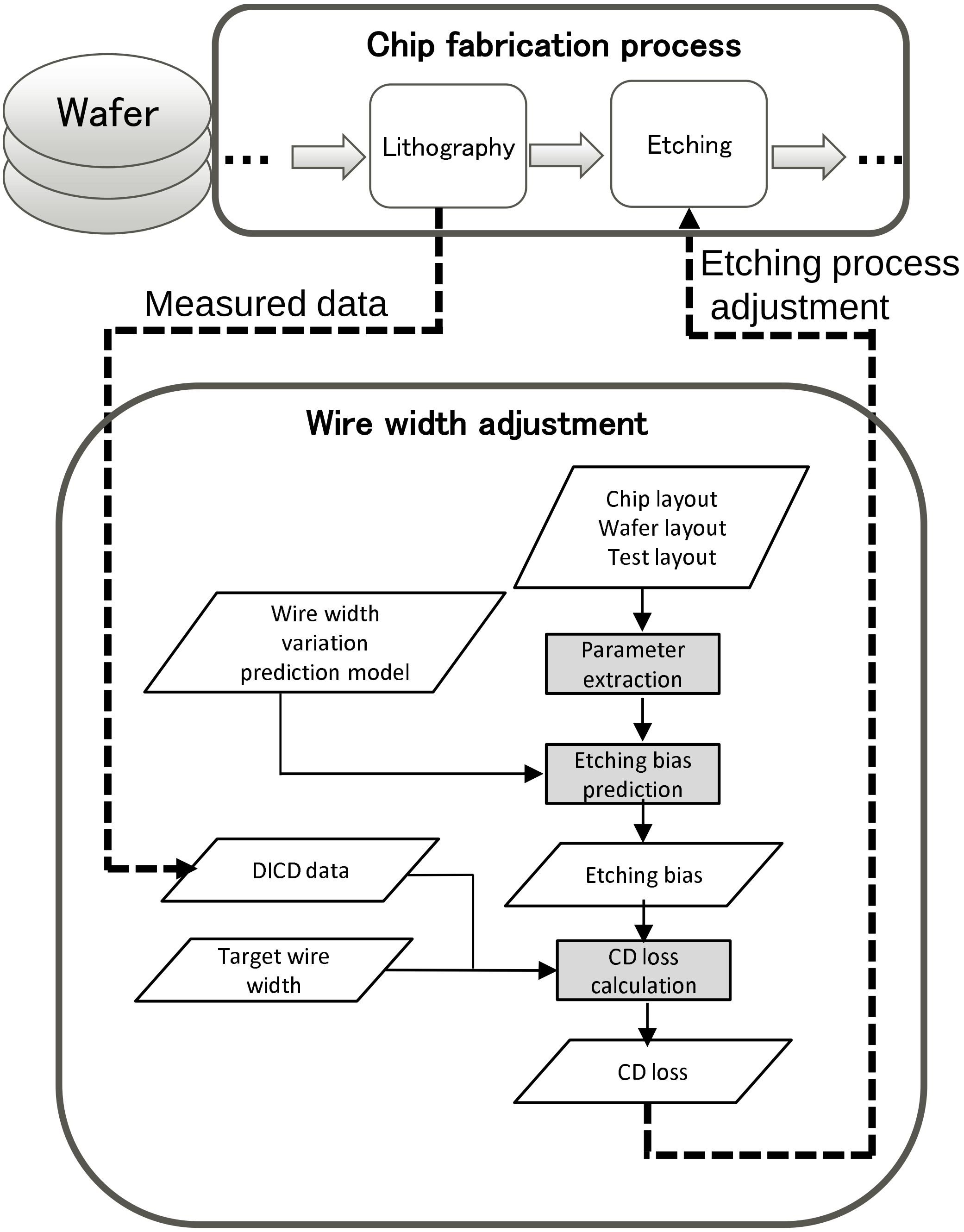

Chip fabrication process
Wafer
Lithography
Etching
Measured data
Etching process adjustment
Wire width adjustment
Chip layout
Wafer layout
Test layout
Wire width variation prediction model
Parameter extraction
Etching bias prediction
DICD data
Etching bias
Target wire width
CD loss calculation
CD loss

Fig. 2.7 Procedure of on-the-fly wire width adjustment via etching process modification.

diction result of Δw, measured DICD and target wire width w_t using equations 2.1 and 2.2. In this way, CD loss g of the test pattern can be predicted in case that normal etching process is applied. Then, etching process is adjusted to eliminate the estimated CD loss of the test pattern. For example, etching time and / or gas flow can be tuned for this purpose [86]. This adjusted etching process is applied to the wafer.

Table 2.1 Details of calibration / validation chip designs.

Chip name	Chip size (mm^2)	# of layer	# of wafers	Average wire density (%)
Calibration chip designs				
A	21.3×20.8	4	133	26.3–33.1
B	7.8×7.8	4	52	30.1–42.6
C	13.3×10.0	4	37	25.5–54.4
D	8.0×6.4	4	445	31.3–43.0
E	8.5×8.5	4	67	31.1–50.5
F	7.8×8.4	5	56	35.3–45.1
G	9.4×9.4	6	42	26.4–32.2
H	9.8×8.8	5	12	34.9–46.5
Validation chip designs				
I	9.9×9.9	4	200	32.7–46.5
J	6.9×8.2	4	40	29.8–42.6
K	6.9×6.9	4	30	30.6–43.5
L	9.0×6.0	4	96	29.0–41.4
M	7.9×8.1	4	72	29.2–41.0
N	18.2×18.1	4	18	24.9–39.7
O	12.1×11.0	5	14	35.2–46.1

2.4 Experimental results

This section first present experimental results to validate the accuracy of the proposed model. 36 etching bias data which are came from 8 chip designs is used for model parameter calibration. In addition, other 29 etching bias data from 7 chip designs is used for validating the efficiency of the proposed model to unknown chip data. Note that each wafer is covered by one of the 15 (= 8 + 7) chip designs and one etching bias data corresponds to a wire layer of each chip design. Each etching bias data is an average of the values measured with multiple wafers. Calibration parameters α, β, γ, and effective length L in the proposed model were calibrated with these data to minimize the root mean square (RMS) value between measured data and estimated value. The mesh size has an impact on a trade-off relation between computational cost and estimation accuracy. In this work, the mesh size was set to $10 \times 10\mu$m. This size was much smaller than effective length L of 2000μm, which will be investigated later, and numerical integration for $\overline{m}$ is be expected to be reasonably accurate.

Table 2.1 shows an overview of all chip data. All the chips were manufactured with the same 65 nm technology node. Each layer of a chip has different average wire density values. “Average wire density” column denotes upper and lower bounds of these values. For all the wafers listed in Table 2.1, FICD and DICD of the common test structure were measured. This measurement data was used for calibration and validation purposes. Note that another calibration is needed if technology node is changed. In this chapter, the coefficient of determination R^2 is used as a metric to evaluate the accuracy of the prediction model.

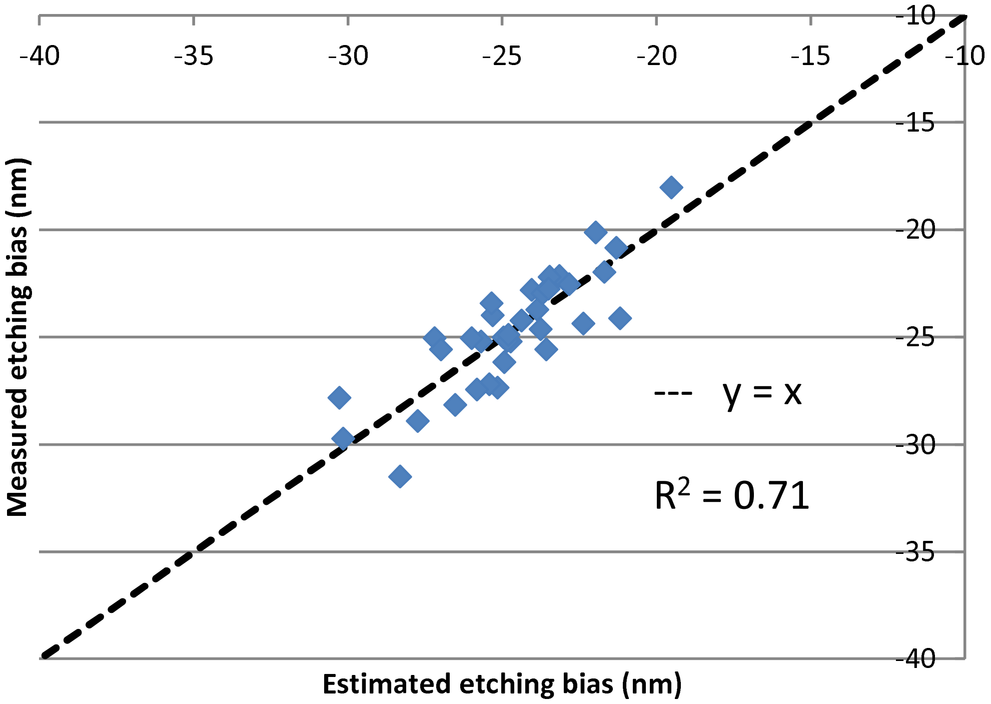


Fig. 2.8 Estimated etching vs. measured etching bias for calibration data.

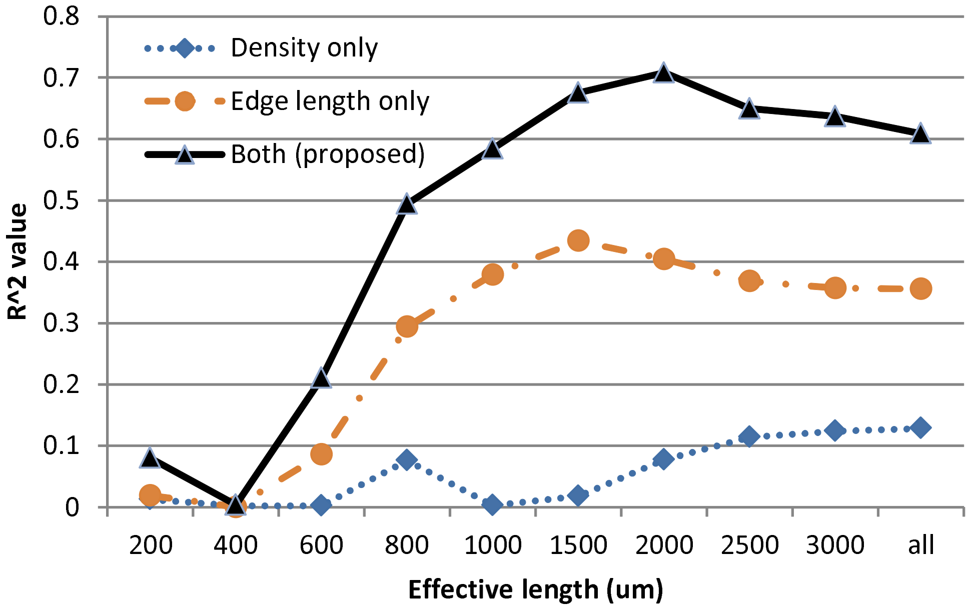


Fig. 2.9 Model calibration results with various effective lengths.

Figure 2.8 shows the accuracy of the model after the calibration process. Horizontal and vertical axes indicate estimated etching bias and measured etching bias, respectively. This result shows that FICD value is smaller than DICD in the technology node used for this experiment since etching bias values are negative. R^2 value was 0.71 and this model achieved good performance in prediction.

Besides, calibration parameters α, β, and γ, were –0.0934, –0.259, and –0.341 respectively. This calibration result indicates that CD loss value takes negative value in our 65 nm technology. Another calibration process and calibration parameter set might be required if positive CD loss value is observed in the measurement data. This calibration result also indicates that, if wire area density d increases, negative etching bias value Δw gets close to 0 and therefore FICD value approaches to DICD value according to equation 2.1. This means that the ability of sidewall etching prevention degrades as the rate of polymer products from substrate material to total sidewall layer component becomes higher. The calibration result also shows that an increase in edge length e results in an increase in both etching bias Δw and FICD. This is because sidewall thickness is inversely proportional to the sidewall area and affects the protection mechanism from isotropic etching.

Figure 2.9 shows R^2 index with various effective length values. “All” in x-axis means that the calibration was carried out supposing the effective length L was infinity. In this experiment, the calibration with tree models below are performed.

- **M1**: Proposed (equation 2.4); both density and edge length are considered.
- **M2**: Density only ($m = d^{\beta}$); only density is considered.
- **M3**: Edge length only ($m = e^{\gamma}$); only edge length is considered.

First, the result of the proposed model (M1) is analyzed. The best performance was obtained in the case that L was 2000μm. The edge bias was affected by the layout in a circle whose radius is 2000μm, and the layout pattern in such a large area must be considered for the edge bias estimation. The effective length of 2000μm was used for other experiments throughout this chapter. Next, the results of M1, M2 and M3 are compared for difference detection. M1 attained the highest R^2, which clarifies that both density and edge length affect the etching bias mechanism. The figure also shows that the edge length e had a stronger impact on etching bias than density d.

Figure 2.10 shows the prediction results for the validation chip data. R^2 value of 0.65 was obtained, which confirmed that the proposed model maintained high accuracy even when unknown data was given.

Finally, it is estimated how much the CD loss can be potentially reduced by the proposed on-the-fly wire width adjustment. In this evaluation, it is assumed that the estimated CD loss using the proposed prediction model could be completely eliminated by etching process modification. Therefore, the CD loss reduction presented in the following corresponds to the maximum value in a case that the etching process modification to increase/decrease Δw is perfect. Table 2.2 shows RMS values and sigma values of CD loss with and without the proposed wire width adjustment. Here, the etching bias data of validation chips was used. Figure 2.11 shows the CD loss distributions. When the proposed wire width adjustment was applied, RMS of CD loss was 1.87 nm and sigma value was 1.66 nm. Compared with the result without adjustment, the proposed method could reduce RMS of CD loss by 68.9% and sigma of CD loss by 40.9%. The CD loss distribution moved toward zero and the spread became tighter.

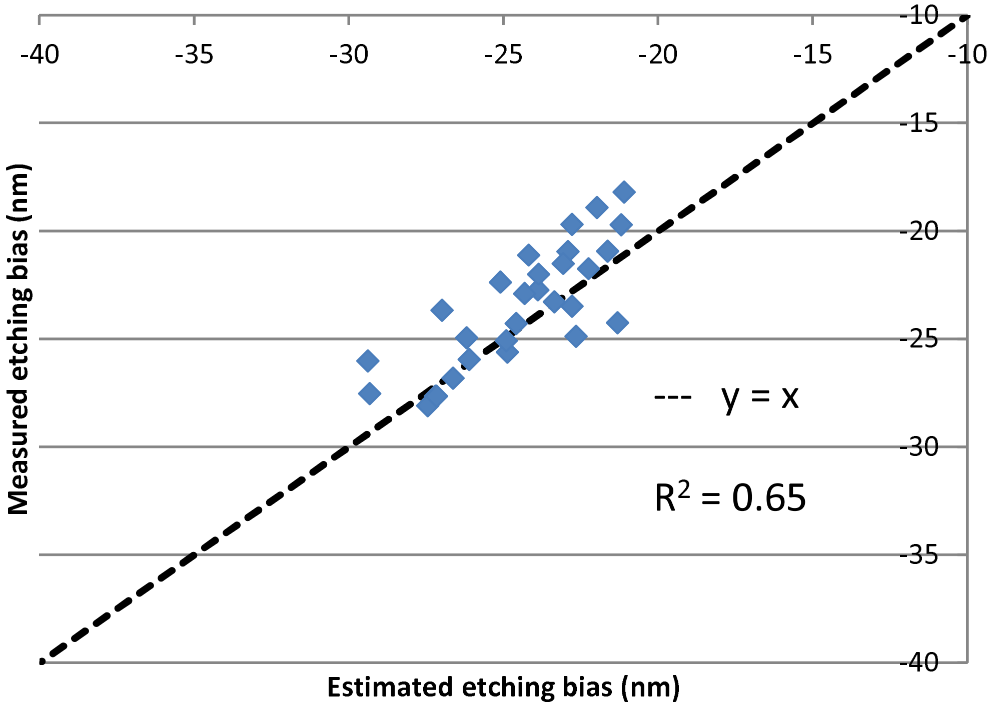


Fig. 2.10 Estimated etching vs. measured etching bias for validation data.

Table 2.2 CD loss value of validation chips.

	Original data (nm)	Proposed method (nm)	Improvement (%)
RMS	6.02	1.87	68.9
sigma	2.82	1.66	40.9

2.5 Conclusion

This chapter proposed a model that predicted wire width variation occurring depending on global layout pattern variation. This chapter also presented a wire width adjustment method that tuned the etching process on the fly using the proposed prediction model and the measured DICD of the common test structure on the wafer. Experiments showed that the proposed model achieved good performance in prediction and could reduce the CD loss between the target wire width and FICD value by 68.9% on an average.

As the technology of VLSI manufacturing process continues to shrink, the allowable value of wire width variation becomes more stringent to satisfy performance and manufacturability requirements. A future work is to improve the accuracy of the model with further analysis of the measurement data.

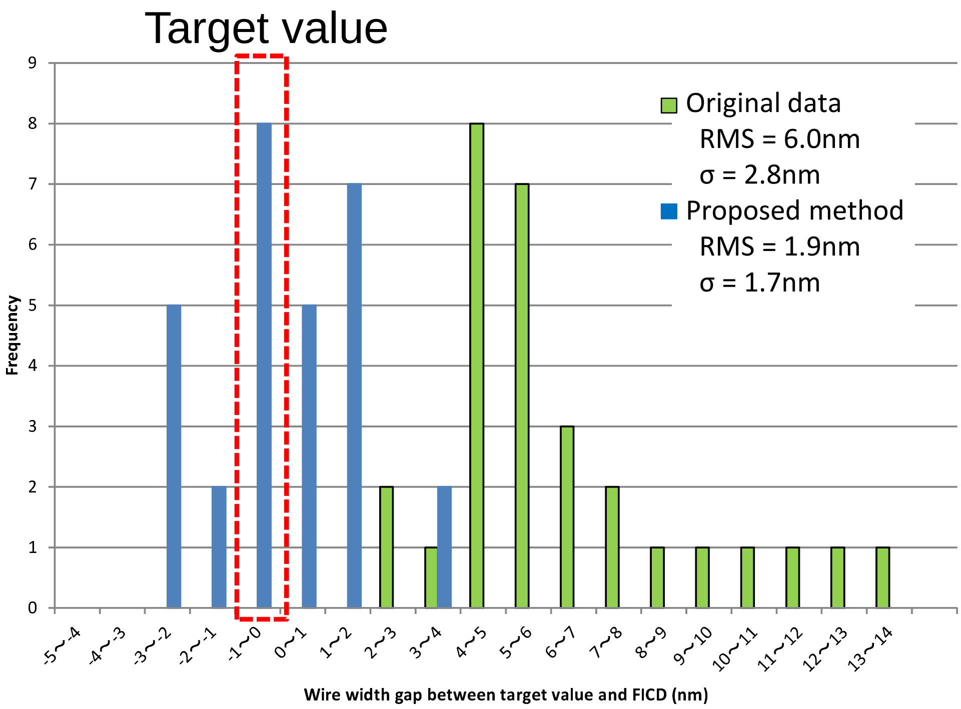


Fig. 2.11 CD loss distribution of validation chips.

Chapter 3

A practical wire height mitigation method with ECP and CMP simulation

This chapter describes a mitigation method of wire height variation with ECP (Electro-Chemical Plating) and CMP (Chemical Mechanical Planarization) prediction model. In this chapter three problems are discussed in implementing the proposed mitigation method. Firstly, a fast extraction method from GDSII with virtual dummy filling method is developed to reduce large processing cost. Secondly, this study proposes a refined ECP model for improving accuracy of prediction. Finally, this chapter proposes an effective hot-spot detection method considering die-to-die variations. Experimental results show that the proposed extraction method can handle huge chip data with small processing cost. In addition, the results show that the proposed ECP model reduces an error of copper height by 68.2% and that of step height by 51.1%. This chapter also shows a case study of the proposed hot-spot detection method. This method reduced wire height variation by 84.4% and avoided short errors before manufacturing.

3.1 Introduction

As discussed in section 1.1.3, ECP is a copper deposition process to fill up wire trenches, and CMP is a process to remove redundant copper according to ECP process. These processes, however, are not perfect and they introduce dishing and dielectric erosion, which causes wire height variation problems (figure 3.1). For designers and manufacturers, dummy fill insertion is one of the popular and effective solutions to mitigate the dishing, erosion, and wire height variation [75]. Dummy fill insertion adds dummy metal features, which affect neither the logic function nor wire topology, to uniformize the copper density aiming to reduce the amount of dishing and erosion. However, it cannot always achieve the target density depending on the original wire utilization. Moreover, it is known that the pattern density is not a sufficient metric to accurately predict wire height variation because of the complexity of CMP process [50].

ECP and CMP simulators based on ECP and CMP process prediction models estimate dishing, erosion and wire height variation, and hence they are expected to be useful for predicting the chip non-uniformity before manufacturing. The advantage of such model-based

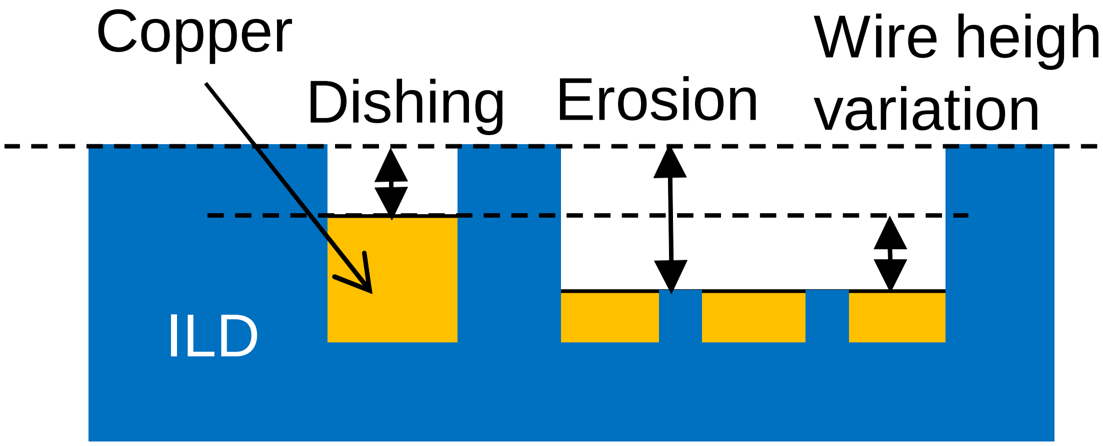


Fig. 3.1 Definition of dishing and erosion.

simulation is that it can guide layout optimization without a loop between layout optimization and fabrication. Thus, this chapter aims to develop a method to mitigate wire height variation with ECP and CMP simulations.

On the other hand, to guide the layout optimization and predict the final wire height variations, the accuracy of ECP and CMP prediction models is very important. Some CMP and ECP models that consider layout pattern dependencies were proposed [2, 32, 33]. However, our preliminary evaluation shows that these ECP models cannot reproduce the non-uniformity of the chips fabricated in our process technology. The cause of large errors in these ECP model should be identified and the ECP model needs to be improved so that it can be applied to various process technologies. In addition, our evaluation shows that the prediction models cannot predict large height variation which occurs in a specific region of a wafer and may miss open / short error. It is found that such large errors heavily depend on the die-to-die variation of ECP and CMP processes. This observation tells us that the prediction models need to consider the die-to-die variation of ECP and CMP processes.

Furthermore, the proposed mitigation method of wire height variation needs to be computationally efficient for putting the proposed method in use. The proposed method uses the chip layout parameters such as wire width and copper density frequently for prediction. In addition, the proposed method modifies the chip layout. Therefore, the proposed method needs to efficiently access and update the layout parameters. However, GDSII format is not suitable for such a purpose. Especially, dummy fill consists of a huge number of metal rectangles, and it is an obstacle making the cost of layout parameter access and modification too expensive.

This chapter provides solutions for these problems and implements the mitigation method of wire height variation. Experimental results show that the proposed method can mitigate the variation originating from ECP and CMP processes. The main contributions of this chapter are as follows.

- This work points out an accuracy degradation problem in the current ECP model and proposes a refined model that can be applied to various process technologies when the accuracy of existing ECP models is not sufficient.
- This work provides a fast technique of layout parameter extraction and revises an easy

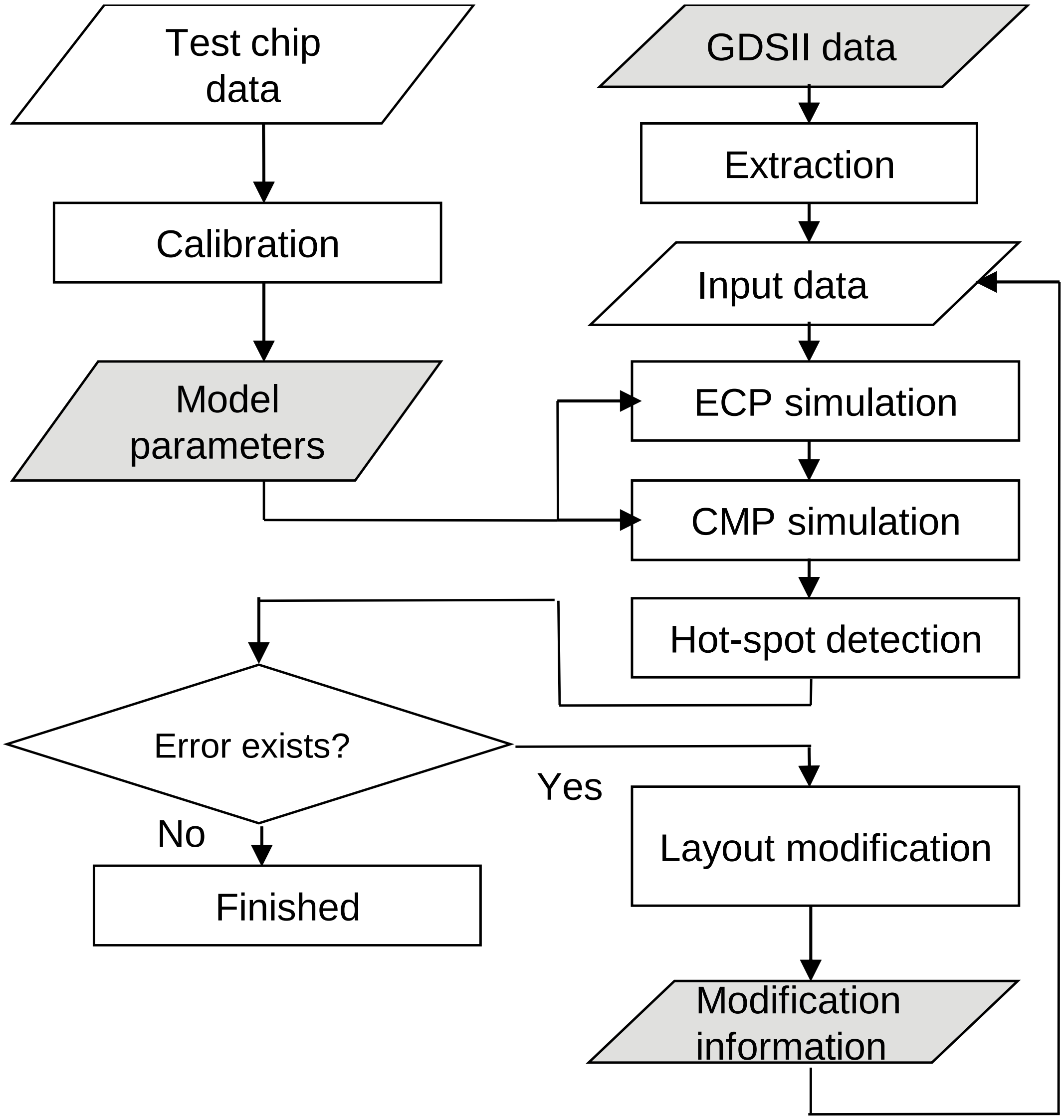

Test chip data
Calibration
Model parameters
GDSII data
Extraction
Input data
ECP simulation
CMP simulation
Hot-spot detection
Error exists?
Yes
No
Finished
Layout modification
Modification information

Fig. 3.2 Flow for mitigating wire height variation.

dummy fill revision method for making it possible to complete dummy fill insertion in a practical CPU time.

- This work highlights the information important for process designers, and makes it possible for process designers and circuit designs to quantitatively discuss features that should be incorporated in a wafer.

The rest of this chapter is organized as follows. Section 3.2 describes the overview of the proposed mitigation method of wire height variation. Section 3.3 discusses the issues to be solved in order to apply the proposed method to real production. The solutions for these issues are given in section 3.4. Section 3.5 shows the prediction results of the final surface of some chips to which the proposed method is applied. Finally, section 3.6 concludes this chapter.

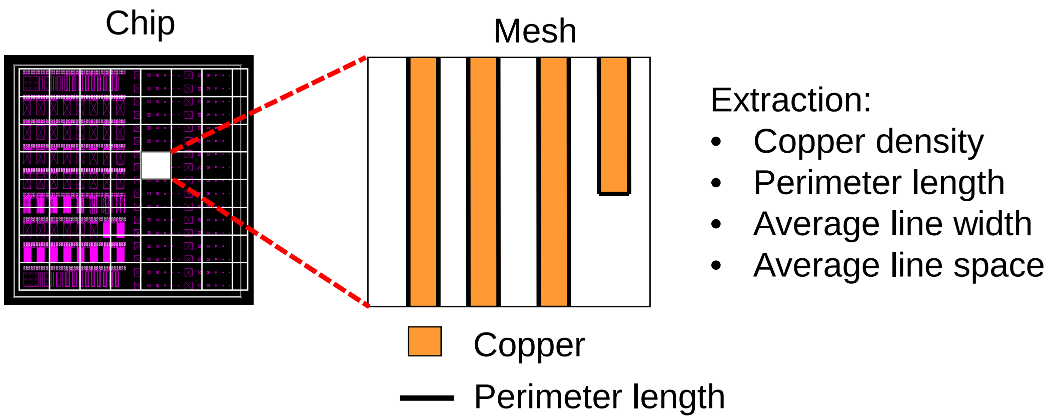


Fig. 3.3 Parameters extracted from a mesh.

3.2 Overview of proposed method for mitigating wire height variation

Figure 3.2 shows a flow of the proposed mitigation method of wire height variation. The input given to the proposed method is the chip data in GDSII format, and the output is the layout modification information. This proposed method firstly extracts the necessary parameters from the given data and then predicts the chip surface topography with ECP and CMP prediction models. Then, the chip surface is analyzed in the hot-spot detection step to check whether an error occurs or not. If errors exist, layout modification process, which updates the layout modification information and the input data of prediction models, is executed. This error analysis and layout modification are performed iteratively until all errors are exterminated or user defined conditions are satisfied. In addition to the main flow explained above, calibration step is required. Calibration step adjusts the prediction models for higher accuracy with the surface measurement data of the test chip designed for this calibration purpose. Calibration step should be used only once as far as the proposed method is done under the same ECP / CMP process conditions.

The detail of each step is discussed in this section.

3.2.1 Extraction

Chip layout characteristics are extracted as parameters that are included in the ECP and CMP process models. It is too time-consuming to calculate the heights of all the individual interconnects on the chip, and hence the chip area is often divided into small meshes (around 10 μm to 40 μm square). For each mesh, copper density and perimeter length are extracted, and average line space / width are calculated (figure 3.3). This extraction step itself is time-consuming if the GDSII data file format is used as it is, because the data size is too large. Moreover, its data structure is not suitable for extracting layout information in each mesh. The solution for this issue will be discussed in section 3.3.1.

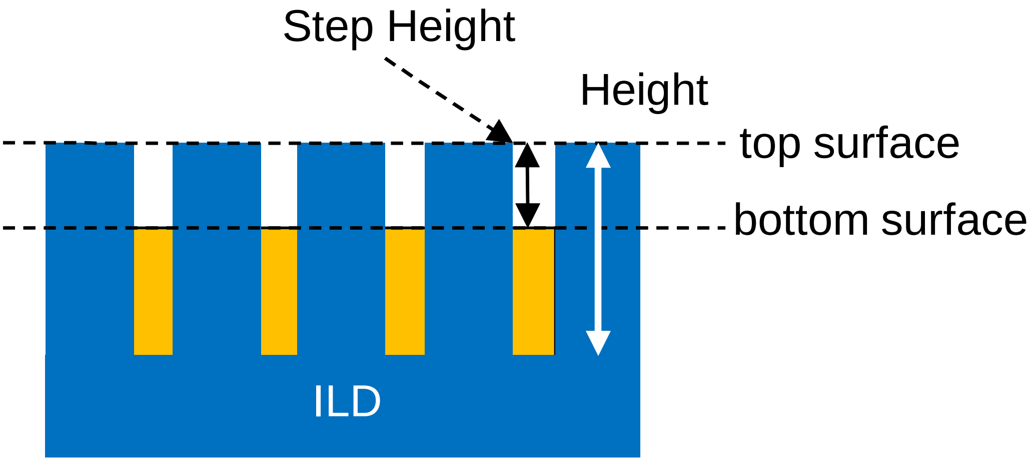


Fig. 3.4 Definition of height and step height.

3.2.2 ECP simulation

ECP process should be simulated accurately to estimate copper thickness variation on the whole chip which CMP process is not applied yet, because the ECP thickness variations strongly affect the final chip surface topography. In [32], Park proposed an ECP model that uses two parameters: average line width W_L and line space W_S within a mesh. In [33], Luo et al. proposed another ECP model considering physical mechanism. Both the models need to be calibrated with the data of ECP experiments to meet accuracy requirements. Calibration step will be discussed in section 3.2.5. On the other hand, these models are not capable of reproducing copper thickness variation in the manufacturing process of our interest. The model enhancement will be explained in section 3.3.2.

3.2.3 CMP simulation

CMP process is simulated with the results of the ECP simulation and the layout pattern parameters extracted at the extraction step explained in section 3.2.1. In [2], Tugbawa proposed a CMP simulation model that consists of two phases in calculation: the global and local phases. During the CMP simulation, the global and local phases are applied iteratively at each time step. Firstly, the global process calculates the distribution of pressure from the polishing pad at each mesh. Besides, each mesh has two height values: the height of the top surface and the height of the bottom surface (figure 3.4). Next, the local phase calculates the removal rates of both the surfaces under the pressure distribution computed in the previous global phase. Then, the local phase updates the heights of both the surfaces based on the obtained removal rates at each mesh.

To build an appropriate CMP model, several process parameters, such as polishing time, characteristics of slurry, shape of pad, pressure, temperature, etc. are required. It is, however, impractical to consider all these parameters, since the run-time could be exorbitant. Therefore, the CMP model should include only a few parameters to which the results of the CMP process are the most sensitive. The other parameters are fixed in calibration, and the CMP simulation is executed assuming they are fixed. If the fixed parameters need to be changed to cope with the new process conditions, the calibration step is to be re-executed.

3.2.4 Hot-spot detection and layout modification

After ECP and CMP simulations, the simulated chip surface data is analyzed to find hot-spots. A hot-spot is defined here as the point which may degrade timing / manufacturing yield due to the wire height variation occurred in ECP and CMP process. Its determination criteria is defined by manufacturers: for example, wire height variation value of a chip, absolute value of wire height, open / short error occurrence, and so on. When hot-spot errors are found in the chip surface data obtained through ECP and CMP simulations, the layout patterns and dummy fills should be modified to achieve target surface planarity. To identify hot-spots efficiently, viewer tools are required to visualize the chip surface and analyze the results. 2D/3D profiles help us to identify the problems in the chip layout. Also, a what-if analysis, which investigates the effect of the layout modifications without re-generating GDSII data files, is very helpful for designers and manufacturers to find appropriate layout modification. At this step, layout modification information is recorded if chip layout is modified. This modification is finally reflected on the GDSII data file.

3.2.5 Calibration

ECP and CMP models require calibration, because the mechanism of these processes is too complex to make accurate enough white-box model as discussed in section 1.3. Calibration adjusts model parameters to minimize the error between prediction results and experimental data. To obtain accurate models for practical use, test chips should contain various layout patterns in terms of line width, line space, and copper density. Usually CMP process consists of multiple steps as explained in section 1.1.3, and they have different process conditions. Therefore, in case of two-step CMP process, the experimental data for calibration is measured before and after each step and halfway during each step.

3.3 Issues to be solved for practical use of the proposed method

To make the proposed mitigation method of wire height variation practical, there are some issues to be solved. This section raises three major issues. These issues will be solved in the next section.

3.3.1 Handling huge chip data

Some chips are larger than 20mm square in area and have more than 10 interconnect layers. Since a huge number of copper rectangles is additionally inserted as dummy fill patterns for each layer, the size of the GDSII data that contains this dummy fill information can be very large (e.g. over 20GB). Extraction step is one of the most time-consuming step with such large data. In addition, dummy fill information is frequently accessed and updated to do a what-if analysis (as discussed in section 3.2.4) in layout modification step. Fast parameter extraction from GDSII data files and easy dummy fill revision method are essential requirements to improve the productivity of designers and manufacturers.

3.3.2 Accuracy of ECP model

The ECP model proposed in [33] and the CMP model proposed in [2] are evaluated using the test chip data to check whether those models can reproduce the experimental data. The CMP model showed good results of chip surface topography, but it is found that the ECP model has large errors for some layout patterns. This large error in the ECP model can mislead the layout modification and dummy fill insertion and prevents the manufacturing uniform surface. On the other hand, the ECP model is too compact to express all possible wire line / space combinations. The ECP model must be improved to handle the practical chip data.

3.3.3 Effective methods for analysis of the results

It is important to find hot-spots and to avoid errors in the chip surface analysis at hot-spot detection step. However, there are few cases that the experimental data includes errors without violating design rules in the typical process condition. On the other hand, when the process condition shifts due to die-to-die variation, some errors occurs. Most of such errors occur only in specific regions of a certain wafer. Effective methods to predict these errors are required.

3.4 Proposed approach

The issues described in the previous section prevent the proposed method from practical use. This section analyzes the causes of these issues and proposes their solutions.

3.4.1 Chip data extraction with virtual dummy filling method

The importance of input file extraction from GDSII data was discussed in sections 3.2 and 3.3. Copper density and perimeter length of wires in each mesh are required to be extracted for calculating average copper line width and line space. They can be extracted with commercial design rule checker (DRC) tools, but it is decided to develop our own extraction tool for the following two reasons. The first reason is the performance in speed and the capacity in memory usage. Since commercial DRC tools have multiple functions and their main purpose is to check design rule violations in a chip layout, they consume excessive CPU time and memory. Instead, a fast and compact extraction tool is needed for the proposed method. The second reason is the need for an incremental dummy fill modification function. Since dummy fills occupy large amount of GDSII data, the data size and CPU time can be reduced if the extraction tool itself can change dummy fills for simulation without changing the dummy fills in the GDSII file directly.

After analyzing the wire height variations, generally dummy fill patterns are to be refined rather than interconnect layout, because dummy fill modification has less impact on chip performance. The incremental modification function of dummy fill enables designers and manufacturers to carry out what-if dummy fill analysis easily and quickly.

This subsection now briefly describes the algorithm of our extraction tool to realize the incremental function. Firstly, each copper object is registered in all the meshes where the

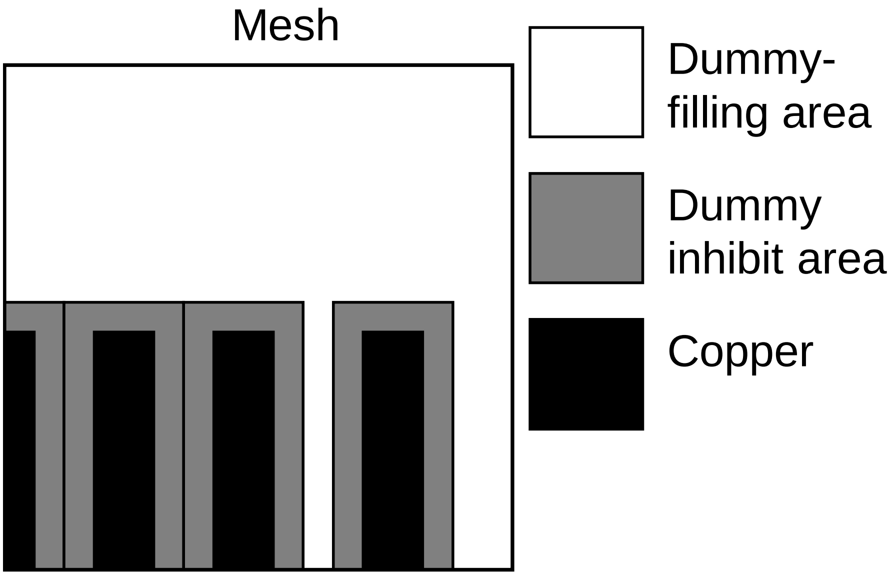


Fig. 3.5 Definition of dummy-filling area.

object lies. Then, in each mesh, copper area and perimeter length are calculated with a line sweep method [76]. The boundaries of each copper object are extended by the dummy-to-object spacing size defined in the design rules for taking into account dummy inhibit area, and the total blank area in the mesh is regarded as a dummy filling area. The dummy filling area, illustrated in figure 3.5, is considered to be the total available area where dummy fill can be placed. Copper area and perimeter length per unit area of the dummy fill pattern are used to calculate copper area and perimeter length of the dummy fill virtually inserted into a mesh. They will be saved in addition to the original copper area and perimeter length calculated without actually placing dummy fills in each mesh. This method is defined as virtual dummy filling. This virtual dummy filling causes some errors because the shape of the dummy fills and the shape of dummy filling area are not considered. However, the errors are small enough to hardly impact the final chip surface. When tuning the values of the copper area and perimeter length for layout optimization, it would be faster and easier not to handle the exact dummy fill shape and the definite dummy filling area as they are, but to control the values directly.

3.4.2 Refined ECP model

As discussed in section 3.3, existing ECP prediction models have large errors for the chips fabricated in our technology of interest. This subsection proposes a refined ECP prediction model based on the model [33] by Luo et al. for improving accuracy. Luo's model and our refined ECP prediction model are constructed by gray-box modeling approach to compensate for a loss of accuracy which originates from the sensitivity to ECP process condition, as mentioned in section 3.2.5.

In this subsection, firstly Luo's model is introduced, and then the causes of large prediction error are estimated from measurement data analysis. Finally, a refined ECP model is proposed.

In ECP process, the wafer is coated with copper in chemical solution containing copper ions. One of the main purposes of ECP process is to fill up the wire trenches with no voids. A void is defined as a hole in copper metal. To achieve void-free copper film, three additives, accelerators, suppressors, and levelers, are introduced [34]. Reid et al. [35] proposed an ECP model that explains additive's behavior.

In Luo's model, which is based on Reid's theory [35], the total volume of copper deposition is thought to be proportional to the amount of accelerators. Accelerators adhere to the whole chip surface, and hence the total volume is proportional to the surface area.

In Luo's model, input parameters are the perimeter length of interconnects L and the density of interconnect area ρ, and output parameters are copper thickness H and step height S. H is defined as the copper film thickness above the oxide area, and S is defined as the gap between the height of copper above the oxide area and the height of copper above the trench. S is positive when the height of copper above the oxide is larger than that above the trench (figure 3.6(B)).

In each mesh of the chip, surface area consists of top / bottom surfaces and sidewall of trenches. Therefore, copper volume V of a mesh can be expressed as

$$V = H_0(T_e L + D^2), \tag{3.1}$$

where H_0 is the copper thickness of the mesh that has no interconnect (figure 3.6(D)) and D is the mesh size. The effective trench height T_e is smaller than trench height T, because the amount of accelerators on the sidewall may be smaller than that on the top / bottom surfaces.

According to the layout pattern, there are three cases of copper deposition topographies (figure 3.6(A)-(C)). In each case, H and S are to be computed.

- **Case A**:
  Step height S is greater than 0 and accelerators outside the trench shrink the trench width by length δ_s. Then, the volume of copper is

  $$V = HD^2 - SD^2\rho_s + TD^2\rho, \tag{3.2}$$

  where ρ_s is the shrunk density after ECP process according to the length δ_s and H is the copper thickness of the mesh. Since the shrinks of the trench only depend on the accelerators outside the trench, the following relation holds.

  $$H_0 D^2(1 - \rho) = HD^2(1 - \rho_s). \tag{3.3}$$

  From equations 3.1, 3.2, and 3.3, H and S are obtained.
- **Case B**:
  Step height is smaller than 0 and accelerators in the trench expand trench width by length δ_e. Then, the volume of copper is

  $$V = HD^2 + SD^2\rho_e + TD^2\rho, \tag{3.4}$$

  where ρ_e is the expanded density after ECP process according to the length δ_e. Since the expansion of the trench only depends on the accelerators in the trench, the equation below holds.

  $$H = H_0. \tag{3.5}$$

  From equations 3.1,3.4, and 3.5, H and S are computed.

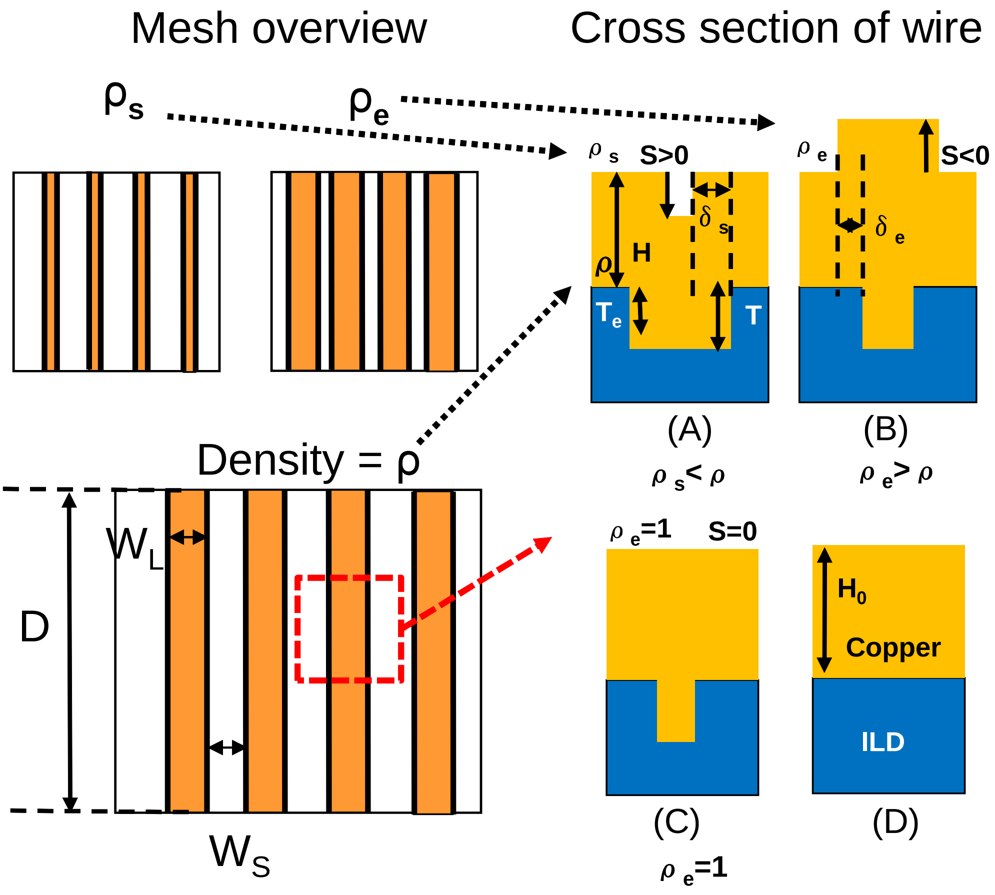

Mesh overview
Cross section of wire
ρs
ρe
ρ s S>0
ρ e S<0
H
ρ
δ s
δ e
Te
T
(A)
ρ s< ρ
(B)
ρ e> ρ
Density = ρ
WL
D
WS
ρ e=1 S=0
H0
Copper
ILD
(C)
ρ e=1
(D)

Fig. 3.6 3 patterns of ECP topography.

- **Case C** :
  Step height equals to 0.

$$S = 0. \tag{3.6}$$

  Then, the volume of copper is

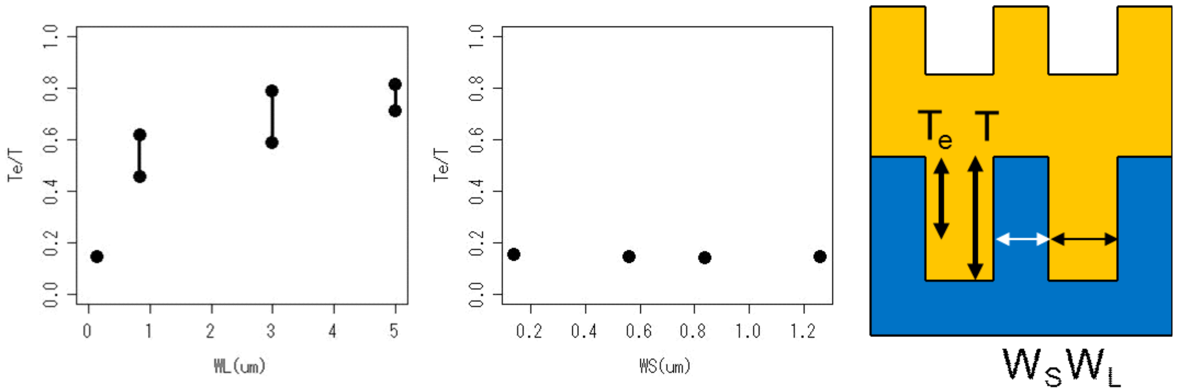
$$V = HD^2 + TD^2\rho. \tag{3.7}$$

  From equations 3.1, 3.6, and 3.7, H and S are obtained.

This is a brief explanation of Luo's model.

In this model, parameter T_e, δ_s and δ_e are calibrated with the measurement data of a test chip after ECP process is executed. Still, large errors are found in some layout patterns. This is because these calibration parameters are fixed regardless of line width and line space value in Luo's model. On the other hand, the proposed refined model regards it as a main cause of the prediction error and redefines these parameters as line size dependent value. To confirm the appropriateness of this treatment, the measurement data is analyzed as follows.

- T_e
  Parameter T_e value is calculated from measurement data of various line space / width



(1) W_L vs. T_e/T (2) W_S vs. T_e/T

Fig. 3.7 Relationship between parameter T_e and line width / space.

combinations in the test chip.

Figure 3.7 (1) shows the relationship between T_e and line width. Line space is fixed in this plot. X-axis means the value of line width and y-axis means the ratio of value T_e to the value T. Figure 3.7 (2) shows the relationship between T_e and line space. Line width is fixed in this plot. X-axis means the value of line space and y-axis means the ratio of value T_e to the value T. The range of each plot denotes the range of T_e value due to the case of the shape of copper deposition (figure 3.6 (A)-(C)).

These figures show that T_e depends on line width and is independent of line space value. It is natural that T_e is proportional to the line width because additives may easily adhere to the sidewall in a wide line and T_e value gets closer to the value T. In the proposed refined model, T_e is defined as

$$T_e = \min(\alpha_1 W_L^{\beta_1}, \gamma_1), \tag{3.8}$$

where W_L is the average line width of a mesh, α_1, β_1, and γ_1 are new calibration parameters instead of T_e. γ_1 is a limiting parameter for T_e value not to exceed T in wider line.

- **δ_s and δ_e**

  Figure 3.8 (1) - (4) show the relationship between δ_s and line width, δ_s and line space, δ_e and line width, δ_e and line space respectively. These figures show that parameter δ_s depends on line space and δ_e depends on line width. This means that expansion / shrunk length depends on the width of higher part of copper deposition topography. δ_s and δ_e are defined as

$$\delta_s = \alpha_2 W_S^{\beta_2}, \tag{3.9}$$

$$\delta_e = \alpha_3 W_L^{\beta_3}, \tag{3.10}$$

  where W_S is the average line space of a mesh, α_2, α_3, β_2, and β_3 are new calibration parameters.

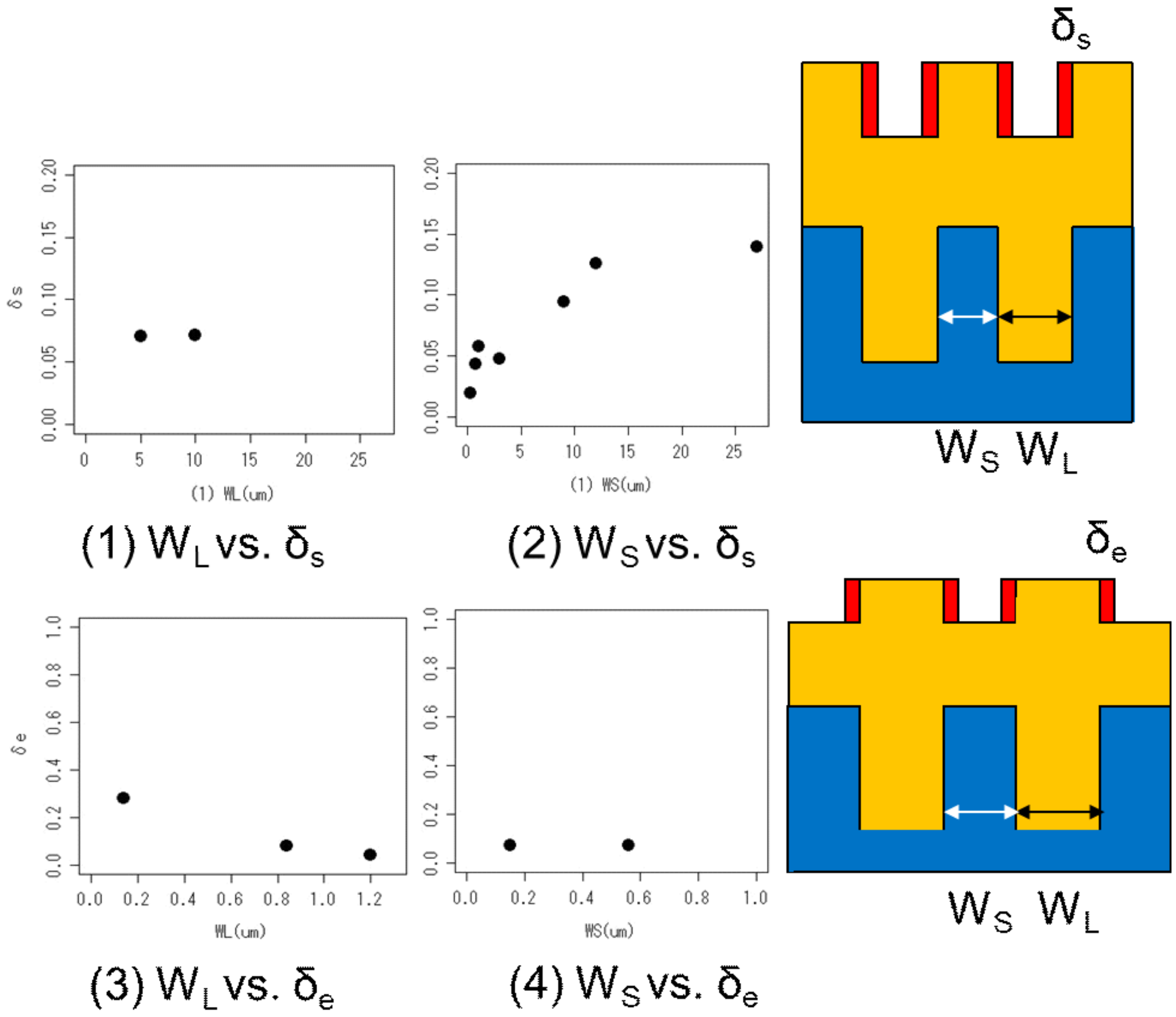


Fig. 3.8 Relationship between parameter δ_s, δ_e and line width / space.

3.4.3 Effective hot-spot detection method

This section discusses an effective hot-spot detection method that considers the die-to-die variations during ECP and CMP processes.

As was discussed in section 3.3, proper design rules and ECP / CMP process recipe seldom cause errors under typical conditions of ECP and CMP processes. So as not to miss hot-spots, die-to-die variations should be considered during ECP and CMP simulations.

From the analysis of the measurement data and mechanism of ECP and CMP processes, it is found that the variation of copper thickness after ECP process and that of over-polishing time have the largest impact on the final chip surface topography. To consider the variation of these parameters, maximum, minimum, and nominal values are set for each parameter corresponding to over, under, typical conditions. The proposed mitigation method of wire height variation is executed for all the combinations of these two parameters. Each parameter has three values, and hence the chip surface prediction is executed under 9 combinations, i.e.

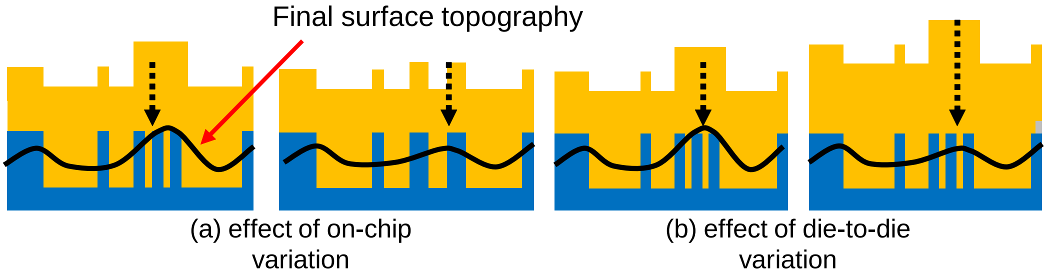

Final surface topography
(a) effect of on-chip variation
(b) effect of die-to-die variation

Fig. 3.9 Relationship between ECP topography and final surface topography.

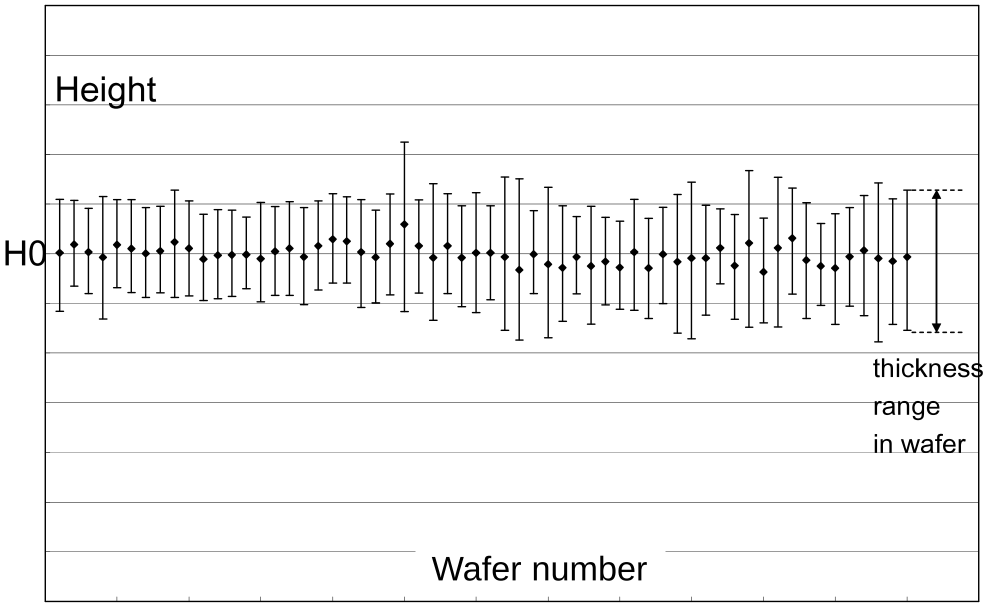


Fig. 3.10 Wafer-to-wafer variation of copper thickness range within a wafer.

9 process conditions.

The following explains initial copper thickness and over-polishing times.

- **Initial copper thickness variation**
  Initial copper thickness variations after ECP process have a great influence on non-uniformity of the chip surface in terms of on-chip and die-to-die variations. Large on-chip variations after ECP may cause final chip non-uniformity because initial height variations are propagated through the entire CMP process (figure 3.9 (a)). However, on-chip variations can be predicted with the accurate ECP prediction model proposed in section 3.4.2.
  On the other hand, the difference of initial copper height caused by die-to-die variations changes polishing time, which has an impact on the final surface. Generally, CMP process reduces surface non-uniformity among the polishing in copper removal stage. The additional polishing of the copper increase makes the final surface to-

pography more uniform than that of normal copper height one (figure 3.9 (b)). This difference is not considered in the CMP prediction model.

Figure 3.10 shows measurement data of the intra-wafer variations and wafer-to-wafer variations of initial copper thickness after ECP process. From these data, the proposed method statistically determines and uses three values of initial copper thickness (over, typical, under) as corner conditions in prediction.

- **Over-polishing time variation**

  Over-polishing time is defined as the polishing duration after endpoint detection in copper removal stage. As described in section 1.1.3, CMP process consists of copper removal stage and barrier removal stage. In the copper removal stage, a sensor in the CMP machine searches the point where barrier metal is exposed during polishing. This technique is the endpoint detection and the key process to achieve planarity of the chip surface. After an endpoint is detected, the barrier removal stage takes over the process from the copper removal stage to clearly remove overburden copper. This technique adjusts polishing time properly to achieve the target height even though initial copper height and removal rate vary widely.

  When an endpoint is detected on a certain chip on a wafer, some chips on the same wafer may have already reached the endpoint. This is because the sensor does not always detect the first endpoint of the wafer. For the chips that has already reached the endpoint, the over-polishing time after the barrier metal exposure becomes longer. Conversely, for the chips that have not reached the endpoint, the over-polishing time after the endpoint detection becomes shorter than expected. This is the mechanism of over-polishing time variation.

  If over-polishing time is too long, dishing progresses more seriously. It is because the removal rate of barrier metal is generally much lower than that of copper at copper removal stage. On the other hand, if over-polishing time is too short, copper residue may cause short errors in interconnect. Thus over-polishing time variation has a great impact on CMP results. The proposed method uses three values of over-polishing time (over, typical, under) in prediction to detect errors occurring only in corner conditions.

The proposed method executes the prediction explained in section 3.2 for every condition and can consider the worst case originating from the die-to-die variations during ECP and CMP processes. If hot-spot is detected even in a single combination, this chip data has high probability of error occurrence. Thanks to the proposed method, designers and manufacturers can predict the hot-spot occurrence correctly before manufacturing.

3.5 Experimental results

Experimental results of the proposed method are discussed in this section. All the experiments were performed on a 2.8GHz Opteron Linux machine with 16GB memory, and test chips for measurement data were manufactured with our 65 nm technology node.

Firstly, the calibration parameters of the model of [33] (T_e, δ_s, and δ_e) and those of the proposed ECP model of section 3.4.2 (α_1–α_3, β_1–β_3, and γ_1) are adjusted. These calibration step is executed with the experimental data of the test chip after ECP process. These data include the results for the line arrays whose width and density range from 0.14 μm to 25 μm and from 5% to 90%, respectively. Figure 3.11 shows simulation results vs. experimental results of copper height H and step height S. These graphs include the results for the line

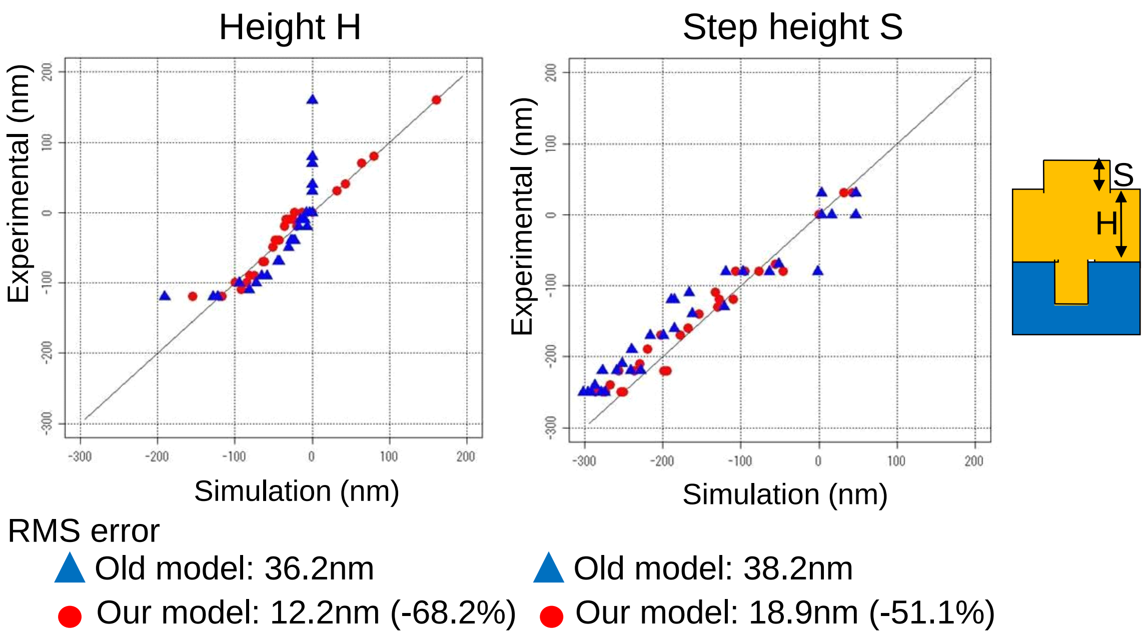


Fig. 3.11 Simulation vs. experimental results of ECP process.

arrays which is used for the calibration step. The results of the model of [33] are also plotted in figure 3.11. Diagonal lines mean there is no difference between the prediction results and the experimental results. Using the proposed model, in comparison with the model of [33], the average RMS errors of H is reduced from 36.2 nm to 12.2 nm (-68.2%) and the average RMS errors of S is reduced from 38.2 nm to 18.9 nm (-51.1%). Especially, the maximum error of copper height H is reduced from 160 nm to 30 nm (-81.25 %).

Input data for ECP and CMP prediction is extracted from GDSII files, and a fast parameter extraction method is developed in section 3.4.1. This fast extraction tool is first compared with a commercial tool on some industrial chip data. Table 3.1 shows that our tool is less time-consuming and uses less memory than commercial tool. Our tool cannot extract input data from GDSII data C, but GDSII data C without dummy fill information can be handled. Our tool can predict and modify these data according to the virtual dummy filling method. The maximum error of copper density caused by this fast extraction and virtual dummy filling is 5.4 % and there is little difference in final chip surface topography.

After extraction, the final chip surface data is obtained by running ECP and CMP prediction. To take into account die-to-die variations, prediction is carried out under different conditions of initial copper height and over-polishing time as discussed in section 3.4.3. In the hot-spot detection stage, chip surface of each condition is checked with a viewer tool. Figure 3.12 shows snapshots of the chip surface. In this case, chip surface prediction is executed under 9 process conditions. The chip surface corresponding to the typical condition has small variation (figure 3.12 (A)). Its wire height variation is 24nm. The worst chip surface variation is observed under the condition that both initial thickness and over-polishing time take the minimum value. Figure 3.12 (B) shows its surface topography. Its wire height variation is 45 nm and unclear copper causes short errors.

From the analysis of chip layout, the causes of this error seem that wide interconnect lines

Table 3.1 Comparison with commercial tool in extraction process.

Chip Data			Commercial tool		Our tool	
Name	Size (mm^2)	Data size	CPU time (min.)	Mem size	CPU time (min.)	Mem size
A	15.5 × 16.0	6.2MB	18.0	10.0GB	5.0	99.0MB
B	4.8 × 3.8	54MB	14.0	2.5GB	0.4	114.0MB
C	9.9 × 9.9	26GB	N/A	N/A	N/A	N/A
C (w/o dummy)	9.9 × 9.9	77MB	N/A	N/A	3.4	210.0MB
D	8.0 × 6.4	4.7GB	N/A	N/A	164.6	9.1GB
E	21.3 × 20.9	6.0GB	N/A	N/A	875.3	13.3GB

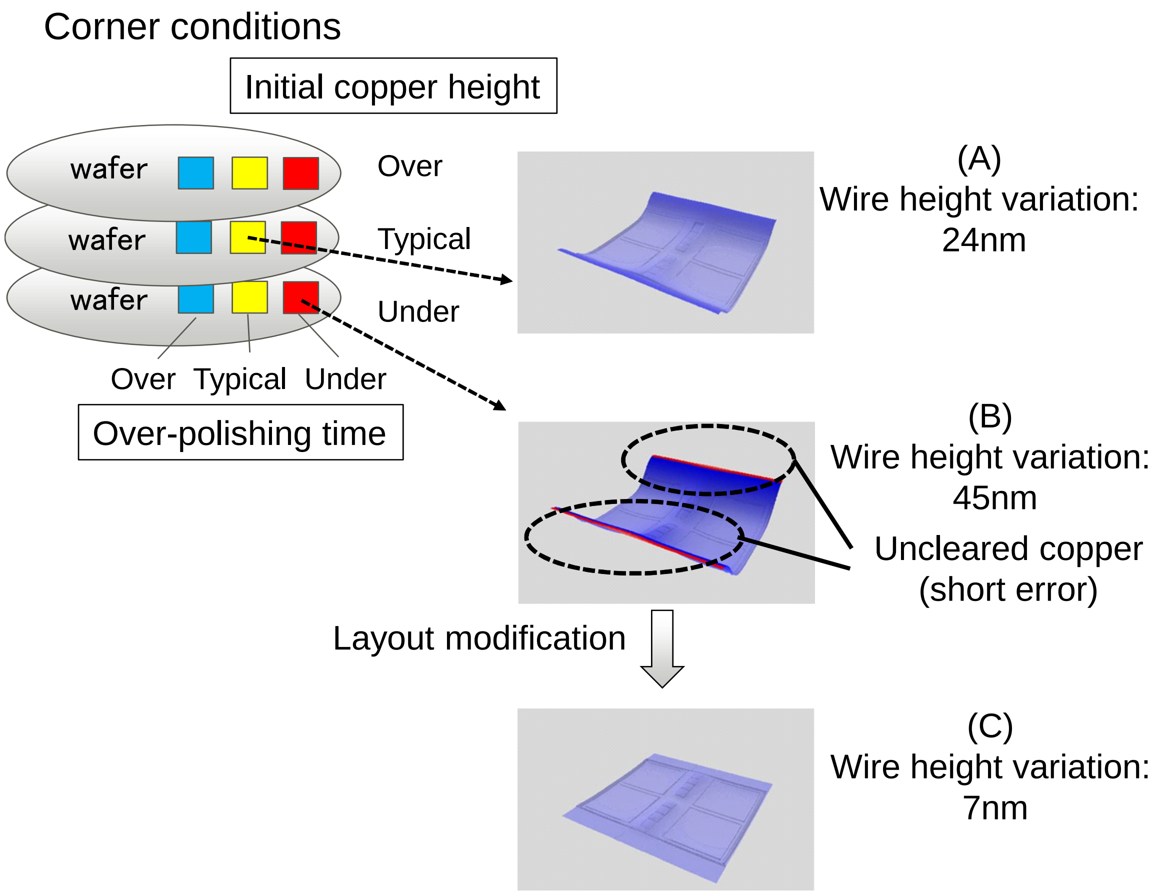

Corner conditions
Initial copper height
wafer
wafer
wafer
Over
Typical
Under
Over Typical Under
Over-polishing time
(A)
Wire height variation:
24nm
(B)
Wire height variation:
45nm
Uncleared copper
(short error)
Layout modification
(C)
Wire height variation:
7nm

Fig. 3.12 Chip surfaces with effective hot-spot detection method and a modification result.

are heavily used in this design. The feature sizes of interconnect and dummy fill become imbalanced, which causes poor performance in ECP and CMP processes and results in short errors. In order to avoid short errors, dummy fill layout is changed to balance the dummy fill size with wide interconnect lines. The input data of prediction is updated without modifying GDSII, which is the feature of the proposed virtual dummy filling method, and simulation is executed again. This process costs only 7 minutes. This is much shorter than the time for initial extraction which is 389 minutes. The reason is that dummy modification is done with virtual dummy filling method without accessing or modifying GDSII data. Figure 3.12 (C) shows the final chip surface of the modified layout under the same corner condition which caused short error before the modification. Wire height variation is decreased to 7 nm (-84.4%) and short errors are successfully avoided before manufacturing.

3.6 Conclusion

This chapter presented a method to mitigate wire height variation with ECP and CMP prediction models and proposed approaches to solve the issues that arose during its practical use. A data extraction tool that could handle large-size chip data within reasonable memory size and CPU time was developed. The ECP prediction model was improved, which reduces average errors in copper height by 68.2% and step height by 51.1%. An effective hot-spot detection method considering die-to-die variations was proposed. This method is helpful to find short errors originating from die-to-die variation. Finally, experimental results showed a case study of wire height variation mitigation. Thanks to the proposed method, wire height variation of chip surface is reduced by 84.4% and short errors are avoided before manufacturing.

Chapter 4

Edge-over-Erosion error prediction based on multi-level machine learning

This chapter describes an Edge-over-Erosion error (EoE-error) prediction method in chemical mechanical planarization (CMP) process that exploits machine learning algorithms. The proposed method consists of (1) error analysis stage, (2) layout parameter extraction stage, (3) model construction stage, and (4) prediction stage. In the error analysis and parameter extraction stages, test chips are analyzed to identify layout parameters which have an impact on EoE phenomenon. In the model construction stage, a prediction model is constructed using the proposed multi-level machine learning method, and designed layouts are checked if EoE-error occurs or not in the prediction stage. Experimental results show that the proposed method attained 2.7–19.2% accuracy improvement of EoE-error prediction and 0.8–10.1% improvement of non-EoE-error prediction compared with general machine learning methods. The proposed method makes it possible to prevent unexpected yield loss by recognizing EoE-errors before manufacturing.

4.1 Introduction

As described in chapter 3, CMP process affects wire height variation. Figure 4.1 shows the cross sectional view of wire height variations. Wire height variations produce chip performance degradation due to an increase in wire resistance and capacitance, and may cause open / short errors. Furthermore, thickness variations are propagated to upper layers, and the accumulated variations could cause an excess of depth-of-focus in photolithography and short errors in the worst case [2, 32].

This wire height variation is getting severer according to device miniaturization, which imposes more precise planarization on CMP process. In recent technologies, wire height variations due to CMP process are major cause of yield loss [9, 10, 93, 94].

Recently Edge-over-Erosion error (EoE-error) is frequently observed [48] in addition to dishing and erosion as discussed in section 1.2.3. Figure 4.1 illustrates the cross section of an EoE-error. This error occurs at copper removal stage of CMP process. At this step, multiple materials are polished simultaneously, where the removal rate of copper is much higher than that of barrier metal. At the location where an EoE-error occurs, the unexpected

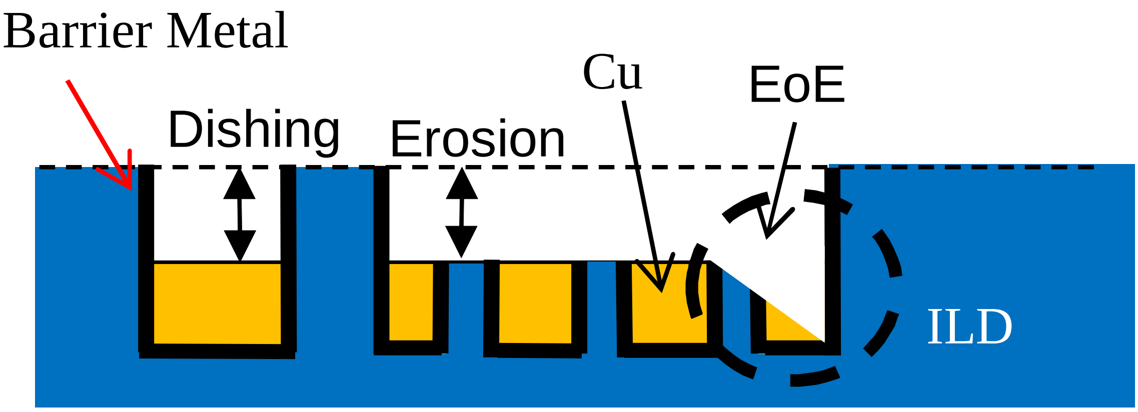


Fig. 4.1 Cross sectional view of interconnect layer.

over-polishing error can be more than ten times larger than an estimate which is predicted from material-dependent removal rates. EoE-errors cause open errors, and furthermore may cause short errors at its upper layer. Although several works investigated the root cause of EoE phenomenon [48, 95], little is known about the mechanism of this problem.

To avoid EoE induced open and short errors, EoE-errors should be eliminated. However, it is too costly to modify chip layout to mitigate EoE-errors after manufacturing and testing. Another approach for EoE mitigation is to tune some CMP process parameters, such as slurry, polishing pad, rotation speed, pressure, etc. [95], but it involves a comprehensive and consequently expensive tuning because CMP process is very sensitive to various parameters and their inter-dependency. As discussed in chapter 3, CMP simulation is an effective method to predict wire height variations before manufacturing and nowadays has become an essential step to optimize wafer surface uniformity in chip design flow [33, 80]. However, no tools take into account EoE-error problem explicitly. Therefore, it is highly demanded to develop a prediction method that systematically estimates EoE-errors in design time to avoid unexpected yield loss.

Motivated by that, this chapter proposes a systematic EoE prediction method aiming at mitigating EoE-errors in design time. Contributions of this work include the followings.

- This is the first work that presents an EoE-error prediction method. Because of the high sensitivity of EoE phenomenon to CMP process condition, there is a certain amount of noise peculiar to individual chips, and hence an overfitting problem easily happens with normal machine learning algorithms when pursuing high accuracy. This work thus explored and applied multi-level machine learning algorithm suitable for EoE-error prediction.
- This work presents a procedure that extracts model parameters which should be included as variables in machine learning for EoE model construction. Analysis of test chips distinguishes the layout parameters which really have an impact on the ambiguous EoE phenomenon, and screen out non-influential parameters which degrade accuracy as noise sources.
- The accuracy of the proposed method is assessed with industrial chip data.

The rest of the chapter is organized as follows. Section 4.2 provides the overview of the proposed method consisting of four stages: error analysis stage, layout parameter extraction stage, model construction stage and prediction stage. Then error analysis and parameter extraction stages is introduced in section 4.3 and model construction and prediction stages in section 4.4. Section 4.5 presents the results and analysis of the proposed method. Finally, section 4.6 concludes this chapter.

4.2 Concept and overview

This section explains the concept and overview of the proposed method.

4.2.1 Concept of EoE-error prediction method

As mentioned in the previous section, the mechanism of EoE occurrence is complicated and is not understood well enough to build a physical EoE model. Thus, instead of constructing a physical EoE model by gray-box modeling approach, the proposed method employs machine learning techniques to predict EoE-error locations by black-box modeling approach with measurement data of real chips. Here, machine learning technique is a general method for statistical data analysis and a powerful tool for finding regularities in the dataset.

The proposed method first selects an appropriate set of layout parameters to model EoE-error by analyzing measurement data of the test chip designed for this EoE-error modeling purpose, because at the beginning there is little information about phenomenon in the process technology of interest. Then the proposed method constructs a model which has these layout parameters as variables using another measurement data of a calibration chip which is designed for a real product and includes various layout patterns.

4.2.2 Overview of EoE-error prediction method

Figure 4.2 shows the flow of EoE-error prediction method. This method consists of four stages: error analysis stage, parameter extraction stage, construction stage, and prediction stage. This method first analyzes the EoE-error measurement data of the test chips to clarify which layout parameter should be included as variables in the prediction model. Next, layout parameters selected in the previous error analysis are extracted from the calibration chips. Then, model construction process is carried out with machine learning methods and a prediction model is constructed. Finally, the constructed model is applied to new designs for predicting EoE-errors before manufacturing.

To find parameters which affect EoE-errors, a detailed analysis is executed with the surface measurement data of the test chip. Figure 4.3 shows the details of the test chip. Two terms are defined in figure 4.3 as follows.

- **Module**
  A module is filled with a set of regular wires. Each module has parameters : wire width, metal density, and module size. Metal density is defined as the ratio of copper wires area to the module area. Within the module, the wire width and space are uniform. A module is filled with copper only when metal density is 100% and filled with dielectric only when metal density is 0%. The area outside modules is filled with dummy fills.
- **Array**

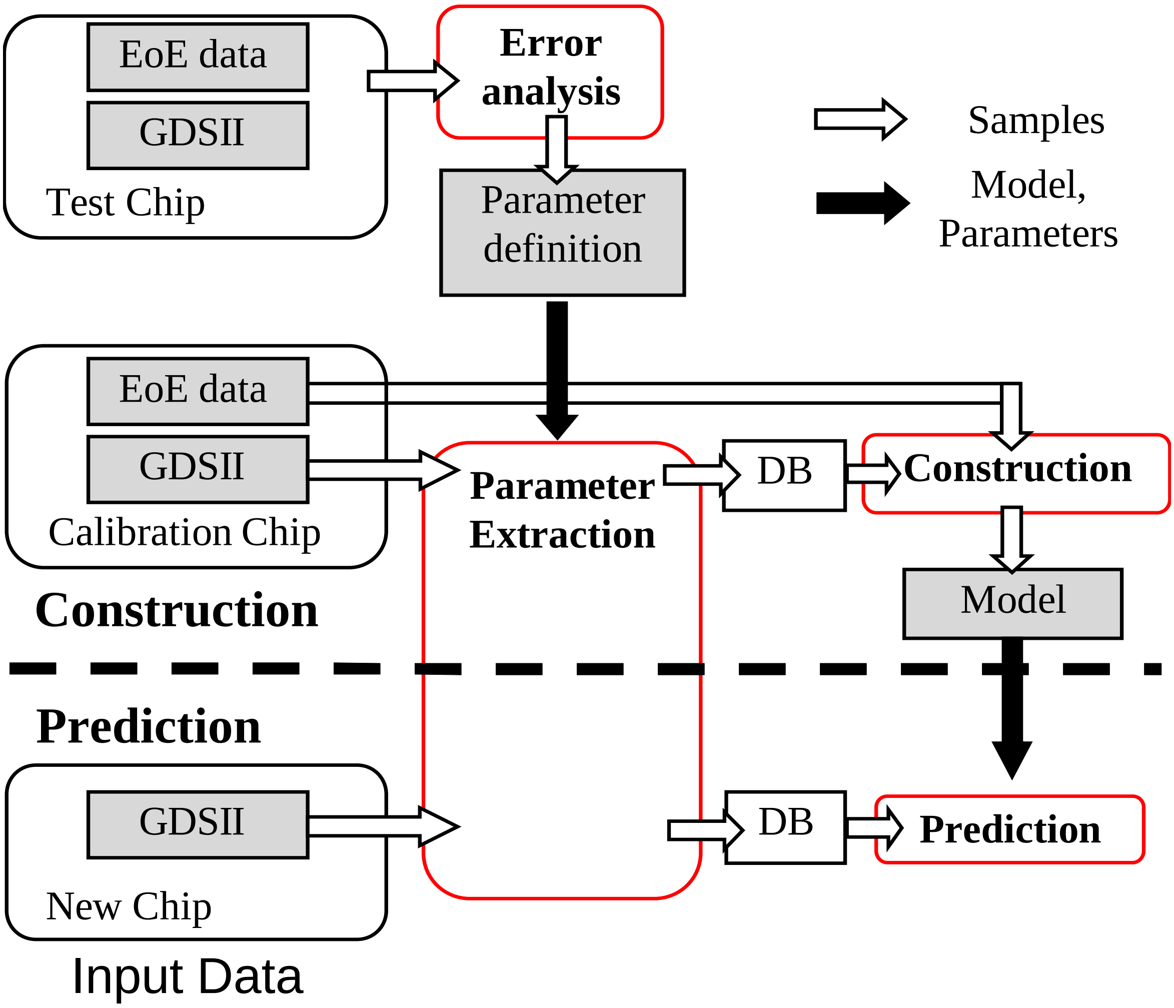

EoE data
GDSII
Test Chip
Error analysis
Parameter definition
Samples
Model, Parameters
EoE data
GDSII
Calibration Chip
Parameter Extraction
DB
Construction
Model
Construction
Prediction
GDSII
New Chip
DB
Prediction
Input Data

Fig. 4.2 Overview of proposed EoE-error prediction method.

> An array consists of modules. Each array has its own target parameter to investigate the EoE dependency on the parameter. In each array, the modules have different values of the target parameter, while other parameters are set to the same value in all the modules.

For example, each module in array A has the same module size, the same wire width, and different metal densities. In array B, module size is various but other parameters are the same. Analyzing the post-CMP surface of such patterns enables us to roughly recognize parameters which affect EoE-errors.

Then, layout parameters of interest, e.g. metal density and line width, are extracted from the original chip data and converted to new database. Hereafter, layout parameters mean these parameters. Generally, the physical chip data is recorded in GDSII format or OASIS (Open Artwork System Interchange Standard) format. These databases have a large file size (more than tens of gigabytes) since they have the entire chip information, and it costs much to get layout parameters directly from the original database. To reduce the size of database and calculation cost, a whole chip is discretized into small meshes and related parameters are

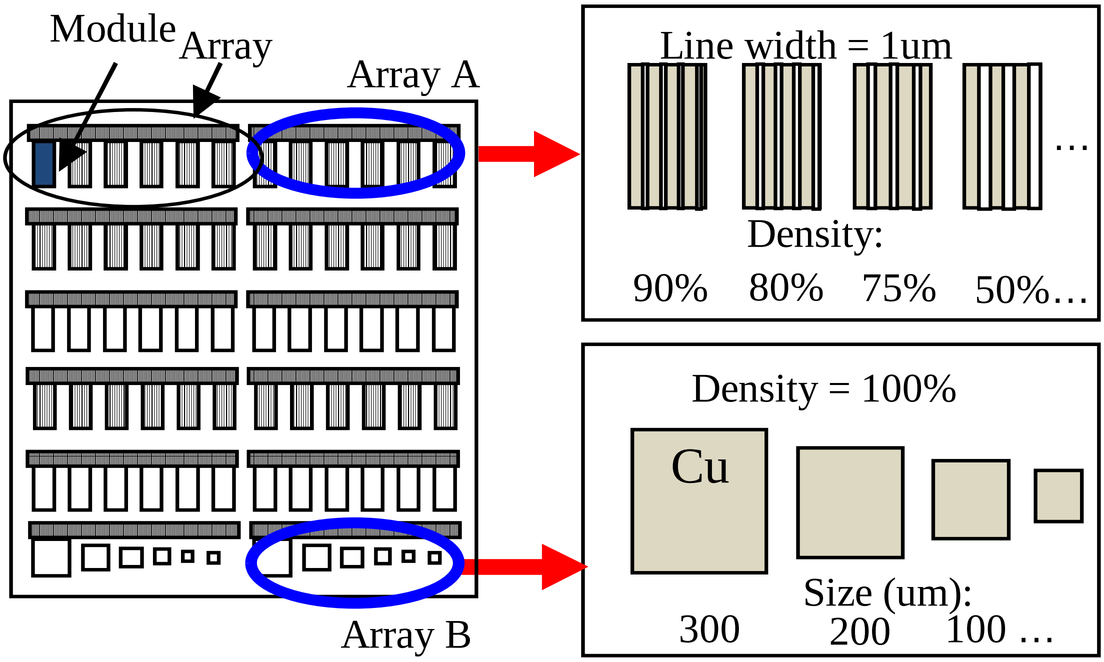


Fig. 4.3 Test chip structure.

extracted and recorded for each mesh in the same way as discussed in section 3.2.1.

In the model construction stage, an industrial chip is used as a calibration chip to build the EoE prediction model that has the layout parameters selected in error analysis stage as variables. In contrast with the test chip mentioned above, a wide range of layout parameter values and more complex combinations of multiple layout parameters are included in a real design. Therefore the training with an industrial chip is suitable for evaluating the effect of each parameter quantitatively. Besides, the EoE-error area is generally very small (< 1% of whole chip area). The number of EoE-error meshes, which are meshes that include EoE-error, is much smaller than that of non-EoE-error meshes in a chip. When building a prediction model, the training dataset from industrial chips becomes imbalanced, i.e. the numbers of EoE-error and non-EoE-error meshes in the training dataset become imbalanced, which causes poor performance of machine learning algorithms. Instead, in order to construct a precise model, the training dataset which includes EoE-error and non-EoE-error meshes with an appropriate ratio (e.g. 50%) must be prepared by non-uniform sampling and given to machine learning algorithms.

After constructing the EoE prediction model with machine learning algorithms, EoE-errors of new chips are predicted in prediction stage. Note that this prediction model can be applied to the chips which will be manufactured under the same process condition. If the process condition is changed, model construction for the new condition needs to be executed.

4.3 Error analysis and parameter extraction stages

This section explains the error analysis and parameter extraction stages in which layout parameters are extracted with analyzing the post-CMP surface data of the test chip.

The test chip includes modules with various values of line width, density, and module sizes. The space between modules is filled with dummy fill patterns. For the purpose of data size reduction, the whole chip is divided into small meshes, as mentioned before. The prediction model is built as a function of average parameters of adjacent meshes instead of individual metal segments. The mesh size has an impact on trade-off relation between computational cost and estimation accuracy, and a mesh size of $10 - 40\mu$m is often used in ECP and CMP process simulation for sub-100 nm processes [33, 96]. In this work, the mesh size was set to $10 \times 10\mu$m thinking much of the accuracy. Considering the impact on wire parameter variation and copper residue of upper layer, the EoE-error is defined as the place at which a height of erosion is larger than 40% of wire height.

Figures 4.4 and 4.5 show the cross section of some modules in the test chip after CMP process. In all cases erosion is observed at the high metal density side of the boundary between module and inter-module area, where the inter-module area is filled with dummy fills. More importantly, in the cases of (a) of both figures, EoE-errors are observed. The height of EoE-error is as tall as wire height and then open error occurs. With analyzing these data carefully, the following layout parameters seem to have a relation to EoE-errors.

1. **Metal density**
   Firstly figure 4.4(a) and (b) are examined. EoE-errors are observed at the place where the metal density is higher than its adjacent area. When the difference in metal density between adjacent areas is not sufficient, EoE-errors are not observed (figure 4.4(b)). On the other hand, not only the difference between adjacent areas, but the absolute value of metal density plays an important role. In figure 4.4(c), the metal density difference is larger than that of case (a), but no EoE-errors are observed. For these reason, this work uses metal density of the mesh and max/min metal density of adjacent meshes.
2. **Effective density**
   In spite that metal density is 0% in the module area in both cases of figure 4.5, EoE-errors are observed only in case (a). This difference suggests that the metal density variation within a small region is filtered out and high frequency components of metal density in space need to be eliminated for EoE-error prediction. For this purpose, a parameter called “effective length” is introduced. Figure 4.6 shows the definition of an effective length. The effective length is the distance in which a feature influences planarization in polishing process. This parameter is also called “planarization length” or “interaction length”, and an appropriate value of effective length is determined by CMP process modeling methodology in each process condition [2, 33, 74, 97]. Using this effective length, this work defines effective density of each mesh such that effective density is the average metal density within the range of effective length from the mesh of interest (figure 4.7).
   With further observations from the test chip, it turns out that EoE-errors occur at the place where the metal density is higher than the effective density. A parameter of density deviation D_d is defined as follows.

$$D_d = \frac{D_e - D}{D}, \tag{4.1}$$

where D is metal density and D_e is effective density. Here, metal density D is defined as the average metal density within the mesh of interest. Figure 4.8 illustrates the

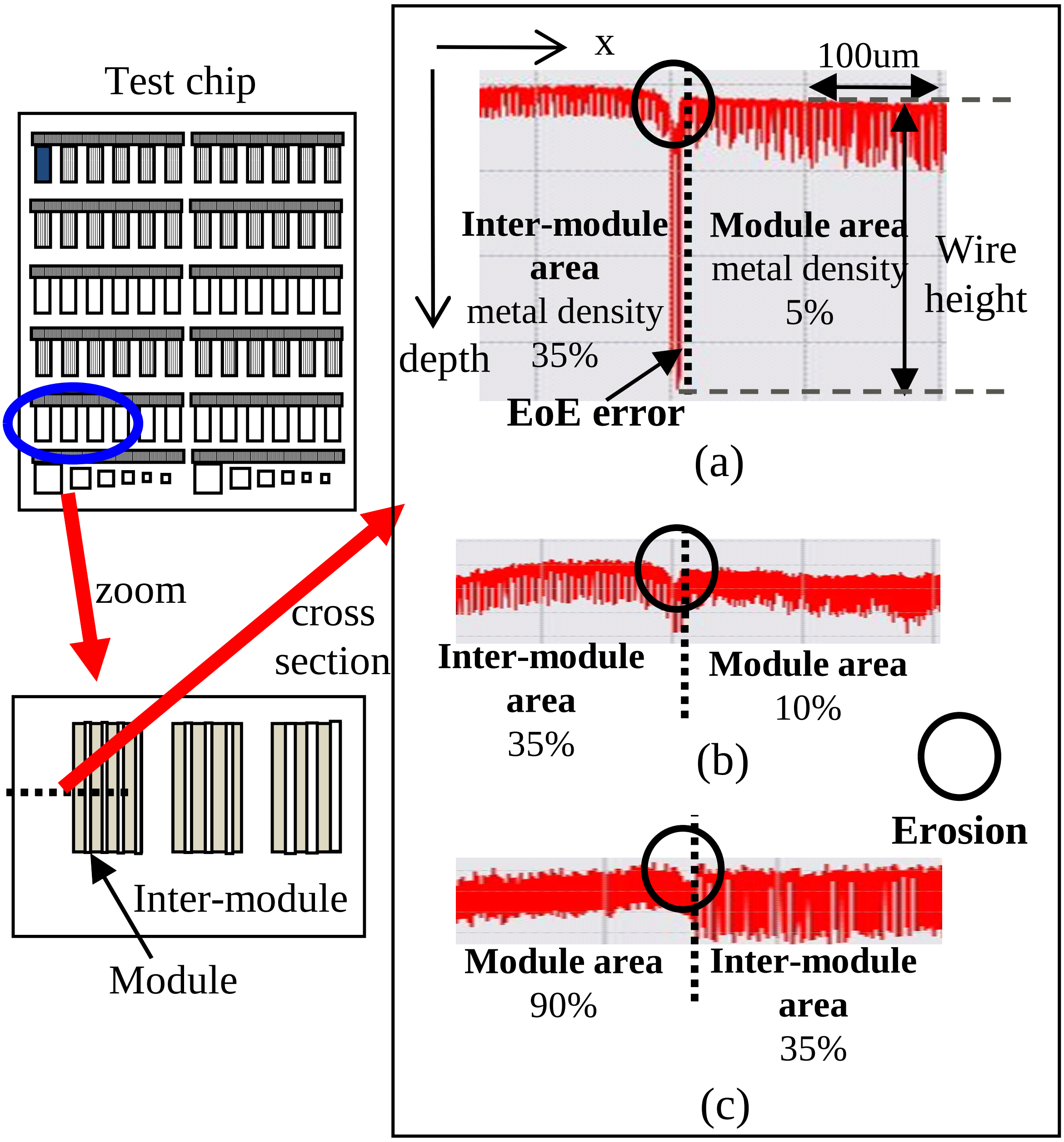

Test chip
zoom
cross
section
Inter-module
Module
x
depth
100um
Inter-module
area
metal density
35%
Module area
metal density
5%
Wire
height
EoE error
(a)
Inter-module
area
35%
Module area
10%
(b)
Erosion
Module area
90%
Inter-module
area
35%
(c)

Fig. 4.4 Relationship between EoE and metal density of module area.

relationship between D_d and erosion depth (EoE occurrence) at the edge of various modules in a 65nm technology node. This result shows that D_d is a good indicator for EoE-error.

3. **Line width**
   Wider metal lines are likely to become a cause of EoE-errors. The EoE-error of narrow lines ranges over multiple materials, while that of wider lines is mainly due to the disappearance of copper metal (figure 4.9). Generally, the polishing rate of barrier metal is much smaller than that of other materials, and hence line width should be considered.

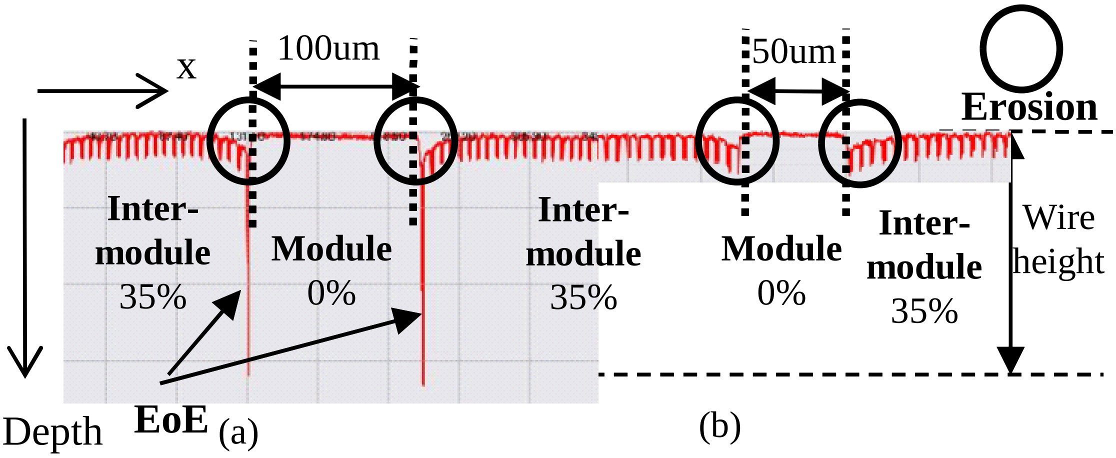


Fig. 4.5 Relationship between EoE and module size.

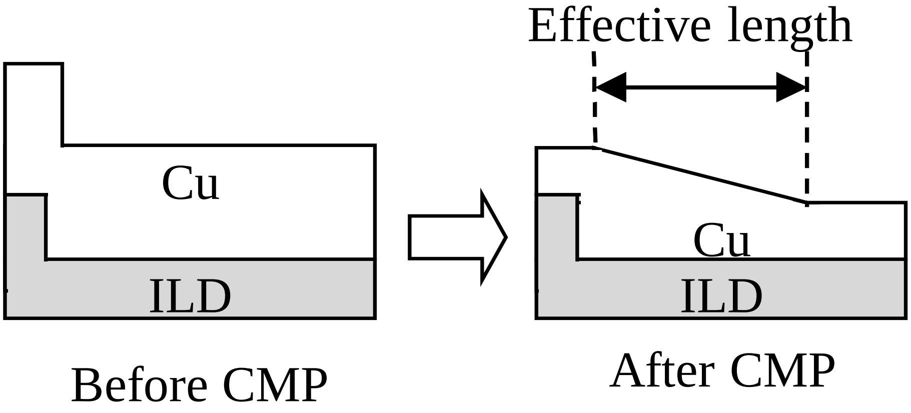


Fig. 4.6 Definition of effective length.

Then a database is constructed including following parameters for each discretized mesh: metal density, max/min metal density of adjacent meshes, effective density, density deviation, and line width. This database will be used in the next model construction stage.

For this 65 nm technology node, this work selects these 6 layout parameters to model EoE-errors. For another technology node, such as advanced technology, the layout parameters that have impact on EoE-errors may change. On the other hand, it is expected that error analysis stage identifies influential layout parameters on EoE-errors at a particular technology of interest, since a test chip fabricated in the technology, which includes various layout patterns and covers wide range of parameters, is newly analyzed. Once the influential parameters are identified, a prediction model is constructed that have the influential parameters as input variables and is used for EoE-error prediction.

It should be noted that these parameters are affected by process variation. Especially etching and lithography processes have a great influence on line width variation [98, 99]. Additional process might be required to eliminate the impact of process variation if the impact is

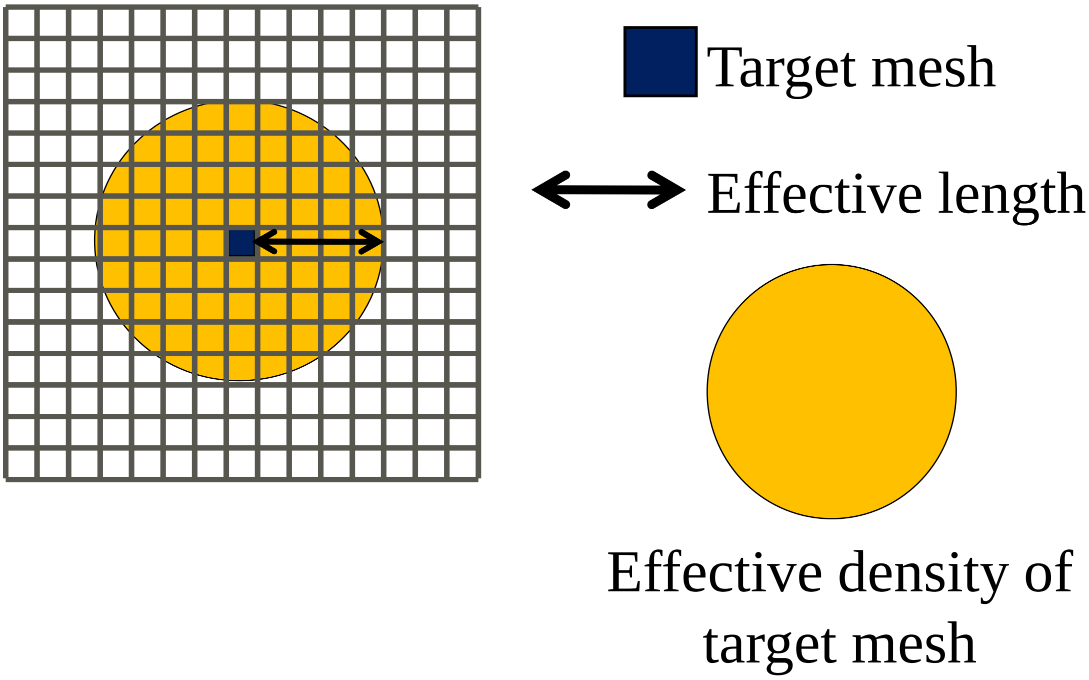

Target mesh
Effective length
Effective density of target mesh

Fig. 4.7 region for effective density computation.

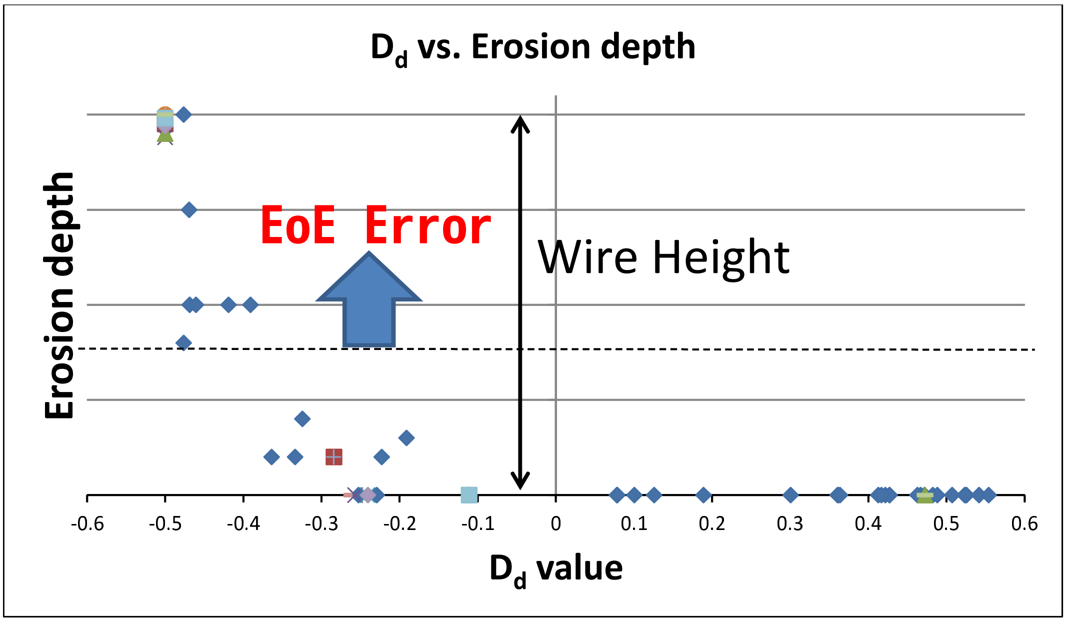


Fig. 4.8 Density deviation vs. EoE-error occurrence in a 65 nm process.

not negligible.

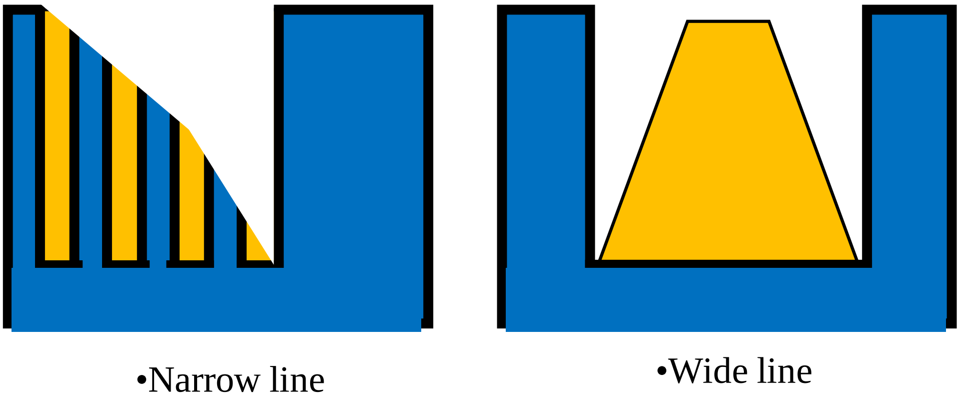


Fig. 4.9 Detailed shapes of EoE cross section.

Table 4.1 Confusion matrix.

		Predicted:	
		EoE-error	Non-EoE-error
Actual:	EoE-error	A	B
	Non-EoE-error	C	D

4.4 Model construction and prediction stage

In model construction stage, a prediction model is constructed that has the layout parameters selected in section 4.3 as variables with binary classification method using machine learning algorithms. In each mesh of the chip, a prediction model with layout parameters of each mesh mentioned in section 4.3 can predict whether EoE-error occurs or not.

Before explaining details of the prediction model construction, an accuracy metric of the prediction, which is considered in this chapter, is introduced. As mentioned before, EoE-error/non-EoE-error ratio of industrial chips is imbalanced. In imbalanced dataset, the model performance cannot be expressed in terms of the average accuracy. Table 4.1 shows the confusion matrix. Each column of the matrix represents the instances of prediction class, and each row represents the instances of an actual class. For example, when 1% samples are EoE-error and others are non-EoE-error, 99% accuracy is achieved by the model that all samples are judged as non-EoE-error ($\frac{A+D}{A+B+C+D}$). In this case, we cannot identify the samples that are likely cause EoE-error with such a model even while the accuracy is 99%. Considering this fact, geometric mean (g-mean) is used as a metric to evaluate the accuracy of the prediction model. G-mean g is defined as:

$$\begin{aligned} g &= \sqrt{P_{err} \times P_{ok}}, \\ P_{err} &= \frac{A}{A+B}, P_{ok} = \frac{D}{C+D}, \end{aligned} \tag{4.2}$$

where P_{err} is the rate of correctly predicted EoE-errors from all EoE-error samples, P_{ok} is that of non-EoE-error samples, A, B, C, and D is the number of instances in table 4.1. Because accuracy is calculated on the majority class and minority class separately, g-mean is suitable for evaluating the accuracy of imbalanced data classification problems [100]. In the previous case, g-mean value is 0 because P_{ok} value is 100% and P_{err} value is 0%.

4.4.1 Machine learning algorithms

This subsection briefly summarizes machine learning kernels employed in this work.

RPART (Recursive PARTitioning)

RPART [101] is a classification method using a 2-stage procedure, and provides resulting models represented by binary trees. This technique splits the samples using one input variable, i.e. a layout parameter in this chapter, with a threshold value which makes the gain of splitting index maximum. This routine is applied to each separated group recursively until the subset size reaches to the minimum threshold or until no improvement can be obtained. This work used Gini index as the splitting index. Gini index is given as follows.

$$I(g) = 1 - \sum_{i=1}^{2} p_i^2, \tag{4.3}$$

where p_i is the fraction of samples belonging to binary class i (error or not) at a given node. This index reaches 0 when all the samples belong to a single class. Larger Gini index improvement indicates better sample splitting.

RF (Random Forest)

RF method [102] is an ensemble learning method for classification aiming to improve prediction ability and stability of RPART. RF method consists of a number of decision trees and performs classification by majority vote of all the trees. This method is processed with the following steps.

- Step 1 N sets of bootstrapped samples are extracted from the original data.
- Step 2 For each set, a tree is built by RPART method with m variables randomly selected out of M variables, where the variables correspond to layout parameters in this chapter.
- Step 3 In prediction process, a new sample is classified by individual trees, and the majority result is selected as the classification result.

SVM (Support Vector Machine)

Suppose that each mesh m can be described as a vector of n layout parameters $x = (f_1, \cdots, f_n)$. SVM [103] constructs hyperplanes that optimally classify the data with these training vectors. Hyperplanes are set so as to attain the largest separation margin, where separation margin is the distance to the nearest training data. The vectors which form the boundary are called as support vectors.

On the other hand, there are a number of data sets which cannot be well separated linearly. For such data sets, kernel trick [104] provides improved separability. The kernel trick maps the original samples into a higher dimensional space, and it provides a method to nonlinearly separate the data set. Besides, there are several popular kernels, and this work used RBF (radial basis function) kernel. RBF kernel is defined as follows.

$$K(x, x_j) = \exp(-\sigma\|x - x_j\|^2), \tag{4.4}$$

where x and x_j are feature vectors, and σ is a free parameter.

Soft margin method [105] is also applied to our SVM prediction model. When error vectors are not separable due to EoE-error complexity and/or noise, slack variable ξ is introduced to allow mislabeled samples by paying violation penalty. The optimization problem is:

$$\begin{aligned} &\min_{a,b,\xi} \frac{1}{2}\|a\|^2 + C\sum_{i=1}^{m}\xi_i, \\ Subject\ to\ \ &\xi_i \geq 1 - y_i(ax_i + b), \\ &\xi_i \geq 0\ \ (i = 1, 2, \ldots, m), \end{aligned} \tag{4.5}$$

where a and b are parameters of hyperplane, y_i is a sign function of $(ax_i + b)$, and C is a parameter of soft margin to control the weight of penalty.

4.4.2 Multi-level machine learning algorithm

When pursuing accurate prediction of EoE-errors with the above algorithms, models tend to be more and more complex. In other word, the size of decision trees becomes large in RPART method and the number of support vectors increases in SVM method.

Figure 4.10 shows the complexity of SVM model in 2-dimensional graph. Figure 4.10(a) shows a simple model composed of two support vectors. All vectors above the dotted line are regarded as EoE-errors. A complex model is shown in Figure 4.10(b), where the number of support vectors is increased. The error region is smaller than that of Figure 4.10(a) and the number of mislabeled samples is decreased.

While a complex model improves the value of equation 4.2, an increase in model complexity may cause an overfitting problem. Overfitting degrades the generality of the model, which results in a bad performance in predicting new data in spite that the prediction for known data is accurate.

To achieve high accuracy without degrading generality, this work introduce a multi-level machine learning algorithm (MML). This method applies multiple trainings to the data in sequence. MML consists of screening and brushup steps. The aim of screening step is to reduce a number of non-EoE-error samples and outliers. This step is helpful for complexity reduction of the model which will be built at the next brushup step. In other words, this step reduces error classification patterns and outlier samples to be considered at brushup step to avoid overfitting problem. At brushup step, prediction model is constructed with samples labeled as an EoE-error in screening step. Details of each step will be explained in the following.

Screening step

At screening step, the first training and EoE-error prediction are applied. The samples labeled as an EoE-error at this step go to next step and the others are regarded as non-EoE-error samples. Because the purpose of this step is the screening of non-EoE-error samples, high P_{err} value in equation 4.2 is required in the model constructed at this step.

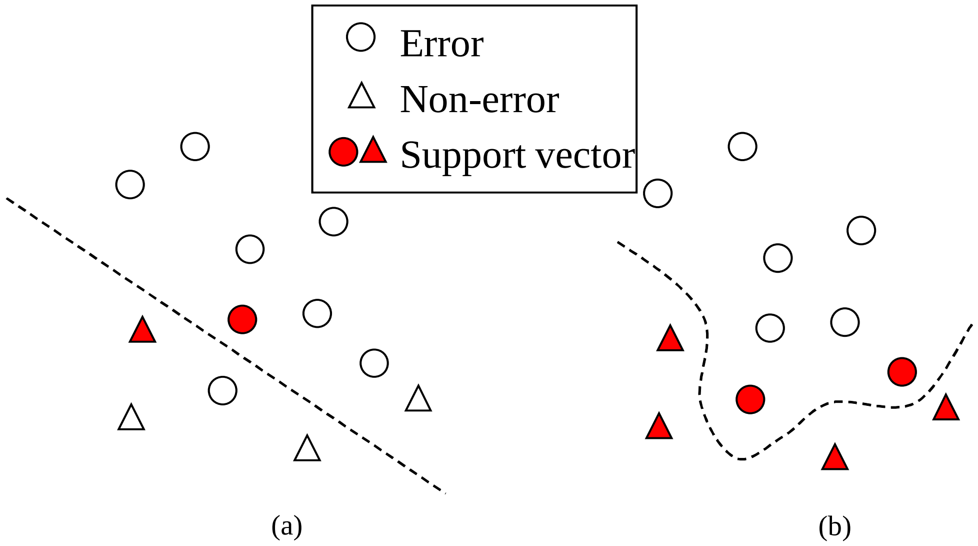


Fig. 4.10 Model complexity of SVM method.

Brushup step

The samples labeled as an EoE-error at screening step include many false errors, which is the non-EoE-error samples misjudged as EoE-error, since improving P_{ok} is scarcely considered at screening step. This brushup step aims to reduce false errors for attaining high g-mean value in equation 4.2. Besides, each learning method has individual features (ensemble/single classifier, linear/non-linear classification, for example), and samples which are poorly classified by one method may be accurately predicted by another method. This multi-step classification is thus expected to attain higher accuracy, since advantages of both methods can be exploited while concealing disadvantages.

Various combinations of learning methods and numbers of learning steps are attempted (strictly speaking various permutations since the order also affects the accuracy). Experimental setup was the same with that in section 4.5, and chip C1 data was used here. The detail will be explained later. This work first tested 2-level permutations that include RF, where RF attained the highest accuracy among single-level prediction methods explained in section 4.4.1, and found that those permutations degraded the accuracy compared to single-level RF. This work thus excluded the permutations that included RF. Then this work evaluated the combinations of RPART and SVM. Figure 4.11(a) shows the accuracy rate of equation 4.2, which denotes that the permutation of RPART as the first stage and SVM as the second stage improved the accuracy, where the accuracy rates of single-stage RPART and SVM were 90.5% and 92.2%. RPART+RPART and SVM+SVM patterns are also tested, but these could not improve the accuracy.

This result indicates that a better classification result can be expected when RPART method is applied to screening step and SVM method is applied to brushup step. There are two reasons for this result. 1) RPART is a simple method and this feature matches the aim of screening. 2) RPART is based on decision tree algorithm. SVM method may compensate weak points of this algorithm in EoE-error classification problem. Moreover, 2, 3, and 4-level

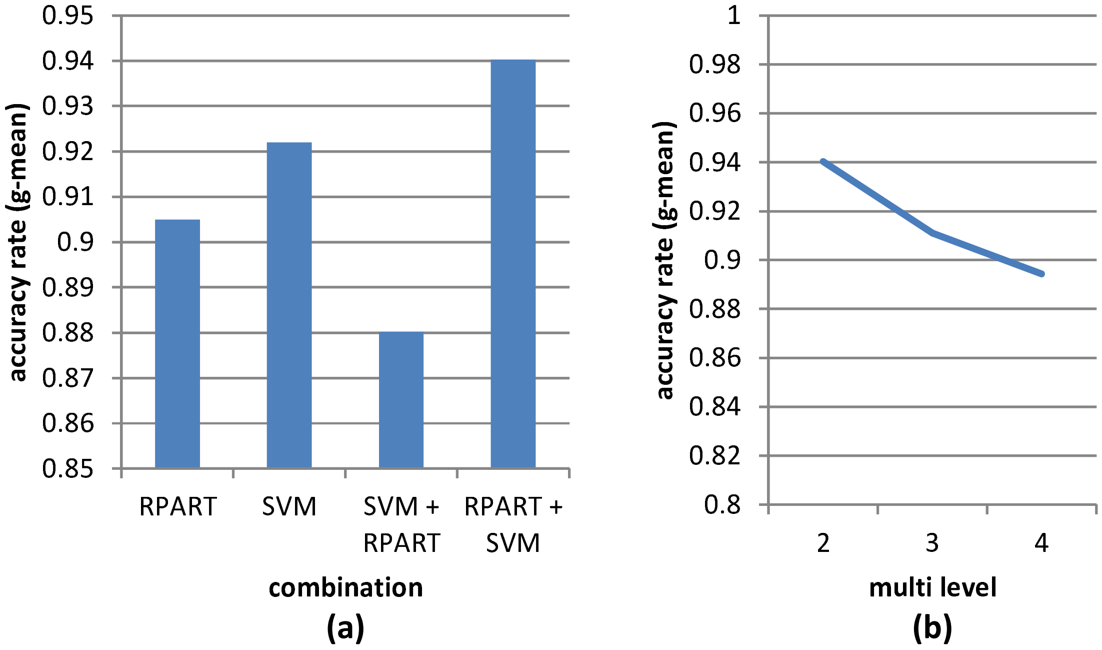


Fig. 4.11 Comparison of Accuracy rate of (a) combinations of learning method and (b) number of multi-level.

learning steps were attempted. RPART was applied to the 1st step and SVM was applied to the other steps. Figure 4.11(b) shows the result. This result shows that the accuracy metric of equation 4.2 starts to degrade when the number of learning steps is 3 and more. It was thus concluded that RPART and SVM methods should be used at screening and brushup steps respectively, and two-step classification with screening and brushup steps was reasonable.

4.4.3 Model construction and prediction flow

Figure 4.12 shows the detailed flow of model construction and prediction stages in figure 4.2. In model construction stage, two prediction models are built with an industrial chip (calib-chip). The overall EoE-error prediction model of MML algorithm consists of Models 1 and 2 constructed in screening stage and brushup stage, respectively.

First, input database that includes layout parameters and the EoE-error information for each discretized mesh is constructed.

Next, EoE-error and non-EoE-error meshes are sampled from the database as a subset1, which is used as the training dataset for Model 1 construction. As previously mentioned, EoE-error/non-EoE-error class distribution in the database is imbalanced. Sampling is a common practice to improve classifier performance and numerous methods are proposed [100, 106–109]. According to a comparison of various sampling methods [110], random under sampling (RUS) method is one of the best sampling techniques for the purpose of the learning from imbalanced data. In RUS method, samples of the majority class are randomly discarded and the training dataset becomes balanced. This work applies RUS method to non-EoE-error samples and make subset1 which includes all EoE-error samples and reduced non-EoE-error

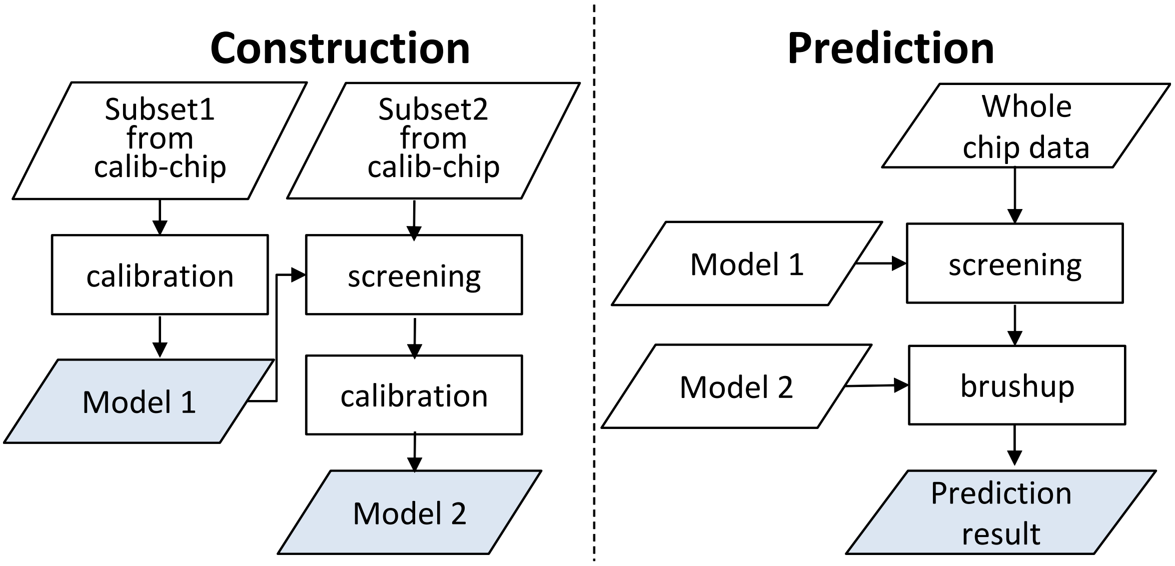


Fig. 4.12 Detailed flow of construction and prediction stages with multi-level machine learning method.

samples, and carries out construction of Model 1 with this training dataset.

In the proposed MML method, samples labeled as non-EoE-error at screening step with Model 1 are discarded before brushup step and EoE-error/non-EoE-error ratio changes. Thus, Model 2 construction is carried out with new training dataset subset2. This dataset is constructed from samples labeled as an EoE-error with Model 1. Because EoE-error/non-EoE-error distribution of the data passing through Model 1 is still imbalanced, RUS method is applied to non-EoE-error samples again to make subset2 which includes all EoE-error samples and reduced non-EoE-error samples. Then the prediction model of brushup step (Model 2) is constructed with subset2.

In prediction stage, EoE-errors of new chips are predicted with Model 1 and Model 2 in sequence.

4.5 Experimental results

This section presents experimental results to validate the proposed method. EoE-error data was obtained from three industrial chips. Note that the silicon measurement to identify EoE-error coordinates requires huge cost, which motivated us to develop EoE-error prediction model. This work used one chip to construct the prediction models and other two chips to validate the efficiency to unknown data.

Table 4.2 lists the details of calibration data (C1) and data for validation (V1, V2) with 65 nm technology node. The mesh size of each data was set to $10 \times 10\mu$m. The number of EoE-error meshes was measured from actual chips whose CMP process had been completed. Layout parameters explained in section 4.3 were extracted, and model parameters were obtained with industrial chip C1. Chip V1 and V2 cover wide ranges of the mesh-by-mesh layout parameter values and have different distribution shapes of the parameters.

This work implemented RPART, RF, SVM, and the proposed MML methods in R lan-

Table 4.2 Details of calibration / validation chips.

Chip Name	C1	V1	V2
Chip size (mm^2)	5.9×5.9	7.5×7.4	7.8×6.2
Average density(%)	34.5	30.2	30.8
# of EoE-error meshes	1045	2431	2604
# of non-EoE-error meshes	343K	544K	489K
EoE-error mesh ratio (%)	0.3	0.45	0.53

Table 4.3 Prediction performance comparison.

Chip		RPART	RF	SVM	MML	
					SC	SC+BU
C1	P_{err}	89.6%	100.0%	91.1%	97.6%	94.5%
	P_{ok}	91.4%	98.1%	93.2%	65.7%	93.5%
	g-mean	**90.5%**	**99.0%**	**92.2%**	**80.1%**	**94.0%**
	Ratio	0.5	4.0	1.0	0.2	0.9
V1	P_{err}	92.3%	82.2%	92.2%	97.2%	87.1%
	P_{ok}	85.2%	91.1%	81.8%	57.9%	92.1%
	g-mean	**88.7%**	**86.5%**	**86.8%**	**75.0%**	**89.6%**
V2	P_{err}	86.3%	74.3%	84.9%	97.8%	88.6%
	P_{ok}	82.5%	90.0%	82.4%	44.4%	90.7%
	g-mean	**84.4%**	**81.8%**	**83.7%**	**65.9%**	**89.7%**

guage [111]. In each method, training dataset consists of all EoE-error samples and proper amount of non-EoE-error samples selected with RUS method. In addition to model parameters, the balance of non-EoE-error/EoE-error class heavily affects prediction performance. Therefore this work calibrates model parameters and non-EoE-error / EoE-error sample ratio of the training dataset in each method. At construction step, this work uses default values of $N = 500, M = 6$, and $m = 2$ in RF method of R library [111]. C and σ in SVM method are set as calibration parameters.

Table 4.3 shows the performance of each method for calibration chip C1. SC and BU represent the screening and brushup steps, respectively. The meanings of P_{err}, P_{ok}, and g-mean are the same with equation 4.2. “Ratio” denotes the ratio of non-EoE-error samples to EoE-error samples in training dataset which achieved the best value of g-mean in C1. Sample ratio affects the relationship between EoE-error and non-EoE-error sample’s misclassification cost. Figure 4.13 shows the value of P_{err}, P_{ok}, and g-mean with various sampling ratio of SVM method ($C = 10$). When sample ratio value becomes large, the misclassification cost of EoE-error sample decreases and that of non-EoE-error sample increases, which results in decrease in P_{err} and increase in P_{ok}.

RF method shows good performance in the calibration chip. RF is the only method that did not miss the actual EoE-errors. MML method also attained high g-mean value. At screening step of MML, RPART method is applied and it uses smaller sample ratio (0.2) than that of single-level RPART method (0.5). In MML method, samples labeled as non-EoE-error at screening step are discarded before brushup step. High P_{err} and low P_{ok} value at screening

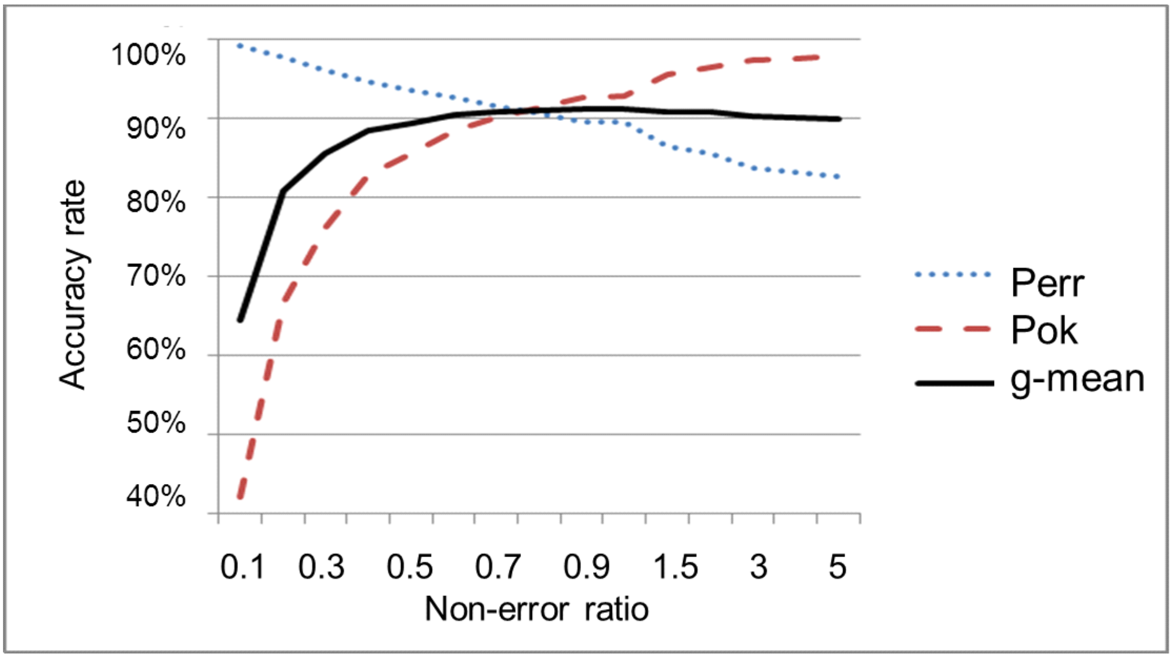


Fig. 4.13 P_{err}, P_{ok}, and g-mean with various sampling ratio in SVM.

step caused by lower sample ratio means that only outlier EoE-error samples and obvious non-EoE-error samples are removed from dataset. Detailed classification is processed in brushup step. According to this step, the complexity of classification is reduced and the g-mean value after brushup step with SVM method is higher than that of single-level RPART and SVM method. According to the result of calibration, density deviation D_d was the most influential parameter to EoE-errors in this 65 nm technology node.

Table 4.3 also shows the performance of each method for the validation chips. While it achieved the highest performance for calibration chip C1, RF method shows the worst performance in both V1 and V2. This is due to the lowest P_{ok} value even though P_{err} value is higher than other single-level methods. It is considered that overfitting problem occurs in RF method.

In chip V1, similar g-mean values are observed in all the methods. In contrast, compared to chip V1, the performance of single-level methods degraded in chip V2 although the proposed MML method kept up its accuracy. A possible reason why the performance in chip V1 was better than that in V2 is that chip V1 had some similarities with calibration chip C1, such as the average density. Compared with other methods, MML shows the best performance in both P_{err} and P_{ok}. MML improved P_{err} by 2.7–19.2% and P_{ok} by 0.8–10.1%. In MML method, multiple simple models are applied aiming to achieve high accuracy without sacrificing generality. This concept prevents overfitting problems in construction process and contributes to sustaining the classification performance to new chip data.

Even while P_{err} attained high percentages of 87.1% and 88.6% in chips V1 and V2, the number of non-EoE-error samples labeled as an EoE-error is more than ten times as large as the numbers of EoE-error samples labeled correctly, since the rate of EoE-error/non-EoE-error samples is imbalanced as listed in Table 4.2. However, the proposed method is still useful in design phase with the following three reasons.

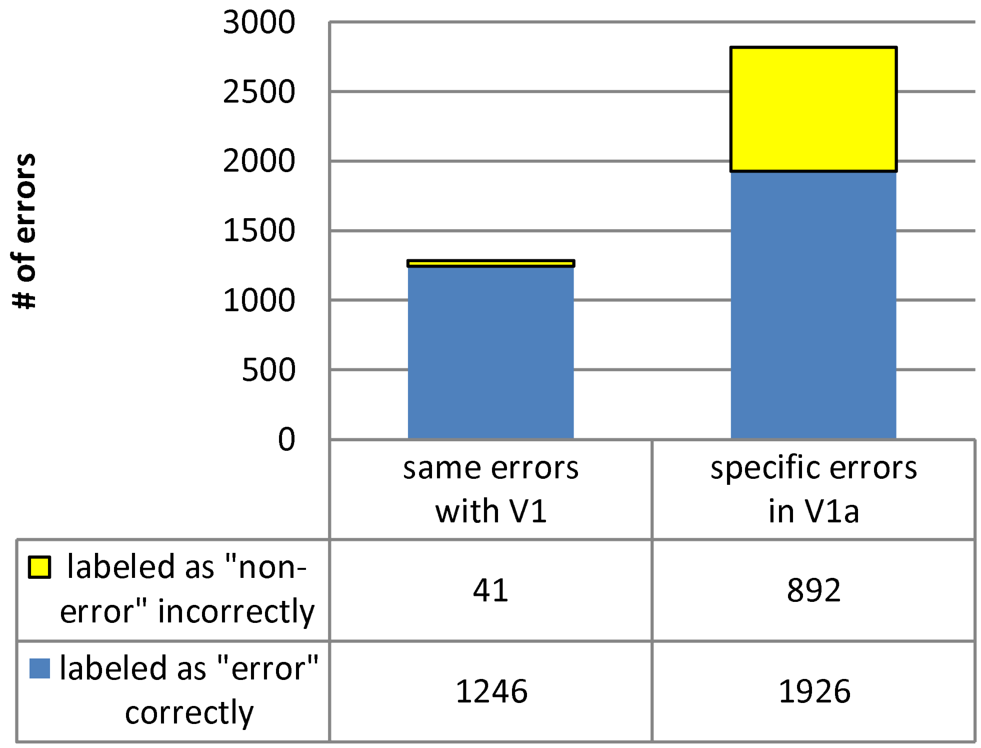


Fig. 4.14 Details of EoE-errors in chip V1a.

Firstly, it is too costly in both mask cost and time to modify layout after fabrication and measurement than to modify layout in pre-manufacturing phase. This proposed method is the first solution to predict EoE-errors before manufacturing.

Secondly, potential EoE-errors are likely to exist in mislabeled non-EoE-error samples. Here potential EoE-error is defined as a non-EoE-error sample which is EoE-error in other chip because of inter-chip variations. According to various process variations due to, for example, CMP, ECP and wafer location, EoE-error location and EoE-error numbers are different between chips. To clarify this, this work measured EoE-error of chip V1a, which was fabricated on the same wafer of chip V1 and has exactly the same layout with chip V1. Figure 4.14 shows the details of EoE-errors of chip V1a. The total EoE-error number is 4105 and the numbers of EoE-errors observed at the same locations with chip V1 is 1287. Other 2818 EoE-errors are potential EoE-errors of chip V1. They are treated as non-EoE-error samples in chip V1, but 1926 samples are labeled as EoE-error in prediction of chip V1. Further evaluation on potential EoE-errors in prediction model is a future work.

Finally, EoE-error reduction cost in design phase is not expensive. In general, dummy fill optimization technique is used to planarize wafer surface and several methods are proposed [50, 80, 94], where dummy fill modification does not affect the logic function of the circuit and wire topology. Guided by the proposed prediction model, dummy fill patterns can be modified so that meshes labeled EoE-error are altered to meshes labeled non-EoE-error.

4.6 Conclusion

This chapter proposed the first EoE-error prediction method with powerful learning algorithms. It consists of error analysis stage, layout parameter extraction stage, model construction stage and prediction stage. In error analysis and layout parameter extraction stages, this work define and extract layout parameters having an impact on EoE phenomenon with analysis of the test chip. In model construction and prediction stages, the proposed method uses multi-level machine learning method which can predict EoE-error locations accurately. This method makes it possible to prevent yield loss with recognizing EoE-error before manufacturing.

Chapter 5

Conclusion

Manufacturing layout patterns as desired is becoming a more and more challenging problem, and wire shape variation is a serious concern both for manufacturers and designers. Here, wire shape variation consists of wire height variation, wire width variation. In addition, irregular open / short error called Edge-over-Erosion error (EoE-error) is frequently observed in recent advanced technologies. Wire shape variation is usually encountered after manufacturing and testing a chip, and then it is mitigated with process or chip layout tuning. However, this operation needs considerably expensive cost, and it degrades the throughput. To improve yield and throughput, the mitigation of wire shape variation should be carried out before manufacturing. For enabling such variation mitigation, accurate prediction models that estimate the final shape of metal wire are required. This thesis focused on the modeling of wire shape variation with utilization of measurement data and various layout characteristics of chips.

Chapter 2 describes the prediction model of wire width variation induced from etching process. The measurement results show that wire width variation heavily depends on the chip layout even far from the wire width measurement point. Motivated by this observation, this chapter proposes a prediction model with gray-box modeling approach from physical properties and hypotheses of etching process with analysis of the measurement data and layout characteristics of many industrial chips. Then, this chapter presents a wire width adjustment method that tunes the etching process on the fly using the proposed prediction model. Experimental results show the accuracy of the prediction model with validation chip data as well as calibration chip data. Also, it is shown that the proposed wire width adjustment method can reduce the gap of wire width between target value and real shape value by 68.9% on an average.

Chapter 3 highlights the problems that arise in implementing a mitigation method of wire height variation and proposes solutions to these problems. Firstly, this chapter proposes a fast extraction method from GDSII data file and virtual dummy filling method. These methods enable us to significantly reduce processing cost of layout feature extraction and dummy fill modification. Secondly, a refined ECP prediction model is proposed. This model is constructed with gray-box modeling approach and it employs additional parameters which express the detailed ECP topography and reduces average errors in copper height by 68.2% and step height by 51.1%. Finally, an effective hot-spot detection method considering die-to-die variations is proposed. In actual operation, it is found that yield loss heavily depends on die-to-die variations, especially variations of initial copper topography after ECP process and over-polishing time after endpoint detection in CMP process. Exploiting this observation, the proposed method carries out the prediction under all corner conditions of ECP and CMP processes. This chapter shows a case study for hot-spot detection and dummy fill modification. The proposed model-based method for mitigating wire height variation reduced wire height variation of chip surface by 84.4% and avoided short errors before manufacturing.

Chapter 4 presents the first EoE-error prediction method with a novel multi-level machine learning technique. The mechanism of EoE is complicated and there are many uncertainties in physical characteristics. Therefore, this chapter develops a model that predicts EoE-error locations using machine learning algorithms instead of deriving a physical EoE model. This EoE-error prediction method consists of error analysis stage, layout parameter extraction stage, model construction stage, and prediction stage. In the first two stages, the relationship between EoE-error location and chip layout characteristics is analyzed with measurement data and layout information of real chips. In the latter two stages, the prediction model is built with black-box modeling approach and machine learning algorithms. This prediction model employs multi-level machine learning method to get rid of the influence of large amount of noise in the measurement data, and is proved to avoid overfitting problem and to have high accuracy from experimental results.

Wire shape variation is now one of the largest sources that degrade chip performance and yield loss. Wire shape variation can be mitigated by layout modification, but it is too costly to modify layout after fabrication and measurement in a repetitive manner. The proposed methods presented in this thesis virtualize the wire shape variation occurring in manufacturing process and enable us to predict wire shape variation in pre-manufacturing phase. Generally, layout modification cost in design phase is much smaller than that after fabrication, and the proposed methods contribute to cost reduction. Thus, the proposed method can mitigate the risk of chip performance and yield loss.

The future work is to integrate the proposed methods in this thesis into a single chip design flow and to develop an optimization method for minimizing the effect of wire shape variation on chip performance and yield. Several optimization methods were proposed [9,51,112–117], but they consider only a single variation problem. Integration of these methods is expected to be challenging because there is a correlation between the variations discussed in this thesis. Correlation aware modeling and optimization is the direction of our future research.

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