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Title	Study on Image Rejection of GNSS CMOS Receiver for Triple-band Signal
Author(s)	Jo, Ikkyun
Citation	大阪大学, 2015, 博士論文
Version Type	VoR
URL	https://doi.org/10.18910/53975
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Doctoral Dissertation

Study on Image Rejection of GNSS CMOS Receiver for Triple-band Signal

Ikkyun Jo

June 2015

Graduate School of Engineering,
Osaka University

Abstract

This thesis presents a receiver of the global navigation satellite system (GNSS) for triple-band signal, which the author studied at the Graduate School of Engineering, Osaka University.

Chapter 1

Chapter 1 introduces the study. It explains the basic GNSS concept, motivation and main goal of the study, and organization of the thesis.

Chapter 2

Chapter 2 describes a radio frequency (RF) characteristic of a metal-oxide semiconductor field-effect transistor (MOSFET) device. Before designing circuit blocks, the gate-region resistive features that affect input impedance are analyzed, and a high-accuracy gate-electrode resistance model is proposed. The gate-electrode resistance, including vertical resistive elements from the gate surface to the channel, is considered. By careful separation of this gate-electrode resistance and the non-quasi-static (NQS) effect, the small-signal gate/source admittance can be analyzed. The proposed model can effectively explain the small-signal gate/source resistance even for a small number of gate fingers.

Chapter 3

Chapter 3 explains the operation principle of the designed triple-band receiver system. It has only a RF path and separates each signal. Using fixed local oscillation (LO) signals, the triple-band signal can be simultaneously received. The signals mixed in the RF path are separated by an image rejection technique and independently obtained at each band port by the proposed receiver architecture. For

these operations, the conventional Weaver architecture is practically modified. For improvement of the image rejection ratio (IMRR), a digital compensation technique is also proposed. The behavior-level and circuit simulation results reveal the receiver system capability.

Chapter 4

Chapter 4 describes the circuit blocks that compose the receiver system. A low-noise amplifier (LNA), active and passive mixers, a poly-phase filter, and an IQ generator are described. These blocks were verified through a post-layout circuit simulation. The receiver system was designed in a 130-nm CMOS process with a 1.2-V power supply. The simulation results reveal the capability of the designed receiver circuits.

Chapter 5

Chapter 5 describes the measurement process and results. The measurements were obtained in three steps. Bare chips were firstly measured with a wafer probing system. A manual tuner was used to measure RF features in this step. From those results, the expected value of the external inductor for the input stage was calculated. With this value, the second process was performed. For the attachment of external components, bare chip were packaged in 24-pin QFN and a module board was designed. Using this module board, the analog features were measured and analyzed. Then, the demodulation output signals were measured with A/D converters (ADCs). In the final step, the improved IMRR of output signals was observed using a digital compensation method with ADCs output signals.

Chapter 6

Finally, Chapter 6 presents the conclusions of this study.

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Chapter 1

Introduction

This chapter explains the necessity of the system receiving global positioning system (GPS) triple-band signal. Firstly, the global navigation satellite system (GNSS) is explained. The calculation principle of local positioning information from the satellite signal is briefly mentioned and the types of GNSS are described. The reason why the GPS system is selected as the target is explained. Some GPS RF front-end integrated circuits have been designed with the CMOS process. In this chapter, the merits of the CMOS process and conventional receiver structure are also explained. Finally, the purpose of this study and structure of this thesis are mentioned.

1.1 Overview of GNSS

GNSS has been steadily gaining attention since its initial development. It is the general name of the system that calculates the target's position and time using satellite signals. In particular, it is a navigation system that is available anywhere on earth regardless of the time, place, and weather conditions. Owing to the affordability, availability, and improvement of position measurement capabilities, applications are increasingly being used for geodetics and surveying in scientific areas where high-accuracy positioning is required, such as in ocean remote sensing systems [1], mobile devices, and navigational vehicle systems.

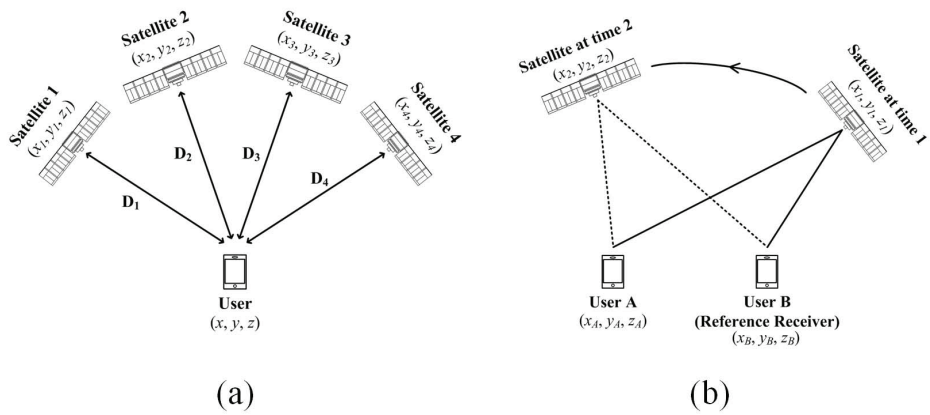

Figure 1.1: Method of (a) a point positioning and (b) relative positioning.

1.1.1 Calculation Principle of the Target's Location

There are generally three methods of calculating the target's location: point, relative, and differential positioning (DGPS in the GPS system) [2, 3].

A. Point Positioning Method

In the point positioning method, the calculation is performed by code tracking through binary pseudo-random number (PRN) codes. After comparing the synchronization of signals generated in the receiver and received from the satellite, the propagation time of the signal from the satellite is estimated. Because of analysis of signal synchronizations, a receiver requires the measurement results of a minimum of four satellites. In Fig. 1.1(a), the point positioning method is illustrated. The position coordinates of each satellite are expressed as (x_i, y_i, z_i) (i is 1 to 4 indicating each satellite). The user's coordinate is given by (x, y, z). Then, the distance from each satellite to the user can be calculated as

$$D_i = \sqrt{(x - x_i)^2 + (y - y_i)^2 + (z - z_i)^2} + c\Delta\delta. \tag{1.1}$$

From this equation, if the simultaneous positioning information of more than four satellites can be obtained, the user's local position can be calculated [4, 5]. Here, c is a light velocity in a vacuum condition. $\Delta\delta(= \delta_i - \delta)$ is the time error between the satellite and user. δ_i is the time variation of the satellite, and δ is the time variation of the user from the standard time.

B. Relative Positioning Method

In the case of relative positioning, the location is decided from the carrier phase tracking method. The phase difference between the received signal from the satellite and synchronization signal generated in the receiver is estimated. It is used to obtain the relative local position in the survey and supports more high-accuracy positioning information than a point positioning method. As illustrated in Fig. 1.1(b), after pre-installing receivers at known points or the target's location, the distance to the baseline is obtained through simultaneous measurements at a pre-installed point (User B in Fig. 1.1(b)) and the target's location (User A in the same figure). The relative positioning method uses the following Eq. (1.2) to calculate the phases of carrier (Φ_i, i is 1 to 2 indicating each satellite) [4, 5].

$$\Phi_i = f \cdot \delta_i + \frac{\rho_i}{\lambda} - f \cdot \delta + N_i, \tag{1.2}$$

where f, δ_i, δ, λ, ρ_i, and N_i denote the reference frequency of the satellite, time variation at satellites and receiver, wave length of the carrier signal, geometric distance between the satellite and receiver, and an unknown factor. Through repeated measurements, the moving position (User A in Fig. 1.1(b)) is estimated and the unknown factors are obtained. Observation equations about User A and User B in Fig. 1.1(b) can be obtained according to the satellite positions. Then, from this position information of User A and User B, the displacement amount can be calculated as in Eq. (1.3).

$$\begin{aligned} x_A &= x_B + \Delta x, \\ y_A &= y_B + \Delta y, \\ z_A &= z_B + \Delta z. \end{aligned} \tag{1.3}$$

This method can support high-accuracy positioning information. However, owing to the pre-installed reference place, it is difficult to employ this method in any location. It is time-intensive to calculate the reference place positioning information. It typically takes more than 1 hour [5]; therefore, this method is used for the observation of terrain, such as altitude.

Table 1.1: Comparison of survey methods using the DGPS.

	Target	Survey Time	Accuracy
Static	Survey of reference point	Very long (over 1 hour)	± 5 mm
Rapid Static	Draw of map	Long	± 10 mm
Kinematic	Survey of terrain and site work	Medium (Initial set-up time)	± 5 cm
Pseudo Kinematic	Draw of map	Short (Repeated Survey)	± 5 mm
Real Time Kinematic	Survey of terrain and site work	Real time	± 1 ~ 2 cm

C. Differential Positioning Method

A recent positioning information calculation, the differential positioning method, is achieved by combining the two methods mentioned above. In the GPS system, this method is called differential GPS (DGPS) [4, 5]. Through a pre-installed receiver, the signal compensation information is pre-calculated. Then, when the positioning information is calculated at any moving point, the compensation information is used to obtain high-accuracy positioning. Generally, a point positioning method is used for calculation of compensation information, and the relative positioning is used as a measurement method. At this time, according to the compensation time with the calibration data, the DGPS is used in real-time as a post-processing technique. In real survey cases using DGPS, the techniques for observing the scene using GNSS signals are classified into the five methods illustrated in Table 1.1.

1.1.2 GNSS Species

The first satellite launched above the Earth's orbit was Sputnik-1 of the Soviet Union in October 1957. In November of that year, after the success of the Sputnik-2 launch, the means for the space age had opened. However, these satellites were small and propagated only simple electric waves. Prompted by these events, the US began to build full-fledged satellite systems.

A. Global Positioning System (GPS) [6]

In the late 1950s and early 1960s, the US military began the construction of survey and navigation systems using satellites. From that point, the predecessor of the GPS system, Navistar GPS, was initiated from a multi-step project. At first, the position of an object was grasped by using aircraft instead of satellites. Then, the measurement of the time and position was introduced by observing the Doppler shift of signals transmitted from satellites, an approach that can calculate more accurate positioning information. The first satellite to operate the GNSS function, Block-I, was launched in February 1978. Until the end of the second step of this project, the nine additional Block-I satellites were launched. During these periods, the satellite system's total structure and verification were performed. By the end of 1985, the second generation satellite, Block-II, was developed. The initial satellites (Block-I) had not worked since 2003 on account of their life span. However, new satellites, such as Block-IIA and Block-IIR, were launched and operated. Today, for the GPS system, satellites operate a total of 28 and three signal bands have been used as L1, L2, and L5.

B. Global Navigation Satellite System (GLONASS) [7]

In the GPS system, the use of signals implies the possibility of restriction by the US, which can control the satellite positioning systems. To prevent this, some countries have been developing their own satellite positioning systems. Russia, for example, developed a satellite navigation system called Global Navigation Satellite System (GLONASS) in 1976. That country then launched satellites in 1982 and more actively developed them. In 1995, it constructed a satellite group for universal utilization. However, with the collapse of the Soviet Union and worsening of the financial situation there, the maintenance of the satellite was impossible. From the 2000s, the development of a satellite navigation systems with active involvement of the Russian government began anew, and a new version of the GLONASS-M satellite was launched in 2003. In 2008, 16 satellite groups for calculating global navigation on the whole earth was re-equipped. However, the cost of the GLONASS receiver based on frequency-division multiple-access (FDMA) was more expensive than that of the GPS receiver based on code-division multiple-access (CDMA). Unable to overcome this disadvantage, it did not succeed in the private market. Finally, a third generation satellite named GLONASS-K1 launched in 2011 began to transmit the L3OC signal based on CDMA. Russia currently intends to launch the

new satellite that can transmit L2 and L5 signals for a target GPS until 2020.

C. Galileo [8, 9]

Another system is Galileo of the EU and European Space Agency. Since 1999, a common team for developing the satellite navigation systems was composed in the EU. That team combined the projects of each country in Europe. Galileo was also initiated to prevent a monopoly by the US. In that project, GIOVE-A in 2005 and GIOVE-E in 2008 were launched. In terms of features, they are sub-projects of GNSS-1 and GNSS-2, respectively. GNSS-1 is intended to compensate the GPS and GLONASS. GNSS-2 is intended for an independent global satellite navigation system. However, owing to the worsening of the EU financial realm and rocket launcher problems, the system's composition and operation are not yet functional.

D. COMPASS [10]

In Asia, China and Japan have developed satellite navigation systems. In China, the COMPASS project was undertaken. It includes a plan to launch 5 geostationary satellites and more than 30 orbit satellites for pan-global communication until 2015. The local navigation system has been operating since 2001. However, it is difficult to know the exact structural requirements because only a partial configuration of the system and signal has been released.

E. Quazi-Zenith Satellite System (JRANS-QZSS) [11]

In Japan, the Japanese regional advanced navigation system - the Quasi-Zenith Satellite System (JRANS-QZSS) - provides high-accuracy positioning information by 100 % coverage of the full domestic area to reinforce the positioning information in combination with the improved GPS system. The MICHIBIKI satellite was launched in 2010. JRANS is composed of three orbit satellites (QZSS), three long elliptical orbit satellites (HEO), and one geostationary satellite. In particular, more effective visual information is provided by the QZSS satellite, which is equipped with time synchronization and remote maintenance functions.

F. Indian Regional Navigation Satellite System (IRNSS) [12]

Otherwise, there is the Indian Regional Navigation Satellite system (IRNSS), which is developed by the Indian Space Research Organization (ISRO). It is composed of three geostationary satellites and four orbit satellites to provide India with local information.

Table 1.2: Features of GPS, GLONASS, and Galileo systems.

	GPS	**GLONASS**	**Galileo**
First Launch (Operation)	Feb. 1978 (July 1995)	Oct.1982 (Jan. 1996)	Dec. 2005 (not yet)
Number of Satellites	24	24	27
Orbital Planes	6	3	3
Modulation Method	CDMA	FDMA	CDMA
Frequency (MHz)	1575.420 (L1) 1227.600 (L2) 1381.050 (L3) 1379.913 (L4) 1176.450 (L5)	1602.000 (G1) 1246.000 (G2) 1204.704 (G3)	1575.420 (E1) 1278.750 (E6) 1191.795 (E5)

A comparison of GPS, GLONASS, and Galileo is presented in Table 1.2 [3].

The GNSS frequency allocations used for global regions are illustrated in Fig. 1.2 [13]. Among these GNSS, the systems that are widely used and open the configuration and signal requirements to the public are GPS and GLONASS. However, recent studies of GLONASS are starting to compensate the GPS signals and improve the accuracy of the positioning information through the co-processing. In other words, the GPS system is still being used in the world and its application ability is seen as the most excellent. Furthermore, the US government is aware of competitors and suspended the selective availability (SA) to promote the GPS satellite navigation system with international standards. It allowed significant improvement of the performance of the GPS in May 2000. In addition, it expanded to the private sector the L5 band signal, which has been used for special purposes, such as civil aviation. It has taken great effort toward the modernization of GPS. For this reason, the GPS system is highlighted in this study.

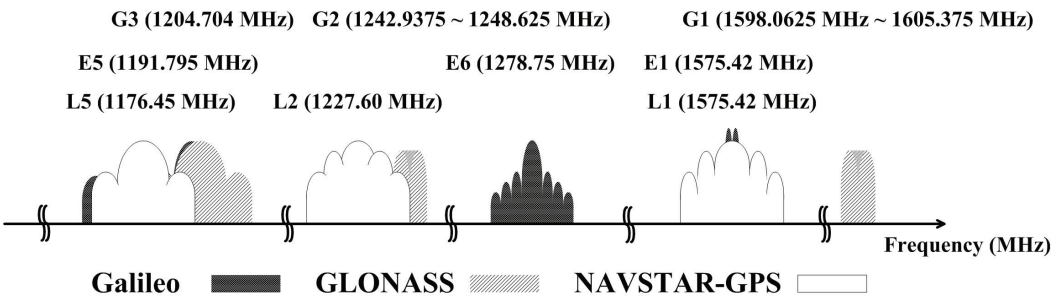

Figure 1.2: GNSS frequency allocations.

1.2 The GPS Receiver

1.2.1 CMOS Integration Circuit in the Receiver

In the receiver design, one of the recent issues is low power consumption [14]. To integrate multi-functions in one device as a smart phone, the effects of the battery on operation time are becoming important. In addition, the signal sensitivity by the system integration is required. A compound semiconductor or superconductor has been developed and studied to minimize noise effects generated from device physics [15]. In a compound semiconductor, it is hard to integrate into a single chip and operate in low power consumption. Thus, the device designed from the CMOS process is spotlighted because of its high integration rate, low power consumption, and low cost for fabrication. In the CMOS process, it is difficult to design the circuit for operating in a high frequency because of limitations of the low unity-current-gain cut-off frequency (f_t). To overcome these problems, some systems have been designed with a mixed process. For example, one system block diagram exists [16]. During the designing of the system, the digital stage, which has a slight noise effect, was designed in the CMOS process. The normal RF-stage was designed in SiGe BiCMOS. The power amplifier, which requires high-frequency large-output-swing operation, was designed in GaAs, as illustrated in Fig. 1.3. Recently, developing of a scaling process technique, f_t has advanced; therefore, the CMOS process has the benefit of integrating circuits for communication systems.

For development of the process, other parts can be designed with the CMOS process, as well as the digital part. Therefore, the fully integrated circuit has been widely studied to decrease loss of interconnection between the blocks. Because it still has a larger noise characteristic and long delay of

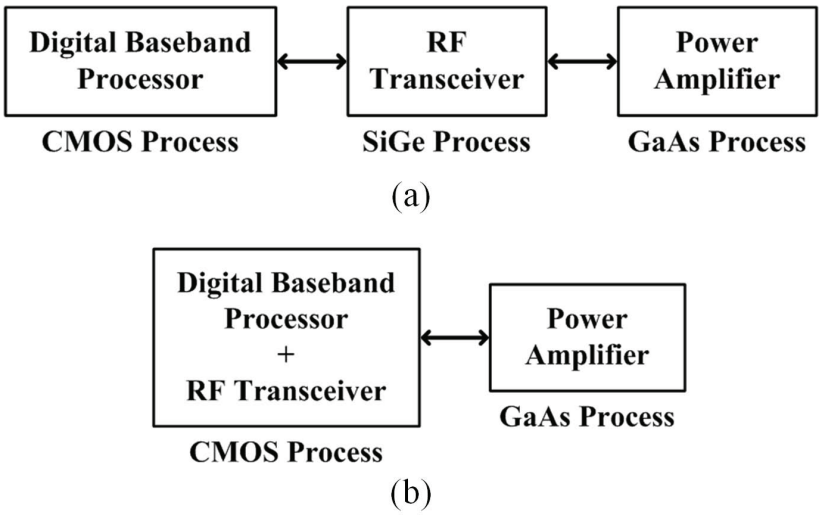

Figure 1.3: Process types for RF system.

the signal amplifier than the compound semiconductor, the integrated circuit with the CMOS process requires close attention. In particular, in the low operation voltage currently being studied, there are several physical problems, such as a high threshold voltage compared to the supply voltage. The characteristics of the process are summarized in Table 1.3.

Table 1.3: Advantages and disadvantages of various process.

Section	Process	Cost	Operation Frequency	Operation Frequency	Power Consumption
Digital Stage	CMOS	Low	Low	High	Low
RF Stage	SiGe BiCMOS	High	High	Low	High
Power Amplifier	GaAs	High	High	Low	High

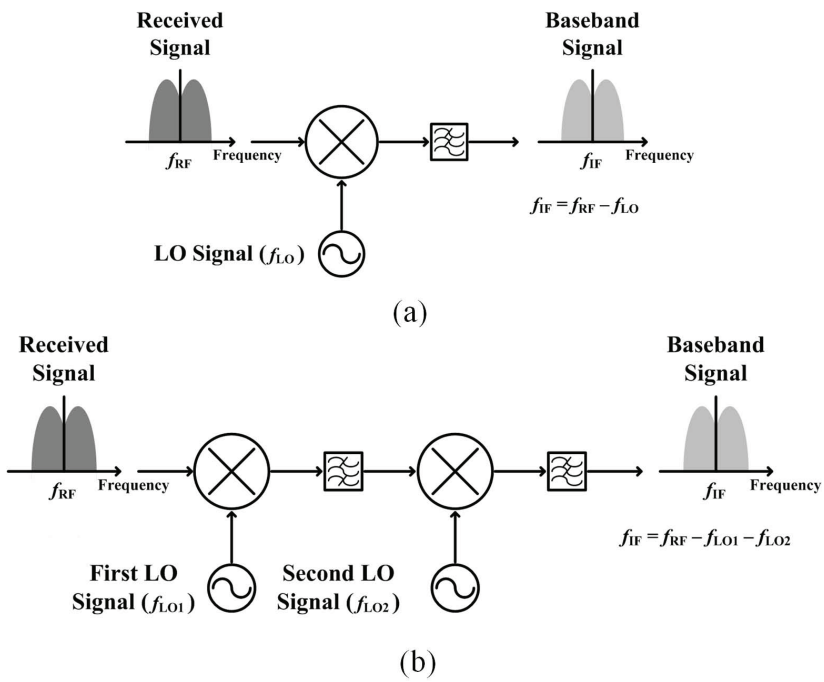

Figure 1.4: Structure of (a) direct-conversion receiver and (b) double-conversion receiver.

1.2.2 General Structure of the Receiver

In general, the receiver structures fall into two divisions as direct-conversion receiver and double-conversion receiver according to the stage of frequency transformation. In the case of the direct-conversion receiver, the frequency of the received signal is converted to the IF frequency through the single local oscillator (LO) signal, as illustrated in Fig. 1.4(a).

It has the advantages of a simple system structure and low power consumption. However, there are some critical problems due to its simple structure as a self-mixing leakage of RF and LO signals, as well as its feed through of RF signals and DC offset. Because of the interference signal generated on account of the poor reverse isolation of the low-noise amplifier (LNA) and the poor port-to-port isolation of the mixer, the DC offset is generated at the IF-stage [17]. To solve these problems, the high-cost filter is needed as a high-performance surface-acoustic-wave (SAW) filter located at the front of the LNA [17]. On the other hand, the double-conversion structure converts the frequency

of received signals to the IF frequency through multiple stages, which can transfer the frequency as illustrated in Fig. 1.4(b). Usually, the signal located among the stages of each frequency transformation can be filtered to match the desired condition. Here, Eq. (1.4) is used to obtain the factor Q, which represents signal selectivity.

$$Q = \frac{\omega_0}{BW}. \tag{1.4}$$

The higher the Q-factor, the more the signal loss is decreased [18]. Normally, the high Q-factor can be obtained at low-frequency; however, it is difficult to obtain a high Q-factor in a high frequency. To overcome this problem, some schemes adapt filters in several stages; however, this structure increases the size and cost.

1.2.3 GPS Receiver for Multi-band Signals

In the current GPS environment, there are three species of signal frequency bands that can be used in a custom field. However, in the GPS receiver, which has been used until now in custom fields, there are very few multi-band GPS systems [19–24]. Some reported receivers for multi-band signals are only composed with a simple single receiver in parallel [23, 25], as illustrated in Fig. 1.5. In this structure, the system size is large and requires high power consumption. These cannot support the simultaneous reception with the same RF signal delays, which is important for some scientific applications [1].

In recent studies, some researches have addressed a dual-band receiver that has good signal isolation [21]. However, these approaches are not fitting to the development of compact low-power and low-cost devices.

1.3 Research Purpose and Thesis Structure

1.3.1 Research Purpose

Use of multi-band signals has the advantage of fast detection in the DGPS, as mentioned above. It uses the real-time kinematic (RTK) for the survey method. To realize it with high-accuracy positioning, the operation of receiving multi-band signals should be simultaneous to reduce the time delay difference between the different band signals. For these goals, this research focuses on the

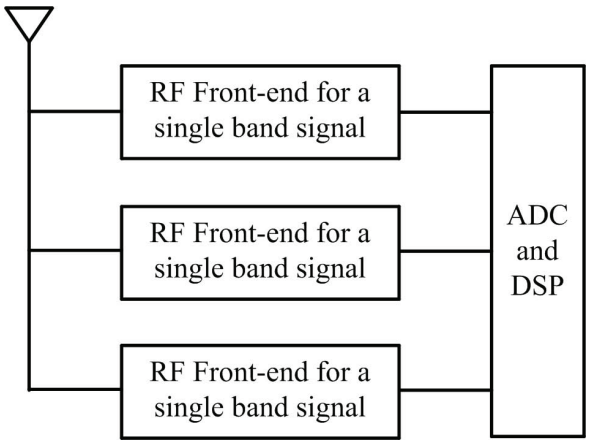

Figure 1.5: Conventional GPS structure for multi-band signals.

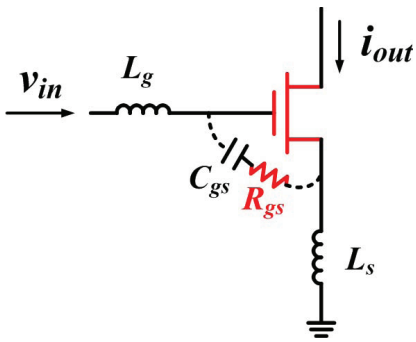

Figure 1.6: Inductive-source-degeneration stage of LNA with the gate-source admittance.

GPS receiver, which can receive the triple-band signal through a single receiver. The proposed architecture is not composed of three individual receivers, but only a single receiver requiring an antenna. Through the single receiver, each band signal can be individually received at separate ports. To avoid the RF signal delay difference, the fixed LO signal is considered through a proper frequency arrangement. This helps the simultaneous detection of each band signal. Through this GPS receiver, the high-accuracy positioning information (through using multi-band signals) and reduction of power consumption and cost (through reducing chip size) are expected. Through the whole integration of the RF front-end, the power loss between the composed blocks can be reduced.

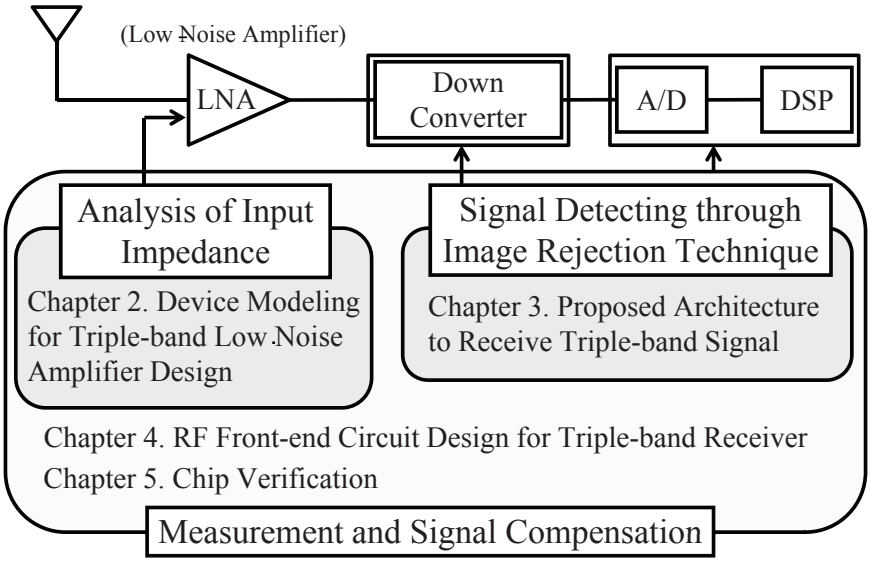

Figure 1.7: Constitution of thesis.

With these objectives, understanding device features is necessary. Input impedance matching can be realized by careful consideration of device's impedances. The designed receiver system includes a part of interconnecting chips and external components for the impedance matching. The separation of desired and undesired signals is an important factor that determines system capability because of the low power level of the GPS system's input signal. It is a main point of this work. Figure 1.6 shows the input impedance of the inductive-source-degeneration stage of the LNA. L_g and C_{gs} are considered in the conventional model. However, R_{gs} in the figure is more effective for input impedance as the device becomes smaller and the operation frequency increases. It is mainly handled to match the input impedance; therefore, the gate-resistance is important to the design of LNA for the triple-band signal.

1.3.2 Thesis Structure

The structure of this thesis is illustrated in Fig. 1.7.

Chapter 2 describes the structural characteristic of the MOSFET device and analyzes the high-accuracy gate-electrode resistance model. The signal detecting method with an image rejection technique is mentioned in Chapter 3. The theoretical background, which can make separate triple-band signal with a minimum RF path, is explained. In Chapter 4, the circuit level implementation of the receiver system is described including the device features explained in Chapter 2 and the system architecture mentioned in Chapter 3. For this work, element circuits, a proper signal line for signal balance, and layout features are considered. Experimental results of the designed chip are shown in Chapter 5. Finally, the conclusions are discussed in Chapter 6.

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Chapter 2

Modeling of Effective Gate Resistance

In this chapter, the gate-electrode resistance of MOSFET and effect of non-quasi-static (NQS) for RF operation are analyzed. The gate-electrode resistance is more precisely analyzed through consideration of the vertical current paths located between the silicide and poly-silicon layers. These elements located there are not effective at long-channel devices, however more significant in short-channel devices. So, in practical RF CMOS circuit design, it occupies the important part. This analysis is undergone by careful separation of the above gate-electrode resistance and NQS effect. To verify it, the extraction method for de-embedded MOS parameters from a 130-nm CMOS process is used. Through these values, the Elmore constant (κ) of NQS gate-source resistance is calculated and compared with semi-empirical model.

2.1 Introduction

CMOS technology realizing a low-power, large-scale integration, and low cost for manufacture are recently matching demands for miniaturization, low-power operation, and low cost in wireless communication system [1–4].

Scaling CMOS devices also are overwhelming the device performance, such as unity-current-gain-cut-off frequency f_t, against bipolar junction transistors and compound semiconductor devices, which were popular in RF circuits [5]. So, RF system on chip (SoC) integration from digital domain to RF analog domain can be realized. Although complexity of such a RF SoC increases, its short development time is always forced. In such a situation, precise simulations of analog/RF circuits are

important, and more accurate MOS device model and analysis of parasitic elements are needed for their implementations [6–8]. One of important issues in the MOSFET model in RF region is about the effective gate resistance. It influences the input impedance, maximum oscillation frequency f_{max}, and noise performance [9–11]. Especially, these features are affected in the design of multi-band and wide-band CMOS low-noise amplifiers (LNAs) [12–15]. The RF input resistance in common-source MOSFET has two factors [8, 16–18]. The first is related to the physical gate-electrode. The second originates from the channel itself in the intrinsic MOSFET region and its coupling with the gate-source capacitance C_{gs}, which causes a relaxation-time dependent phenomenon of channel charge response for a time-varying input signal, so called non-quasi-static (NQS) effect [19, 20]. As semi-empirical model, the NQS gate-source resistance R_{gsi} of the MOSFET operating in saturation region is approximately given by

$$R_{gsi} \approx \frac{1}{\kappa\, g_m}, \tag{2.1}$$

where g_m is the transconductance, and the Elmore constant κ is five for long-channel and is reported to be as small as one for short-channel devices [17]. Because the above two resistance factors have a different gate size dependence [18], their separate analysis is important in scalable MOSFET model and is also useful in RF circuit design [8]. Therefore, the accurate resistance model of extrinsic gate-electrode is required in advanced short-channel devices as well as the accurate prediction of κ. The accurate value of κ can be useful in some analytical design approaches of LNA [15, 21].

In this chapter, high-accuracy gate-electrode resistance model is mentioned. The model includes the vertical current paths between the silicide and poly-silicon layers in MOSFET. Through the separation between the gate-electrode resistance and NQS effect, the small-signal gate-source admittance is analyzed. Some parameters extracted in a 130-nm CMOS process such as κ are derived, verified and discussed.

2.2 Analysis of Gate-electrode Resistance

The gate of conventional MOSFET model is composed of gate insulator, poly-silicon, silicide and metal. Figure 2.1(a) illustrates top-view and cross section of n-channel MOSFET with a gate length L and gate width W in the silicided poly-silicon gate technology. When feeding the signal to gate, it propagates in horizontal direction of the silicide on the gate-electrode surface, and then in

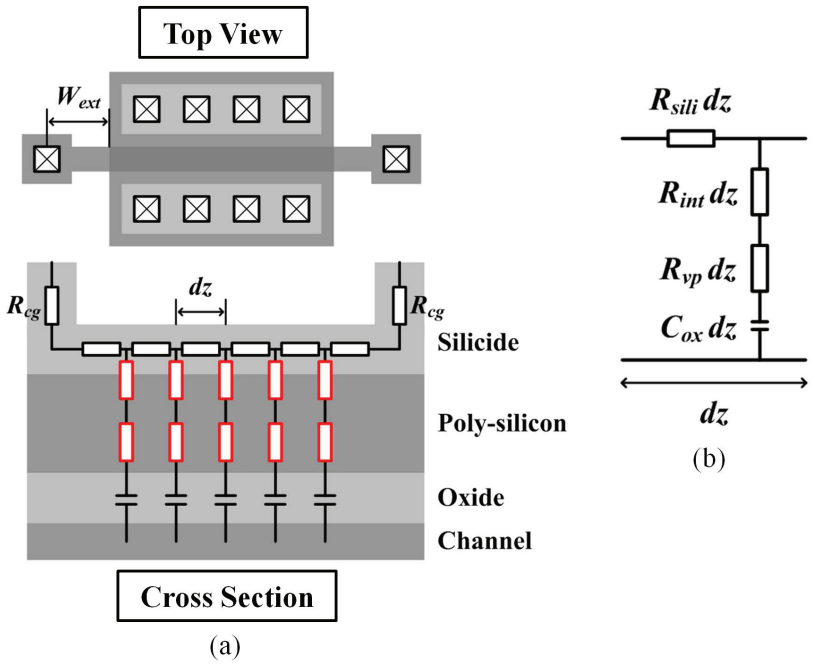

Figure 2.1: (a) Top-view and cross-section of MOSFET (both-side gate connection) and (b) equivalent circuit of gate unit element.

vertical direction of poly-silicon and gate insulator to effect channel. Gate resistance of MOSFET is composed with gate contact resistance between the metal and silicide, resistance of the silicide itself, the interface resistance between the silicide and poly-silicon, and the vertical resistance of the poly-silicon itself [22]. The interface resistance is important in the vertical signal propagation [11], and its typical values are about 25 $\Omega\mu m^2$ ($TiSi_2$) [11] and about 2$\sim$3 $\Omega\mu m^2$ (NiSi) [23]. In long channel MOSFET, vertical elements of the gate-electrode are less effective than gate contact and silicide resistance. However, as gate length decreases, the influence of vertical elements is becoming more important. As gate width decreases, the horizontal resistance decreases, while the vertical resistance increases inversely proportional to the gate width.

Each part of gate-electrode resistance can be expressed with lumped elements for the signal path length in a horizontal gate width direction dz using a transmission line model as illustrated in Fig. 2.1(b), which is similar to that in silicided diffusion region [24]. Here, R_{cg} is unit gate con-

tact resistance between the silicide and poly-silicon, ρ_{sili} is the sheet resistivity of the silicide, ρ_{int} is an interface resistivity between the silicide and poly-silicon, ρ_{vp} is the vertical resistivity of poly-silicon layer per unit dimension. C_{ox} is unit capacitance of the gate insulator. For simplification in mathematical expression, let $R_{sili} = \rho_{sili}/L$, $R_{int} = \rho_{int}/L$, $R_{vp} = \rho_{vp}/L$. When C_{gc} is defined as the capacitance between the gate and channel, it can be considered as $C_{gc}/W \propto C_{ox}L$.

Considering the steady state at the angular frequency ω in Fig. 2.1(b), the total admittance of vertical current path elements for unit signal propagation length on the gate-electrode surface, Y_{vp}, is given by

$$Y_{vp} = \frac{j\omega C_{gc}/W}{1 + j\omega C_{gc}\big(R_{int} + R_{vp}\big)/W}. \tag{2.2}$$

From the manipulation described in Appendix A, the gate-electrode resistance seen from the gate contact position for unit gate finger with length W_f is expressed as

$$R_{g,ele} = \frac{k}{3}\rho_{sili}\frac{W_f}{L} + \frac{\rho_{int} + \rho_{vp}}{LW_f}, \tag{2.3}$$

where k is 1 and $1/4$ for a single-side and a both-side gate connections, respectively.

Additionally, considering the gate contact between the silicide and metal as well as the gate extension to the channel area in a similar way based on the previous work [7], the gate-electrode resistance for the number of gate finger N_f is expressed as

$$R_{ge} = \frac{k}{3}\rho_{sili}\frac{W_f + W_{ext}/\sqrt{k}}{LN_f} + \frac{\rho_{int} + \rho_{vp}}{LN_fW_f} + \frac{R_{cg}}{N_{cg}N_f}, \tag{2.4}$$

where W_{ext} is the distance between the channel area edge and gate contact, and N_{cg} is the number of gate contacts per finger [7]. Capacitive coupling of the gate extension to the substrate is also considered in the above equation by using a factor $1/3$. Compared to the previous works [7, 8], Eq. (2.4) has the second term inversely proportional to the channel area LN_fW_f, which originates from the vertical resistance elements. As the channel area decreases, this influence increases.

2.3 Parameter Extraction for NQS Resistances

In low-frequency operation, carriers in the channel can respond immediately to the applied terminal voltages, which corresponds to charging and discharging of the gate-source capacitance C_{gs}.

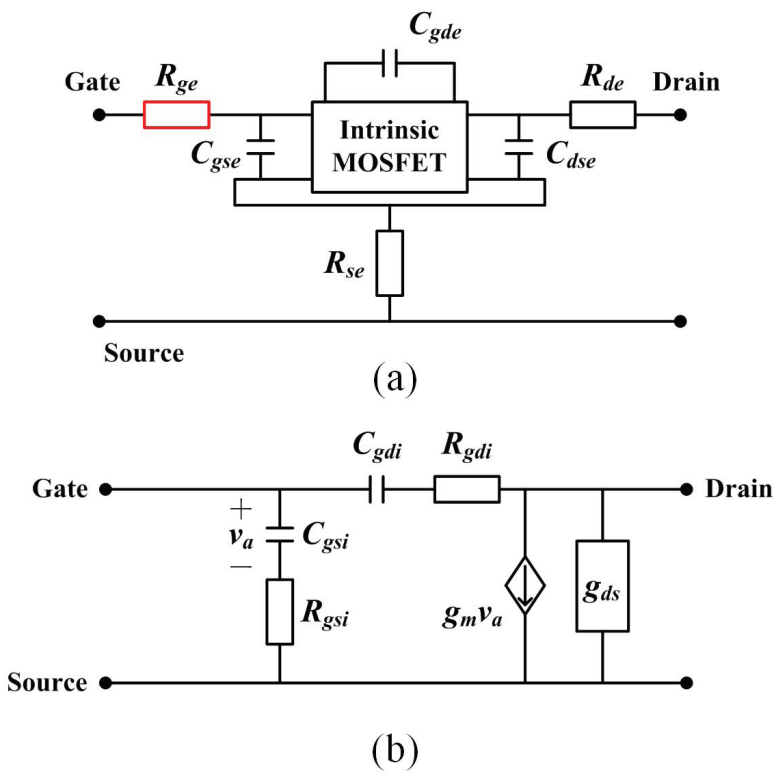

Figure 2.2: (a) Small-signal equivalent circuit including external parasitic elements and (b) its intrinsic part.

This is considered as quasi-static operation. On the other hand, as the operation frequency gets much higher, the channel resistance influences response time of the carriers, which is NQS operation. Although the transconductance, drain conductance and large-signal operation are influenced by the NQS effect, the influence of the small-signal gate-source admittance y_{gs} is crucial in the multi-band and wide-band LNA designs. This work focuses on the small-signal gate-source admittance.

To estimate the NQS effect, the careful parameter extraction for MOSFET model is required. Figure 2.2(a) shows the small-signal equivalent circuit which includes external parasitic elements. In this work, the body is connected to the source, resulting in no body effect. R_{gsi} and R_{gdi} in Fig. 2.2(b) give NQS effect. R_{ge} is a gate-electrode resistance, R_{de} and R_{se} are series resistances of drain and

source, and C_{gse} and C_{gde} are overlap capacitances between the gate and source/drain. C_{dse} is the external capacitance between the drain and source (body in this case). Extraction method separates extrinsic and intrinsic parameters from two-port parameters of the MOSFET. In the first step, the external resistances (R_{ge}, R_{de}, and R_{se}) and the external capacitances (C_{gde}, C_{gse}, and C_{dse}) are de-embedded from the two-port parameters of the MOSFET, using the de-embedding technique [8]. The estimation techniques of the external resistances and capacitances are described later. In the second step, the equivalent circuit including only intrinsic parameters can be obtained.

To estimate the external parameters, the cold biasing (V_{GS} = V_{DS} = 0 V) is utilized. It is assumed that the intrinsic parameters except for drain-source conductance g_{ds} are not presented in cold bias. External parameters are nearly independent of V_{GS}. Thus the Z-parameters of the MOSFET in the cold biasing can be obtained as follows:

$$Z_{11} = R_{ge} + R_{se} - \frac{g_{ds}C_{gde}^2}{A(\omega)} - j \cdot \frac{g_{ds}^2\big(C_{gse} + C_{gde}\big)/\omega + \omega B\big(C_{gde} + C_{dse}\big)}{A(\omega)}, \quad (2.5)$$

$$Z_{12} = Z_{21} = R_{se} + \frac{g_{ds}\big(C_{gse} + C_{gde}\big)C_{gde}}{A(\omega)} - j \cdot \frac{\omega B C_{gde}}{A(\omega)}, \quad (2.6)$$

$$Z_{22} = R_{de} + R_{se} + \frac{g_{ds}\big(C_{gse} + C_{gde}\big)^2}{A(\omega)} - j \cdot \frac{\omega B\big(C_{gde} + C_{gse}\big)}{A(\omega)}, \quad (2.7)$$

$$A(\omega) = \omega^2\big(C_{gde}C_{dse} + C_{gse}C_{gde} + C_{gse}C_{dse}\big)^2 + g_{ds}^2\big(C_{gse} + C_{gde}\big)^2,$$

$$B = C_{gde}C_{dse} + C_{gse}C_{gde} + C_{gse}C_{dse}.$$

In the cold bias condition, g_{ds} is negligibly small. Assuming it, real parts of the Z-parameters in high frequency can be approximated as

$$\Re[Z_{11}] = R_{ge} + R_{se}, \quad (2.8)$$

$$\Re[Z_{12}] = \Re[Z_{21}] = R_{se}, \quad (2.9)$$

$$\Re[Z_{22}] = R_{de} + R_{se}. \quad (2.10)$$

From these equations, R_{ge}, R_{de}, and R_{se} can be estimated. In addition, Using Eqs. (2.5)-(2.10) with

the same assumption of small g_{ds}, imaginary parts of the Z-parameters can be approximated as.

$$\Im[Z_{11}] = -\frac{C_{gde}+C_{dse}}{\omega B}, \tag{2.11}$$

$$\Im[Z_{12}] = \Im[Z_{21}] = -\frac{C_{gde}}{\omega B}, \tag{2.12}$$

$$\Im[Z_{22}] = -\frac{C_{gde}+C_{gse}}{\omega B}. \tag{2.13}$$

From these equations, C_{gse}, C_{gde}, and C_{dse} can be estimated.

The intrinsic Y-parameter matrix $[Y_{int}]$ can be obtained from the embedded Z-parameter $[Z_{em}]$ matrix of the MOSFET model shown in Fig. 2.2 by using the following equations.

$$[Z_{ext}] = \begin{bmatrix} R_{ge}+R_{se} & R_{se} \\ R_{se} & R_{de}+R_{se} \end{bmatrix}, \tag{2.14}$$

$$[Y_{ext}] = j\omega \begin{bmatrix} C_{gse}+C_{gde} & -C_{gde} \\ -C_{gde} & C_{gde}+C_{dse} \end{bmatrix}, \tag{2.15}$$

$$[Y_{int}] = \big[Z_{em} - Z_{ext}\big]^{-1} - \big[Y_{ext}\big]. \tag{2.16}$$

Based on the equivalent circuit shown in Fig. 2.2(b), the parameters of MOSFET's intrinsic parts can be calculated from relations of real and imaginary parts of Eq. (2.16) as following equations.

$$C_{gsi} = \frac{\Im[Y_{11,int}] + \Im[Y_{12,int}]}{\omega}, \tag{2.17}$$

$$C_{gdi} = -\frac{\Im[Y_{12,int}]}{\omega}, \tag{2.18}$$

$$R_{gsi} = \Re\Big[\frac{1}{Y_{11,int}+Y_{12,int}}\Big], \tag{2.19}$$

$$R_{gdi} = -\Re\Big[\frac{1}{Y_{12,int}}\Big], \tag{2.20}$$

$$g_m = \Re\Big[Y_{21,int}\Big]_{\omega=0}, \tag{2.21}$$

$$g_{ds} = \Re\Big[Y_{22,int}\Big]_{\omega=0}. \tag{2.22}$$

2.4 Verification of Gate-electrode Model and NQS Effect

In this work, instead of on-chip high-frequency S-parameter measurement, simulated small-signal S-parameters are used with a RF MOSFET model (BSIM4 with GATEMOD=3 [25]), which can

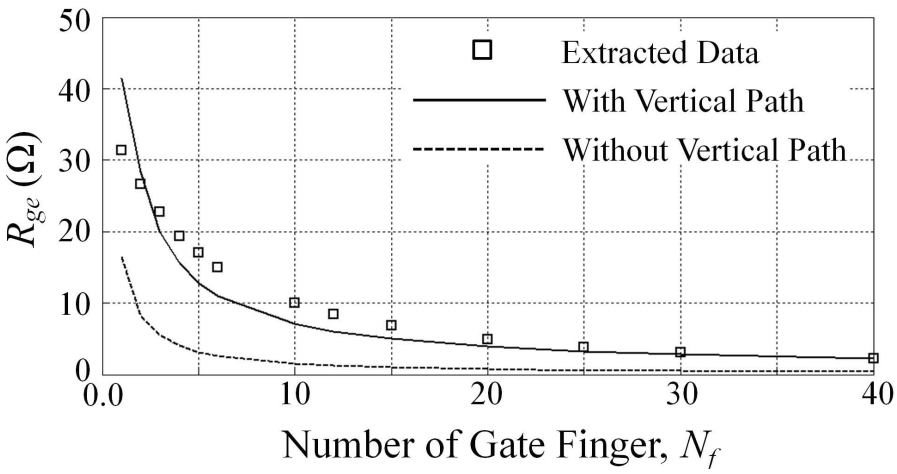

Figure 2.3: Extracted and calculated values of gate-electrode resistance R_{ge} versus the number of gate figners N_f ($L = 140$ nm, $W_f = 3$ μm, both-side gate connection).

reproduce RF and DC characteristics well with many parameters for a commercial 130-nm CMOS process. This can realize cost-effective verification of device models. As narrow gate width under 3 μm has an effect of the interface resistance on the gate resistance, NMOS devices with single finger width of 3 μm and both-side gate connection are used in this work. The embedded Z-parameter $[Z_{em}]$ matrix can be obtained from the simulated S-parameters of the device for the maximum frequency of 50 GHz.

The external gate-electrode resistance R_{ge} is extracted by using Eqs. (2.5)−(2.10), and is compared with calculated ones by using Eq. (2.4). The results are illustrated in Fig. 2.3. The second term of Eq. (2.4) originates from the vertical current paths. To confirm the influence of the vertical current path in Fig. 2.1, R_{ge} with and without the second term (solid and dotted lines in Fig. 2.3, respectively) was calculated. The value of $R_{int} + R_{vpoly}$ is determined by curve fitting as 12.5 Ωμm^2 which is reasonable value considering the reported typical values [11, 23]. From this figure, consideration of the vertical current path becomes significant for small gate finger numbers. It is more effective for short-channel devices.

Based on the extracted external parameters, NQS gate-source resistance R_{gsi} and transconductance g_m are extracted by using Eqs. (2.19) and (2.21). In this parameter extraction, to neglect

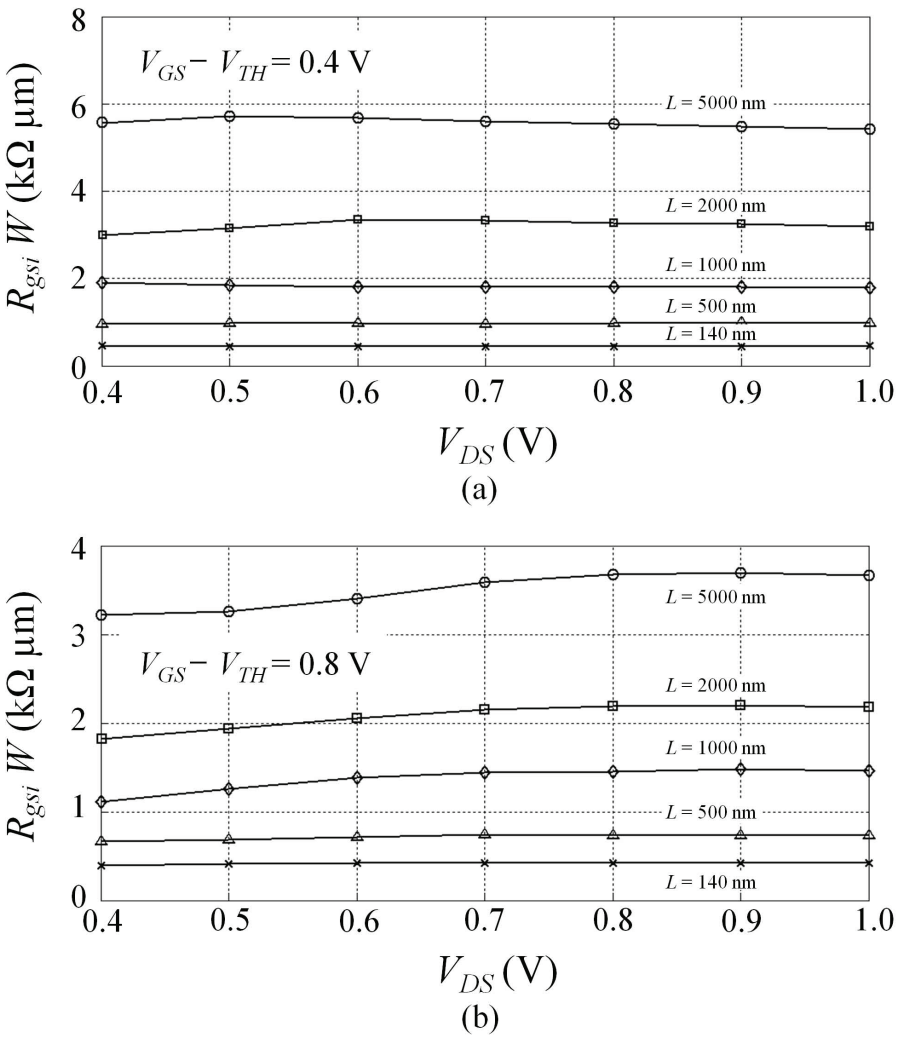

Figure 2.4: Extracted values of NQS gate-source resistance R_{gsi} of NMOS devices with gate length $L = 140, 500, 1000, 2000$ and 5000 nm at gate-source overdrive voltages (a) $V_{GS} - V_{TH} = 0.4$ V and (b) $V_{GS} - V_{TH} = 0.8$ V (gate width is 120 μm (3 μm $\times$ 40 fingers), both-side gate connection).

high-order NQS effect [26] and delays in transconductance and drain conductance [8], the maximum frequency is set to 6.5 GHz. Figure 2.4 shows the dependence of R_{gsi} on drain-source voltage V_{DS} at the gate-source overdrive voltages $V_{GS} - V_{TH} = 0.4$ V and 0.8 V for various gate lengths. In

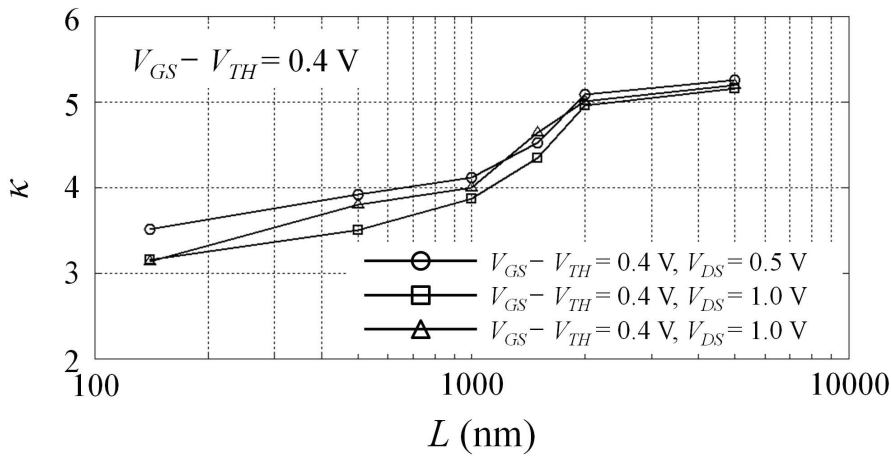

Figure 2.5: Gate length dependence of extracted elmore constants κ.

saturation region ($V_{DS} > V_{GS} - V_{TH}$), R_{gsi} has little V_{DS} dependence.

Figure 2.5 shows Elmore constant κ obtained from extracted R_{gsi} and g_m with Eq. (2.1) as a function of gate length. As mentioned above, κ is around 5 for $L > 1$ μm. For $L < 1$ μm, it decreases to about 3, which may originate from velocity saturation [27]. The small-signal local channel conductance in the velocity saturation region is smaller than that in the non-velocity-saturation source-side region. However, the value of κ around one, as reported in previous works [8, 17], could not be confirmed even for minimum gate length ($L = 140$ nm) in this work. The κ for short-channel devices may have a dependence on channel-length modulation, drain-induced barrier lowering, and so on, which show significant and complicated dependence on device structure.

2.5 Conclusion

In this chapter, the gate-electrode resistance of MOSFET and NQS effect are analyzed using a 130-nm CMOS process. The vertical current paths between the silicide and poly-silicon are considered in MOSFET. The vertical current paths are not effective in the devices with large channel area, but become more significant as the channel area decreases. The gate-electrode resistance including vertical current paths can reproduce well the practical RF characteristics. With the scaling of CMOS

technology, this effect is not considered till now in RF CMOS circuit designs, however it has significant effect in the design of multi-band and wide-band CMOS LNAs. By careful separation of the above gate-electrode resistance and the NQS effect, the intrinsic small-signal parameters were extracted. The high-accuracy analysis considering physical characteristic with the vertical elements is verified. Elmore constant of the NQS gate-source resistance (κ) about five was confirmed for the long-channel devices, while it decreases down to about three for the short-channel devices. The value of κ around one, reported in previous works, could not be confirmed even for minimum gate length in this work. The NQS effect in short-channel devices may have significant and complicated dependence on device structure. For further studies, the analyses on various processes with various device structures are more required for RF CMOS circuit designs.

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Chapter 3

Triple-band Signal Receiver Architecture

In this chapter, the theory of signal separation on a path at the same time is mentioned. Based on the theory, new architecture which can receive simultaneously multi-band signals with a RF path is explained. The image rejection technique for it is explained. Parameter mismatch deteriorate the performance of the receiver. Compensation technique which can overcome this deterioration is described.

3.1 Introduction

Recently, the global positioning system (GPS), which was originally developed for military purposes, has been widely used to obtain the location information in applications such as a car navigation system. The widespread use of civilian GPS signals in consumer applications has been promoted by a single GPS receiver chip fabricated on a CMOS process due to its significantly reduced size, cost, and power consumption [1]. It is also becoming attractive to scientific applications, such as ocean remote sensing [2], which higher positioning accuracy is required. One way of achieving this is to use multiple civilian GPS signals at different frequencies, and such an approach can also offer advantages for robust GPS services such as those used in aviation. GPS with multi-band signals has come closer to reality with the launch of a satellite transmitting in the L5 band, to compliment the L1 and L2 civilian bands that are already in use [3]. Thus, the GPS receivers that can detect all signals of three bands simultaneously are now in demand.

One of key issues in designing a triple-band GPS receiver is how to implement a highly integrated

RF front-end that can operate at low power consumption. To date, few multi-band receivers have been reported [4–10]. Although dual-band receivers with good signal isolation have been developed that use a band-selection architecture [6] or a simple parallel arrangement of several receivers [9], these approaches cannot realize miniaturized low-power and low-cost devices. Simultaneous reception with the same RF signal delay, which is important for some scientific applications, is also not possible [2]. To realize compact low-power triple-band GPS receiver with simultaneous reception, signal separation for the triple-band signal on the single RF signal path is a key technique.

In this chapter, the image rejection technique as the principle of removing unwanted band signal and image rejection ratio (IMRR) for estimation of proposed architecture's capability are explained. The proposed method of independently and simultaneously detecting each band signal by using that technique, and verification through behavior-level and circuit simulations are shown. Finally, the theory of digital compensation technique is mentioned to improve IMRR.

3.2 Image Rejection Technique

In RF receiver, frequency translation is a base of signal receiving. Generally, received signals are demodulated through A/D converter (ADC) after frequency translation to base-band. This process is operated through RF mixer. The operation is carried out through the multiplication of RF and LO signals. During this operation, the image part of RF signal at opposite side against LO signal degrades receiving capability. The simple method to reject image signal is a use of external band-pass filter like the SAW filter. In integrated circuit, high-Q-values of filter, supporting enough selectable capability, is hard to be used.

There is another method to reject image signal. By using symmetric structures, the effect of image signals can be rejected. In this study, phase-converting method to apply the image reject technique has been used for signal selecting. So the general image reject technique through phase-converting method is explained, and how to adapt this method for signal selecting is described.

3.2.1 Conventional Architecture of Image Rejection Technique

Image rejection method is one of methods rejecting unwanted image signal through phase converting as much as 90°. In typical, the image rejection method is realized by using system structure as

Hartley and Weaver architectures. For analysis of image rejection method by equations, description about 90° phase shifter of signal is needed [11].

Illustrated in Fig. 3.1(a), the phase shifter of 90° has a role converting $\sin(\omega t)$ to $-\cos(\omega t)$ and $\cos(\omega t)$ to $\sin(\omega t)$. This figure shows the signal in time domain. The 90° phase shifter means time delay in time domain as a quarter of signal period. This operation in frequency domain can be expressed in Fig. 3.1(b). The function which is multiplied by $\sin(\omega t)$ signal is presented as $H(\omega) = -j\ \mathrm{sgn}(\omega)$, where $\mathrm{sgn}(\omega)$ is sign function. 90° phase shifter can be realized by several methods like a RC-CR network [11]. In this study, poly phase filter is used.

The conventional Hartley and Weaver structures are shown in Fig. 3.2. In Hartley structure, the single-stage mixer is used to translate phases. Then, phase of one of these signals is converted by 90° phase shifter. Then, the signals from both signal paths are added together for rejection of unwanted image signal. In Weaver structure, the two-stage mixers are used to translate phases. In both of cases,

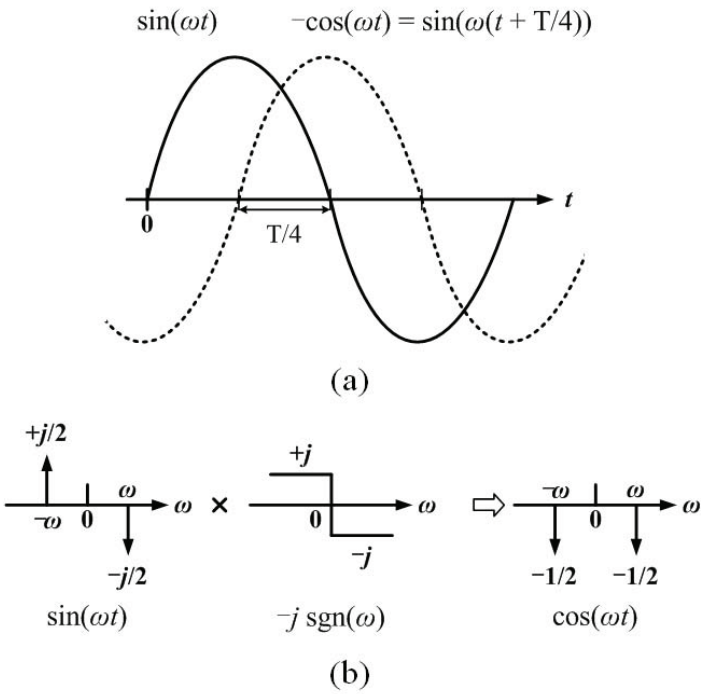

Figure 3.1: 90° phase shifting in (a) time and (b) frequency domains [11].

for mixer's operation, the quadrature phases of the local oscillator as $\sin(\omega_{LO}t)$ and $\cos(\omega_{LO}t)$ are used.

The graphical processing which rejects image signal is illustrated in Fig. 3.3. The basic concept of the phase converting differently for desired and image signals is that the signals of mixer's output are located at positive and negative frequencies on the basis of LO signal's frequency. Suppose the RF input signal including image signal is $RF(t) = \cos(\omega_{RF}t) + \cos(\omega_{IM}t)$, where $\omega_{RF} = 2\pi f_{RF}$, $\omega_{IM} = 2\pi f_{IM}$. f_{RF} is the desired part's frequency of RF signal, and f_{IM} is the unwanted part (image part)'s. To verify principle of image rejection method, this signal does not include amplitude factor. Then, the output signals of mixers can be expressed as having opposite phases for each other like Eqs. (3.1) and (3.2). In this time, ω_{LO} locates in the middle of ω_{RF} and ω_{IM} (The mixer converts the image signal to the same IF frequency as the desired signal by frequency mirror effect between the RF and LO signals.).

$$A_H = -A_{H,RF}\sin((\omega_{RF} - \omega_{LO1})t) + A_{H,IM}\sin((\omega_{LO1} - \omega_{IM})t), \quad (3.1)$$

$$B_H = B_{H,RF}\cos((\omega_{RF} - \omega_{LO})t) + B_{H,IM}\cos((\omega_{LO} - \omega_{IM})t). \quad (3.2)$$

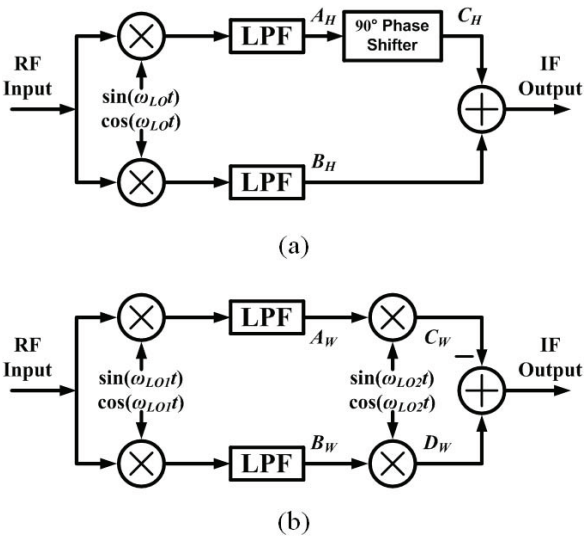

Figure 3.2: (a) Hartley and (b) Weaver image rejection structures [11].

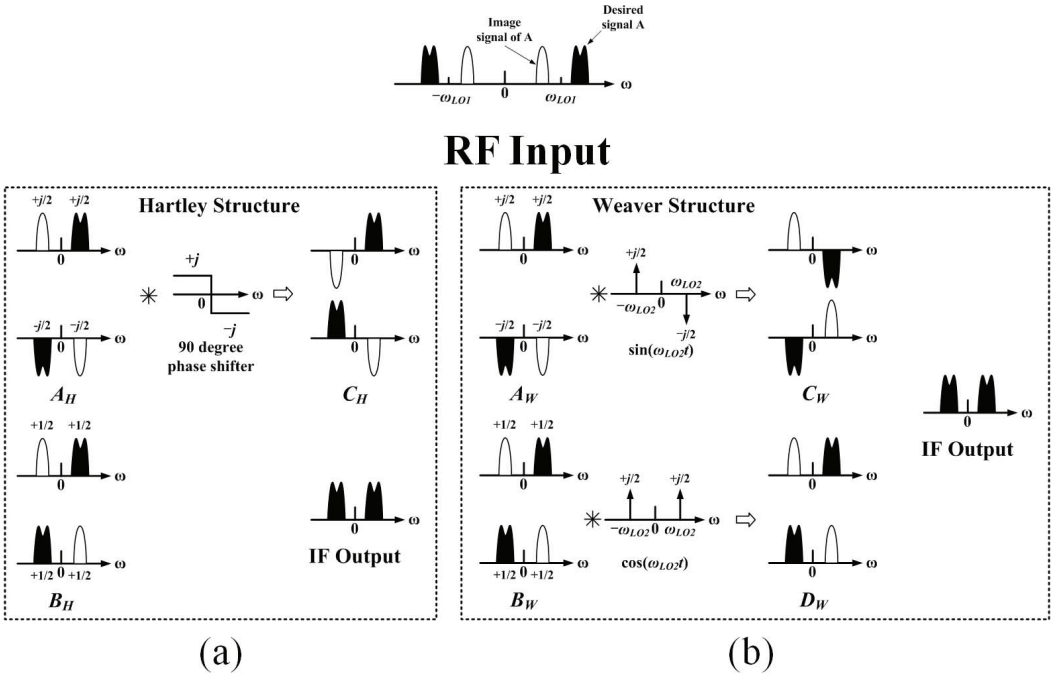

Figure 3.3: Graphical signal flow of (a) Hartley and (b) Weaver image rejection structures [11].

In Hartley structure, one phase of the two mixer output signals is converted through phase shifter as much as 90°. Then, the point C_H's signal in Fig. 3.2(a) can be obtained as follows:

$$C_H = C_{H,RF}\cos((\omega_{RF} - \omega_{LO})t) - C_{H,IM}\cos((\omega_{LO} - \omega_{IM})t). \tag{3.3}$$

As shown in Eqs. (3.2) and (3.3), these two signals have the same phase on desired signal and an opposite phase on unwanted signal. With the assumption of no amplitude error between these two signals ($B_{H,RF} = C_{H,RF}$, $B_{H,IM} = C_{H,IM}$), the unwanted image signal can be rejected through summation. In Weaver structure, there is a different way to obtain signals which have opposite phases for each other. As illustrated in Fig. 3.2(b), phases are converted one more time by second-stage mixers. Equations (3.4) and (3.5) show these output signals of second-stage mixers as C_W and D_W in Fig. 3.2(b). Finally, unwanted signal by using these two signals can be removed.

$$C_W = -C_{W,RF}\cos((\omega_{RF} - \omega_{LO1} - \omega_{LO2})t) + C_{W,IM}\cos((\omega_{LO1} - \omega_{LO2} - \omega_{IM})t), \quad (3.4)$$

$$D_W = D_{W,RF}\cos((\omega_{RF} - \omega_{LO1} - \omega_{LO2})t) + C_{W,IM}\cos((\omega_{LO1} - \omega_{LO2} - \omega_{IM})t). \quad (3.5)$$

In image rejection technique using phase conversion of signals, the errors of amplitude and phase of comparing signals are mostly important. Normally, the IMRR is used to evaluate these errors. IMRR is defined as the power ratio between the desired signal and unwanted image signal as follow.

$$\text{IMRR} = \frac{\text{Image Signal Power}}{\text{Desired Signal Power}}. \quad (3.6)$$

This is calculated by difference of amplitude and phase of compared two signals as:

$$\text{IMRR} = \frac{1 + 2A\cos\delta + A^2}{1 - 2A\cos\delta + A^2}, \quad (3.7)$$

where A is the amplitude difference and δ is the phase difference.

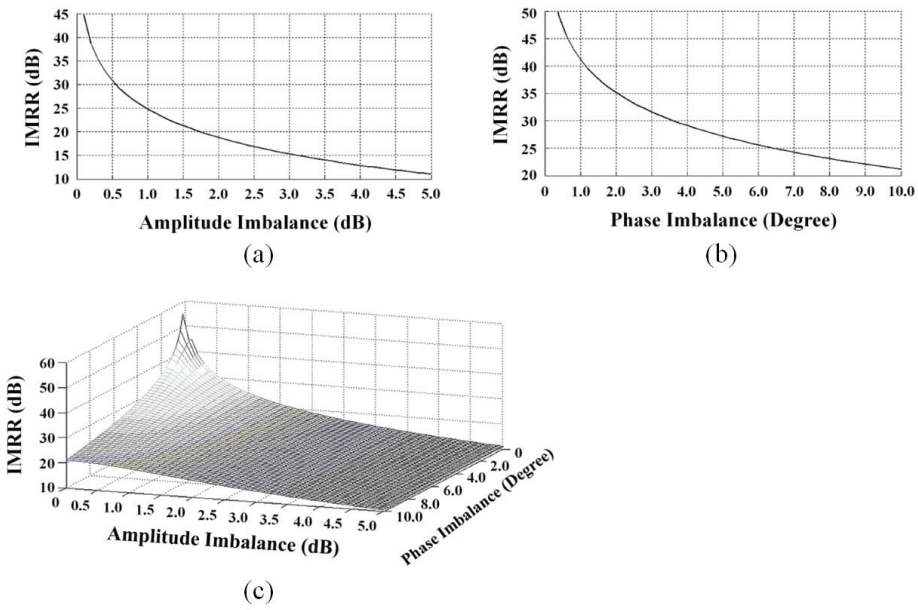

Figure 3.4: IMRR with (a) ampitude, (b) phase, and (c) amplitude and phase imbalances.

Figure 3.4 shows the IMRR versus amplitude and phase imbalances between two signals. As these results, IMRR is around 42 dB with the phase imbalance of 1°, and around 25 dB with the amplitude imbalance of 1 dB. In practical case, the imbalances of amplitude and phase occur at the same time. The IMRR results versus amplitude and phase imbalances are illustrated in Fig. 3.4(c). From this result, the imbalances of amplitude and phase are under 1 dB and under 2 to 3° to obtain IMRR over 40 dB.

3.2.2 Concept of Triple-band Receiver

Based on the image rejection method mentioned above, a band signal can be separated from other band signals of RF path in the same way. In short, two independent port are equipped for subtraction and summation at IF-stage in Fig. 3.2. Then, the desired and image signals can be obtained at each port. Like this method, the dual-band signals can be received independently at each port using conventional Weaver and Hartley structures [12, 13].

The proposed receiver takes the Weaver structure which converts RF frequency to IF frequency by two-stage mixers as illustrated in Fig. 3.5. The phases of signals are converted two times through these mixers as well. There are also second-stage poly-phase filters (PPFs) between the first- and second-stage mixers. The signals' phases are converted more times than conventional Weaver structure, because of 90° phase shifting function of these PPFs, which is similar to PPF in Hartley structure. For proper phase translations of signals, the summation and subtraction are used to provide input signals of second-stage mixer and PPFs. This method will be mentioned later in more detail.

3.3 Signal Processing in Triple-band Receiver

The proposed triple-band receiver architecture is based on Weaver image rejection method. The architecture is basically modified from that of a dual-band GPS receiver developed in a previous study [12, 13]. For explanation about operation principle of proposed triple-band signal receiver, the flow block diagram of the signal processing of that is shown in Fig. 3.5. The system converts frequency of signals to IF-stage through first- and second-stage mixers. In this time, the mixer works with quadrature LO signals (I and Q phase signals), and through this operation, the signals have a different phase for each other. In the same time, the PPF which is located between the first- and second-

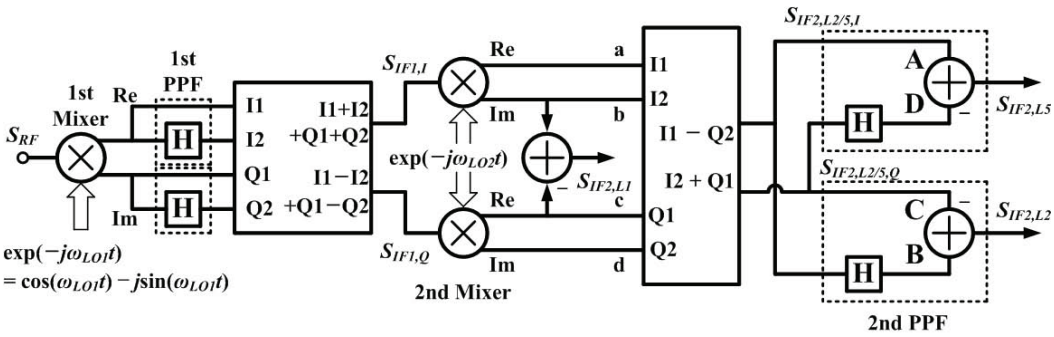

Figure 3.5: Signal processing of the proposed triple-band receiver.

stage mixers translates the signal phase one more time. During these signal processing, the proper summation and subtraction of signals are used to remove undesired image signals. Through these processes, the triple-band signal on different each port can be received independently. Undesired signals are image signals with respect to the desired signal. In simple words, the Weaver image rejection method separates the L1 band signal from the L2 and L5 band signals, which are image signals with respect to the L1 band signal. Then, the second PPFs translate the phase of the L2 and L5 band signals to create one signal as an image signal with respect to the other signal. Through these steps, each band signal can be received independently at each port.

For the image rejection method, the concept of complex signal processing and the Hilbert transform (denoted as "H" in the figure) were used to give concise expressions [14, 15]. The RF input signal can be expressed as

$$s_{RF}(t) = \Re[a(t)\exp(j\omega t)], \tag{3.8}$$

where $a(t)$ is a complex base-band signal and ω is the angular frequency of the RF signal. The frequency and phase of this RF signal are converted along with the quadrature LO signals as $f_{LO1}(= \omega_{LO1}/2\pi)$ in the first-stage mixer as follows:

$$s_{RF}(t)\, e^{-j\omega_{LO1}t} = \frac{1}{2}[a(t)e^{j(\omega-\omega_{LO1})t} + a^*(t)e^{-j(\omega+\omega_{LO1})t}]. \tag{3.9}$$

The first term in the brackets on the right hand side is the desired down-converted component. The

first PPF generates the Hilbert transforms of the real and imaginary components of their input signals to change their phases [15]. The resulting outputs consisting of four differential pairs are intertwined to cancel the undesired band signals, which is implemented by using proper resistive adders. Through resistive adders, the PPF's output signals are re-combinated through following calculating step as shown in Fig. 3.5.

$$s_{IF1,I}(t) = I1 + I2 + Q1 + Q2, \tag{3.10}$$

$$s_{IF1,Q}(t) = I1 - I2 + Q1 - Q2, \tag{3.11}$$

these signals can be expressed using Hilbert transform as follows:

$$\begin{aligned} s_{IF1,I}(t) &= \Re[s_{RF}(t)e^{-j\omega_{LO1}t}] + \Im[s_{RF}(t)e^{-j\omega_{LO1}t}] \\ &\quad + H[\Re[s_{RF}(t)e^{-j\omega_{LO1}t}]] + H[\Im[s_{RF}(t)e^{-j\omega_{LO1}t}]], \end{aligned} \tag{3.12}$$

$$\begin{aligned} s_{IF1,Q}(t) &= \Re[s_{RF}(t)e^{-j\omega_{LO1}t}] + \Im[s_{RF}(t)e^{-j\omega_{LO1}t}] \\ &\quad - H[\Re[s_{RF}(t)e^{-j\omega_{LO1}t}]] - H[\Im[s_{RF}(t)e^{-j\omega_{LO1}t}]]. \end{aligned} \tag{3.13}$$

As the transfer function of the Hilbert transform is $-j\ \mathrm{sgn}(\omega)$, where $\mathrm{sgn}(\omega)$ is the sign function, these intertwined signals can be expressed as:

$$\begin{aligned} s_{IF1,I}(t) &= \Re[a(t)e^{j(\omega-\omega_{LO1})t}]u_{\omega_{LO1}-\omega} \\ &\quad + \Im[a(t)e^{j(\omega-\omega_{LO1})t}]u_{\omega-\omega_{LO1}} + \Re[a(t)e^{j(\omega+\omega_{LO1})t}], \end{aligned} \tag{3.14}$$

$$\begin{aligned} s_{IF1,Q}(t) &= -\Im[a(t)e^{j(\omega-\omega_{LO1})t}]u_{\omega_{LO1}-\omega} \\ &\quad + \Re[a(t)e^{j(\omega-\omega_{LO1})t}]u_{\omega-\omega_{LO1}} + \Im[a(t)e^{j(\omega+\omega_{LO1})t}], \end{aligned} \tag{3.15}$$

where $u_\omega = (1 + \omega/|\omega|)/2$. Note that the frequency components of $\omega - \omega_{LO1}$ in $s_{IF1,I}(t)$ and $s_{IF1,Q}(t)$ have opposite polarity and both have opposite polarity for $\omega > \omega_{LO1}$ and $\omega < \omega_{LO1}$. These features are useful for the signal separation between the L1 and the other (L2 and L5) band signals.

The obtained signals that had their frequency and phase translated through the above process are converted again in the second-stage mixer. Here the quadrature LO signals of the LO frequency $f_{LO2}(= \omega_{LO2}/2\pi)$ are used to convert the phase and frequency. To separate L1 from the other signals, the outputs of the second mixers are properly added and subtracted to extract the L1 band signal and to generate the combinations of the L2 and L5 band signals with different polarity, as follows:

$$\begin{aligned} s_{IF2,L1}(t) &= -\Im[s_{IF1,I}(t)e^{-j\omega_{LO2}t}] + \Re[s_{IF1,Q}(t)e^{-j\omega_{LO2}t}] \\ &= \Re[a(t)e^{j(\omega-\omega_{LO1}-\omega_{LO2})t}]u_{\omega-\omega_{LO1}} \\ &\quad -\Im[a(t)e^{j(\omega-\omega_{LO1}-\omega_{LO2})t}]u_{\omega_{LO1}-\omega}, \end{aligned} \tag{3.16}$$

$$\begin{aligned} s_{IF2,L2/5,I}(t) &= \Re[s_{IF1,I}(t)e^{-j\omega_{LO2}t}] - \Im[s_{IF1,Q}(t)e^{-j\omega_{LO2}t}] \\ &= \Im[a(t)e^{j(\omega-\omega_{LO1}+\omega_{LO2})t}]u_{\omega-\omega_{LO1}} \\ &\quad +\Re[a(t)e^{j(\omega-\omega_{LO1}+\omega_{LO2})t}]u_{\omega_{LO1}-\omega} \\ &\quad +\Re[a(t)e^{j(\omega+\omega_{LO1}-\omega_{LO2})t}], \end{aligned} \tag{3.17}$$

$$\begin{aligned} s_{IF2,L2/5,Q}(t) &= \Im[s_{IF1,I}(t)e^{-j\omega_{LO2}t}] + \Re[s_{IF1,Q}(t)e^{-j\omega_{LO2}t}] \\ &= \Re[a(t)e^{j(\omega-\omega_{LO1}+\omega_{LO2})t}]u_{\omega-\omega_{LO1}} \\ &\quad -\Im[a(t)e^{j(\omega-\omega_{LO1}+\omega_{LO2})t}]u_{\omega_{LO1}-\omega} \\ &\quad +\Im[a(t)e^{j(\omega+\omega_{LO1}-\omega_{LO2})t}]. \end{aligned} \tag{3.18}$$

Note that the frequency components of $\omega - \omega_{LO1} + \omega_{LO2}$ in $s_{IF2,L2/5,I}(t)$ and $s_{IF2,L2/5,Q}(t)$ have opposite polarity. As described in the next step, an appropriate combination of these frequency components and their Hilbert transforms can exhibit different polarities for $\omega > \omega_{LO1} - \omega_{LO2}$ and $\omega < \omega_{LO1} - \omega_{LO2}$. These features are useful for the separation of the L2 and L5 band signals.

To convert the center frequencies of the L1, L2, and L5 band signals to the same IF frequency $f_{IF2}(= \omega_{IF2}/2\pi)$, along the signal path from the first to the second mixer, the LO1 and LO2 frequencies (f_{LO1} and f_{LO2}) are set as follows:

$$\omega_{LO1} = \frac{\omega_{L1} + \omega_{L2}}{2}, \tag{3.19}$$

$$\omega_{LO2} = \omega_{LO1} - \frac{\omega_{L2} + \omega_{L5}}{2}, \tag{3.20}$$

where $f_{Li}(= \omega_{Li}/2\pi)$ is the center frequency of the L_i band (i=1, 2, and 5). In this case, $\omega_{IF2} = (\omega_{L2} - \omega_{L5})/2$. Since $f_{L1} = 1575.42$ MHz, $f_{L2} = 1227.6$ MHz, and $f_{L5} = 1176.45$ MHz, $f_{LO1} = 1401.51$ MHz, $f_{LO2} = 199.485$ MHz, and $f_{IF2} = 25.575$ MHz. In the first down-conversion and the first PPFs, the L1 and L2 band signals are converted to $\pm$ 173 MHz images of each other with opposite polarity, as seen in the first and second terms of Eqs. (3.14) and (3.15). On the other hand, the L5 band signal is converted to 225.06 MHz in this stage. With regard to the second down-conversion with the following appropriate signal additions, Eq. (3.16) indicates that $s_{IF2,L1}(t)$ contains the L1 band signal at f_{IF2}. Similarly, Eqs. (3.17) and (3.18) reveal that the second terms in $s_{IF2,L2/5,I}(t)$ and $s_{IF2,L2/5,Q}(t)$ contain the L2 and L5 band signals at $\pm f_{IF2}$.

To separate each of the L2 and L5 band signals after the second mixing and the following signal additions, the $s_{IF2,L2/5,I}(t)$, $s_{IF2,L2/5,Q}(t)$, and their Hilbert transform generated in the second PPF are properly manipulated as follows:

$$\begin{aligned} s_{IF2,L2}(t) &= -s_{IF2,L2/5,Q}(t) + H[s_{IF2,L2/5,I}(t)] \\ &= 2\Im[a(t)e^{j(\omega-\omega_{LO1}+\omega_{LO2})t}]u_{\omega_{LO1}-\omega}u_{\omega-\omega_{LO1}+\omega_{LO2}} \\ &\quad -2\Re[a(t)e^{j(\omega-\omega_{LO1}+\omega_{LO2})t}]u_{\omega-\omega_{LO1}}, \end{aligned} \tag{3.21}$$

$$\begin{aligned} s_{IF2,L5}(t) &= s_{IF2,L2/5,I}(t) - H[s_{IF2,L2/5,Q}(t)] \\ &= 2\Re[a(t)e^{j(\omega-\omega_{LO1}+\omega_{LO2})t}]u_{\omega_{LO1}-\omega_{LO2}-\omega} \\ &\quad +2\Re[a(t)e^{j(\omega+\omega_{LO1}-\omega_{LO2})t}], \end{aligned} \tag{3.22}$$

where $\omega_{LO1} > \omega_{LO2}$ is utilized to simplify the expressions such that $u_{\omega-\omega_{LO1}}u_{\omega-\omega_{LO1}+\omega_{LO2}} = u_{\omega-\omega_{LO1}}$. Equations (3.21) and (3.22) reveal that $s_{IF2,L2}(t)$ and $s_{IF2,L5}(t)$ contain the L2 and L5 band signals at f_{IF2}. The last term in $s_{IF2,L1}(t)$, $s_{IF2,L2}(t)$ and $s_{IF2,L5}(t)$, which corresponds to the higher frequency component, can be filtered out in the following stage (It will be mentioned in Chapter 5.).

Figure 3.6 shows the graphical signal spectrum of signal processing which are expressed by above equations. This figure shows the signals from second-stage mixer outputs to final signal after second-stage PPF. Each point of alphabet is the same point of Fig. 3.5. The signals of points “a” to “d” of the left first dotted line in Fig. 3.6 include L1, L2, and L5 in the same position. However, these

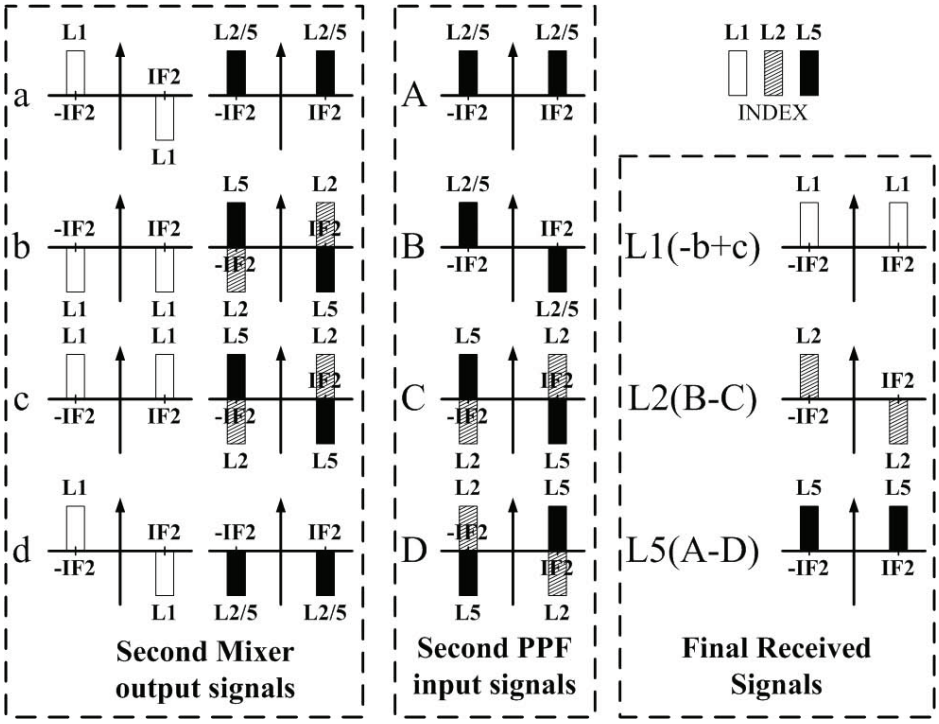

Figure 3.6: Graphical signal processing flow at the locations indicated in Fig. 3.5.

signals have different phases for each other. There is the phase difference of 90° between the L1 and L2/5 and 180° between the L2 and L5. So, these signals are distinguished for each signal. In this stage, L1 band signal is obtained by subtraction of points "b" and "c". At the point of second-PPF input, there is not L1 band signal. For proper summation and subtraction, the L1 band signal can be rejected. Then, from these signals (A to D), L2 and L5 band signals can be separated. As illustrated in Fig. 3.6, L2 and L5 band signals are obtained by (B−C) and (A−D).

3.4 Simulation of Proposed Receiver Architecture

To verify the proposed receiver architecture for triple-band signal, the simulations are carried out. Firstly, the signal flow was verified using behavior-level numerical simulations under MATLAB. Then, through ideal functional blocks in Keysight ADS simulator, system operation on frequency

translation and signal demodulation were carried out using circuit simulations. The Hilbert transform mentioned in the last section is realized through second-stage PPF with ideal RC component. Based on it, the PPF with real components is designed in next chapter.

The proposed architecture was simulated to show the possibility of receiving the wanted signal at each port. For simple calculation, each signal was set as the L1 band signal was 1600 MHz, the L2 band signal was 1200 MHz and the L5 band signal was 1100 MHz. The first and second LO signals were 1400 MHz, and 250 MHz, respectively. Figure 3.7 shows the MATLAB simulation results. In calculation results, each band signal can be obtained at each port. The baseband frequencies for each band signal are the same as 50 MHz.

Continuously, the RF front-end composed with ideal elements was verified by Keysight ADS simulator. In case of circuit simulation, the L1 band signal of 1575.42 MHz, the L2 band signal of 1227.6 MHz and the L5 band signal of 1176.45 MHz were used. The first LO signal was 1401.51 MHz, the second LO signal was 199.485 MHz as the same specifications of real GPS signal. The RF input powers were -75 dBm. The gains of LNA and active mixer were 25 dB and 10 dB.

To distinguish each band signal easily, the BPSK-modulated RF input signals with different sequences per each band are used. As results in Fig. 3.8, each band signal is independently received at separated ports. To verify image reject, the analog output's amplitudes are illustrated in Fig. 3.9. In

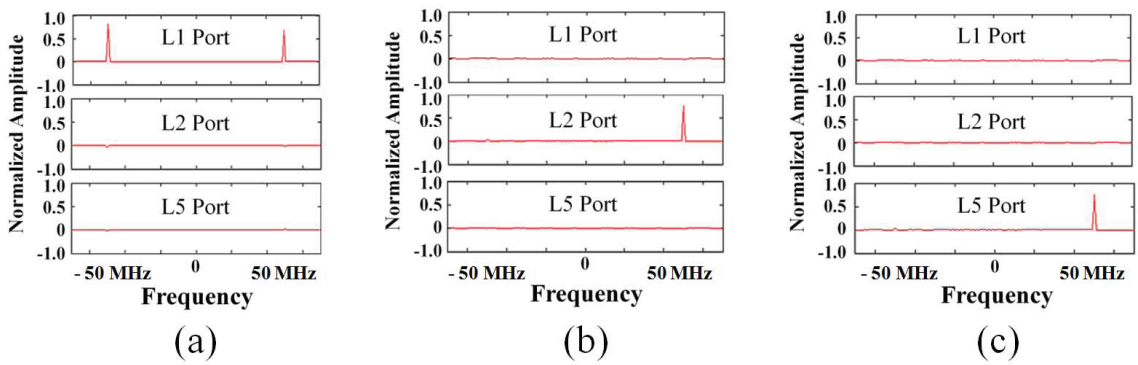

Figure 3.7: Behavior-level numerical simulation results of frequency translation with only (a) L1 band signal, (b) L2 band signal, and (c) L5 band signal.

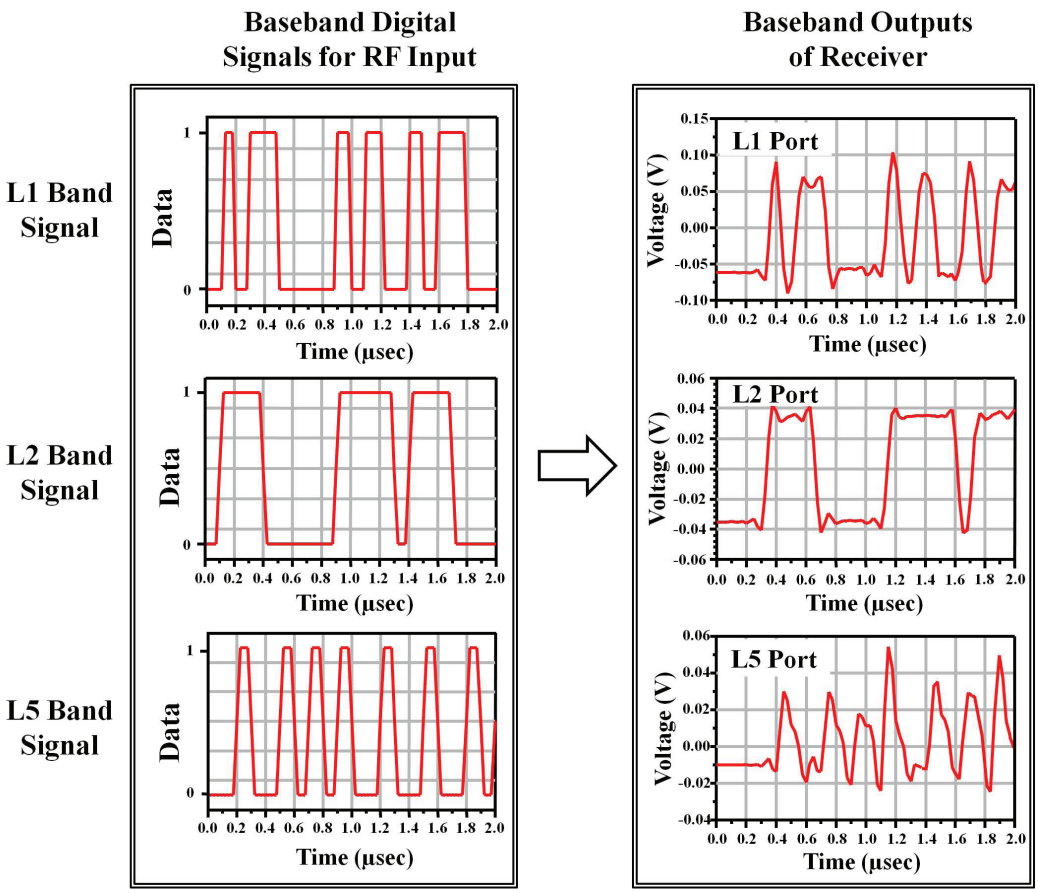

Figure 3.8: Circuit simulation results of RF front-end using modulation signals.

Fig. 3.9(a), the result for signal of L1 band is shown. At that time, there are no signals at L2 and L5 band ports. On the other hand, in Figs. 3.9(b) and (c), the signals are shown at only L2 and L5 band port. As shown in results, IMRRs for each band signal are shown around 50 dB. This simulation used ideal elements, so there are no parameter mismatch. However in result, the value of IMRR is not an ideal (In ideal case, the IMRR has an infinite value.). It is due to second-stage PPF features used to frequency extension. The detail on it will be described in Chapter 4.

Differently from the dual-band reception, the simultaneous triple-band reception requires two frequency conversions. The most important point of the proposed architecture is use of the same LO1

and LO2 signals for each of triple-band signal to realize the same RF signal delay which is important in some scientific applications (e.g. [2]), as described in Chapter 1. However, simultaneous generation of the LO1 and LO2 signals using one PLL synthesizer in some literatures [4, 5] is impossible. As the simple solution, the LO1 and LO2 signals can be generated using the first PLL with reference frequency f_0 (= 10.23 MHz) and division ratio 137 and the second PLL with reference $f_0/2$ and division ratio 39, respectively. In addition, the expected sampling frequency in A/D conversion of $s_{IF2,Li}(t)$ (i= 1, 2, 5) in Fig. 3.5 is $5f_0$ (= 51.15 MHz). When the external reference frequency is set to $5f_0$, the LO1, LO2, and the A/D conversion clock signals can be realized using the first and the second PLLs and some frequency dividers. Compared to the literature [8], which uses two PLLs with the same circuit, the proposed architecture requires the first PLL operating at higher frequency and the second PLL operating at lower frequency. The power consumption of the second PLL can be much smaller than that in the first PLL. Thus the first PLL is expected to dominate power consumption for LO generations. To reduce occupation area, the second PLL can use the high-frequency LC VCO with frequency divider instead of low-frequency LC VCO. It means there is trade-off between the occupation area and power consumption in the second PLL, as shown in the literature [16]. By optimizing design of the second PLL, the drawbacks of the proposed architecture in occupation area and power consumption is expected to relax.

3.5 Theory of Digital Compensation Technique

The image rejection simulation results used ideal elements, so there are not parameter mismatches. However in practical case, they exists and degrade IMRR. As seen in Fig. 3.5, the L1 band signal is received through the first PPF, while the L2 and L5 band signals are received through the first and second PPFs. From the different signal path, the IMRR of L2 and L5 band signals is worse than L1 band's. To improve the IMRR, compensation technique was considered. Normally, the compensation can be applied with an analog or digital technique [17, 18]. When the analog scheme is used, there are so many considering points like circuitry complexity. Above all, to avoid large area occupation and high power consumption, the digital compensation of the IMRR is investigated in this study. In this technique, the relation of the signals at A and D and those at B and C in Fig. 3.5 are implemented digitally by using four ADCs.

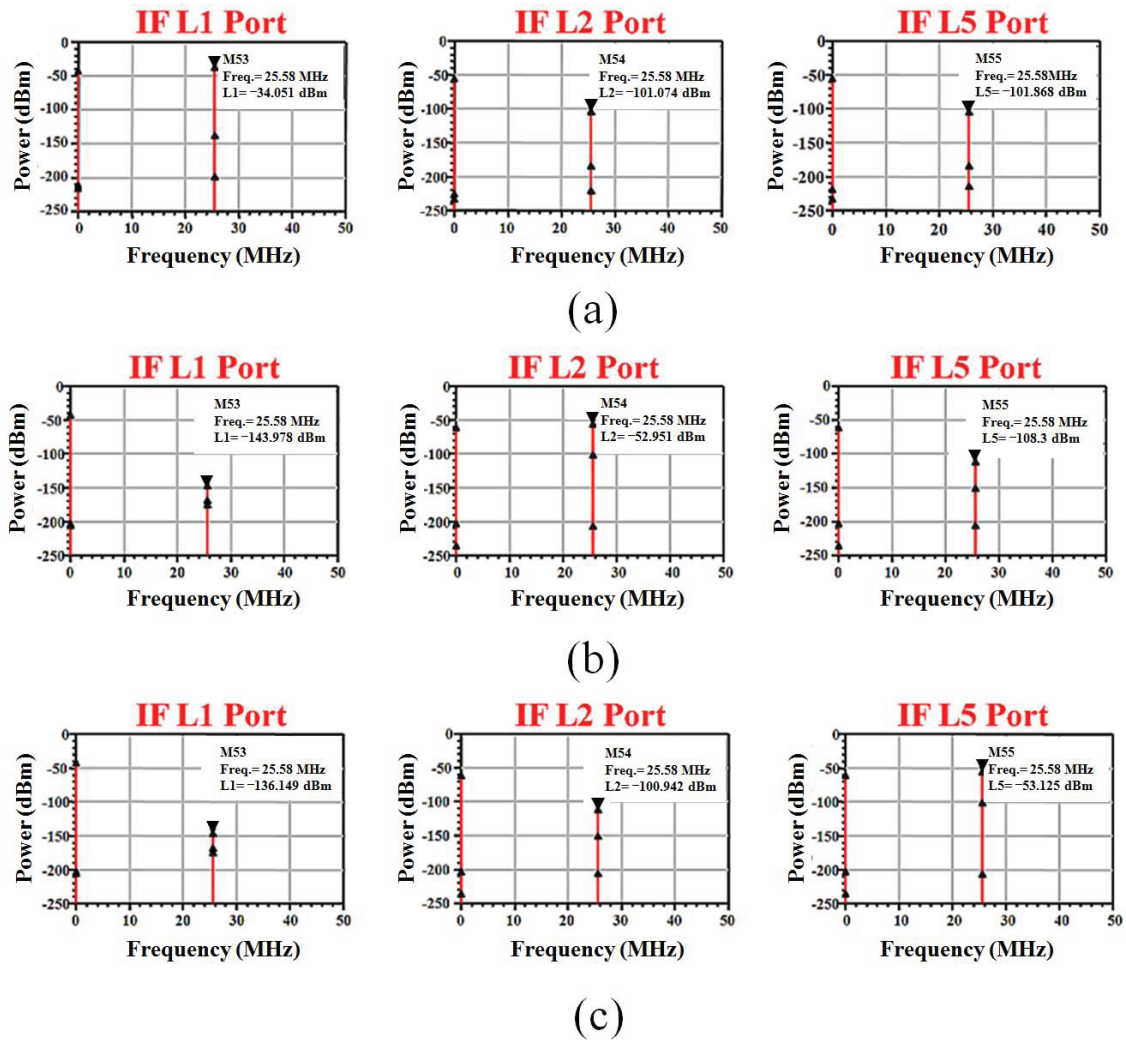

Figure 3.9: Circuit simulation results of image rejection with input signal of (a) L1 band, (b) L2 band, and (c) L5 band.

The block diagram of the digital compensation is conceptually shown in Fig. 3.10. For digital compensation technique, it is important to detect amplitude and phase errors. Phase errors are more significant than amplitude errors since GPS receivers usually use low-resolution ADCs. This suggests that the amplitude errors of the L2 and L5 band signals in the second PPF can experience

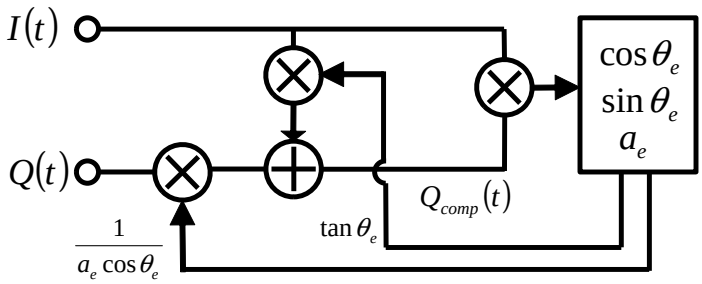

Figure 3.10: Block diagram of the phase and amplitude compensation.

quantization errors from the ADC.

For detecting of digital signal's phase error, there are some limitations. The effective number of ADC bit determines detectable signal variation. On the other hand, the sampling rate limits detectable phase difference between two signals. These two factors have trade-off relation. In other words, for low sampling rate, high effective number of bits are available for enough detecting capability.

For case of detecting some degree's phase error, proper relation between the sampling rate and effective number of ADC bit are expected. To explain this, ADC output of 25 MHz CW signal is illustrated in Fig. 3.11. Opened squares in this figure show the reference signal's ADC output with 200 MHz sampling rate. In Figs. 3.11(b) and (c), the dotted line shows a quadrature signal with 90° against the reference signal and the solid line shows a quadrature signal with 15° phase error. In these figures, the opened triangles and opened circles present the sampling point at 200 MHz sampling rate. When difference of these two signal amplitudes is less than ADC's resolution, there is no influence after ADC. (In custom GPS system, the bit of ADC is normally 1 or 2-bit, so this assumption is reasonable.) Figure 3.11(b) shows the sampling points made for 2-bit ADC, so its resolution is $V_{FS}/4$. In Fig. 3.11(c), the ADC is 3-bit, so its resolution is $V_{FS}/8$. As shown in square box in figures, when the phase error occurred at points "a" to "c". In Fig. 3.11(b), the ADC output change is less than the resolution, so it cannot be detected. However in Fig. 3.11(c), ADC output change at point "a" due to phase error can be detected. Such detection error of phase change can be relaxed using integration of ADC output for a period. As shown in these figures, effective number of ADC

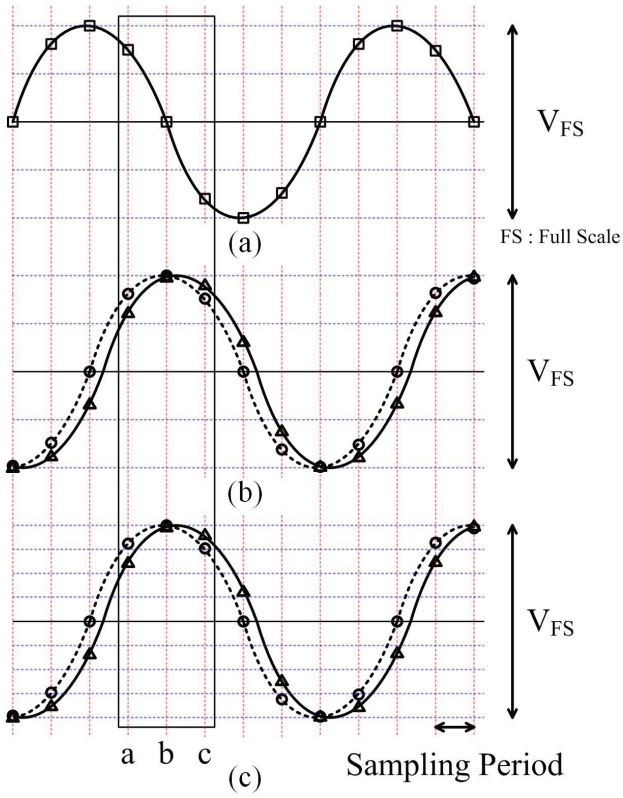

Figure 3.11: (a) CW signal of in-phase reference signal, (b) quadrature signal with 2-bit ADC, and (c) quadrature signal with 3-bit ADC (The solid line and dashed line corresponds to the signals with and without 15° phase error, respectively. Each mark is sampling point.).

bit and sampling rate determine detecting capability. This relationship can be expressed by

$$\text{Detectable Phase Error} \approx \frac{2\pi/M}{2^n}, \tag{3.23}$$

where M is the ratio of the ADC sampling rate to the target frequency, and n is the effective number of bits of the ADC for the input level.

With these detecting conditions, in-phase and quadrature signals with error terms of Fig. 3.10 can be expressed as follows:

$$I(t) = m(t)\ \cos(\omega_{IF2}\, t), \tag{3.24}$$

$$Q(t) = a_e\, m(t)\ \sin(\omega_{IF2}\, t + \theta_e), \tag{3.25}$$

where a_e is the amplitude error, θ_e is the phase error between the $I(t)$ and $Q(t)$ signals.

To obtain the phase error between the $I(t)$ and $Q(t)$ signals, a multiplier with a gain of 2 (6 dB) is used for the initial condition of $a_e = 1$, and its output is integrated in a single period to pass a low-frequency error component related to the compensation factors ($\sin\theta_e$, $\cos\theta_e$, and a_e in Eq. (3.26)). From the calculation using the feed-back loop in Fig. 3.10, a compensated signal can be obtained as follows:

$$Q_{comp}(t) = \frac{Q(t)}{a_e\ \cos\theta_e} - \ I(t)\ \tan\theta_e = m(t)\ \sin(\omega_{IF2}\ t). \tag{3.26}$$

Through above process, the quadrature signal with phase error can be compensated, and the IMRR against in-phase signal can be improved.

3.6 Conclusion

The architecture which can receive triple-band GPS signal (L1, L2, and L5 bands) is proposed. Proposed architecture can receive signals through only one RF path by using the phase-converting image reject method to separate signals. The Weaver structure is used, but PPF is adapted to translate the signals' phases as like the Hartley structure. Consequently, through four phase translations of mixers and PPFs, each band signal can be selected and separated from the other signals. To verify phases translation, the behavior-level numerical and circuit simulations of the MATLAB and Keysight ADS are used. Digital compensation technique improves the received signal separation capability through error correction between the in-phase and quadrature signals. Through this technique, the effects of parameter mismatch can be reduced.

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Chapter 4

RF Front-end Circuit Design for Triple-band Receiver

In this chapter, the circuit blocks in the RF front-end architecture are described. The design issues and methods are explained. In addition, the simulation results from the verification of these blocks are shown. With these circuit blocks, the issues to be considered for the layout of the proposed RF front-end circuits are also explained.

4.1 Introduction

In this chapter, the designs of the circuit blocks composing the proposed system are described. The key issue of the proposed system is to receive the triple-band signal through a single RF path. Basically, to compose this topology, a single antenna and single low-noise amplifier (LNA) are necessary. For signal frequency translation, doubly-balanced mixers are used. Two types of mixers, active and passive, are used to reduce the power consumption without influencing the system's total noise figure (NF). To generate the quadrature LO signals for operation of the balanced mixers, the balun and poly-phase filter (PPF) are used. The passive adder with a large value resistance and PPF are used to remove undesired image signals using the phase relation of the triple-band signal. The balancing of the output signals of these circuit blocks is important because the image rejection ratio (IMRR) of the system is limited by the amplitude and phase mismatch of these output signals. To reduce these errors, all blocks are designed with symmetry structure. These points are also considered in the layout.

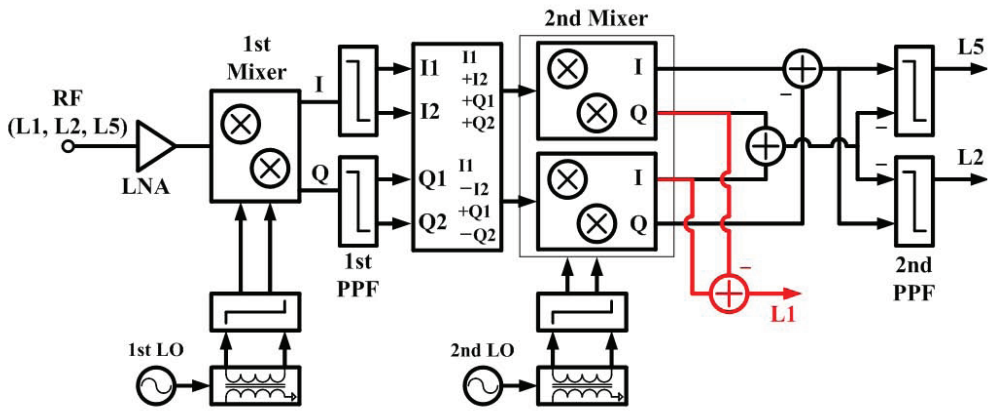


Figure 4.1: RF front-end architecture for triple-band signal.

4.2 RF Front-end Architecture

Figure 4.1 shows the designed RF front-end architecture. As mentioned in the previous chapter, this structure receives the triple-band signal through a RF path. To operate it, it is composed of an LNA, two species of mixers (active and passive), and phase translators. These mixers have a doubly-balanced structure; accordingly, to operate it, an IQ signal generator is designed. To remove the undesired image signals and retain the desired signal from the output of the PPF, the addition and subtraction operations implemented with the resistive adder are used. The designed circuits are laid out in a 130-nm CMOS process with a 1.2-V power supply. The post-layout simulations are carried out using Cadence Spectre. Table 4.1 shows the target specifications of the RF front-end.

4.3 CMOS LNA Stage for Triple-band

4.3.1 LNA Stage Outline

The design of the LNA for the GPS triple-band signal range (L1, L2, and L5) will be discussed. As mentioned above, the LNA is located at the first-stage of the proposed system. Thus, its gain and noise characteristic are most effective for the system characteristics among whole blocks. In a

Table 4.1: Specification of designed RF front-end.

	Specification		Specification
Operation Frequency (MHz)	1170 ~ 1600	Input Reflection Coefficient (dB)	< 10
Power Consumption (mW)	< 10	Noise Figure (dB)	< 8
		IMRR (dB)	> 40

general case of a cascaded system shown in Fig. 4.2, the total NF (NF_{total}) can be calculated as

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \cdots \frac{NF_N - 1}{G_1 G_2 \cdots G_{N-1}}, \tag{4.1}$$

where NF_i and G_i are a noise figure and an available power gain of i-th-stage block, respectively.

The NF and gain of components closest to the input of the whole system are the most important factors. In this study, the LNA with a less than 1.5 dB NF during the 500 MHz operation frequency range (1.1 $\sim$ 1.6 GHz) is designed. In this case, the LNA is located between the antenna and mixer, as shown in Fig. 4.1. This means that the signal power delivery is also important. In this work, the LNA is designed to maintain the input impedance matching condition of S_{11} under -10 dB during the operation frequency ranges. In addition, the mixer input of the next-stage should be considered. The doubly-balanced type mixers are used in this work, which require differential input signals. It is important in adequate signal phase translation in the mixers, which influences total IMRR. To reduce the phase and amplitude mismatches of these signals, the single-ended cascade LNA and active balun are used for the LNA stage.

4.3.2 LNA Stage Design Issues

In the first step of designing the LNA stage, the single-ended LNA is designed. The scheme of the inductive-source-degeneration structure to minimize NF and satisfy input impedance matching is used [2–5]. A single-gain-stage of the LNA can save power and keep high linearity. The cascode-

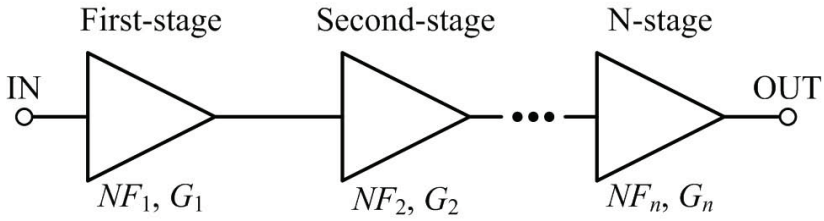


Figure 4.2: Block diagram of cascaded system.

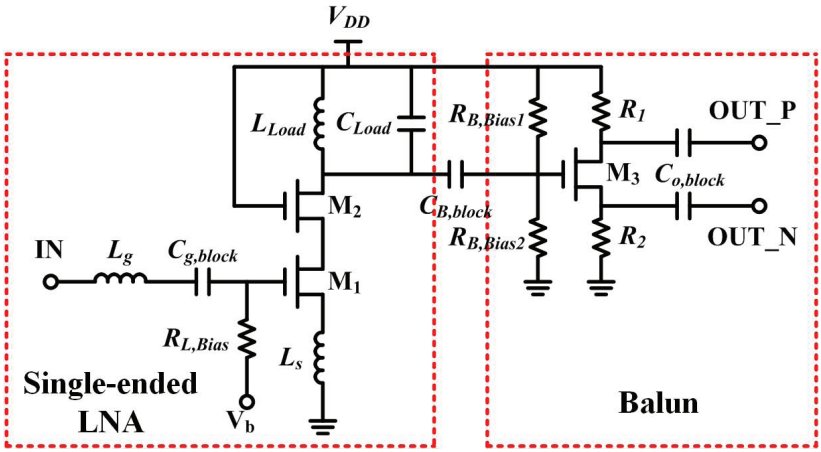


Figure 4.3: Schematic of LNA stage.

stage plays the role of reducing the Miller effect and enhancing reverse isolation between the input and output ports.

Figure 4.3 the designed LNA stage. The single-ended LNA is shown in the left red box; the active balun for the differential output is shown on the right. In this design, the wide-band operation frequency range and low NF as well as the input impedance matching are highlighted.

In the case of inductive-source-degeneration LNA, the circuit noise is affected by the following factors:

1. Gate thermal noise due to resistance of gate and parasitic resistance of the gate inductor.
2. Channel thermal noise.
3. Induced gate noise.

The NF of a block expressed with the above noise factors is given by [2]

$$NF = 1 + \frac{R_{L_g} + R_g}{R_s} + \frac{\gamma}{\alpha} \cdot \chi \cdot R_s \cdot g_m \cdot \left(\frac{\omega_0}{\omega_T}\right)^2, \tag{4.2}$$

where R_{L_g} is the parasitic resistance of gate inductance(L_g), R_s is a source impedance (usually 50 Ω), and R_g is the gate parasitic resistance. α is the ratio of the device transconductance to zero-bias drain conductance, γ is the drain noise current factor, δ is the induced gate noise current factor, c is the correlation coefficient between these noise currents, and κ is the Elmore constant [2, 12]. $f_T(= \omega_T/2\pi)$ is the unity-current-gain cut-off frequency of the device, and $f_0(= \omega_0/2\pi)$ is the operating frequency. The factor χ is defined as [6, 7]

$$\chi = 1 - 2|c|\alpha\sqrt{\frac{\delta\alpha^2}{\kappa\gamma}} + \frac{\delta\alpha^2}{\kappa\gamma}(1 + Q_{in}^2). \tag{4.3}$$

Q_{in} is the input Q-factor of the series LC resonator at the input. In Eq. (4.2), the last term is the most dominant one, which is generated on account of the channel thermal noise [2]. Therefore, the equation can be simplified as

$$NF \simeq 1 + \frac{\gamma}{\alpha} \cdot \chi \cdot R_s \cdot g_m \cdot \left(\frac{\omega_0}{\omega_T}\right)^2. \tag{4.4}$$

The magnitude of the input reflection coefficient $|S_{11}|$ is given by

$$\left|S_{11}\right| = \left|\frac{jQ_{in}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)}{2 + jQ_{in}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)}\right|. \tag{4.5}$$

From Eqs. (4.3), (4.4), and (4.5), the NF and input reflection coefficient can be expressed as a function of Q_{in}. To define Q_{in}, Fig. 4.4 shows the small-signal model of the LNA input-stage. Here, g_m is a transconductance of M1 of Fig. 4.3, r_o is an output impedance of M1, and R_{Load} is a load impedance.

For input impedance matching, based on the small-signal model, input impedance (Z_{in}) can be calculated as

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + g_m\frac{L_s}{C_{gs}}. \tag{4.6}$$

The capacitance between the gate to drain (C_{gd}) is sufficiently small to be ignored. R_{L_g} can be ignored as well, because L_g is used as an external inductor with a high-Q-factor. The MOSFET of the

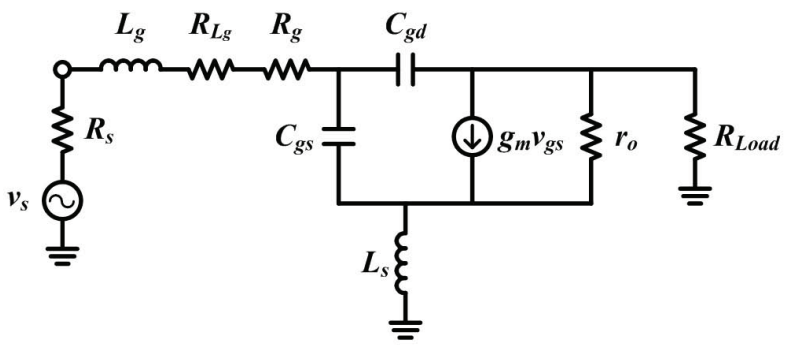


Figure 4.4: Small-signal model of LNA input-stage.

LNA input-stage is composed of 64 multi-fingers, as shown in Fig. 4.8. As described in Chapter 2, the effect of R_g is sufficiently low to increase the number of fingers. At the input series resonant frequency given by the following equation, the imaginary term of Eq. (4.6) can be ignored.

$$\omega_0 = \frac{1}{\sqrt{(L_s + L_g)C_{gs}}}. \tag{4.7}$$

Therefore, the input impedance can be expressed as

$$Z_{in} = g_m \frac{L_s}{C_{gs}}. \tag{4.8}$$

The equivalent series LC resonator at the input consists of a gate inductor (L_g), source degeneration inductor (L_s), capacitance between the gate and source (C_{gs}), and the effective resistance (R_{eff}). Here, the effective resistance is originated from the source degeneration inductor and can be expressed as

$$R_{eff} = \omega_T L_s. \tag{4.9}$$

where ω_T is the cut-off angular frequency (= g_m/C_{gs}). From these values, Q_{in} is obtained as

$$Q_{in} = \frac{1}{\omega_0 C_{gs} R_{L_s}} = \frac{1}{\omega_0 C_{gs} \omega_T L_s}. \tag{4.10}$$

With the matching condition, from Eqs. (4.9) and (4.10), the input Q-factor can be calculated as

$$Q_{in} = \frac{1}{\omega_0 C_{gs} R_s}. \tag{4.11}$$

As shown in Eq. (4.11), Q_{in} is dependent on the MOSFET gate size at the matching condition. To determine the Q_{in} value, Eqs. (4.4) and (4.5) can be used.

4.3.3 LNA Design

4.3.3.1 Single-ended LNA

The LNA is designed through the following steps.

Step 1. Specify Q_{in} from input reflection coefficient $|S_{11}|$ during the desired frequency ranges. (Eq. (4.5))

Step 2. Determine the MOSFET gate width. (Eq. (4.11))

Step 3. Determine g_m to satisfy the desired NF from Q_{in}. (Eq. (4.4))

Step 4. Determine L_g and L_s values to satisfy the matching condition. (Eq. (4.6))

Step 5. Determine the load inductor and capacitance from the operation frequency.

Before the design process, the target specifications and basic process parameters will be described. These values are shown in Table 4.2 and Table 4.3. The target frequency range is located at 1.1 $\sim$ 1.6 GHz. The GPS signal bands are L1, L2, and L5, which are located at 1.57542 GHz, 1.2276 GHz, and 1.17645 GHz. The GPS input signal power level (from the satellite to antenna) is approximately -95 dBm. The active antenna, which is at the front of the LNA, has an approximate 20 dB gain. The input signal power level at the LNA is approximately -75 dBm. It is a relatively small signal level. The system NF typically requires less than 7.5 dB. To satisfy this value, the LNA NF should be under 1.5 dB to give some margin to the next block. To reduce the influence of the following blocks on total NF, the power gain of LNA is over 20 dB. When the following blocks have NF over 10 dB, this LNA gain can keep the degradation of total NF under 1 dB. The designed LNA block has power consumption under 2.5 mW (the drain current is approximately 2 mA). The input reflection coefficients are maintained under -10 dB in the wide frequency bands.

Table 4.2: Specification of designed LNA.

	Specification
Frequency	1.1 to 1.6 GHz
Noise Figure	< 1 dB
Power Gain	> 20 dB
Power Consumption	< 2 mW
Input Reflection Coefficient ($\|S_{11}\|$)	< −10 dB

Table 4.3: Process parameters.

Parameter	Value	Comment
α	0.8	$\alpha = g_m / g_{d0}$ (g_{d0} : zero-bias conductance)
γ	2	Drain noise factor $\gamma = \frac{2}{3}$ (Long channel), $\gamma > \frac{2}{3}$ (Short channel)
δ	4	Induced gate noise factor
κ	1 to 5	Elmore constant $\kappa = 5$ (Long channel)
c	j 0.395	Coefficient of correlation between the drain and induced gate noises

To design the LNA for the wide frequency range, the gate width must be chosen to satisfy the input reflection coefficient ($|S_{11}|$). To specify Q_{in} in Eq. (4.5), these process parameters (Table 4.3) are used. Concurrently, the NF should be considered. As shown in Eqs. (4.3) and (4.4), the NF is related

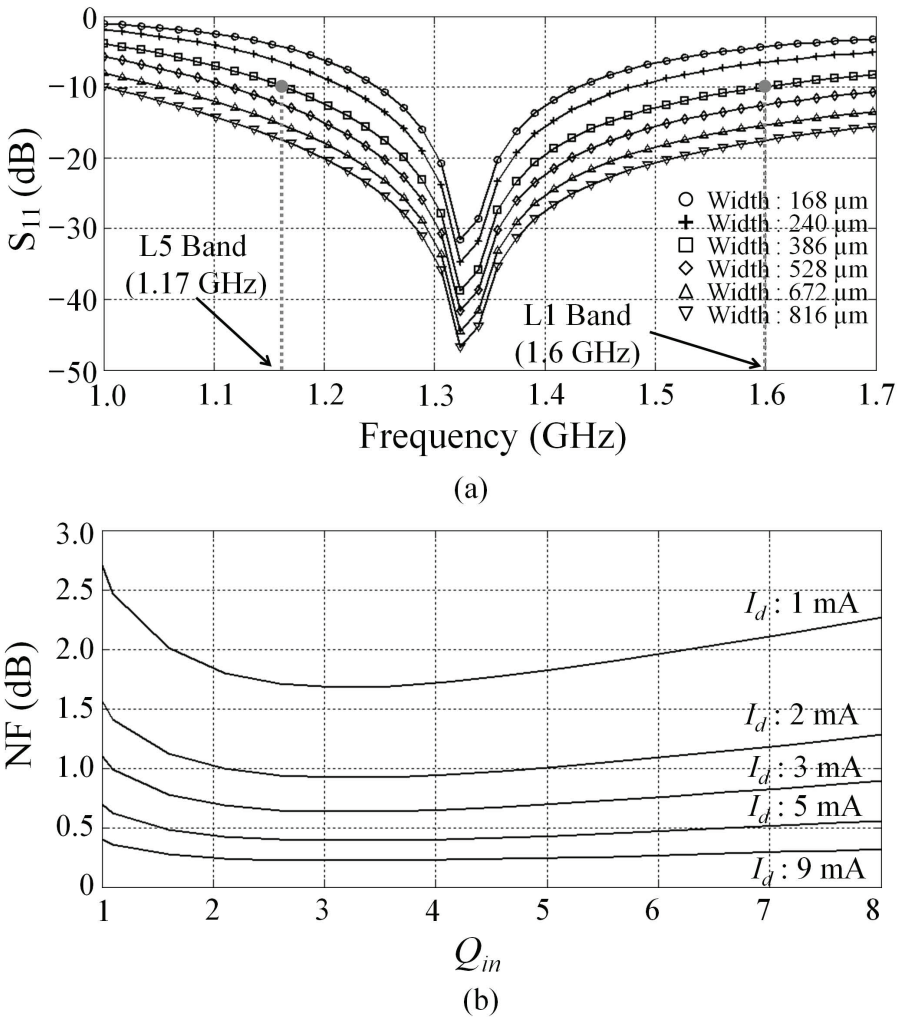


Figure 4.5: Calculated (a) input coeffienct and (b) NF of LNA.

to Q_{in}. In this step, with consideration of the gate width to satisfy the desired $|S_{11}|$, the NF should be calculated versus Q_{in} according to various drain currents. Step 1 to Step 3 in the above design process should be carried out repeatedly to satisfy specifications of $|S_{11}|$ and NF.

The input reflection coefficient ($|S_{11}|$) versus the gate width is illustrated in Fig. 4.5(a). The input reflection coefficient of -10 dB during the target frequency range (1.17 $\sim$ 1.6 GHz) can be obtained

when the gate width is more than 386 μm. Figure 4.5(b) shows the NF versus Q_{in}, which satisfies $|S_{11}|$. When Q_{in} is approximately 3 with a 2 mA drain current, the NF of less than 1 dB can be obtained. Through the above design steps, the capacitance between the gate and source (C_{gs}) is calculated as 450 fF (The gate width is 384 μm). The values of g_m and ω_T can be obtained as 47 mS and 16.7 GHz from the following MOSFET basic equations.

$$C_{gs} = \frac{2}{3} C_{ox} W L, \tag{4.12}$$

$$g_m = \sqrt{2\beta I_d}, \tag{4.13}$$

$$\omega_T = \frac{g_m}{C_{gs}} = \frac{R_s}{L_s}. \tag{4.14}$$

The values of L_s and L_g are obtained from the resonant condition (Eq. (4.7)) and input impedance matching condition (Eq. (4.8)). Here, it is assumed that the input impedance is matched with the source impedance as 50 Ω. With this condition, these values can be obtained as 3 nH and 11.1 nH from Eqs. (4.7) and (4.14).

About the bias condition, the drain current and device size determined at the previous step provide the over-drive voltage (V_{od}) as 67 mV in this case. Through the following load resonant condition, the load inductor (L_{Load}) can be chosen. The output capacitance (C_{out}) is also considered including the input capacitance of the balun described later. It is noted that gate width of cascode-stage MOSFET (M2) is reduced by biasing its gate at V_{DD}, which can reduce parasitic capacitance of its drain terminal. Consequently, the load inductor (L_{Load}) has a value of 17.6 nH with the output capacitance value of about 810 fF.

$$\omega_0 = \frac{1}{\sqrt{L_{Load} C_{out}}}. \tag{4.15}$$

4.3.3.2 Resistive Balun

The passive balanced-unbalanced circuit (balun) is very useful in RF and mm-wave regions. However, in the case of SoCs, the cost should be considered. Conventionally, the passive balun is composed with micro strip-lines of $\lambda/4$ (λ is a wave length.). Thus, the strip-line length depends on the operation frequency. In this work where the target frequency range is near 1.5 GHz, the passive balun is difficult to implement in the integrated circuit. In some cases, an external balun and lumped components for impedance matching are used. However, in that case, the signal loss is significant

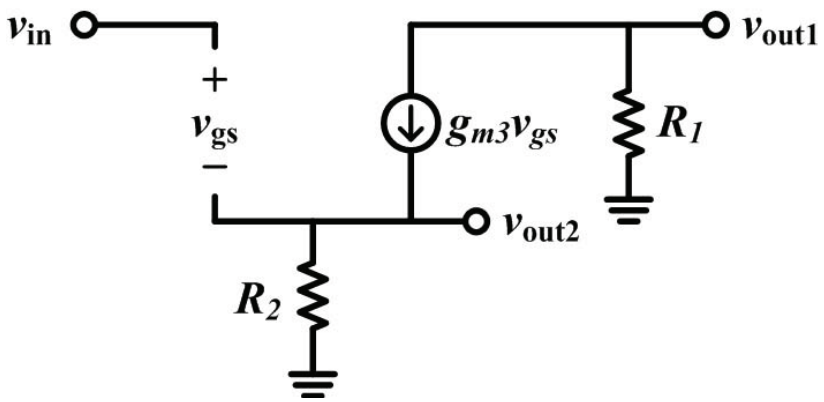


Figure 4.6: Small-signal model of balun.

and the phase and amplitude balances are not good. Therefore, in this study, a simple active balun is used. For less burden to the whole system balance, the most simple single MOSFET is used with two resistors at the source and drain sides. This structure has the advantage of easy control of signal unbalance as described later. Accordingly, the reduction of phase and amplitude errors between the two differential output signals can be achieved.

The circuit block of the balun designed in this paper is illustrated in the right red box in Fig. 4.3. Figure 4.6 shows the small-signal equivalent circuit for the balun. The voltage gains, $A_{v,out1}$ and $A_{v,out2}$, can be presented as

$$A_{v,out1} = \frac{v_{out1}}{v_{in}} = -\frac{R_1}{R_2 + \frac{1}{g_{m3}}}, \tag{4.16}$$

$$A_{v,out2} = \frac{v_{out2}}{v_{in}} = \frac{R_2}{R_2 + \frac{1}{g_{m3}}}, \tag{4.17}$$

where g_{m3} is a transconductance of MOSFET M3 in Fig. 4.3. The negative sign in Eq. (4.16) means a phase converting as 180°. The amplitude balance between the v_{out1} and v_{out2} can be simply handled with a ratio of R_1 with R_2. Thus, the transconductance of M3, which determines the power consumption, can be more flexibly designed. In practical case of this balun, parasitic capacitances of M3 cause amplitude and phase errors of the differential output. These errors can be reduced by slightly changing R_1/R_2 to ignore their influence on receiver's IMRR.

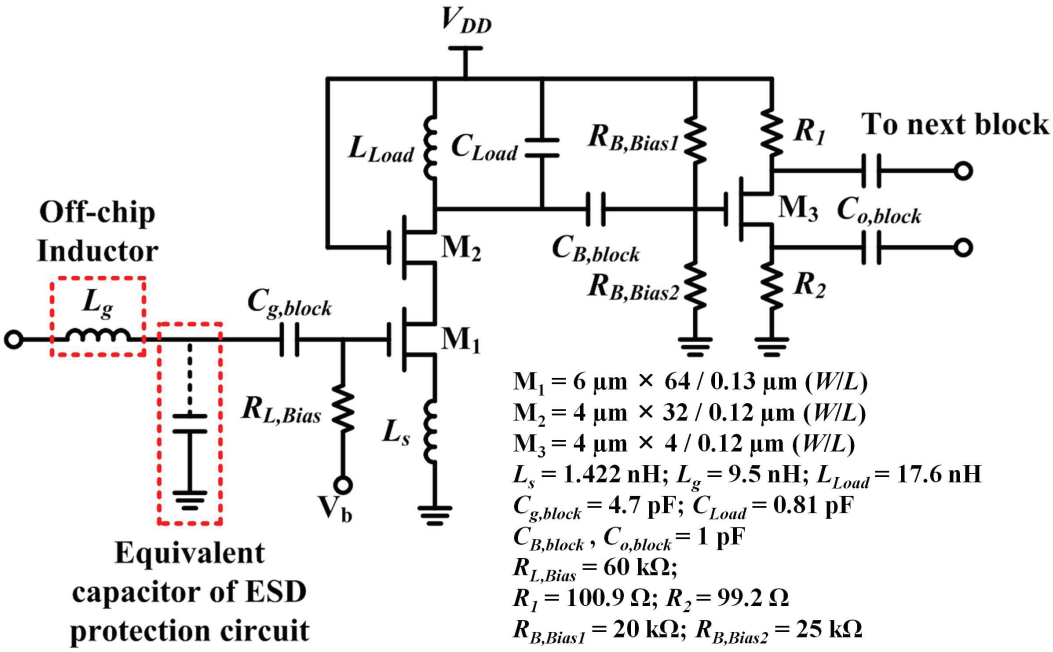


Figure 4.7: Schematic of LNA stage.

4.3.4 LNA Stage Circuit Simulation

The LNA stage in the previous section is designed and verified on Cadence circuit simulation tools. During these steps, a 130-nm CMOS process is used and a 1.2-V supply voltage is commonly employed. To satisfy the above design conditions, the gate inductor (L_g in Fig. 4.3) is required as a huge value inductance. If this inductor is on the chip, it requires a large area. Therefore, in this study, the external inductor (lumped element) is used as L_g. As an off-chip inductor, the Murata inductor (LQW18AN9N5D00) is used. For verification with a practical external inductor in a simulation, the S-parameters of the inductor supplied from the Murata company are used. Using the external inductor can control the LNA input impedance matching condition. Figure 4.7 shows the schematic of the designed LNA stage.

For accurate circuit simulation, physical layout data are important. Figure 4.8 shows the the physical layout of the first-stage device of the LNA. It is comprised of 6 µm × 64 fingers. As mentioned in Chapter 2, multi-fingers can reduce the gate-electrode resistance. There is an equivalent capacitor

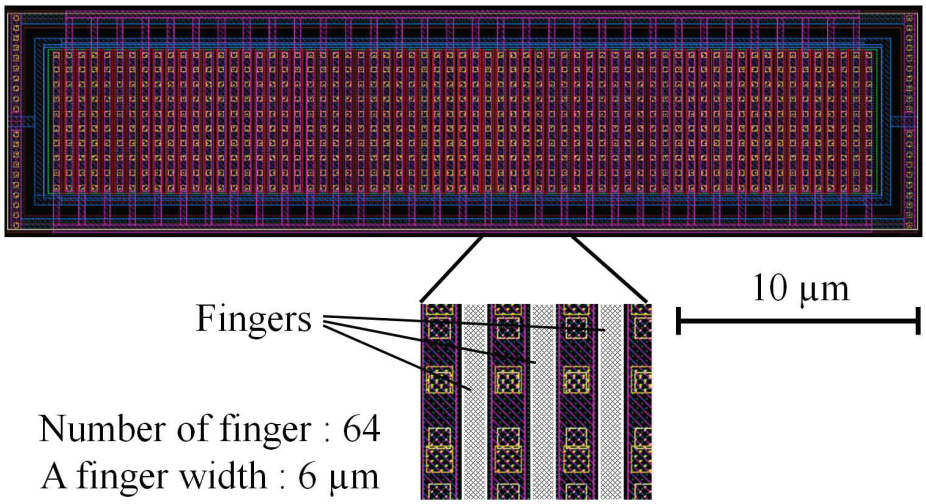


Figure 4.8: LNA input device layout.

for the electric-static-discharge (ESD) protection circuit as well, as shown in Fig. 4.7. The ESD protection circuit is modeled as a double-diode-based circuit. The input bias of the LNA is provided via a resistor ($R_{L,Bias}$). To prevent the effect of the bias-feeding resistor on the input impedance, the value of the resistor is approximately 60 kΩ. It is sufficiently large to ignore. In the small-signal model, it can be ignored, as shown in Fig. 4.4.

For verification of the designed LNA's features, the input reflection coefficient ($|S_{11}|$) and NF are simulated through the circuit simulator (Cadence Spectre). The simulation is performed in post-layout format, including a metal line, ESD protection circuit, and the Murata inductor. For process variation, the normal condition (variation type: Typical NMOS, Typical PMOS (TT), temperature: 17°C) is used. The other conditions, such as SS, FF, and other temperatures, are adapted in the whole system simulation.

Figure 4.9 shows the input reflection coefficient ($|S_{11}|$) and NF. As shown in Fig. 4.9(a), the designed LNA has $|S_{11}|$ less than -10 dB in the desired frequency range. The NF is approximately 1 dB in the target frequency ranges (1.17 $\sim$ 1.6 GHz). These results mean that the input impedance can be accepted for the triple-band signal. Figure 4.10 shows the amplitude and phase of the differential output signals of the designed LNA. Two output signals of the designed LNA stage have an

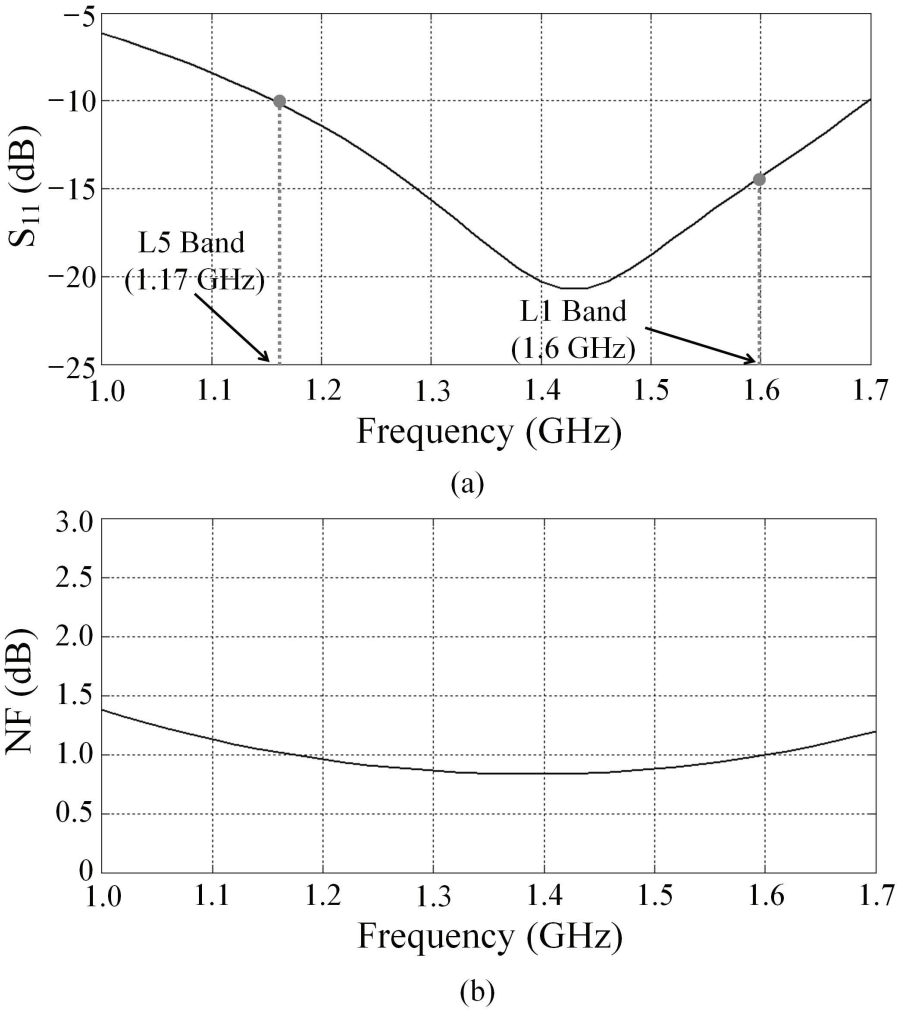


Figure 4.9: (a) Input reflection coefficient ($|S_{11}|$) and (b) NF of LNA.

amplitude error of approximately 0.1 dB in the whole frequency range, and a phase error of 0.4 $\sim$ 0.7° for each one at L1, L2, and L5 band frequencies.

These two signals are fed into the balanced mixer's input. These imbalances of amplitude and phase significantly affect the IQ signals of the mixer's output signals. In short, the imbalanced level of the first-stage output signals is greatly influenced toward the rear-stage. As a result, the

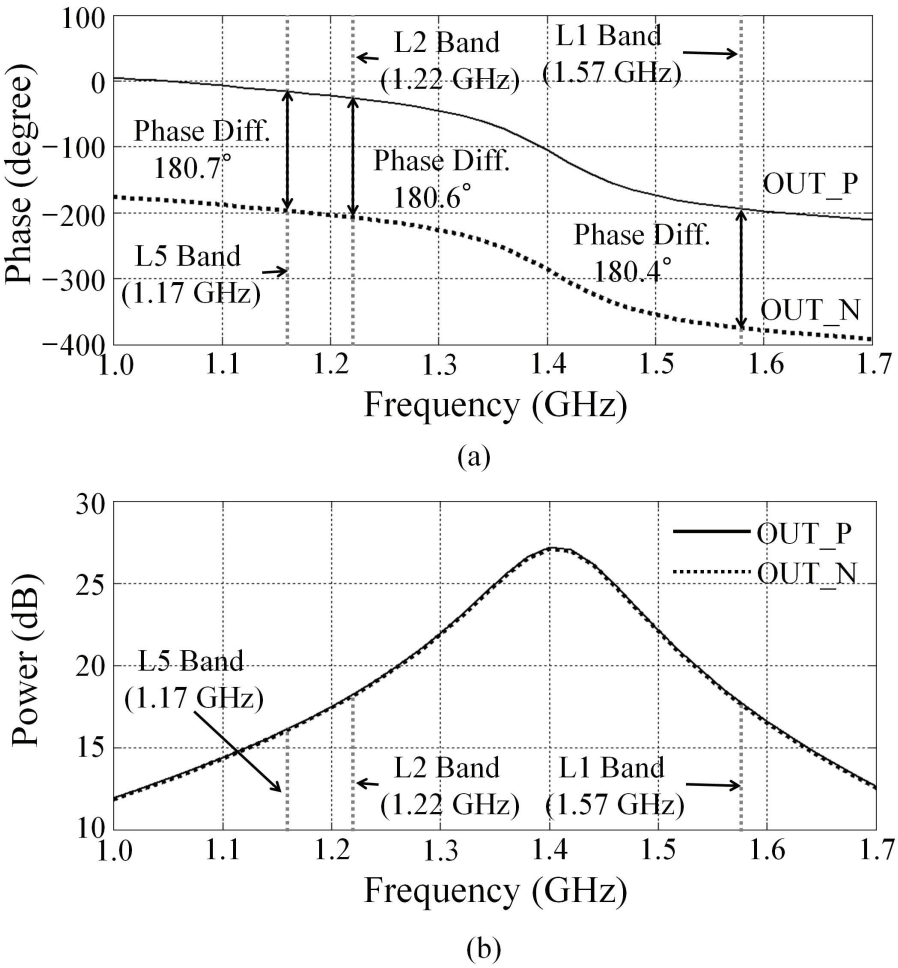


Figure 4.10: (a) Phase and (b) power of LNA's differential outputs.

amplitude and phase errors of these signals greatly affect the whole system IMRR. In this study, the designed balun can generate differential signals with sufficiently small imbalances. From these circuit simulation results, the usability of the designed LNA with an active balun can be confirmed for the triple-band frequency range. The sufficiently low NF and balance of different output signals also satisfy requirements of GPS applications.

4.4 Mixers

4.4.1 Outline of CMOS Doubly-Balanced Mixers

In this study, two types of mixers are used. One is a Gilbert-cell differential mixer [8, 9] for image rejection, high conversion gain and a low NF. The other is a CMOS passive mixer for low power consumption. In the active mixer case, it is located at the next-stage of the LNA as the second-stage of the whole system. Generally, the second-stage NF is not as important as that of the first-stage, as mentioned in previous section. Indeed, the passive mixer as the third-stage has a small effect on the total receiver NF as well. When designing the mixer, the 1 dB compression point (P1dB) and third-order intercept point (IIP3) are considered for linearity. The P1dB point means the input power that causes the gain to decrease by approximately 1 dB from the expected small-signal gain. Normally, the mixer input should be below this point to avoid the gain compression and non-linear gain. The IIP3 means the point of which the third-order inter-modulation distortion signal is expected to be the same as the fundamental one for two-tone signal. It also presents the indicator of linearity. However, the balance of signals is more important in this design [10, 11]. To realize this function, these blocks are designed with a focus on the signal amplitude and phase errors. The whole structure, including devices and the metal line, are laid out symmetrically for signal feeding balance.

4.4.2 Doubly-Balanced Active Mixer

For the second-stage, the doubly-balanced active mixer based on the Gilbert-cell topology is designed. Figure 4.11 shows the designed mixer. Using a doubly-balanced topology, the feed through RF to IF and LO to IF ports can be reduced. Its topology is expected to have high P1dB, IIP3, and impedance. The active mixer can achieve the high conversion gain and drive with low LO signal power compared with the passive mixer. In the target, a single pair of mixers has resistive loads to cover the frequency range of triple-band signal. The active mixer is designed with the parameters shown in Table 4.4.

In the active mixer, all transistors operate in the saturation region to achieve switching-mode mixing [11]. As shown in Fig. 4.11, all biases except the current tail are constructed by resistive voltage dividing. The linearity of the mixer is considered more than in the LNA stage. The degeneration resistor R_{source} in Fig. 4.11 increases the input voltage range which can obtain the linear gain. To

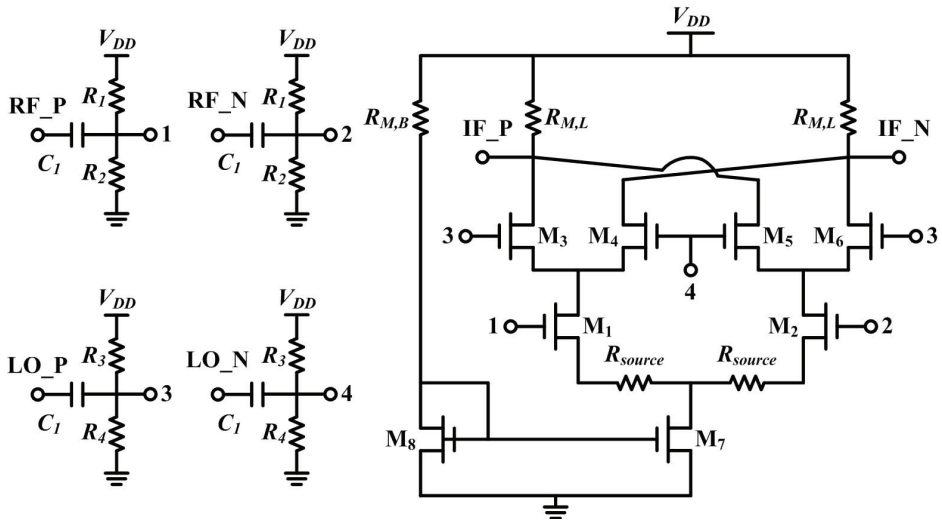


Figure 4.11: Schematic of doubly-balanced active mixer.

Table 4.4: Design parameters for active mixer.

Parameter	Value	Parameter	Value
W/L (M_1, M_2)	4 μm × 32 / 0.12 μm	C_1	0.9 pF
W/L (M_3 to M_6)	4 μm × 16 / 0.12 μm	$R_{M,B}$, $R_{M,L}$	250 Ω , 760 Ω
		R_{source}	10 Ω
W/L (M_7)	5 μm × 64 / 0.18 μm	R_1 , R_2	20 kΩ , 10 kΩ
W/L (M_8)	0.48 μm / 0.12 μm	R_3 , R_4	17 kΩ , 9 kΩ

verify this, the transfer characteristic versus various DC inputs is presented in Fig. 4.12. The slope of the transfer characteristic in this figure means the voltage gain. As R_{source} increases, the input range to obtain stable small-signal gain expands. In other words, the linearity is in a trade-off relation with the conversion gain. In some cases, the reactive degeneration with inductor or capacitor is used to reduce gain degradation and NF. However, in that case, a large chip area is required. In this design, the resistive degeneration is used. The loss is compensated at the interconnecting buffer block between

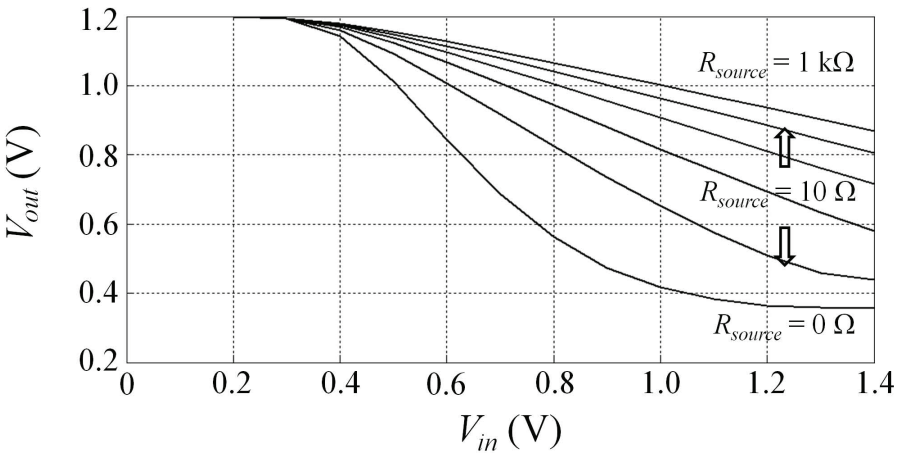


Figure 4.12: DC transfer characteristic of mixer's core device (V_{in} is the voltage of Port 1 and Port 2 in Fig. 4.11. V_{out} is the voltage of Port IF_P and Port IF_N in Fig. 4.11.).

the next-stages.

The conversion gain can be expressed as

$$CG \simeq \frac{2}{\pi} \frac{R_{M,L}}{R_{source} + 1/g_m}, \tag{4.18}$$

where g_m is transconductance of M1 and M2. For sufficient conversion gain, a small R_{source} is needed. In this design, R_{source} is used as a value of 10 Ω.

4.4.2.1 Active Mixer Design

To determine the MOSFET device features in the active mixer, the conversion gain versus the transconductance (g_m) is calculated through Eq. (4.18). The gain of the mixer is proportionally increased to the load impedance ($R_{M,L}$). To calculate the proper values of g_m and $R_{M,L}$, their relation is illustrated in Fig. 4.13. The conversion gain is shown as a power gain. With larger values of g_m and $R_{M,L}$, the conversion gain increases. In the design, to obtain a 10 dB conversion gain, g_m and $R_{M,L}$ are used at approximately 30 mS and 700 Ω. The value of $R_{M,L}$ is set to be greater than that of $1/g_m$ to reduce the device current. The initial current is set to 1 mA.

Under the above specifications, the expected NF can be calculated at the mixer stage. The cascade NF can be calculated as Eq. (4.1). The LNA as the previous-stage of the mixer is expected to have a

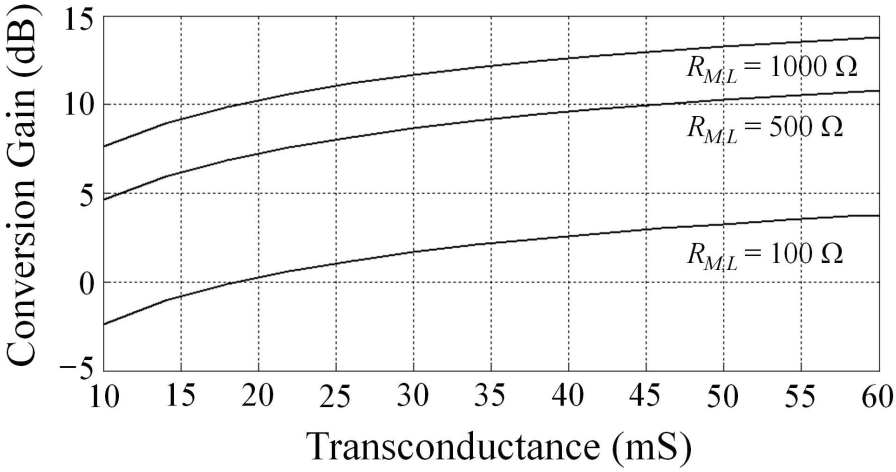


Figure 4.13: Conversion gain against transconductance ($R_{source} = 10\ \Omega$).

gain of approximately 20 dB and a NF of 1.5 dB. In the whole system, a NF less than 7 dB is needed. Thus, the NF of the mixer can be calculated as

$$NF_{Mixer} < G_{LNA}NF_{system} - G_{LNA}NF_{LNA} + 1, \tag{4.19}$$

where NF_{Mixer} is a single-side band NF of mixer, G_{LNA} is a gain of LNA, NF_{system} is a total NF of system, NF_{LNA} is a NF of LNA. From that equation, the mixer NF is expected to be less than 15.7 dB.

With above considerations, the device gate width can be calculated with the minimum gate length of 120 nm. As a normal equation of MOSFET at the saturation region, the device width is calculated as 130 μm. From these conditions, the mixer NF can be verified. If switching MOSFETs ideally work, the NF can be calculated as [13]

$$NF_{Mixer} = 2 + \frac{4\gamma}{g_m R_s} + \frac{\pi^2}{2g_m^2 R_s R_{M,L}}, \tag{4.20}$$

where R_s is the source impedance of the RF port and γ is the drain noise current factor [2, 12]. For simple calculation, R_s is ideally set as 50 Ω. With the input impedance matching, the mixer NF is predicted at approximately 8.5 dB. The NF for the impedance mismatch conditions is checked with the simulation results with device process parameters. The verification of the design is performed

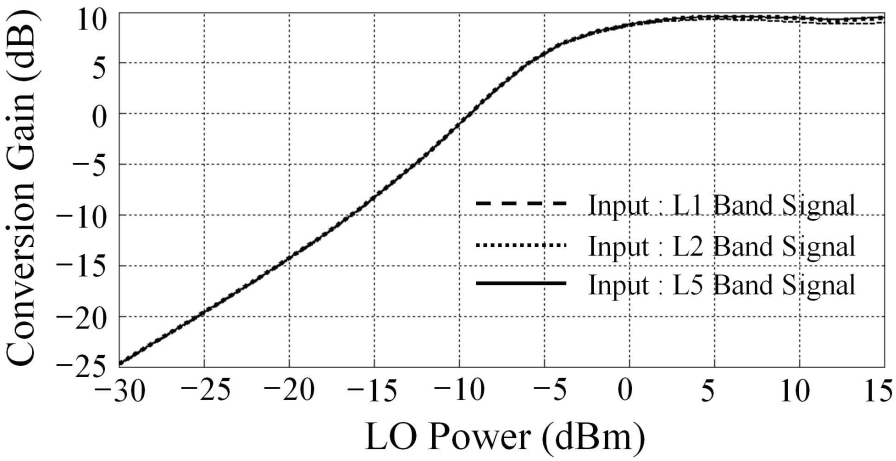


Figure 4.14: Mixer's conversion gain against LO power at triple-band signal.

through a post-layout simulation including metal line. In the layout, as with the LNA, primarily considering the output signal balances, the devices are located as close as possible to each other to minimize the metal line loss. For a pair of long differential metal lines, symmetric structure is used to reduce imbalances of signal loss and phase change.

4.4.2.2 Active Mixer Circuit Simulation

Figure 4.14 shows the conversion gain versus various the LO powers. The input power of the mixer is approximately -67 dBm. The conversion gain is approximately 9 dB with 5 dBm LO power, as shown in Fig. 4.14. This conversion gain begins to saturate to 9 dB for LO power over 5 dBm (50 mV_{pp} swing in this case), indicating switching mode mixing. Thus, all mixer features are then verified with 5 dBm LO power.

In Fig. 4.15, the output signal amplitude and phase versus the input power levels are illustrated. Figure 4.15(a) shows the amplitude of the mixer output signals. The amplitude errors of I, Q, $\overline{\mathrm{I}}$, and $\overline{\mathrm{Q}}$ are under 1 dB. The predicted mixer input power level in a practical case is about -50 dBm. At that point, the amplitude error is shown as 0.5 dB. Figure 4.15(b) shows the phase error of the output signals. The error of the phase for each signal is less than about 0.5°. From the simulation result,

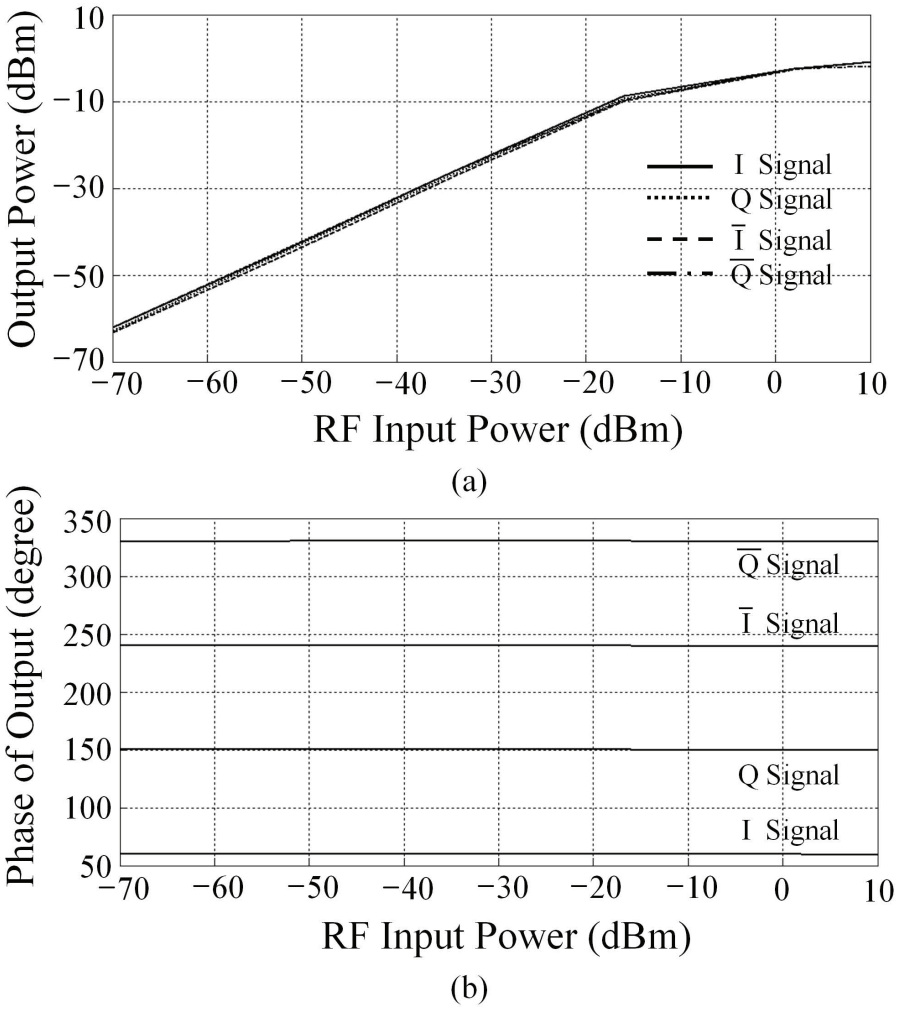


Figure 4.15: (a) Power and (b) phase imbalances of mixer's output signals against input signal (LO power: 5 dBm).

the time delay is approximately 3 $\sim$ 5 ps for L1, L2, and L5 bands of the signal. In the GPS system, normally a 1 ms time error occurs with the 1 m positioning error. Thus, the mixer delay occurs under the 5 nm positioning error. This error is sufficiently small compared with the positioning accuracy. (5 mm even in the static method as described in Chapter 1).

Figure 4.16 shows the P1dB and IIP3 to verify the mixer linearity. As shown in this figure, the

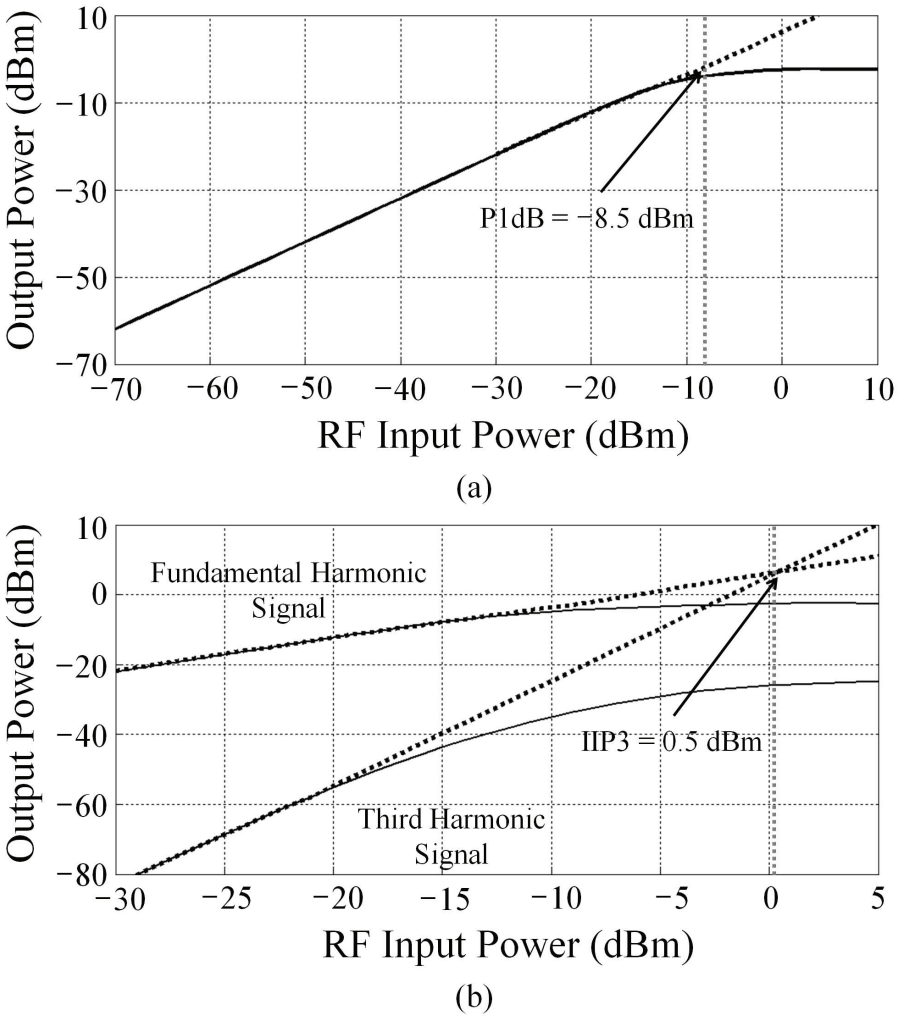


Figure 4.16: (a) P1dB and (b) IIP3 against mixer's input signal level (LO power: 5 dBm).

P1dB and the IIP3 are about −8.5 dBm and about −16 dBm, respectively. The input power level of the mixer is approximately −50 dBm. That signal is located far from these P1dB and IIP3 points. Thus, the designed mixer can obtain sufficient linearity at the least desired power level. The designed mixer has 1.44 mA for the current with a 1.2-V power supply. With the LO power of 5 dBm, the port-to-port isolations are over 50 dB between any ports.

4.4.3 Doubly-Balanced Passive Mixer

The balanced CMOS passive mixer is used as the second-stage mixer. The passive mixer has a conversion loss; however, it has low NF, low power consumption, and high linearity compared with the active mixer. A doubly-balanced topology can have the high isolation between the RF and LO ports compared with a normal single passive mixer. The typical passive mixer structure is the ring-type mixer. The schematic of the designed mixer is illustrated in Fig. 4.17. As shown in the figure, differential LO inputs are inserted into the MOSFET gate. The input and output signals are obtained at the source and drain [14]. As shown in the schematic, there is little voltage between the drain and source due to linear-region operation with small current.

4.4.3.1 Passive Mixer Design

This mixer is basically operated by channel resistance modulation by large LO signals. In the operation region, it is switched between the depletion and inversion regions according to gate voltages. Without enough large LO signals, the conversion loss becomes larger and linearity is degraded [15, 16].

The designed passive mixer consists of four transistors, as shown in Fig. 4.17. M2 and M3 operate with a positive LO signal LO_P, and M1 and M4 operate with a negative LO signal LO_N. MOSFET switching operation according to these complementary LO signals determines which RF signal (RF_P or RF_N) can pass to either output port. When the passive mixer idealy works, the conversion gain is given by

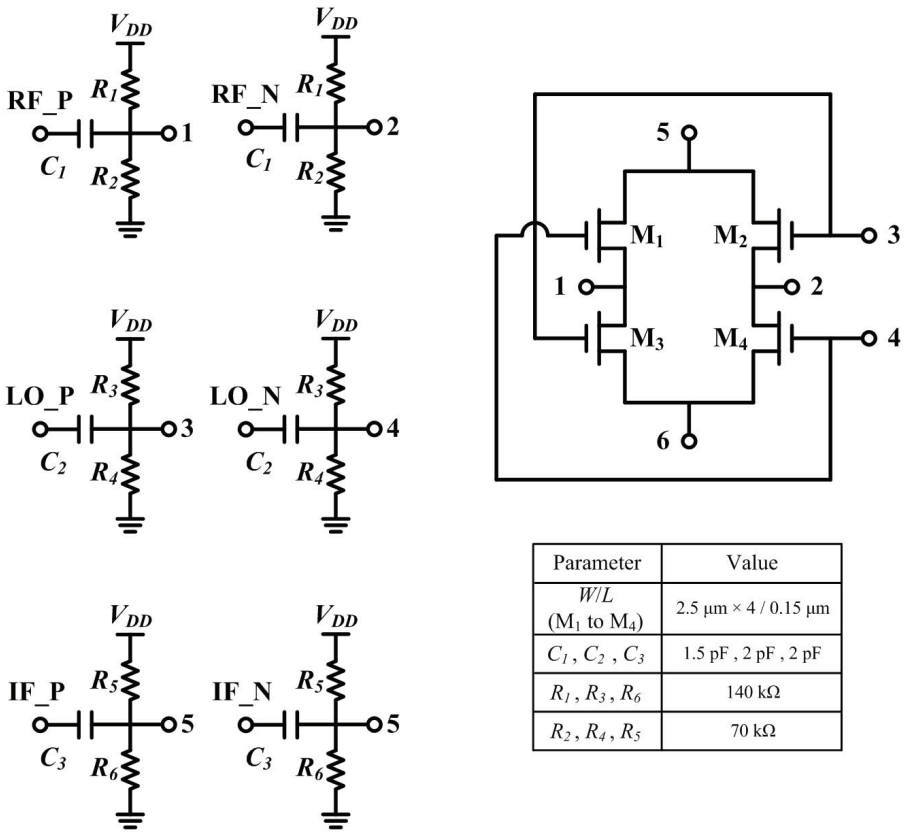
$$CG = \frac{2}{\pi}. \tag{4.21}$$

In the passive circuit, the loss corresponds to the NF. From Eq. (4.21), the conversion gain of the mixer can be calculated as -3.9 dB and the NF is 3.9 dB in the best case.

The practicel conversion gain is limited by drain-source resistance R_{ds} of the turn-on device and parallel parasitic capacitance (C_{gs} and C_{ds}) of the turn-off device [17, 18]. From the MOSFET equation in the linear region, R_{ds} can be expressed as

$$R_{ds} = \frac{L}{\mu C_{ox} W (V_{gs} - V_{th} - V_{ds})}. \tag{4.22}$$

As shown in the equation, R_{ds} is decreased as W and V_{gs} increase. However, a large width leads to high parasitic capacitance, and this degrades the operation characteristic at a high frequency. Instead



Parameter	Value
W/L (M_1 to M_4)	2.5 μm × 4 / 0.15 μm
C_1 , C_2 , C_3	1.5 pF , 2 pF , 2 pF
R_1 , R_3 , R_6	140 kΩ
R_2 , R_4 , R_5	70 kΩ

Figure 4.17: Schematic of doubly-balanced passive mixer.

of increasing the device width, a large LO signal is useful, which enhances V_{gs} in turn-on MOSFET to reduce R_{ds}. In this design, the LO signal power is limited by the quadrature LO generating balun. Considering this limitation, the DC bias is also used at each node in the passive mixer, as shown in Fig. 4.17.

4.4.3.2 Passive Mixer Circuit Simulation

The features of the designed mixer are verified through the simulation. As with the previous block cases, it is performed as a post-layout simulation including layout parasitic effects. Figure 4.18 shows the conversion gain versus the LO signal power. The conversion gain is under -5 dB. Thus,

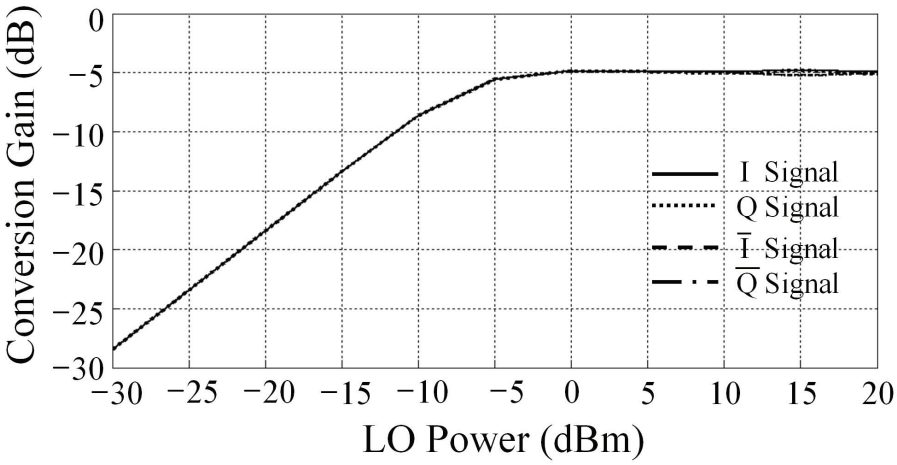


Figure 4.18: Conversion gain of passive mixer against LO power.

the second mixer NF is under 5 dB as well.

P1dB and IIP3 are used to verify the linearity as shown in Fig. 4.19. The P1dB point and the IIP3 point are 5 dBm and 8 dBm. When considering the input power level, these linearity factors are sufficiently large; therefore, they cannot influence system characteristics.

Figure 4.20 shows the amplitude and phase of the mixer outputs against input signal power. The input power of the second mixer from the previous-stage is about $-55 \sim -50$ dBm. At that input power, the output power is about $-60 \sim -55$ dBm. To show the amplitude balances of the signals, the output IQ signals (I, Q, $\overline{\mathrm{I}}$, $\overline{\mathrm{Q}}$) are presented. When the LO signal power is less than 5 dBm, the amplitude error is approximately 0.2 dB. However, when the LO signal power is increased over 5 dBm, the errors occur at about 1 dB in the worst case. In this work, the LO signal power is chosen as 5 dBm. In the case of the phase, when the input power is greater than -10 dBm, the phase error occurs at about $1 \sim 2°$. However, at the target input power level (approximately -55 dBm), the phase imbalance is about $0.2 \sim 0.3°$. As this affects the amplitude and phase imbalance to the IMRR, these errors can be reasonable.

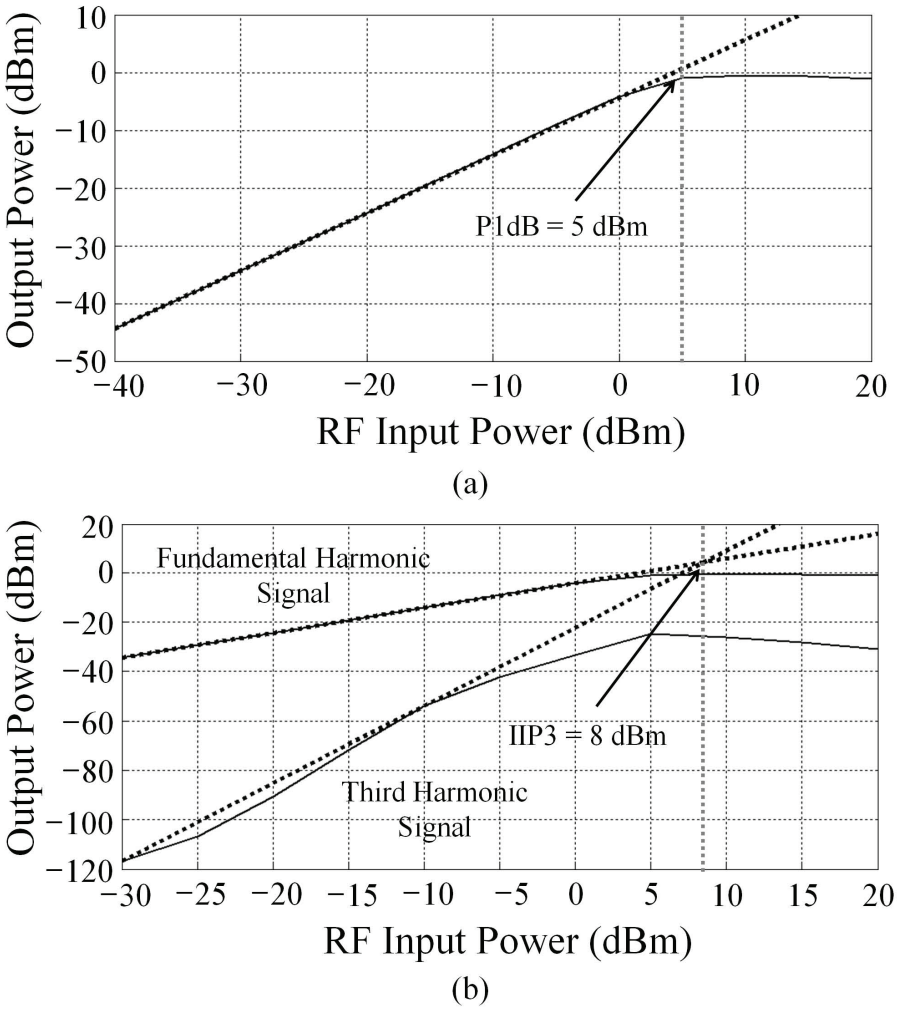


Figure 4.19: (a) P1dB and (b) IIP3 against passive mixer's input signal level (LO power: 0 dBm).

4.5 PPF

4.5.1 Outline of PPF and IQ Generator

In this study, to separate the triple-band signal, phase translation of signals is used. The numbers of the target signals separated is not two, but three. Compared with the conventional dual-band structures, a proper phase translation that rejects more undesired signals is required. The PPF following

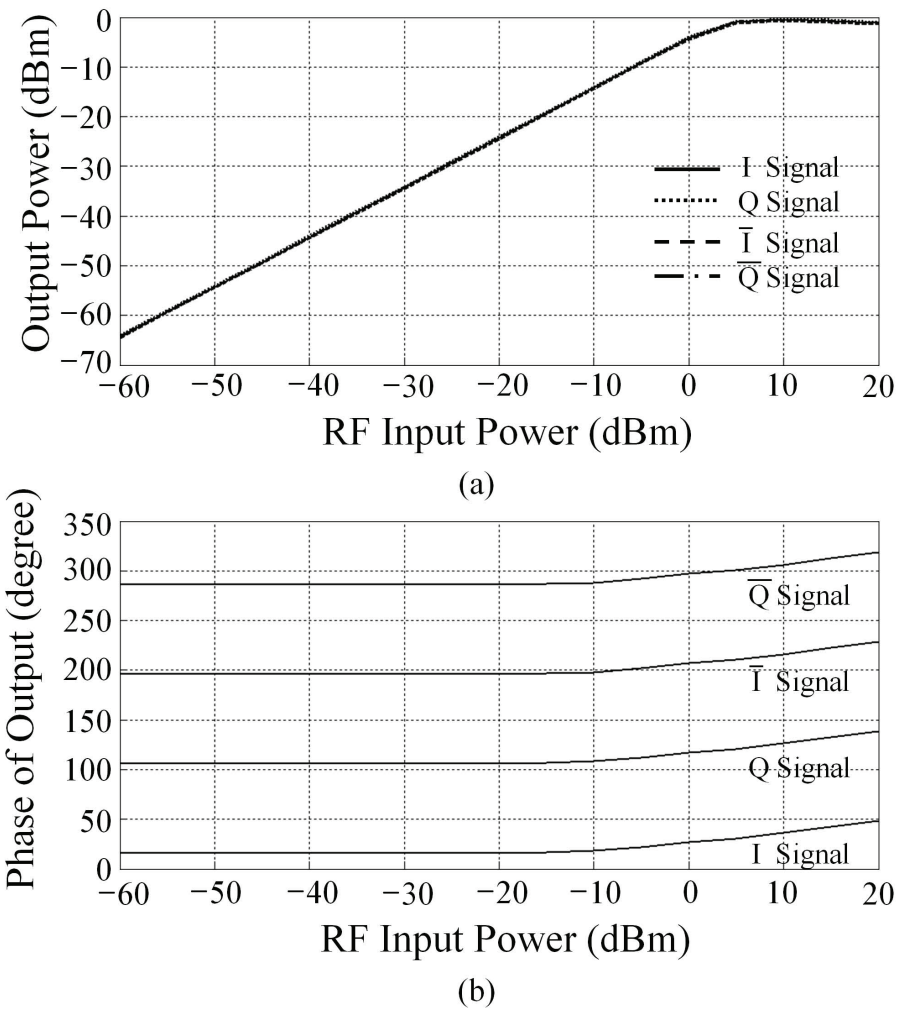


Figure 4.20: (a) Amplitude and (b) phase of passive mixer's outputs against input signal level (LO power: 0 dBm).

mixers, and the adder, which adds and subtracts PPF output signals to remove undesired signals, are used. To achieve these advancements with a good signal balance, the frequency translator, circuits are designed as balanced structures.

For operation of these circuits, the IQ signal generator is required to generate the two differential signals with a different phase for each other as much as 90°. Using an external signal source has many

factors causing errors, such as the difference of signal feeding wirings, impedance mismatching at the input port (a general signal source has a 50 Ω internal impedance), etc. Thus, it is hard to generate IQ signals without errors of amplitude and phase. In this study, the balun (balanced and unbalanced) and PPF for internal IQ signal generation on chip are therefore designed.

4.5.2 Single and Two-stage PPFs for IQ Generator

In this work, one of the most important points is two times of image signal rejection through phase translation with a Weaver structure. To achieve this, RC PPFs are designed as a phase translator. A basic PPF was developed for generation quadrature signals by Gingell [19] in the 1970s. However, with the early PPFs, there were many problems, such as process variation and component mismatching. An advanced RF CMOS process realized the practical implementation of PPF [20]. In Fig. 4.21, the single-stage PPF is shown. It is composed of individual elements of four resistors and four capacitors. With differential input, it generates four outputs which have 90° phase difference to each other. In practical case, multi-stage cascaded connection of PPFs is used to cover required frequency range even with process variation [11, 21]. However, due to the passive components of the PPF, a 3 dB amplitude loss occurs per stage. The resistive components generate thermal noise and it degrades the system NF. In this study, considering impedance matching with the previous-stage output impedance and the next-stage input impedance to maximize the power delivery, resistance and capacitance values are controlled.

For the input-stage structure, the phase and amplitude balances are focused. In Fig. 4.21, these two type of PPF are illustrated. Figure 4.21 shows a balanced input signal type and a single input signal type. The balanced input signal type PPF outputs as follows.

$$\begin{aligned} V_{O1} - V_{O3} &= \frac{1}{1 + j\omega R_1 C_1} \cdot (V_{IN_P} - V_{IN_N}), \\ V_{O2} - V_{O4} &= \frac{j\omega R_1 C_1}{1 + j\omega R_1 C_1} \cdot (V_{IN_P} - V_{IN_N}), \end{aligned} \tag{4.23}$$

where ω is an angular operation frequency.

The single input type PPF shown in Fig. 4.21(b) outputs as

$$\begin{aligned} V_{O1} - V_{O3} &= (V_{IN_P} - V_{IN_N}), \\ V_{O2} - V_{O4} &= \frac{1 - j\omega R_1 C_1}{1 + j\omega R_1 C_1} \cdot (V_{IN_P} - V_{IN_N}). \end{aligned} \tag{4.24}$$

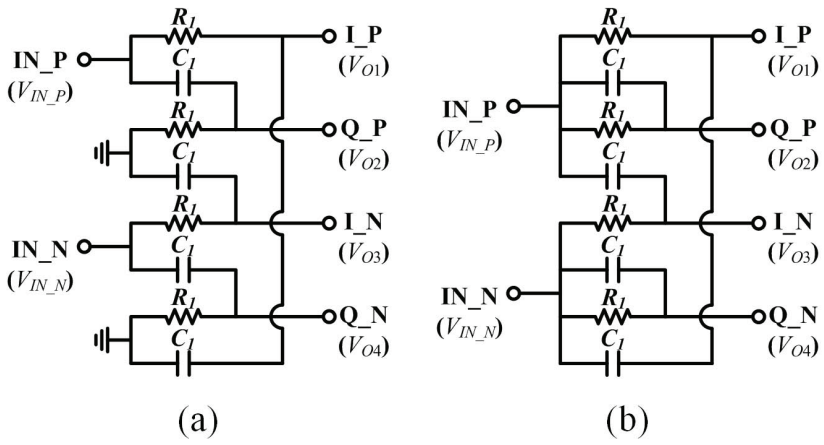
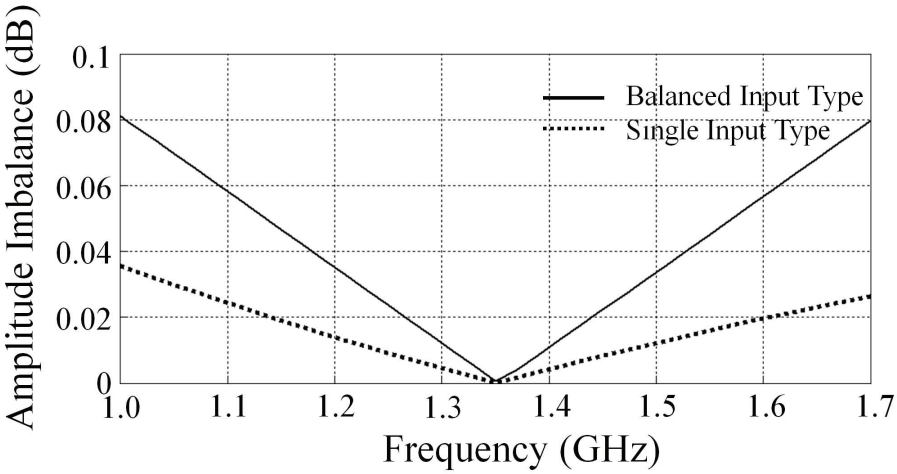


Figure 4.21: A single-stage PPF of (a) balanced and (b) single input type.

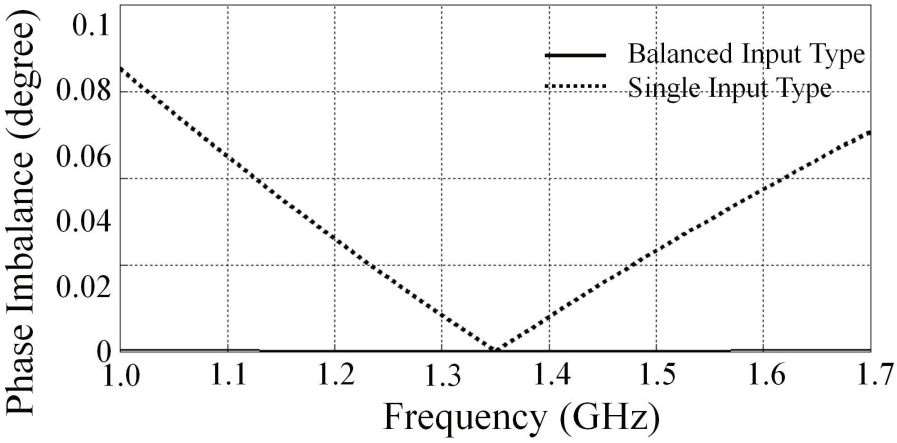
As shown in Eqs. (4.23), if the value of R_1C_1 is far from $1/\omega$, the amplitude error increases; but, the I and Q phases differ by as much as 90°. On the other hand, the PPF in Fig. 4.21(b) has little amplitude error even for the value of ωR_1C_1 far from unity, but it can cause phase error according to ωR_1C_1. Thus, depending on the importance of amplitude and phase balances, the poly-phase input-stage type can be chosen.

The change of frequency features according to input-stage types is verified by circuitry simulations. Figure 4.22(a) shows the amplitude imbalances according to the input-stage types. As shown in Eqs. (4.23) and (4.24), the the single input type has amplitude error less than that of the balanced input type. However, as shown in Fig. 4.22(b), the balanced input type has less phase imbalance than the single input type. The allowed phase and amplitude imbalances are under 0.05° and under 0.03 dB in the target frequency range in this work. Among these errors, the amplitude error has more influence than the phase error. Furthermore, the phase error can be compensated through a compensation technique mentioned in Chapter 3. Thus, in this study, the single input type, which can reduce the amplitude imbalance, is used as the input-stage type.

The two-stage PPF shown in Fig. 4.23 has a wider frequency characteristic than the single-stage PPF. Among the PPFs used in the proposed architecture, the part used at the IQ generator for the LO1 signal is the most sensitive because the operation frequency is 1.4 GHz. Thus, the operation feature



(a)



(b)

Figure 4.22: The output imbalance simulation results of a single-stage PPF for (a) amplitude and (B) phase according to input-stage type.

is verified at this frequency, as shown in Fig. 4.24. The parameter values with a center frequency of the PPF at the operation frequency are calculated as follows: R_1 and R_2 are 130 and 96 Ω, C_1 and C_2 are 1 pF.

Figure 4.25 shows the IMRR of the first mixer output with the IQ generator composed with the

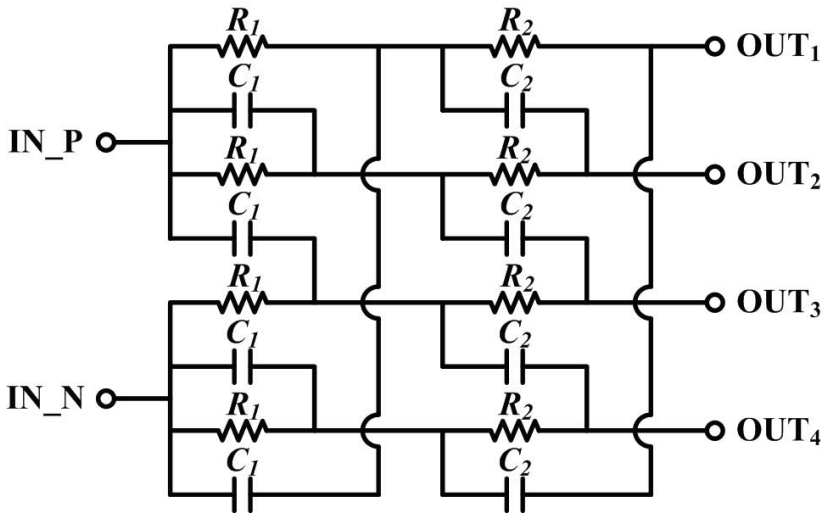


Figure 4.23: The two-stage PPF schematic based on single input type.

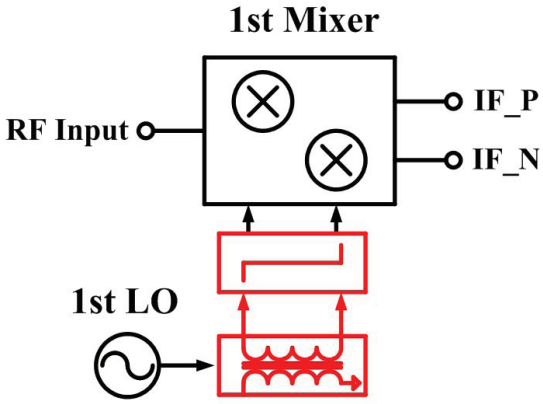


Figure 4.24: First mixer with IQ generator composed two-stage PPF and balun.

two-stage PPF and balun. The dotted line denotes the results with the single-stage PPF; the solid line represents the results with the two-stage PPF. Although the maximum IMRR with the single-stage PPF is higher than that with the two-stage PPF, the frequency operation range of the two-stage PPF is wider than that of the single-stage PPF.

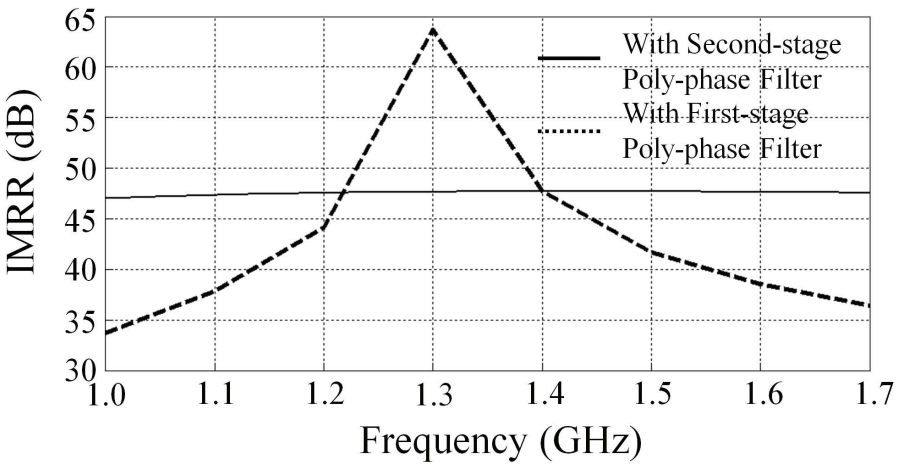


Figure 4.25: IMRR of first mixer with IQ generator composed two-stage PPF and balun.

Amplitude and phase balances are verified as well. Figure 4.26 shows the amplitude and phase errors of the PPF output. The component values are re-calculated with the post-layout circuit simulation including layout features. From the results, the amplitude errors are under 0.1 dB and the phase errors are under 0.01° at the target frequency. The values of resistors and capacitors in Fig. 4.23 are modified a little by considering parasitic elements based on metal line.

4.5.3 Influence of PPFs Load on IMRR

Differently from the PPF used in the IQ generator, the first PPF, which is located between the first and second mixers, must be carefully handled with some points. It is connected to the resistive adders for signal phase translation to realize image rejection. The process mismatch causes the output signal balance degrading IMRR. To avoid the load impedance effect, the adder's resistance is much larger than that of the PPF. In the design, the adder resistance is over 1 kΩ. There still remains the mismatch of the adder's large resistance.

For simplification, the single-stage PPF shown in Fig. 4.27(a) is considered with the mismatch in the resistive adders ($\Delta R_{o,p}$, $\Delta R_{o,n}$). Using the equivalent circuit in Fig. 4.27(b) to obtain V_k (k= 1,

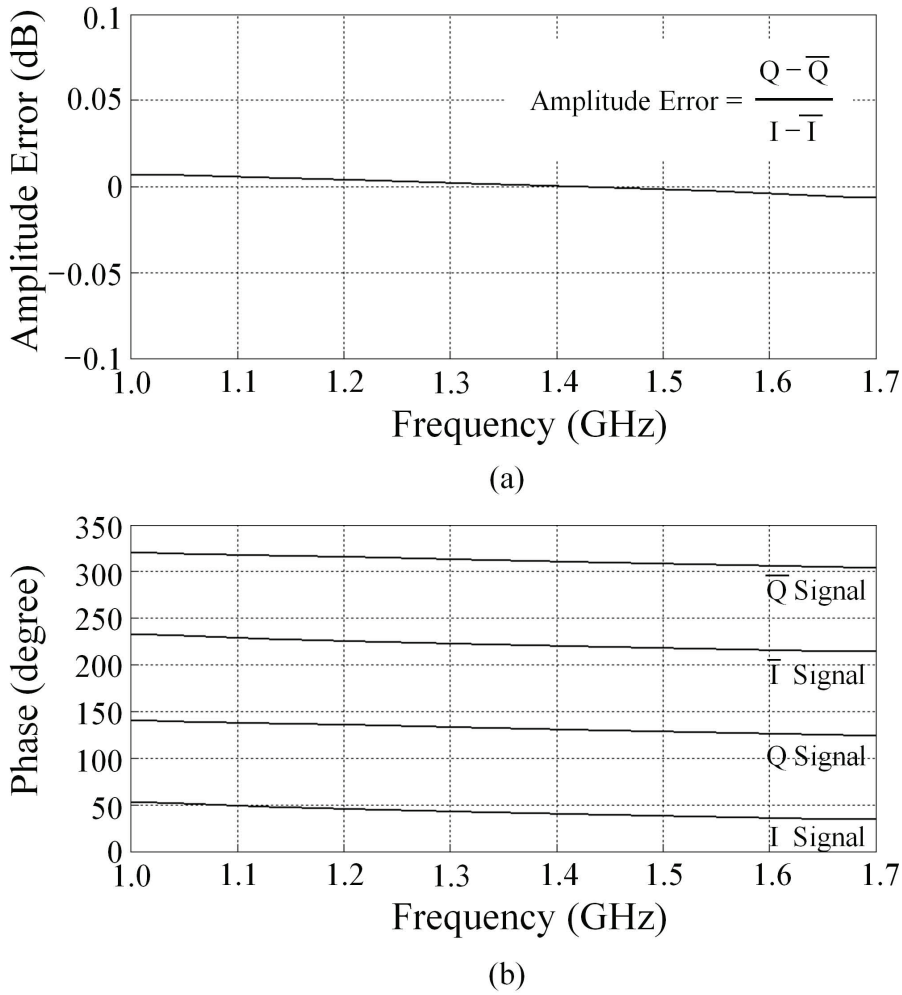


Figure 4.26: (a) Amplitude and (b) phase balance of two-stage PPF's output signals.

2, 3, 4), $V_{out,p}/V_{in}$ is calculated as

$$\begin{aligned}\frac{V_{out,p}}{V_{in}} &= \frac{1+\omega CR}{1+j\omega CR}\frac{(1+j)(Z_{ppf}+R_{o,p})+\Delta R_{o,p}}{2(Z_{ppf}+R_{o,p})+\Delta R_{o,p}} \\ &\approx \frac{1+j}{2}\frac{1+\omega CR}{1+j\omega CR}\left(1-\frac{j}{2}\frac{\Delta R_{o,p}}{Z_{ppf}+R_{o,p}}\right). \end{aligned} \tag{4.25}$$

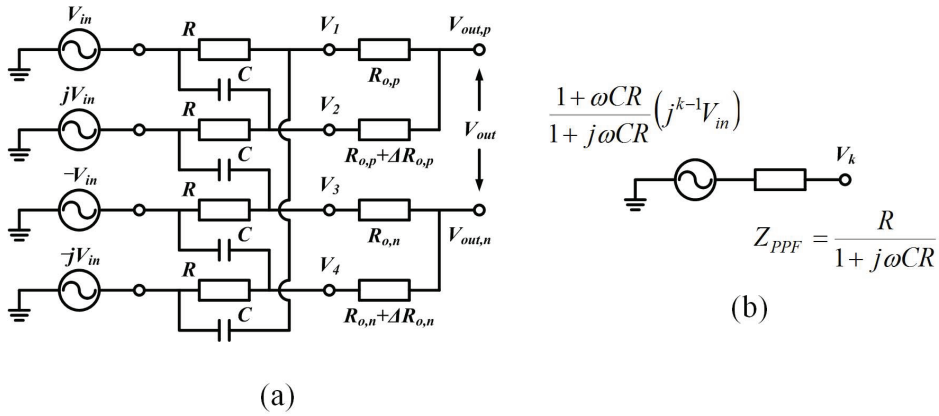


Figure 4.27: (a) Simple PPF with resistive adder and (b) equivalent circuit to calculate V_k (k = 1, 2, 3, 4).

As $V_{out,n}$ can be calculated similarly, V_{out}/V_{in} is expressed as follows.

$$\frac{V_{out}}{V_{in}} \approx \frac{1+j}{2}\frac{1+\omega CR}{1+j\omega CR}\left[1-\frac{j}{2}\left(\frac{\Delta R_{o,p}}{Z_{ppf}+R_{o,p}}+\frac{\Delta R_{o,n}}{Z_{ppf}+R_{o,n}}\right)\right]. \tag{4.26}$$

The factor $1+\omega CR$ represents image rejection, and it is not influenced by a mismatch in the resistive adders.

The components for the first PPF are used as follows. R_1 and R_2 are 160 Ω and 217 Ω, C_1 and C_2 are 9.5 pF for the operation frequency from 170 $\sim$ 230 MHz. In the second PPF, R_1 and R_2 are 210 Ω and 260 Ω, C_1 and C_2 are 12.5 pF for the operation frequency from 20 $\sim$ 30 MHz. Both cases have an amplitude error of less than 0.1 dB and phase errors of 0.01°. The circuit simulation results, including load effect, will be shown for the system IMRR in the next chapter.

4.6 Passive Components Consideration and Layout

4.6.1 On-chip Passive Components

Some characteristics of on-chip passive components influence performance of circuits using them. In this subsection, some considerations for them are explained.

A. Inductor

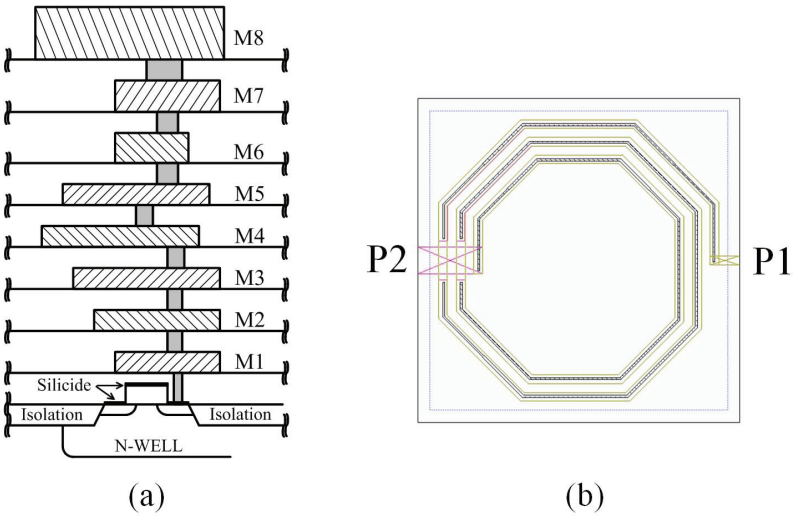


Figure 4.28: (a) Cross-section of used process and (b) layout structure of used inductor.

The inductor occupies the large area and it is very sensitive to parasitics of metal lines. In the design step, the inductor model with connecting metal is used. The 130-nm CMOS process used in this work has three thin metals, two thick metals, and three RF-use thick metals, as illustrated in Fig. 4.28(a). Figure 4.28(b) shows layout example of an inductor. As shown in the figure, it has the structure of a dual-layer parallel stacked spiral. The core part of the inductor is composed of top two metal layers (M7 and M8) to reduce parasitic resistance. Accordingly, a higher quality factor (the Q-factor) can be achieved.

The Q-factor can be calculated as

$$\text{Q-factor} = \frac{\text{Energy}_{\text{stored}}}{\text{Average Power}_{\text{Dissipated}}} = \frac{\omega L}{R_{s,L}}, \tag{4.27}$$

where L is a pure inductance and $R_{s,L}$ is the series resistance of the inductor. It means the energy loss relative to the amount of energy stored in some elements. As a higher Q-factor, the energy loss decreases.

Figure 4.29 represents the Q-factor and inductance values of the inductor used in the design, including metal line parasitics. These values are calculated through circuit simulation. Figure 4.29(a) shows the Q-factor of L_s and L_{Load} in Fig. 4.3. This Q-factor of L_s are approximately 11 $\sim$ 13, and

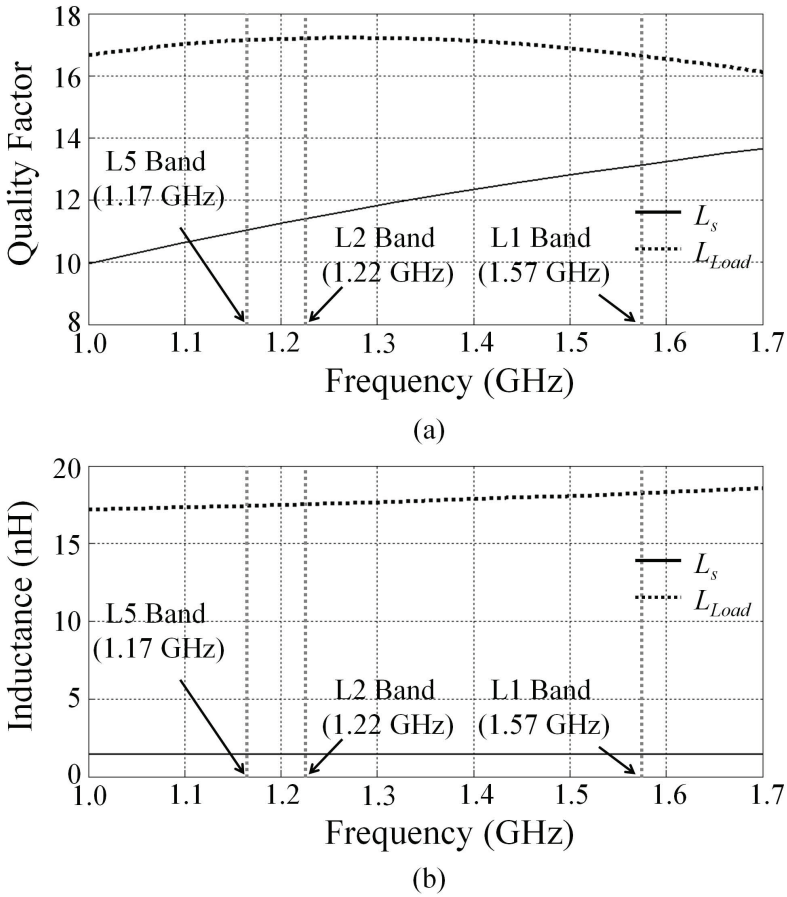


Figure 4.29: (a) Q-factor and (b) inductance including layout condition of used inductor.

L_{Load} are about 17 in the target frequency ranges. The inductance values of L_s are approximately the same as 1.45 nH and of L_{Load} are 17.4 $\sim$ 18.2 nH at L1, L2, and L5 band frequencies. The inductor values are almost constant to satisfy the input impedance matching condition in the target frequency range. The Q-factor of the L_{Load} is adequate value for triple-band application in this study without using additional series resistor [4].

In this study, the external inductor (Murata LQW18AN9N5D00 [1]) is used to satisfy the LNA input condition. As a reference, the Q-factor and inductance of the external inductor used in the designed circuit are illustrated in Fig. 4.30. These Q-factors are 80 $\sim$ 105 and the inductances are

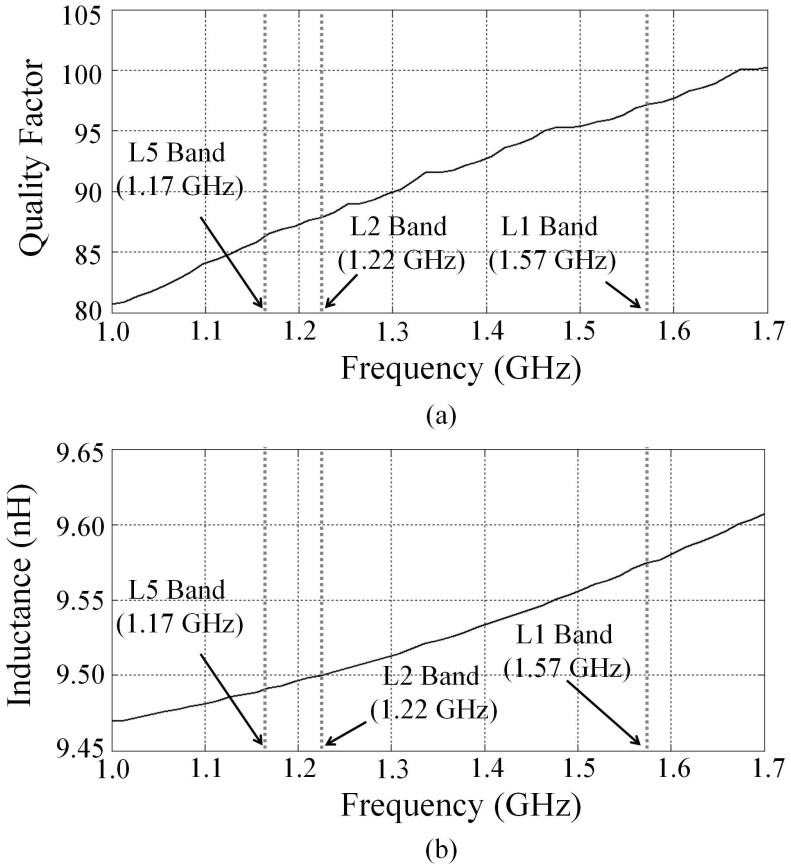


Figure 4.30: (a) Q-factor and (b) inductance of Murata inductor for simulation of lumped elements.

9.5 $\sim$ 9.6 nH during the target frequency ranges.

B. Capacitor

The metal-insulator-metal (MIM) capacitor is used, as illustrated in Fig. 4.31(a). The MIM capacitor is composed of M6 to M7 layers with the thin metal (M5 layer) in the eight level metal process shown in Fig. 4.28(a). Figure 4.31(b) shows the layout structure of that capacitor. The MIM structure needs a large size, but it guarantees high-accuracy.

The variation of the Q-factor according to the width and length of the MIM capacitor should be

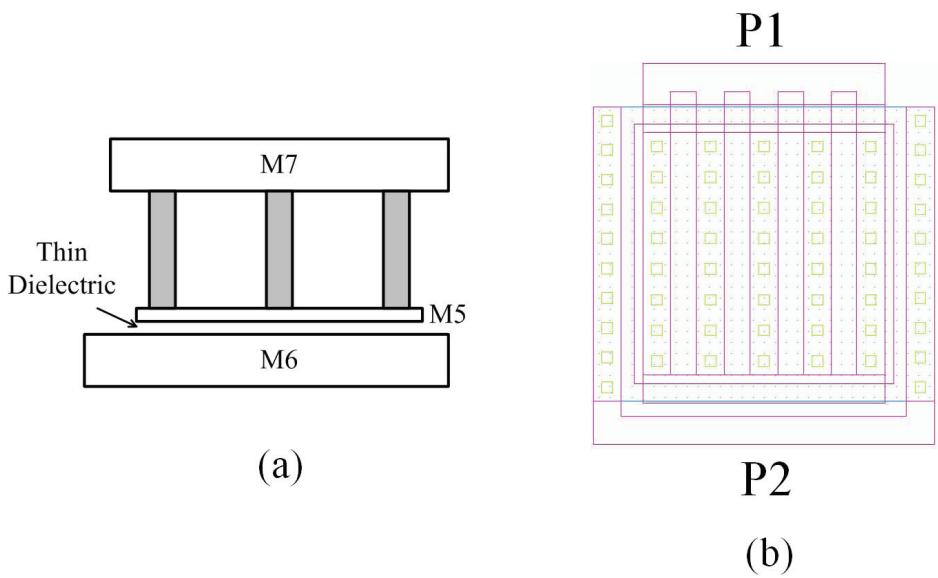


Figure 4.31: (a) Structure and (b) layout component of MIM capacitor.

considered. In the same way as the previous inductor case, the loss is generated within the elements. Although the number of vias for port P1 does not depend on the length and the width, that for the port P2 is influenced by them, as shown in Fig. 4.32. Figure 4.33 shows the MIM capacitor Q-factor and capacitance. Although capacitance values little change, the Q-factors have greater values with a larger width. In short, the type shown in Fig. 4.32(a) has a smaller parasitic resistance than the type shown in Fig. 4.32(b). From those results, the proper type of capacitor can be used in the design.

C. Resistor

A un-silicided poly-silicon resistor is used in this work. Sheet resistance of this resistor is 340 Ω per unit dimension, and it has a ±15 % tolerance. It has small sensitivity to temperature and voltage variation. It has a high sheet resistance, which is useful for small occupied area and small parasitic capacitance to the substrate.

D. Pad

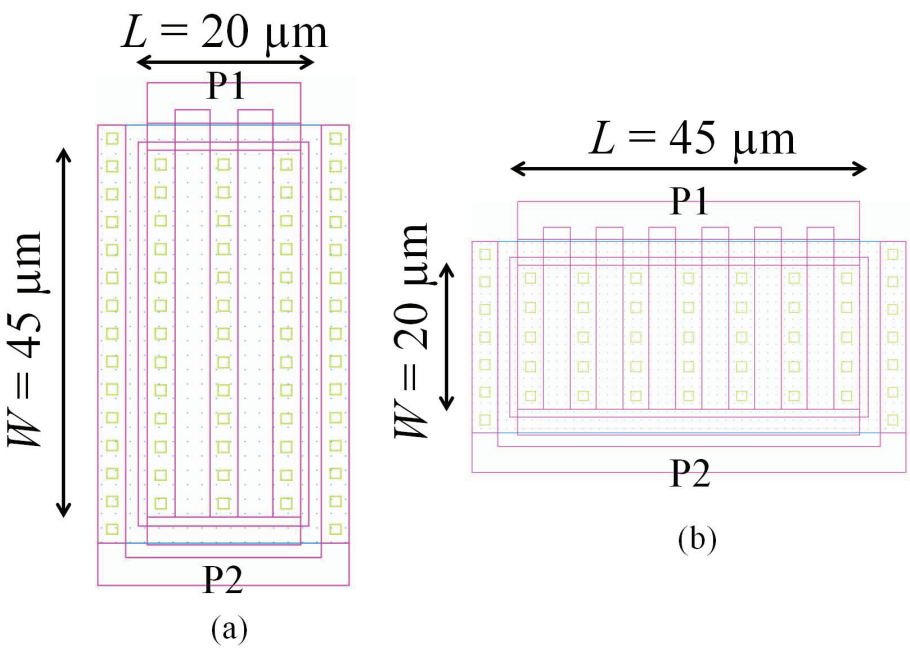


Figure 4.32: Differential length and width size ((a) 20 μm × 45 μm and (b) 45 μm × 20 μm) of same value's MIM capacitor.

The RF pad illustrated in Fig. 4.34 is used. By eliminating M2 to M7 layers, parasitic capacitance is reduced. The parasitic resistances for input/output signals are reduced by ground shielding with M1 metal, as shown in Fig. 4.34. The M1 ground metal is connected to the p-type substrate with a lot of vias (parasitic resistance $\sim$ mΩ) to stabilize the substrate bias.

4.6.2 Layout of RF Front-end Architecture

In Fig. 4.35, the designed layout is illustrated. A is an LNA core, and B and C are an inductor of the source and load of LNA, respectively. D is a first mixer, E is a second mixer, and F and G are first and second PPFs. H and I are IQ generators for LO1 and LO2, respectively. All blocks are symetrically arranged.

For the signal line, the high frequency line and long signal line has a structure similar to a coplanar waveguide (CPW) structure. Figure 4.36(a) shows a part of these signal lines. As shown, the signal

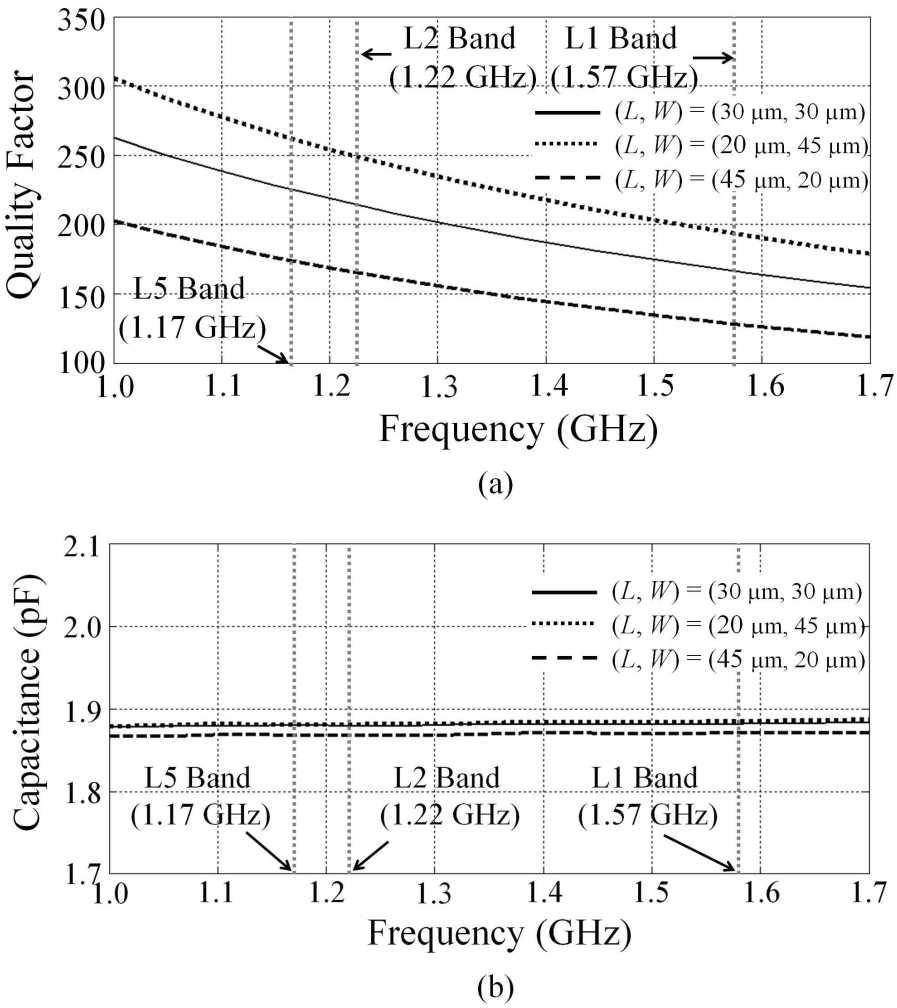


Figure 4.33: (a) Q-factor and (b) capacitance of MIM capacitor.

line is covered with a ground line. This CPW structure can maintain the signal phase features and protect them from the jitter signal of the ground path more than a single signal line. To maintain the ground line as a reference voltage line, the large-size substrate lines are located at several parts around the signal feeding.

Figure 4.37(a) shows the layout of inductor. To isolate the signal line from the ground plane, a

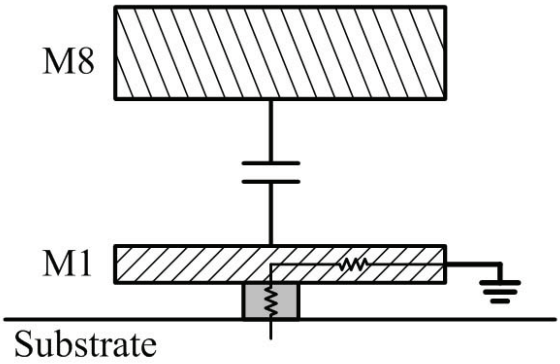


Figure 4.34: Cross-section of pad with ground and substrate plane.

safety place is located outside the inductor. The guard line is used around the inductor. This part helps with isolation from the substrate.

In Fig. 4.36(b), the LNA core MOSFET is shown. The signal feeding line into the gate is drawn as a covering whole gate dimension. The both-side gate connection is used to reduce gate-electrode resistance. Thus, when using various gate fingers, the signal feeding delay can be matched. Figure 4.37(b) shows the PPF. The capacitor occupies large area. The structure of the capacitor is symmetrically configured. In the capacitor case, as mentioned earlier, the width is smaller than the length for lower parasitic resistance.

4.7 Post-layout Circuit Simulation of RF Front-end Architecture

To verify the RF front-end architecture characteristic, it is assumed that a low-pass filter (LPF) and an ADC after the second PPF output are used. The LPF has a 40 MHz cutoff frequency and the ADC is assumed to be of Analog Devices AD9639 (4-channel, 12-bit). With this assumption, the architecture is simulated with the Cadence Specter with process variation.

Figure 4.38 shows the voltage level at each block. For this simulation, the input power at the LNA is -75 dBm through the active antenna of a 35 dB gain. The ADC requires an input voltage level greater than 342 μm, which becomes the second PPF's minimum output voltage level. Based on the simulation results, in the worst case (variation type: Slow NMOS, Slow PMOS (SS)), the minimum

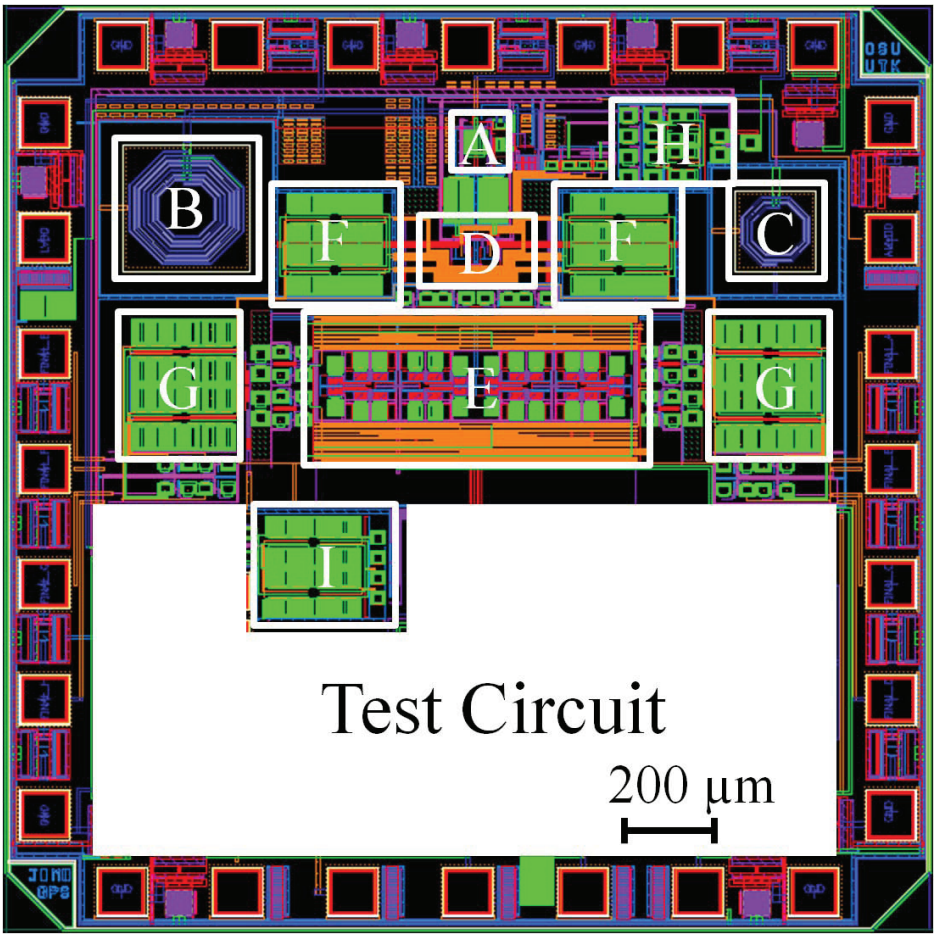


Figure 4.35: Designed layout of RF front-end architecture for triple-band signal.

condition is satisfied. Table 4.5 shows the NF and IMRR at each port with Monte-Carlo simulation (1000 trials). In the simulation, the NF is approximately 7 dB, and the IMRR is 38 $\sim$ 42 dB.

4.8 Conclusion

The RF front-end architecture is comprised of the LNA, active and passive mixers, PPF, and IQ generator. After layout of these blocks, the proposed architecture was verified through post-layout circuit simulations. The required input voltage level of the ADC (AD9639, 4-channel, 12-bit, which

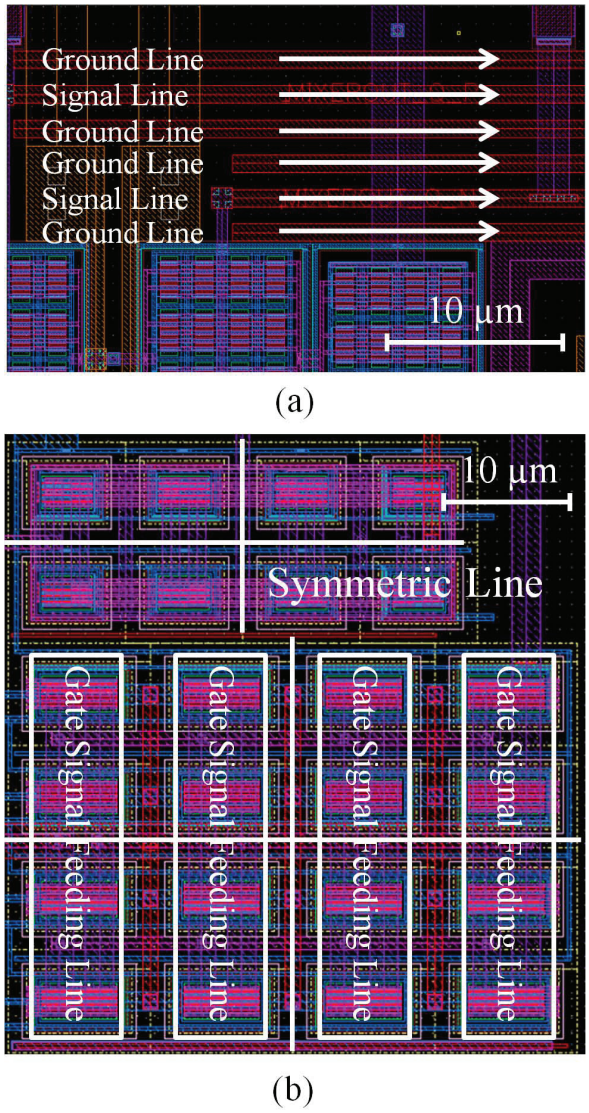


Figure 4.36: Layout issue point as (a) signal line and (b) MOSFET array.

is detailed in Chapter 5) was confirmed even for the worst case of process variation. With 1,000 times of the Monte Carlo simulation, the NF and IMRR are verified as approximately 7 dB and 38 $\sim$ 42 dB. From these simulation results, the proposed architecture could receive the triple-band GPS

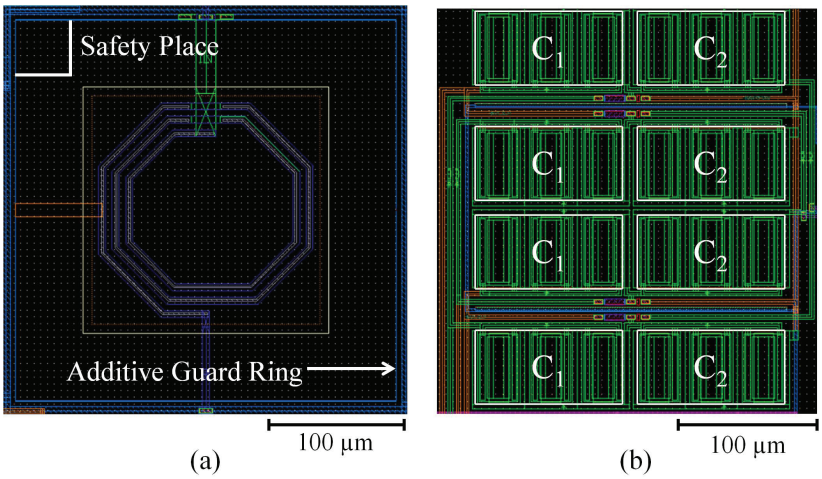


Figure 4.37: Layout issue point as (a) inductor (1.45 nH) and (b) PPF with capacitor array ($C_1 = C_2 = 1$ pF in Fig. 4.23).

Table 4.5: NF and IMRR results with post-layout circuit simulation (Monte-Carlo, 1000 trials).

Input Power	– 75 dBm		
LO1 Power	5 dBm		
LO2 Power	0 dBm		
NF	L1 Band Signal	L2 Band Signal	L5 Band Signal
	6.9 dB	6.8 dB	7.0 dB
IMRR	At L1 Port	At L2 Port	At L5 Port
	41 dB	39 dB	38 dB

signal.

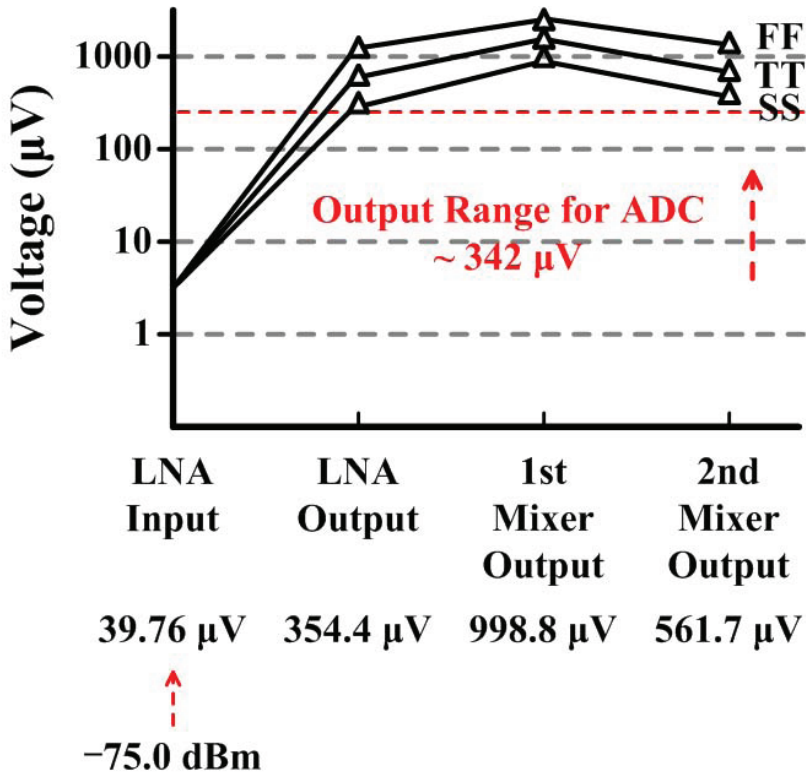


Figure 4.38: Process variation simulation results of RF front-end output voltage level at each block.

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Chapter 5

Experimental Results and Discussion of Triple-band RF Front-end Chip

In this chapter, measurement of fabricated RF front-end IC-chip and the compensation process are discussed. Specially, an improved receiving capability from an image-rejection-ratio (IMRR) improving technique by the digital compensation technique mentioned in Chapter 3 is described.

5.1 Introduction

The chip was fabricated from a 130-nm CMOS process with eight level metal. The RF front-end designed in this study was verified through both on-wafer and on-board measurements. Using a wafer probing system, the pads of the device-under-test (DUT) were directly contacted with the high frequency probe card. In the on-board case, the IC-chip with the 24-pin QFN package was mounted on a printed circuit board. From the on-wafer measurement, the external inductor value for the LNA input condition was estimated. The noise figure (NF) of the total RF front-end was measured as well. During this step, the noise factor of external equipment that was attached to measure the on-wafer IC-chip was compensated. A module board was fabricated with the promising external lumped inductor and low-pass filter (LPF), and A/D converter (ADC) to confirm capability of triple-band signal reception. Digital compensation to improve IMRR, which is mentioned in Chapter 3, was also performed.

5.2 Bare Chip Measurement

The chip-level measurement was carried out using a wafer probing system. Figure 5.1 shows the fabricated IC-chip photograph. The IC-chip area of the core blocks, including pads and ESD protection circuits, occupied 2.4 mm^2. Except for the IF output pads for low frequency (approximately 25 MHz), the pads for RF and LO signals were constructed with a ground-signal-ground structure for minimization of interferences between the signal lines. The ports of A(+,−) to D(+,−) in Fig. 5.1 correspond with A to D in Fig. 3.5 in Chapter 3. The subtractors of these signals were implemented by using a precise power splitter (Agilent 11667B, 50±2 Ω). The probe needle with the shunt capacitor was used for stable DC power supply and biases. In Fig. 5.2(a), the manufactured RF probe needle is illustrated.

The on-wafer measurements have the advantage of high accuracy results without the package lead line. The input signal of the chip - in other words, the input signal of the low-noise amplifier (LNA) - was received through L_g, which was located in front of the LNA input stage. In this study, because of the size and reasonable quality factor of the inductor, the external inductor was used. For the input impedance matching condition of the chip, the impedance passive manual tuner was used instead of the external inductor. In connecting as in Fig. 5.3, the input impedance condition could be set by controlling the manual tuner. The insertion loss for the input matching circuit, cable, and probe needle were also compensated [2].

5.2.1 Input Reflection Coefficient of the Bare Chip

Through measurement of the bare chip, the input reflection coefficient and NF were measured as RF features. The case of the input reflection coefficient was checked using the vector network analyzer HP 8722ES. For high accuracy measurement, the network analyzer was calibrated through the probe needle's contact with the coplanar line impedance sheet illustrated in Fig. 5.2(b). To avoid instrumental errors originating from the bonding wires, the small-signal and noise characteristics of the receiver chip with an ideal inductor L_g (in Fig. 4.7 of Chapter 4) in series with the gate of LNA input stage were estimated with the basis of the measured data [3]. The method is described in Appendix B.

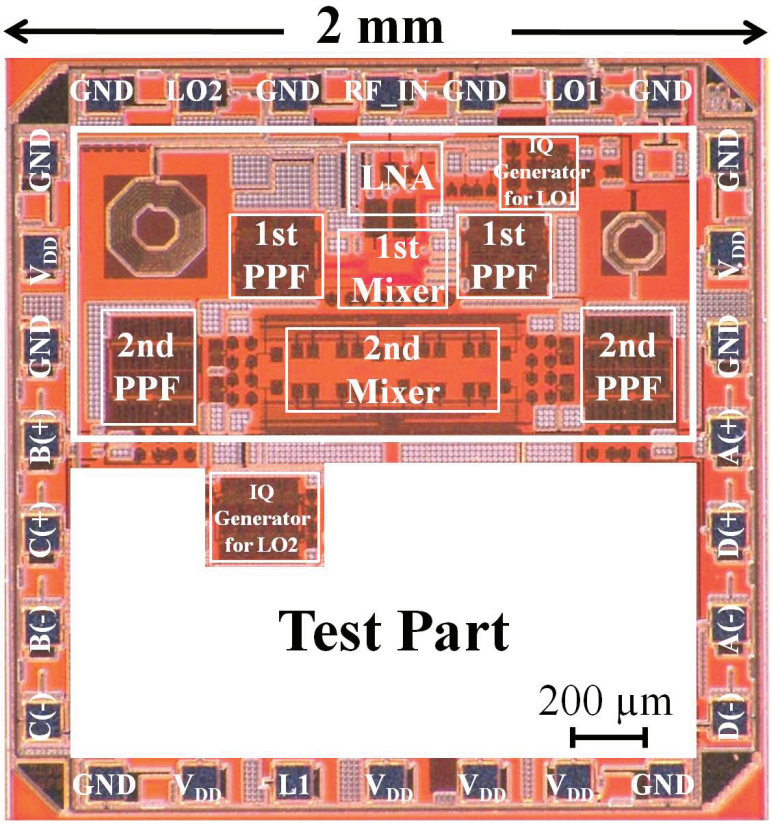
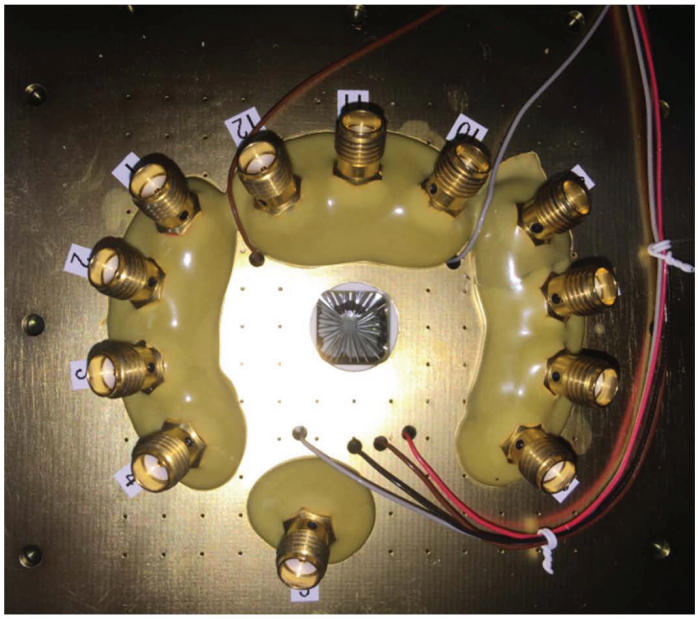


Figure 5.1: Fabricated chip photo.

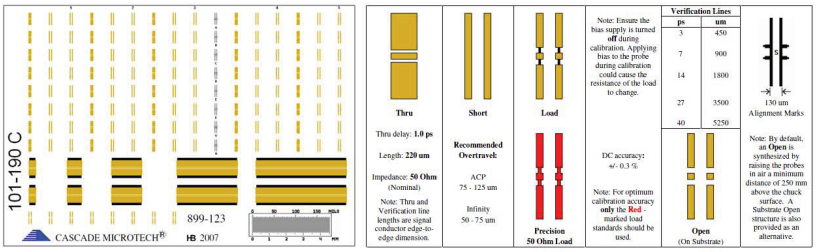
5.2.2 Noise Figure of the Bare Chip

The NF was measured using the NF meter HP 8970A, and the noise source HP 346C. Figure 5.3(b) shows the equipment setup for measurement of the NF. A manual tuner and probe needle were used for input impedance matching in the target frequency. The equivalent blocks of these measurement equipments are illustrated in Fig. 5.4. The passive blocks (manual tuner, cable, and probe needle) have noise. To evaluate the performance of the chip, the loss and noise from the signal source to the surface of the chip's pad had to be compensated.

As shown in Fig. 5.4, the noise source controlled by the NF meter generates a test signal into the DUT. The NF meter calculates the DUT NF through analysis of the received noise. In this study, the



(a)



(b)

Figure 5.2: (a) Probe card for high-frequency DUT measurement and (b) impedance standard substrate for calibration.

effective NF was recalculated by converting the unwanted noise of the above passive blocks into the noise source [4]. The detailed theoretical explanation is provided in the Appendixes B and C.

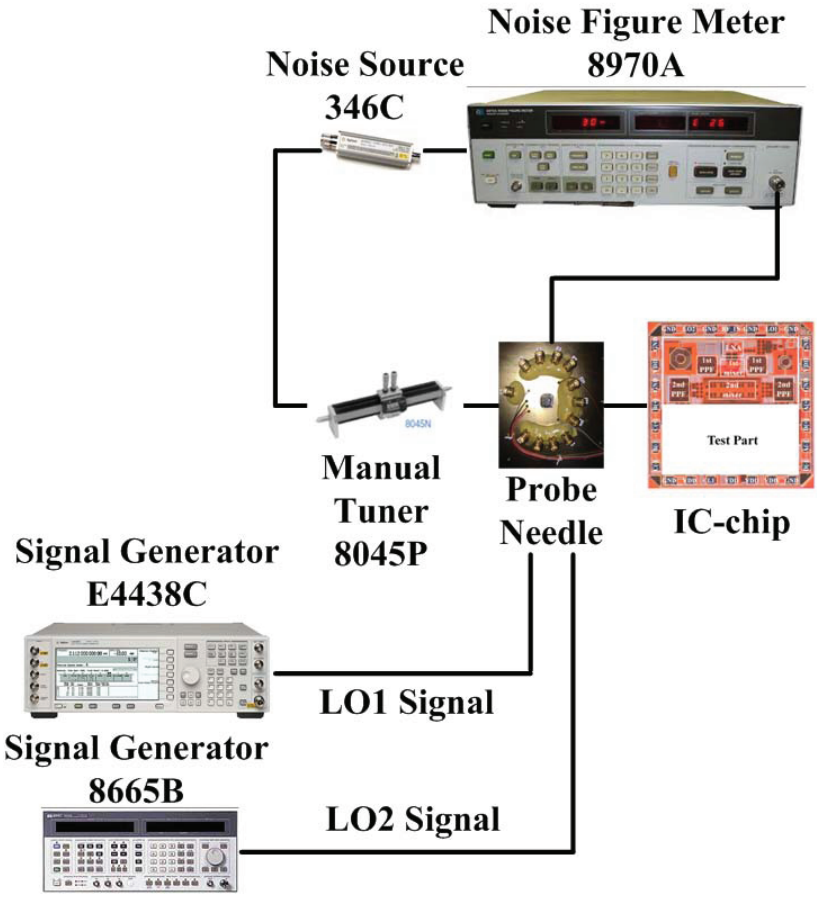


Figure 5.3: Equipment set-up for NF measurement.

5.2.3 Measurement Results of the On-wafer IC-chip

In the measurement, the power consumption was approximately 7.2 mW with a 1.2-V supply voltage, which was mainly for the LNA and mixer core blocks. Figure 5.5 shows the measurement results of the input reflection coefficient based on the input reflection results with promising value of L_g estimated 8.2 nH, and the NFs compensated the insertion loss for the input matching circuit, cable, and probe needle with re-calculated noise source. The input reflection coefficient for the input impedance matching condition was under -10 dB. The NF for the RF front-end chip was less than 7.1 dB over a wide frequency range covering the L1, L2, and L5 bands.

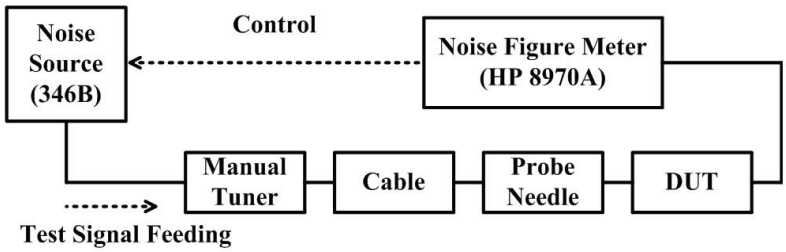


Figure 5.4: Equivalent set-up of measurement equipments for NF.

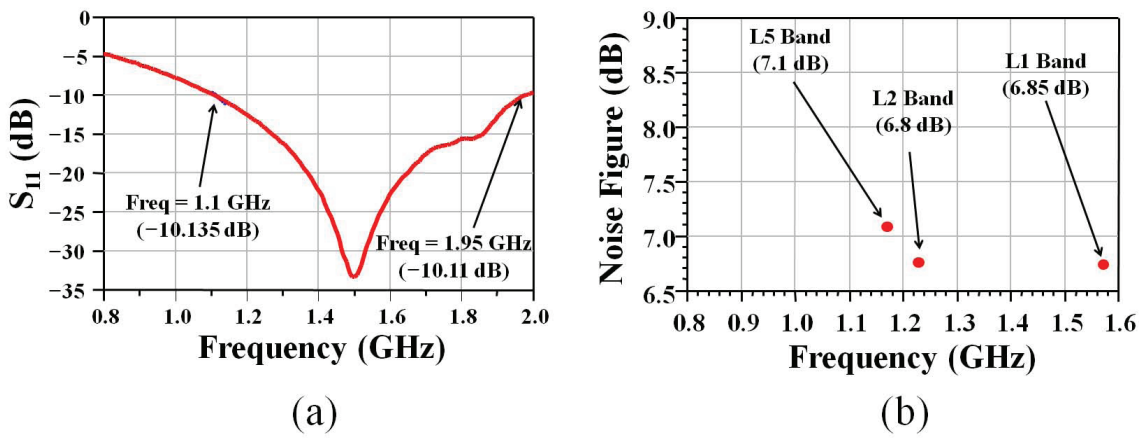


Figure 5.5: Measurement results of on-wafer IC-chip: (a) input reflection coefficient and (b) NF.

5.3 Module Measurement

For the on-board measurement, the IC-chip was packaged in 24-pin QFN package. The parasitic inductance of bonding wire (∼1 nH) for LNA input was small in this case.

The PCB module board was fabricated for attaching the promising external inductor calculated from the previous measurement, as shown in Fig. 5.6. In addition to the chip packaged and the external inductor for input impedance matching, the module has ADCs for observing the received data on a specific time domain and anti-alias IF passive low-pass filters (pass-band loss: ∼1 dB, 3 dB-bandwidth: 25 MHz). The subtractions of the second PPFs output signals for the ADC input

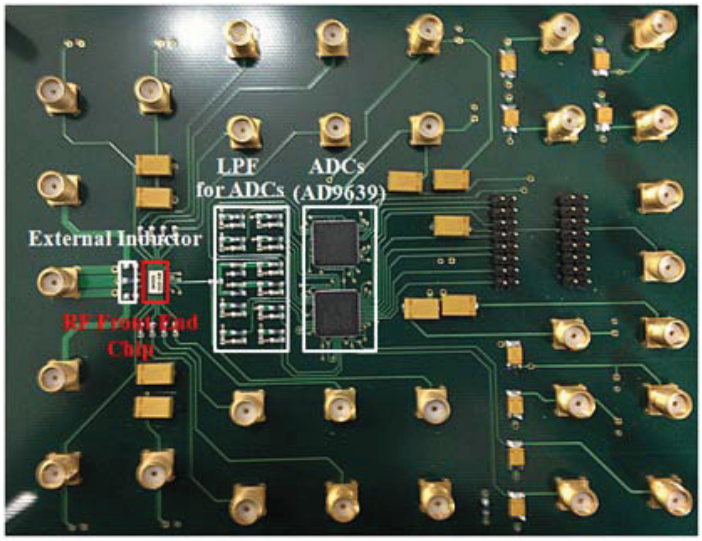


Figure 5.6: Designed module PCB board.

signals are implemented by using precise external resistances (∼1 kΩ) on the module, which provide much higher load resistances of the second PPFs (∼200 Ω resistances are used) in addition to the ADC input resistances (4.3 kΩ) and have little influence on the IMRR in this design, as described in Chapter 4. The input reflection coefficient and NF were measured as shown in Fig. 5.7.

The analog outputs were simultaneously measured by inserting the modulation input signals. For the easy check, 5 MHz and 2.5 MHz BPSK modulation signals for L2 and L5 band signals were used, and a CW signal was used for the L1 band signal. The analog output signals were measured at each band port. Figure 5.8 shows the inserted input signals and the measured output signals per each port. Compared to the differently modulated signal at the same port, the IMRR could be calculated. From the measurement results, the IMRR of L1, L2, and L5 band signals were 40 dB, 38 dB, and 39 dB, respectively. As predicted in the previous chapter, owing to the differences of receiving paths, the IMRR of L2 and L5 band signals were degraded more than that of the L1 band signal.

Signal separation in the ADC output was also verified. As the AD9639 [1] used in this work has four ADCs inside, the two ADC components embedded on the module (total eight ADCs) can afford for evaluation of this digital compensation. As described later, the required bit number of the ADC is four. To provide signal with adequate level to each of the ADC inputs, the differential probes

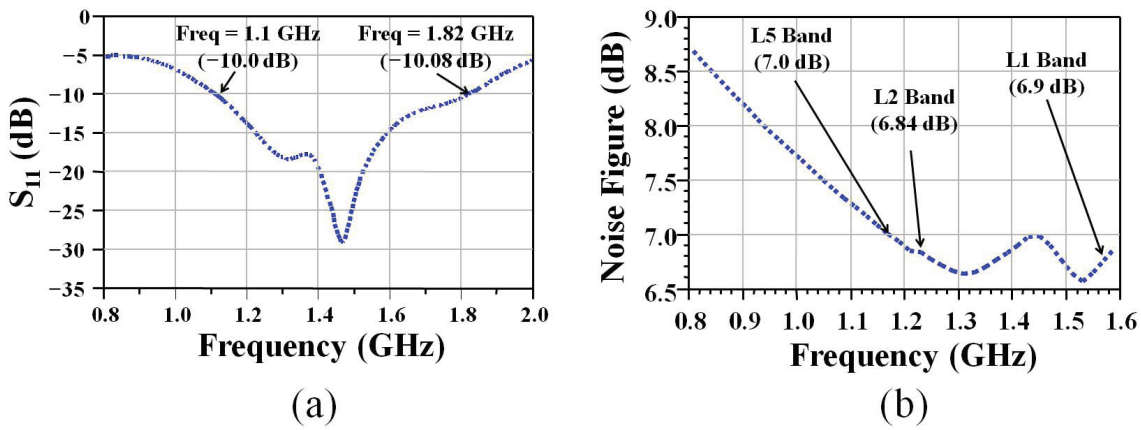


Figure 5.7: Measurement results of RF front-end on module board: (a) input reflection coefficient and (b) NF.

(Tektronix P6247, attenuation 10:1) were used as IF amplifiers in this work. To measure the received signal at each independent port, 10 MHz, 5 MHz, and 2.5 MHz BPSK modulation signals were used for L1, L2, and L5 bands. Figure 5.9 shows the input modulation signals that were measured directly on the signal generator and the measured output signals of the ADCs. The ADC sampling period is 5 ns. This figure implies that the data rates of the measured signals at the L1, L2, and L5 ports are 10 MHz, 5 MHz, and 2.5 MHz, respectively.

5.4 Discussion on the IMRR Digital Compensation

As mentioned in the Chapter 3, among the triple-band signal, L2 and L5 band signal IMRRs were worse than that of the L1 band signal. Through previous measurement results, the L1 band signal IMRR was more than 40 dB. However, the L2 and L5 band signal IMRRs were approximately 37 $\sim$ 38 dB. These IMRRs were due to the signal received path. This is because the L1 band signal was received through the first poly-phase filter (PPF), while the L2 and L5 band signals were received through the first and second PPFs. In this study, for compensation, a digital method was used instead of an analog method [5, 6] to avoid large area occupation and high power consumption. Figure 5.10 shows the end parts of the proposed architecture's signal flow block.

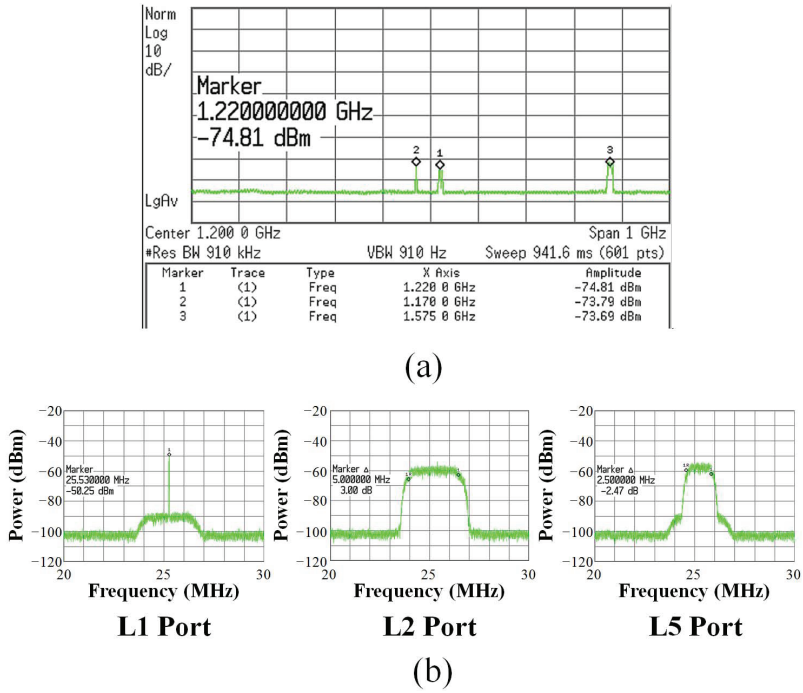


Figure 5.8: (a) Triple-band RF input signals and (b) analog outputs at each band port on board.

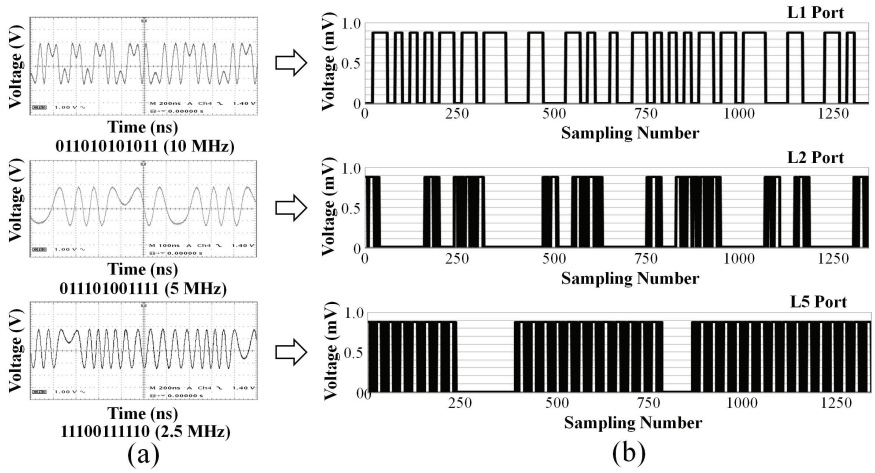


Figure 5.9: (a) Modulated RF input signals (observed at low-frequency output of the signal generator) and (b) demodulation 2-bit binary output singals after ADC (LSB: ∼439 μV).

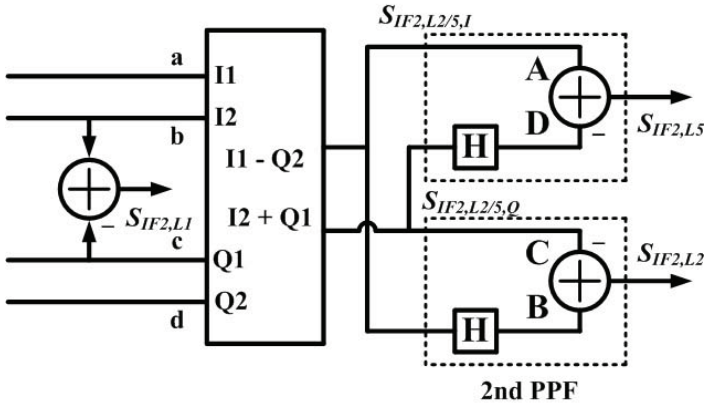


Figure 5.10: End parts of proposed architecture's signal flow block.

For this technique, the relation of the signals at A and D, and those at B and C, in Fig. 5.10 were digitally implemented through the four ADCs. From the calculation, the required bit number of the ADC was four.

The concept of an image-rejection technique has the same meaning of the cancellation of unwanted band signals on the target band signal. For example, for detection of the L5 band signal, the output signals are denoted A and D in Fig. 5.10. In those node signals, the L5 band signals have different phases, and the L2 band signals have the same phase. Therefore, through a subtraction operation, the L5 band signal without the L2 band signal could be received. If the L2 and L5 band signals had amplitude and phase errors, the errors degraded the IMRR. Therefore, the goal of digital compensation was the fit of amplitude and phase of the signals of these two nodes. To this end, utilizing $I(t) - H[Q_{comp}(t)]$ instead of $I(t) - H[Q(t)]$ could improve the IMRR. To improve the IMRR at the L5 port, $I(t)$ and $Q(t)$ were assigned to the signals at A and C in Fig. 5.10, and $H[Q_{comp}(t)]$ could be obtained in the following digital signal processing. The Hilbert transform could be simply calculated with the delay by a quarter of a signal period in the over-sampled digital signal data. Based on the above approximated formula, the approximated signal of $H[Q_{comp}(t)]$ could be calculated from only $H[Q(t)]$ (the signal at D in Fig. 5.10) after obtaining a_e and θ_e in Fig. 3.10. The L2 band signal

could also be improved in the same way.

$$\begin{aligned} H[Q_{comp}(t)] &= \frac{H[Q(t)]}{a_e \cos\theta_e} - \tan\theta_e \, H[I(t)] \\ &\approx \frac{H[Q(t)]}{a_e \cos\theta_e} + \tan\theta_e \, H[H[Q(t)]]. \end{aligned} \tag{5.1}$$

To verify the digital compensation technique for the L5 port, the ADC outputs at A and D in Fig. 5.10 were measured. The phase error θ_e could be obtained from the ADC outputs at A and D in Fig. 5.10 in the following overview. $I(t)$ in Fig. 3.10 corresponded to the signal at A. Considering interconnection modifications on the board, the inverse Hilbert transform ($H^{-1}[\cdot] = -H[\cdot]$) of the signal at D were used as $Q(t)$ instead of that at C. As a result, the $Q_{comp}(t)$ and $H[Q_{comp}(t)]$ signals were approximately calculated only from the ADC output at D using Eq. (5.1).

The amplitude error could be compensated after this phase error compensation. By considering the amplitude errors, the signals at A and D ($s_A(t)$ and $s_D(t)$) are expressed as

$$s_A(t) = m_{L2}(t)\cos(\omega_{IF2}t + \theta) + m_{L5}(t)\cos(\omega_{IF2}t), \tag{5.2}$$

$$s_D(t) = (1+\varepsilon_1)\, m_{L2}(t)\cos(\omega_{IF2}t + \theta) - (1+\varepsilon_2)\, m_{L5}(t)\cos(\omega_{IF2}t), \tag{5.3}$$

where θ means the phase difference between the L2 and L5 band signals, and $|\varepsilon_1|, |\varepsilon_2| \ll 1$. Considering $s_A(t) - s_D(t)$ based on the above expressions, the IMRR for L5 port without the digital amplitude error compensation is given by $|(2+\varepsilon_2)/\varepsilon_1|^2 \approx 4/\varepsilon_1^2$. To compensate the amplitude error, the following calculation with a small compensation parameter ε_1' is used.

$$s_A(t) - (1-\varepsilon_1')s_D(t) \approx (\varepsilon_1' - \varepsilon_1)\, m_{L2}(t)\cos(\omega_{IF2}t + \theta) + (2 + \varepsilon_2 - \varepsilon_1')\, m_{L5}(t)\cos(\omega_{IF2}t). \tag{5.4}$$

In this case, the IMRR for the L5 port is given by $|(2+\varepsilon_2-\varepsilon_1')/(\varepsilon_1'-\varepsilon_1)|^2 \approx 4/|\varepsilon_1'-\varepsilon_1|^2$. By setting $\varepsilon_1' = \varepsilon_1$, the IMRR can be well improved. The IMRR for the L2 port can be improved in the same way using the signals at B and C in Fig. 5.10.

From the measurement results, ε_1 and ε_2 were obtained as 0.0252 (-31.9 dB) and 0.0266 (-31.5 dB). By setting $\varepsilon_1' = \varepsilon_1$ with these conditions, the IMRR between the L2 and L5 band signals became approximately 49 dB. Figure 5.11 shows the measured result where the BPSK modulation signals of 5 MHz and 2.5 MHz modulation frequency were used for the L2 and L5 band signals. To ensure the IMRR improvement, the obtained FFT data were processed through band-pass filtering and moving

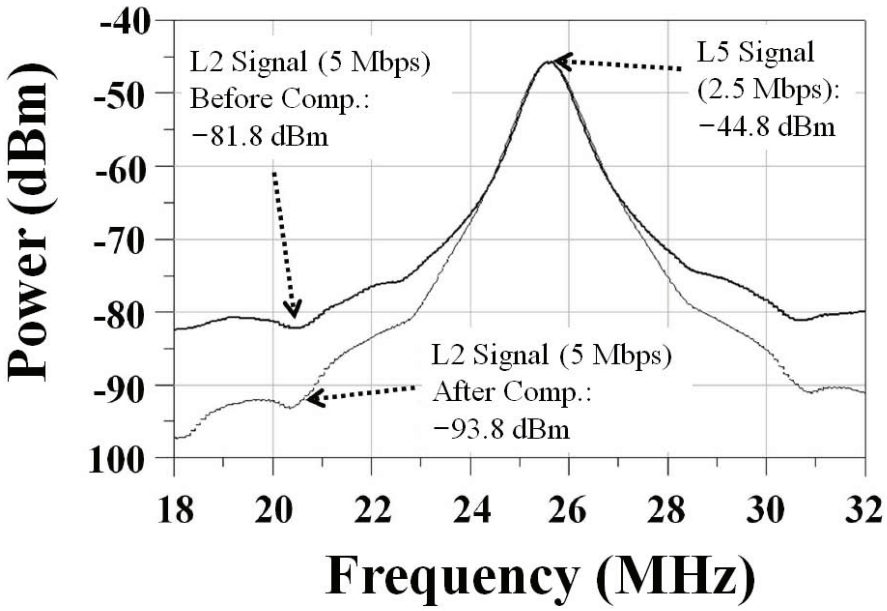


Figure 5.11: Signal spectrum at the L5 port with IMRR correction (dotted line) and without IMRR correction (solid line). The obtained FFT data are processed through band-pass filtering (center frequency: 25.595 MHz, pass-band width: 10 MHz, pass-band ripple: 0.01 dB) and 61-point moving averaging. The resolution bandwidth is 50 kHz.

averaging. As a result, an improvement of approximately 12 dB of IMRR between the L2 and L5 band signals was observed by using the digital compensation technique described above. In this experiment, at least a 4-bit ADC was required to detect a phase error of under 3° at the second PPF outputs. Although a 4-bit ADC may have been somewhat heavy for GPS applications, the allowable mismatches in the PPFs could be relaxed.

5.5 Conclusion

The proposed RF front-end through measurement was verified. For fabrication, a 130-nm CMOS process was used. The circuits worked with a 1.2-V supply voltage. During operation, the power-consumption of the main blocks including LNA and mixers is 7.2 mW. For input impedance matching

of the chip, an external inductor of 8.2 nH (Murata LQW18AN8N2D00) was used. The bonding wire of 24-pin QFN package at the LNA input had regrettably small parasitic inductance. The proposed RF front-end had less than a -10 dB input reflection coefficient and 7 dB NF during the target frequency range. Through the output signals of the analog and ADC, each band signal at each band port was verified. At that time, the IMRR was more than 40 dB in the L1 band signal and $37 \sim 38$ dB in the L2 and L5 band signals. For improving the degraded IMRR of the L2 and L5 band signals, the digital compensation technique was used. In this way, the IMRR degraded on account of PPF which is an essential block for construction of the proposed architecture could be improved.

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Chapter 6

Conclusion

RF front-end architecture has been studied for the global positioning system (GPS). GPS has been used most widely among various global navigation satellite system (GNSS) applications. The receiver studied in this work can simultaneously receive multi-band signals for high-accuracy positioning information, such as ocean remote sensing. Through the proposed method, a different real-time kinematic global positioning system (RTK DGPS) can be realized with high-positioning-accuracy. In this study, RF front-end architecture which can receive the triple-band GPS signal (L1, L2, and L5) was designed and evaluated.

Chapter 1 introduced the study. It mentioned the basic concept of GNSS and explained the motivation and main goal of this study. It additionally described the organization of the thesis.

In Chapter 2, the high-accuracy equivalent circuit of MOSFET operating in RF frequency was described. In particular, the gate-electrode resistance including the vertical current paths was highlighted. This is important to achieve the input impedance matching condition in the design of a low-noise amplifier (LNA) that covers the wide frequency range including triple-band signal. The vertical current path elements, such as the interface resistance between the silicide and poly-silicon, have large influence on the gate-electrode resistance in the small-dimension devices. Multi-finger structure can reduce the gate-electrode resistance. In addition, it is revealed that the non-quasi-static gate resistance has Elmore constant around 5 for long-channel devices and smaller values for gate lengths under 1 μm. Based on these knowledges, the effective gate resistance in the input stage of the LNA could be accurately estimated.

In Chapter 3, the RF front-end architecture for a triple-band GPS signal was proposed. The archi-

tecture has only a single RF path and uses an image rejection technique based on Weaver architecture. Independent signal separation was realized by inserting the poly-phase filters (PPF) into the conventional Weaver structure. The behavior-level and circuit simulation results verified the feasibility of the proposed architecture. A digital compensation technique and its theoretical explanation were also studied to improve the degraded image rejection ratio (IMRR) of the L2 and L5 band signals.

In Chapter 4, the circuit blocks composing the proposed RF front-end were described. A LNA, active and passive mixers, PPFs, and a balun were used for these circuit blocks. The LNA has a frequency characteristic that can receive the triple-band signal. A proper noise figure (NF) is required, which limits the receiving sensitivity. Input device characteristics that determine the frequency features, as mentioned in Chapter 2, were used in the design. All blocks were designed with a balanced structure. In particular, the amplitude and phase balance of output signals were mainly considered during the design. The receiving capability of whole blocks was verified through the IMRR, which was calculated from imbalance ratios of output signals. Through circuit simulations, it was demonstrated that the RF front-end can simultaneously receive the triple-band GPS signal. NF was 6.8 $\sim$ 7.0 dB in target frequency range, and the IMRR was 38 $\sim$ 41 dB at each band port with 6.5 mW power consumption of main blocks including LNA and mixers.

Chapter 5 described experimental results of the RF front-end integrated circuit fabricated with a 130-nm CMOS process and a 1.2-V power supply. The measurements were carried out in three steps. The RF features of the bare chip were first measured with a wafer probing system and a manual tuner. Through this step, the promising value of the external inductor for the input stage was obtained. As the second step, bare chips were packaged and the module board was fabricated with the promising external inductor, low-pass filter, and analog-digital converter (ADC). The fabricated RF front-end module had the input reflection coefficient less than -10 dB and 7 dB NF during the target frequency range. Experimental results revealed that the fabricated RF front-end integrated circuit could simultaneously receive the triple-band GPS signal through a single path. The received signals were individually separated at each band port. The IMRR was more than 40 dB in the L1 band signal and 37 $\sim$ 38 dB in the L2 and L5 band signals. The power-consumption of the main blocks including LNA and mixers was 7.2 mW. These show good agreement with simulation results shown in Chapter 4. As a final step, the improved IMRR of the output signal was observed through a digital compensation method from the ADC output signals. It was demonstrated that the degraded

IMRR was improved by more than 10 dB.

The small-size low-power multi-band receivers with the simultaneous signal reception will be more attractive in the future. This study has demonstrated the feasibility of simultaneous GPS triple-band reception with a single RF path. The proposed receiver architecture is expected to become one of promising techniques for them.

Appendix A

Gate Impedance of MOSFET with Vertical Current Path Elements

The lumped elements of MOSFET's horizontal and vertical gate resistance can be composed as Fig. 2.1(b) in Chapter 2. The steady state at the angular frequency ω in only the gate-electrode on the channel ($z = 0 \sim W_f$) is considered now. Using Eq. (2.2) in Chapter 2, the admittance of vertical current path terms for signal propagation length dz on the gate-electrode surface is expressed as $Y_{vp}dz$. The signal voltage $v(z)$ and current $i(z)$ on the gate-electrode surface can be obtained by solving the following differential equations

$$\frac{dv(z)}{dz} = -R_{sili}\, i(z), \tag{A.1}$$

$$\frac{di(z)}{dz} = -Y_{vp}\, v(z). \tag{A.2}$$

Thus the voltage $v(z)$ and current $i(z)$ can be expressed as

$$v(z) = V_+\, e^{-\gamma z} + V_-\, e^{\gamma z}, \tag{A.3}$$

$$i(z) = \frac{Y_{vp}}{\gamma}(V_+\, e^{-\gamma z} - V_-\, e^{\gamma z}), \tag{A.4}$$

where γ is given by

$$\gamma = \sqrt{R_{sili}\, Y_{vp}}. \tag{A.5}$$

The boundary conditions to obtain V_+ and V_- in case of a single-side gate connection ($v(0) = v_{gs}, i(W_f) = 0$) give the gate-electrode impedance as $Z_g = v(0)/i(0)$. Similarly, in case of a

both-side gate connection ($v(0) = v(W_f) = v_{gs}$), the gate-electrode impedance can be obtained as $Z_g = v(0)/(i(0) + (-i(W_f)))$. As a result, the gate-electrode impedance is given by

$$\begin{aligned} Z_g &= \frac{\sqrt{k}\,\gamma}{Y_{vp}}\,\coth\Big(\sqrt{k}\,\gamma\,W_f\Big) \\ &\approx \frac{1}{Y_{vp}W_f} + \frac{k}{3}R_{sili}\,W_f \\ &\approx \frac{1}{j\omega C_{gc}} + \frac{\rho_{int}+\rho_{vp}}{LW_f} + \frac{k}{3}R_{sili}\,W_f, \end{aligned} \tag{A.6}$$

where k is 1 and $1/4$ for a single-side and a both-side gate connections, respectively. The approximation is valid for $|\sqrt{R_{sili}\,Y_{vp}}|W_f \ll 1$. The second and third terms of Eq. (A.6) contribute to the gate-electrode resistance.

Appendix B

NF Re-calculation with the External Inductor

To estimate the NF value with the external inductor, the noise parameters are required. The NF for source admittance Y_S seen from the surface of the chip pad is given by

$$NF = NF_{min} + \frac{R_n}{\mathrm{Re}[Y_S]}\left|Y_S - Y_{opt}\right|^2, \tag{B.1}$$

where the noise parameters NF_{min}, R_n, and Y_{opt} are the minimum NF, noise resistance, and optimum source admittance, respectively. These noise parameters can be obtained from the NF values obtained for various Y_S values by using the manual tuner. The source admittance Y_S seen from the surface of the chip pad can be obtained by using scattering parameters $[S]$ of the passive 2-port block from the signal source described in Appendix C. When the impedance of the noise source is approximated to Z_0, $Y_S \approx (1/Z_0)(1 - S_{22})/(1 + S_{22})$.

To re-calculate the NF value with the external input inductor $L_{g,ext}$ based on the noise parameters, the following equation for Y_S is used:

$$Y_{\text{S with ext. ind.}} = \frac{1}{Z_0 + j\omega L_{g,ext}}, \tag{B.2}$$

where the impedance of the signal source is set to the characteristic impedance Z_0.

To obtain $[S]$, it is expressed as

$$[S] = [S_1][S_2], \tag{B.3}$$

where $[S_1]$ is the scattering matrix from output of noise source to cable output including manual tuner and $[S_2]$ is from SMA connector to the tip of the probe needle. The $[S_1]$ can be obtained using the conventional co-axial measurement. To obtain the scattering matrix $[S_2]$ values of passive 2-port block, the variable impedance conditions of probe needle (open, short, and known impedance) and the reciprocity ($S_{12} = S_{21}$) are used.

Appendix C

Excess Noise Ratio with Compensation of Signal Loss

Figure C.1 shows a block diagram of the chip-level NF measurements with a wafer probing system, which has a probe needle, cable, and a manual tuner for input impedance matching. To evaluate the performance of the chip, while including the loss of the pad, the loss from the signal source to the surface of the chip's pad must be compensated. When measuring the NF, a reference point of the controllable noise source with a known excess noise ratio (ENR) (port 1-1' in Fig. C.1) must be changed to the surface of the chip's pad (port 2-2' in Fig. C.1). This effectively changes the ENR used in the NF measurement.

The available noise power of the controllable noise source during the off-state and on-state are expressed as $k_B T_{off} \Delta f$ and $k_B T_{on} \Delta f$, respectively. Here, k_B is the Boltzmann constant, Δf is the bandwidth, and T_{off} and T_{on} are the equivalent absolute temperatures used to express the off-state and on-state noises, respectively. Using the noise source resistance R_S, the corresponding noise voltages $e_{ns,off}$ and $e_{ns,on}$ are given by

$$\overline{|e_{ns,off}|^2} = 4k_B T_{off} R_S \Delta f, \tag{C.1}$$

$$\overline{|e_{ns,on}|^2} = 4k_B T_{on} R_S \Delta f. \tag{C.2}$$

The ENR value is defined as follows.

$$ENR = \frac{\overline{|e_{ns,on}|^2} - \overline{|e_{ns,off}|^2}}{\overline{|e_{ns,off}|^2}} = \frac{T_{on} - T_{off}}{T_{off}}. \tag{C.3}$$

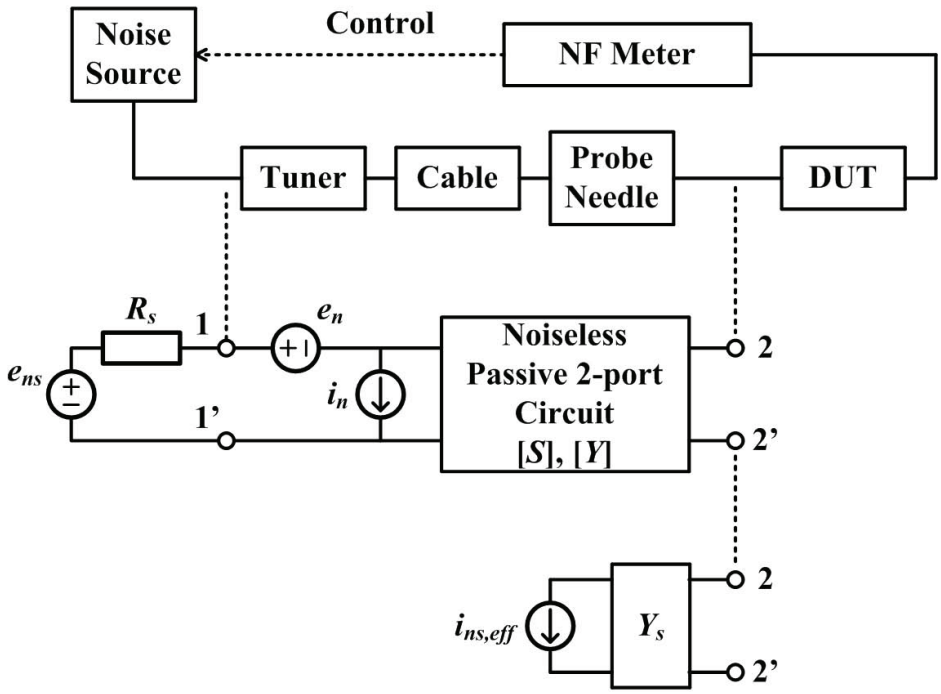

Figure C.1: On-wafer IC-chip NF measurement block diagram with the equivalent passive blocks.

Noise figure NF can be obtained by using the ENR as follows:

$$NF = \frac{ENR}{Y-1}, \tag{C.4}$$

where the Y factor is defined as the ratio of the noise power measured at the output for the on-state and off-state noise sources.

To calculate the effective value of the ENR with reference port 2-2' in Fig. C.1 (ENR_{eff}), the passive 2-port block from the signal source to the surface of the chip's pad is focused. The correlation matrix of the noise waves at both ports in the passive 2-port block at absolute temperature T is expressed as

$$[C_S] = k_B T([E] - [S][S^\dagger]), \tag{C.5}$$

where $[E]$ is the unit matrix and $[S]$ is the scattering matrix of this block [1, 2]. Using this equation, the correlation matrix of the input-referred noise voltage e_n and current i_n can be obtained from $[C_S]$

as follows:

$$[C_A] = \frac{1}{\Delta f}\begin{bmatrix} \overline{|e_n|^2} & \overline{e_n i_n^*} \\ \overline{e_n^* i_n} & \overline{|i_n|^2} \end{bmatrix} = [T][C_Y][T^\dagger], \tag{C.6}$$

$$[C_Y] = ([E] + Z_0[Y])[C_S]([E] + Z_0[Y^\dagger]), \tag{C.7}$$

where $[Y]$ is the admittance matrix of this block, Z_0 is the characteristic impedance, and $[T]$ is the transformation matrix from the admittance representation $[C_Y]$ to the chain representation $[C_A]$ [3]. By using elements of $[C_A]$ calculated by the above equations, ENR_{eff} can be expressed as follows.

$$\begin{aligned} ENR_{eff} &= \frac{\overline{|e_{ns,on} + e_n + i_n R_S|^2} - \overline{|e_{ns,off} + e_n + i_n R_S|^2}}{\overline{|e_{ns,off} + e_n + i_n R_S|^2}} \\ &= \frac{ENR}{1 + \overline{|e_n + i_n R_S|^2}/4R_S k_B T_{off}\Delta f}. \end{aligned} \tag{C.8}$$

The value of ENR_{eff} can be calculated by using the ENR, R_S, and the elements of $[C_A]$. By using ENR_{eff} instead of ENR in Eq. (C.4), the NF with loss compensated from the signal source to the surface of the chip's pad can be obtained.

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Acknowledgements

Thank GOD for giving permission and accomplishing all this.

Since my first day in Graduate School of Engineering, Osaka University, in July 2009, six years have been passed. At that time, I felt a lot of lacking as in intellectual and mental skills. Many people around me have given a lot of help. I would like to thank those who have supported me to carry out the studies and prepare for PhD degree.

First and foremost I want to thank my advisor, Associate Professor Toshimasa Matsuoka about kindness and in-depth teachings. In particular, I gained a lot of understanding to learn attitude to solve the problems with more fundamental approach in research.

There are precious advices from Professor Tetsuya Yagi and Professor Shigemasa Takai as thesis readers who have been a great help to increase the completeness of the thesis.

I will remember and thank Professor Toshimichi Ito, Professor Yusuke Mori, Professor Mitsuhiro Katayama, Professor Masanori Ozaki, Professor Toshiaki Suhara, Professor Masahiko Kondow, and Professor Nobuya Mori of Graduate School of Engineering, Osaka University, about giving many opinions in as my thesis committee members.

I would like to thank Associate Professor Takuji Ebinuma of Chubu University for financial and technical supports.

There are precious advices from many people. I thank Professor Emeritus Kenji Taniguchi for giving me an opportunity to study at Osaka University. The lessons given sometimes are sure to be a great asset to my life. Thank you to Associate Professor Yoshinari Kamakura as well.

I would like to thank Dr. Takatsugu Kamata of SPChange, LLC. for technical advices. I would like to thank ex-secretary Noriko Furuta and Yuko Shimizu and present-secretary Kayoko Iwahara for advices and helping my daily life in Japan and laboratory. I also thank Jungnam Bae and Sai

Chandra Teja Radhapuram about meaningful discussions as the same research group, Dr. Jun Wang, Donggyu Kim, Dr. Hyunju Ham, and Dr. Jongpil Kim about advices as the senior.

Thanks to my family for always cheering from afar. I would like to thank my mother for showing un-conditional faith and supporting everything. I will pay it back all. And thanks father and my sister Miyoung Cho about watching at beside of mother in illness. And thanks Aunt Jihye Kim, Uncle Sangsun Kim, and sisters Heeju and Heeji for being able to find relief as the family.

I have to thank Professor Jongkyun Mok and his family about giving advice and worrying about my life in Japan. And I will never forget the prayer of many faithful peoples. I would like to thank the schoolmates, Daejin Yun, Gwangun Jung, Soojin Lee, Sangsoo Parkm, and Huijin Choi, who gave encourage for enduring the life in Japan.

I would like to thank Professor Moonque Lee about valuable advices and Dr. Sungmo Moon and schoolmates of University of Seoul. And thanks to Junggon Kim, Heesuk Jung, Kyunwoo Bae, Sunghyun Kim, Seoyun Lee, and Suelhee Kim about refreshing in Korea as friends.

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