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An offset distribution modification technique of stochastic flash ADC

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Abstract: A new non-linearity reduction technique for stochastic flash ADC (SF-ADC) is proposed, focusing on distribution of comparator input-referred offsets. The SF-ADC test chip fabricated in a 130-nm CMOS process demonstrated the proposed technique can improve SNDR. In addition, the digital re-quantization also can improve the linearity more, where quantization level and fractional correction can be optimized using genetic algorithm.

Keywords: stochastic flash ADC, comparator, mismatch, CMOS, genetic algorithm

Classification: Integrated circuits

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1 Introduction

The continuous downscaling of CMOS technology has resulted in remarkable advances in chip area reduction and high-speed operation, but device mismatch increasingly becomes a serious problem [1, 2]. Especially in mixed-signal circuit design, low-voltage RF/analog operation is required in order to keep compatibility with digital circuitry [3].

In flash analog-to-digital converters (flash ADCs) for high-speed broadband communication systems, comparator offset due to mismatch has direct influences on accuracy [4]. Techniques for restraining the mismatch generation through dimensional coordination or physical layout control generally tend to reduce operation speed or require additional area occupation and power consumption. Thus, the vigorous research efforts for maintaining accuracy of the conventional flash ADCs have generally focused on techniques for alleviating its effects [5, 6, 7].

There has been a different approach utilizing mismatch rather than minimizing or mitigating it. This approach has led to the proposal of stochastic flash ADCs (SF-ADCs), which apply the statistical nature of comparator offsets to detect signals below the offset level thereby maintain good dynamic range even in fine-process devices with substantial mismatch [8, 9, 10]. This technique originates from a detection principle of small signal with noise, so-called stochastic resonance [11, 12, 13, 14]. The previous work using a 1.2-V 65-nm CMOS process [15] experimentally demonstrated basic operation for signal detection in 500 MS/s sampling. However, non-linearity of SF-ADC is still one of the most important issues even using the non-linearity reduction technique proposed in the previous work [9, 15].

This letter proposes a new non-linearity reduction technique for SF-ADC. It consists of modification of comparator offset distribution and digital re-quantization.

2 SF-ADC and its linearization technique

In conventional flash ADC architectures, devices must be large in order to achieve the desired ADC resolution. Although the offset can be reduced by using offset calibration techniques with small area, it becomes more difficult as the CMOS process is refined. On the other hand, the SF-ADC uses the comparator offset. Fig. 1(a) shows the architecture of the SF-ADC. In the SF-ADC, a number of comparators are connected in parallel, and input-referred offset voltages are used as

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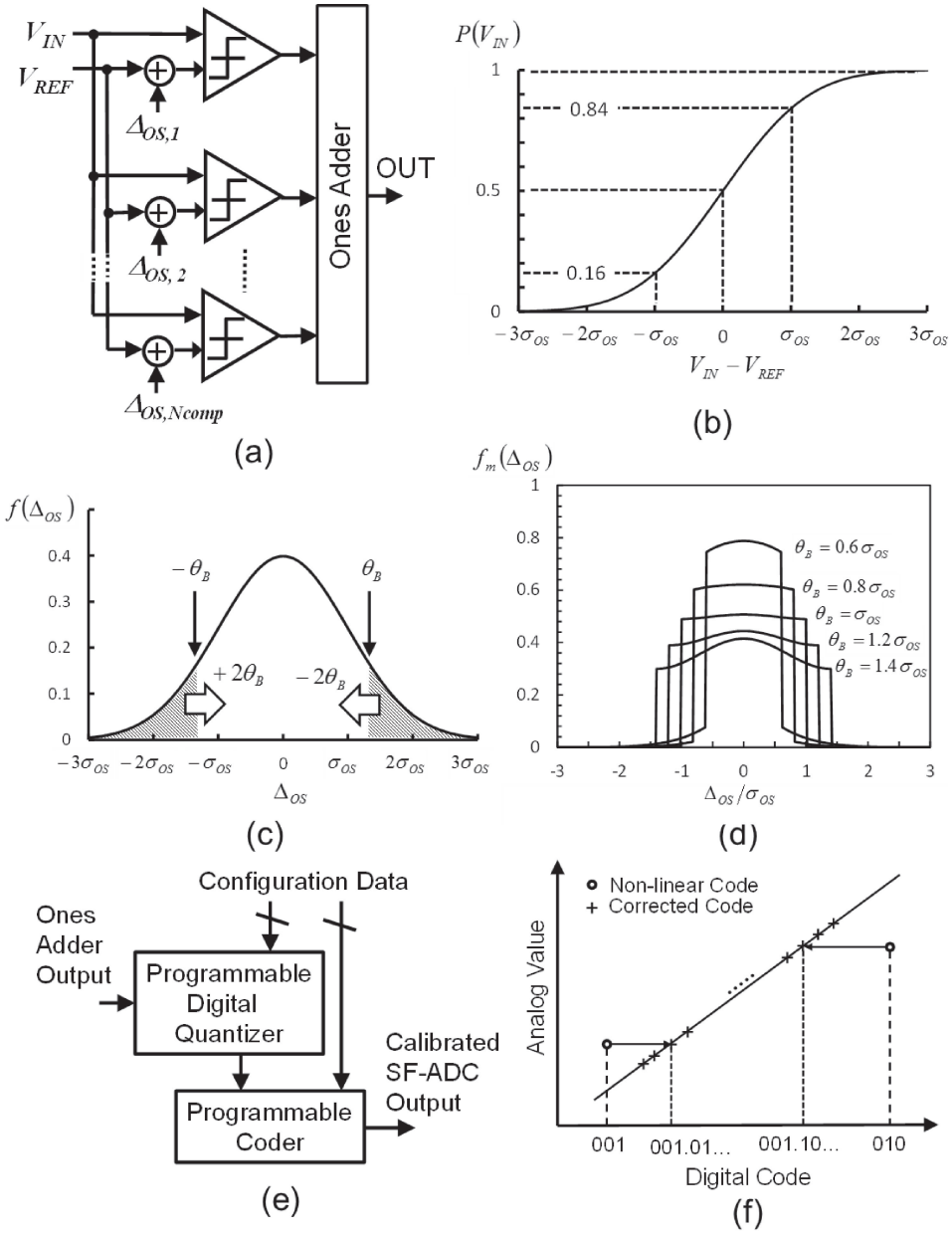

Fig. 1. (a) Concept of SF-ADC, (b) its characteristics, (c) concept of comparator offset distribution modification, (d) calculated results of $f_m(V_{IN})$ shown in Eq. (3), (e) configuration of digital re-quantizer, and (f) concept of the coder's operation with fractional correction.

reference voltages. Each offset $\Delta_{OS,i}(i = 1, 2, \cdots, N_{comp})$ is random and difficult to estimate, where N_{comp} is the total number of comparators. However, the offsets are usually modeled as a Gaussian probability density function (PDF), and the standard deviation of the offsets, σ_{OS}, can be estimated to some extent in the circuit design [9, 15].

Next, considering a set of N_{comp} comparators with a reference voltage V_{REF}, the probability P of obtaining outputs equal to one for an input signal voltage V_{IN} depends on the cumulative distribution function of the Gaussian PDF. This probability can be expressed as follows [9, 15]:

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$$P(V_{IN}) = 1 - \frac{1}{2}\,\mathrm{erfc}\left(\frac{V_{IN} - V_{REF}}{\sqrt{2}\sigma_{OS}}\right) \approx \frac{n_H}{N_{comp}}, \tag{1}$$

where $\mathrm{erfc}(x) = (2/\sqrt{\pi})\int_x^\infty \exp(-z^2)dz$ is the complementary error function, and n_H is the number of comparators for which the output is one (high). As shown in Eq. (1), this probability is approximately equal to the proportion of the comparator counts for which the output is one, i.e., n_H/N_{comp}. The SF-ADC determines its digital outputs by n_H. The SF-ADC uses comparators' input offsets as reference levels and so does not require any offset cancellation or calibration. The comparator is designed with minimum sized transistors in [8] and any offset cancellation is not used. This leads to decreasing the area occupation. Although the offset calibration techniques can be used even in an SF-ADC, the input range is decreased and sensitivity is increased.

The maximum input voltage range of the SF-ADC depends on the PDF of comparators' input offsets. The SF-ADC uses the linear range of the cumulative distribution, as shown in Fig. 1(b). Therefore, the maximum input range is determined by the standard deviation of the comparators' input offsets, σ_{OS}.

Assuming the cumulative Gaussian distribution of the comparator thresholds shown in Eq. (1), the PDF of the comparators with the input offset voltage Δ_{OS} is expressed as

$$f(\Delta_{OS}) = \frac{dP(V_{REF} + \Delta_{OS})}{d\Delta_{OS}} = \frac{1}{\sqrt{2\pi}\sigma_{OS}} \exp\left(-\frac{\Delta_{OS}^2}{2\sigma_{OS}^2}\right). \tag{2}$$

The function $f(V_{IN} - V_{REF})$ shows the PDF of the responding comparators for the input voltage V_{IN}. In previous works [9, 15], the comparators with the same offset distribution were divided into two groups, and their reference voltages were assigned with $V_{REF} \pm \sigma_{OS}$. In this case, the PDF of the responding comparators for the input voltage V_{IN} is modified as $(f(V_{IN} - V_{REF} + \sigma_{OS}) + f(V_{IN} - V_{REF} - \sigma_{OS}))/2$. This offset PDF modification (OSDM) can improve linearity of the SF-ADC. However, the SNDR for small input signal below σ_{OS} degrades under the finite number of comparators due to smaller number of responding comparators [9].

To enhance linearity of the SF-ADC without SNDR degradation for small input signal below σ_{OS}, a novel OSDM technique shown in Fig. 1(c) is proposed in this work. By modifying individual reference voltage, each comparator offset out of desired range is effectively shifted so as to enter within it. The modified PDF of the comparators' input offsets, $f_m(\Delta_{OS})$ is given by

$$f_m(\Delta_{OS}) = \begin{cases} f(\Delta_{OS} - 2\theta_B) & (\Delta_{OS} < -\theta_B) \\ f(\Delta_{OS}) + f(\Delta_{OS} - 2\theta_B) + f(\Delta_{OS} + 2\theta_B) & (|\Delta_{OS}| \le \theta_B) \\ f(\Delta_{OS} + 2\theta_B) & (\Delta_{OS} > \theta_B) \end{cases} \tag{3}$$

The function $f_m(V_{IN} - V_{REF})$ shows the PDF of the responding comparators for the input voltage V_{IN}. Fig. 1(d) shows $f_m(\Delta_{OS})$ for some values of θ_B. When $\theta_B = \sigma_{OS}$, $f_m(\Delta_{OS})$ is similar to uniform PDF.

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Table I. Analytical expressions of the probability of obtaining 'high' comparator outputs for an input signal voltage ($P(V_{IN})$) and the parameters of their approximations expressed by Eq. (5).

Technique	$P(V_{IN})\left(\xi_{IN}=\frac{V_{IN}-V_{REF}}{\sqrt{2}\sigma_{OS}}\right)$	α	β
Conventional	$1-\frac{1}{2}\mathrm{erfc}(\xi_{IN})$	1	$\frac{1}{3}$
Ref. [9, 15]	$1-\frac{1}{4}\left[\mathrm{erfc}\left(\xi_{IN}+\frac{\sqrt{2}}{2}\right)+\mathrm{erfc}\left(\xi_{IN}-\frac{\sqrt{2}}{2}\right)\right]$	$\frac{1}{\sqrt{e}}$	0
Proposed	Eq. (4)	$1+\frac{2}{e^2}$	$\frac{1}{3}\left(1-\frac{6}{e^2}\right)$

Assuming the cumulative Gaussian distribution of the comparator thresholds shown in Fig. 1(b), the input voltage for 16% 'high' comparator outputs corresponds to $-\sigma_{OS}$. Similarly, the input voltage for 84% 'high' comparator outputs corresponds to σ_{OS}. Therefore, by adding $2\sigma_{OS}$ and $-2\sigma_{OS}$ to the reference voltages for the comparators with threshold below $-\sigma_{OS}$ and over σ_{OS}, the comparator thresholds can have more linear distribution near its center effectively, as shown in Fig. 1(c).

From Eq. (3) and $\theta_B=\sigma_{OS}$, the probability of obtaining 'high' comparator outputs for an input signal voltage V_{IN} can be expressed as

$$P(V_{IN})=\begin{cases}1-\frac{1}{2}\left[\mathrm{erfc}(\xi_{IN}-\sqrt{2})\right] & \left(\xi_{IN}<-\frac{\sqrt{2}}{2}\right)\\ 2-\frac{1}{2}\left[\mathrm{erfc}(\xi_{IN}+\sqrt{2})+\mathrm{erfc}(\xi_{IN})+\mathrm{erfc}(\xi_{IN}-\sqrt{2})\right] & \left(|\xi_{IN}|\le\frac{\sqrt{2}}{2}\right)\\ 1-\frac{1}{2}\left[\mathrm{erfc}(\xi_{IN}+\sqrt{2})\right] & \left(\xi_{IN}>\frac{\sqrt{2}}{2}\right),\end{cases} \tag{4}$$

where $\xi_{IN}=(V_{IN}-V_{REF})/\sqrt{2}\sigma_{OS}$. The analytical expressions for this technique and the previous techniques are shown in Table I. To compare their non-linear characteristics, the following approximation is used under $|V_{IN}-V_{REF}|<\sigma_{OS}$.

$$P(V_{IN})\approx\frac{1}{2}+\frac{\alpha}{\sqrt{\pi}}\xi_{IN}-\frac{\beta}{\sqrt{\pi}}\xi_{IN}^3. \tag{5}$$

The coefficients α and β for each technique are also shown in Table I. Although the technique in [9, 15] ideally can eliminate the third-order non-linear distortion ($\beta=0$), its sensitivity ($\propto\alpha$) is degraded by a factor $1/\sqrt{e}$ compared with the conventional one. This can explain degradation of SNDR for small input signal as described above. On the other hand, the proposed technique can enhance sensitivity by a factor of $1+2/e^2$ and reduce third-order non-linear distortion by $1-6/e^2$, compared with the conventional one. The improvement factor of the third-order non-linear distortion is $(1-6/e^2)/(1+2/e^2)\approx 0.148$ (-16.6 dB). The linearization of the piecewise inverse Gaussian approximation in digital domain was proposed as a different approach [10]. However, it has no sensitivity enhancement

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and requires larger ensemble of comparators to enhance sensitivity. The proposed technique can relax significant input capacitance effect described in [10].

Even after using this modification of the PDF of the responding comparators, there remains non-linearity in the SF-ADC characteristics. To reduce residual non-linearity, re-quantization (RQ) in the digital domain is used, which was also proposed as D/A converter error calibration technique in feed-forward multi-bit Δ-Σ A/D modulators with the SF-ADC [16]. The digital re-quantizer consists of a programmable digital quantizer and a programmable coder, as shown in Fig. 1(e). The RQ characteristics can be finely adjusted by threshold data of digital comparator units in the programmable digital quantizer. Moreover, the programmable coder uses a fractional part to output codes in order to correct the non-linear codes, as shown in Fig. 1(f). The correspondence of coder inputs to the output data can be easily changed by the data of the register table. The number of bits of the coder output must be larger than the required resolution of the SF-ADC. The configuration data for a programmable quantizer and programmable coder can be determined after production by employing metaheuristics such as genetic algorithm (GA) [16]. The configuration data correspond to chromosomes. The minimum of effective-number-of-bits (ENOB) in input range was used so as to maximize as fitness function in this work. Differently from the linearization of the piecewise inverse Gaussian approximation [10], the RQ technique has tolerance for the assumption of Gaussian comparator offset distribution.

3 Circuit implementation

The SF-ADC is designed with a 1.2-V supply voltage in a 130-nm CMOS process. As shown in Fig. 2(a), it consists of parallel ensembles of comparators with reference selectors, followed by an ones adder. The comparator outputs are random digital outputs rather than thermometer code, thus an ones adder is designed to obtain the binary code. Based on previous study [14], number of comparator is 511 in this design, which is a relative small number considering high-speed sampling operation. In contrast to the previous works [9, 15], each comparator can have one of three differential references (V_{REFC}, $V_{REFC} \pm 2\sigma_{OS}$) according to its own input offset to realize the modified PDF of the responding comparators, $f_m(V_{IN} - V_{REF})$ shown in Eq. (3).

The two differential references $V_{REFC} \pm 2\sigma_{OS}$ (V_{REF84} and V_{REF16}) are generated using resistor-ladder D/A converters (DACs) shown in Fig. 2(b). The PMOS switches are used in the DAC considering output voltage range in this design. The stored data in the register of the DAC are determined in the foreground test which uses digital ramp signal to detect the input voltages for 16% and 84% 'high' comparator outputs as described in Sec. 2. To shift reference by $2\sigma_{OS}(-2\sigma_{OS})$, the voltages V_{TOP16} (V_{TOP84}) and V_{BOT16} (V_{BOT84}) are controlled with keeping the DAC switch selection for $-\sigma_{OS}$ (σ_{OS}) output through the register.

Fig. 2(c) shows the comparator circuit designed to realize high-speed operation over a broad band. In contrast to the previous design [9, 15]. The pre-amplifiers were not used to reduce power consumption and occupation area. The comparator core circuit is designed using small-size devices with minimum gate length

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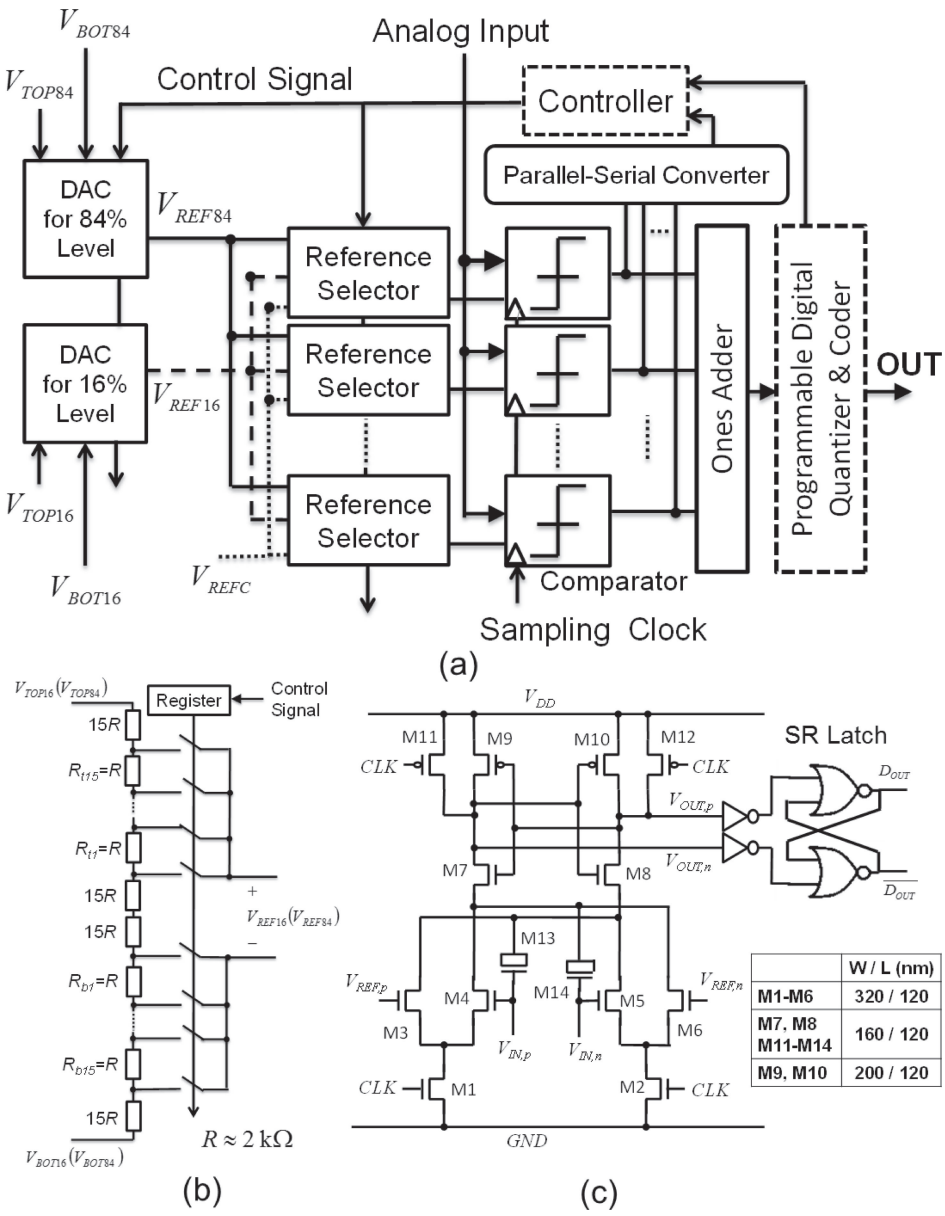

Fig. 2. (a) Configuration of proposed SF-ADC (dashed block: externally implemented), and schematics of (b) resistor-ladder DAC and (c) comparator in this design.

(120 nm). The NMOS capacitors M13 and M14 can suppress kickback noise. The SR latch maintains comparator output during sampling phase. Considering fan-out balance, its positive and negative outputs (D_{OUT} and $\overline{D_{OUT}}$) are provided to the ones adder and the parallel-serial converter for the controller, respectively.

The ones adder shown in Fig. 2(a) counts the number of comparators outputting 'high' (n_H) and outputs the n_H as binary code. It is implemented with hardware-efficient architecture called Wallace-tree ones adder. The output number of bits k determined by the total comparator counts N_{comp} must meet the inequality as follows,

$$k \geq \log_2(N_{comp} + 1). \tag{6}$$

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The Wallace-tree ones adder consists of $(k-1)$ stages of adders. In this design, $N_{comp} = 511$ and $k = 9$. To relax the timing requirement by pipelining [10, 16], D-flip-flops are placed after the first, the fourth, the sixth, and the last adder stages, resulting in three sampling cycles of the latency.

As this work focuses on the feasibility of the proposed SF-ADC, some digital blocks were not implemented on the integrated circuit. The controller in Fig. 2(a) was realized using LabVIEW FPGA (NI USB-7845R). In addition, the digital RQ shown in Fig. 1(e) was also implemented as software-based signal processing including optimization of the configuration data using MATLAB. The RQ in this work uses 127 levels (7 bits) and their 6-b fractional codes.

4 Experimental results

The test chip shown in Fig. 3(a) was fabricated in a 8-metal 130-nm CMOS process. The occupation area is $1.28 \times 1.40\,\mathrm{mm}^2$, and the power consumption is 3.26 mW at 100 MS/s sampling. The input-referred comparator offset in this test chip has the standard deviation as $\sigma_{OS} = 48.2\,\mathrm{mV}$ with 1.2-V supply voltage. The systematic offset of the comparator array was calibrated by tuning V_{REFC}, V_{TOP16}, V_{BOT16}, V_{TOP64}, and V_{BOT64} shown in Fig. 2(a). The first and the second adders have six and three stages of the Wallace-tree ones adder, respectively.

Fig. 3(b) shows the output spectra without and with the proposed OSDM. The input signal has amplitude of $1.2\sigma_{OS}$ (= 57.8 mV) and frequency of 8.78 MHz. The sampling rate is 100 MS/s. The values of SNDR without and with the proposed OSDM were 22.7 and 29.3 dB, respectively. The proposed OSDM can improve SNDR by about 6 dB. The enhancement of fundamental tone corresponds to enhancement of α ($20\log_{10}(1+2/e^2) \approx 2$ dB). The reduction of third-order harmonic distortion is smaller than expected one of β ($20\log_{10}(1-6/e^2) \approx -14.5$ dB based on Table I) due to non-ideal comparator offset distribution. Fig. 3(b) also demonstrates effectiveness of the digital RQ technique. The combination of the proposed OSDM and the digital RQ can achieve the SNDR of 32.1 dB.

Fig. 3(c) shows SNDR versus differential input amplitude (input signal frequency: 8.78 MHz, conversion rate: 100 MS/s). In contrast to OSDM in the previous works [9, 15], the proposed technique can improve SNDR even for small input signal region. To obtain optimized configuration data for the digital RQ, the GA optimization with population size of 60 and generation of 100 was carried out for input amplitude range from $\sim 0.2\sigma_{OS}$ to $\sim 5\sigma_{OS}$, which corresponds to the input range shown in Fig. 3(c). The crossover fraction in the GA optimization was 0.8, and the mutation was also introduced using default setting in MATLAB Global Optimization Toolbox.

The fabricated SF-ADC can achieve the similar SNDR at the sampling rate upto 110 MHz, as shown in Fig. 3(d). Considering difference in fabrication process, the operation speed is reasonable compared to sampling at 500 MS/s in the previous work (65-nm CMOS process) [15]. The different test chips also demonstrate similar characteristics described above.

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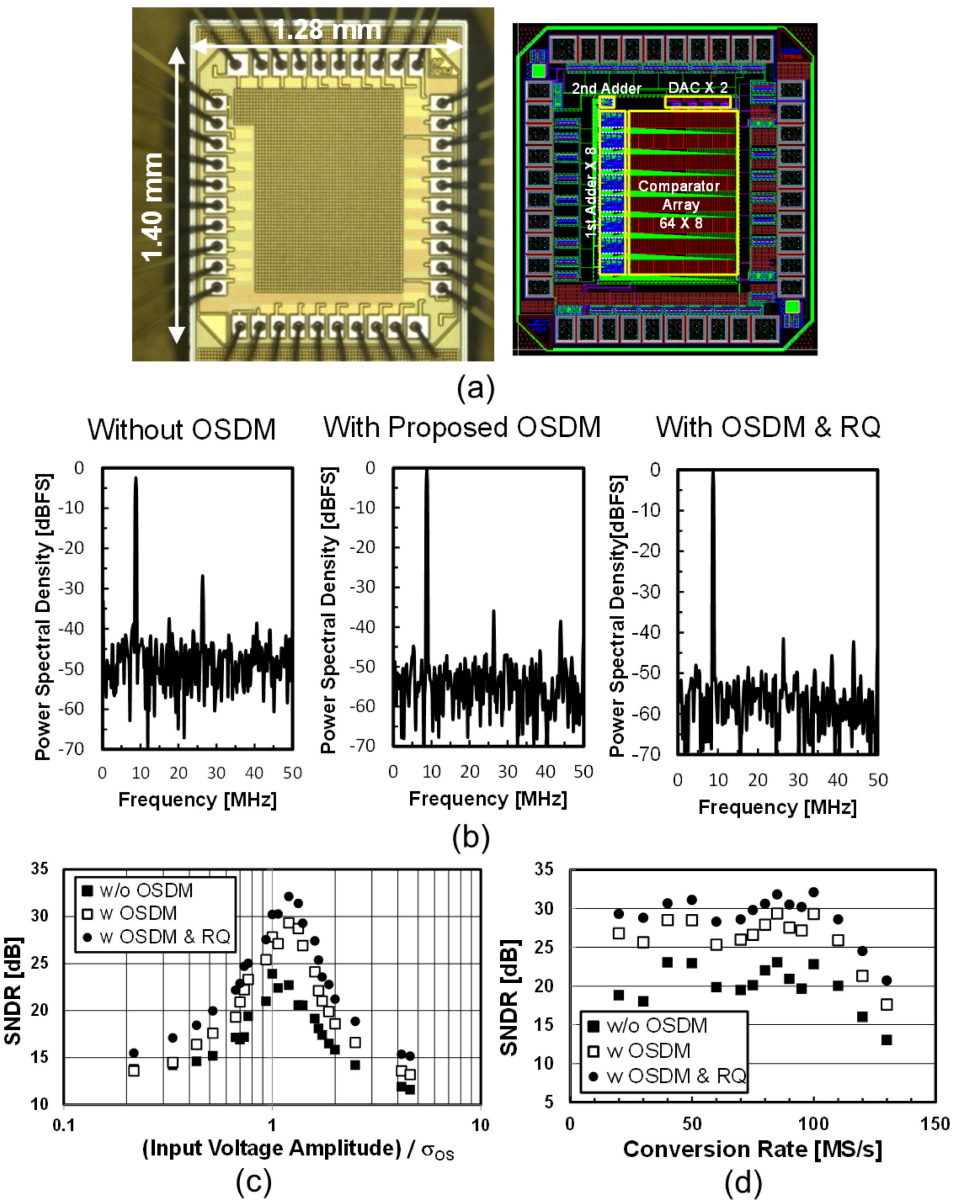

Fig. 3. (a) Micrograph (left) and physical layout (right) of the test chip, (b) FFT spectrum of the output data (differential input signal amplitude: $1.2\sigma_{OS}$ (= 57.8 mV), input signal frequency: 8.78 MHz, conversion rate: 100 MS/s), (c) SNDR versus differential input amplitude (input signal frequency: 8.78 MHz, conversion rate: 100 MS/s), and (d) SNDR versus conversion rate (input signal frequency: 8.78 MHz, differential input signal amplitude: $1.2\sigma_{OS}$.

5 Conclusion

The new OSDM technique for SF-ADCs was proposed. The proposed technique can improve SNDR even for small input signal region. In addition to it, the digital RQ can be applied for more linearity improvement, where quantization level and fractional correction can be optimized using GA. The SF-ADCs with the proposed techniques was fabricated in the 130-nm CMOS process and demonstrated its effectiveness.

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Since the present study is still preliminary, extensive future study is necessary. However, we believe that the present study will help to establish a new solution to the growing problem of device mismatch in advanced device technologies.

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