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論文内容の要旨

This thesis discusses the performance and reliability analysis in variation-aware VLSI (Very Large Scale Integration) design. With the advancement of semiconductor manufacturing process, CMOS (Complementary Metal Oxide Semiconductor) circuits are expected to gain their performances all the time. However, problems with regard to variation effects have become severe especially as the process technology reached below sub-100 nm. Such problems are attributed to unavoidable randomness that occurs during fabrication process and fluctuations depending on the circuit behavior. The former is called process variations and the latter is referred to as environmental variations. Process variation directly affects a device property, such as channel length, dopant density, and silicon dioxide film thickness. Environmental variations change dynamically during the operation time and are composed of voltage noise and temperature fluctuation. Voltage noises might induce a timing failure. The concentration of the heat not only causes the degradation of performance and reliability, but also could permanently damage a circuit. These variations can have a different impact on each device, even if two devices are adjacently located. Circuit designers must consider the effect of variations and predict the actual performance and reliability before chip fabrication.

This thesis first discusses thermal problems in local interconnects to understand how large degradation could arise from temperature variations. While thermal analyses for interconnects have been extensively studied, most of them focused on global wires that are located on high metal layers because the current flows in such wires are much larger than those in local wires and it was believed that the thermal problem should arise only in a global wire. However, this thesis reveals that such an understanding is not necessarily correct in future process technologies. Interconnect structures in a high-performance chip are evaluated in a practical condition based on ITRS (International Technology Roadmap for Semiconductors) prediction. The evaluation is performed with an electrical simulation of the actual circuit and a thermal simulation of the thermal circuit constructed with the materials and structure in a chip on the basis of an electrical-thermal analogy. A finite-difference approach is adopted to solve the heat diffusion equation. The experimental result shows that the maximum temperature difference between the hottest point in the wire and the Si (Silicon) substrate reaches to 40.4°C at 14-nm technology node, while it is 0.90°C at 90-nm process. It is also revealed that the temperature in a local signal wire will elevate more aggressively than that in the optimal repeater-inserted global wire as technology advances. There is a possibility that underestimation of the temperature in local wires may cause an unexpected reliability failure. On the other hand, it has a limited impact on their performance.

Next, this thesis provides a gate-delay model over wide range of PVT (Process-Voltage-Temperature) variations. The feature of the proposed model is an indirect modeling of a performance variation, which does not model the delay directly but focuses on an output-current fluctuation due to PVT variations. The proposed model is useful to characterize the performance of a circuit that suffers from PVT variations. It

modifies the output load and input waveform to embed PVT variations, and hence it can be used as a wrapper to any conventional models with a small amount of additional characterization cost. The accuracy of this model is validated by simulations using 90- and 45-nm process technologies, and it is revealed that the average error of the fall and rise delay estimation in single- and multi-stage gates is approximately 5% on average over a wide range of input slews, output loads, and PVT variations. Moreover, the proposed model can be used in statistical timing analysis in addition to corner-based timing analysis.

Post-silicon tuning is getting important as the amplitude of variations increases. The information of actual variations is required to compensate the performance and reliability appropriately. For this purpose, RO(Ring-Oscillator)-based sensors have been studied, because they can be easily implemented and measured. However, there were no specific guidelines on better RO component selection, variational parameter extraction technique, and design methodology. This thesis finally demonstrates to designers how to efficiently implement an RO-based variation sensing system in a chip. A parameter-extraction method using MLE (Maximum Likelihood Estimation) is devised. The proposed method explicitly considers random variations which were assumed to be canceled out, and achieves the enhancement of the accuracy compared to that neglecting random variations. Sensor selection methods are investigated and it is found that the RO selection using the condition number of the frequency-sensitivity matrix provides the most accurate estimation. It is also revealed that an RO component whose sensitivity is controlled could save the area o the whole sensor set.

論文審査の結果の要旨

本論文は、ばらつき考慮 VLSI 設計における性能・信頼性解析に関する研究の成果をまとめたものであり、以下の主要な結果を得ている。

1. ナノスケール VLSI 配線における自己発熱問題の評価

回路設計者は、チップの製造前段階で製造・環境ばらつきの影響を考慮し、 実際の回路の性能及び信頼性を予測することが求められる。本論文ではまず、ばらつきの一要因である温度変動によってナノスケール VLSI 配線に生じる性能・信頼性の劣化について評価を行った。高性能チップを仮定して行ったシミュレーション結果から、ローカル配線の温度上昇はプロセスの微細化に伴い急激に増加し、14 nm プロセスにおいては 40.4℃に達するという知見を得た。また、この温度上昇の要因を分析した結果、従来は重視されてこなかった配線断面積というパラメータが、28 nm プロセス以降では消費電力や絶縁材料と同等の温度上昇効果を持つということを示した。

2. 広範囲の製造・環境ばらつきに対応したゲート遅延モデルの提案

ばらつきは半導体製造プロセスの微細化が進むにつれ増大しているため、広範囲のばらつきに対し高精度な推定を実現するゲート遅延モデルが要求される。本論文では、遅延を直接モデル化するのではなく、電流変動をモデル化し、それに基づいて出力負荷及び入力波形に補正を行うことで、既存モデルにおけるばらつき対応を可能とした。90 nm 及び 45 nm プロセスを仮定したシミュレーションにより、5 種類のゲートについて、広範囲のばらつき下において平均 5 % 程度の誤差で遅延が見積り可能であることを確認した。

3. オンチップばらつきセンサを用いたデバイスパラメータ推定手法の提案

製造前に予測できるばらつきには限界があるため、製造後に性能を補償する技術が注目されている。そのような技術の実現にはオンチップばらつきセンサを用いたパラメータ推定が必須となるが、高精度なパラメータ分離法はまだ実用段階に至っていない。本論文では、最尤推定法を用いてランダム成分の影響を考慮することにより、高精度な推定を実現した。また、3 種類のセンサ選択法を比較した結果、感度行列の条件数を利用する手法において、従来手法と比べてパラメータ推定誤差を 11.1％～73.4 % 削減可能であることを示した。

以上のように、本論文で述べたばらつき考慮 VLSI 設計における性能・信頼性解析に関する研究は、ばらつきの影響が増すなか、設計者の想定通りに動作する回路の製造を容易にするという点で非常に有用である。これにより、回路性能・信頼性の継続的な向上に貢献するものと期待できる。従って、博士（情報科学）の学位論文として価値のあるものと認める。