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<th>A Study on Accurate Delay Estimation Considering Process and Supply Voltage Variations</th>
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Osaka University
This thesis discusses the modeling and estimation methods for gate delay variation due to manufacturing variability and power supply noise. As the LSI (Large Scale Integrated Circuit) process technology advances and the device feature size scales, process variation becomes a critical issue in designing LSI products. In addition, current density in a chip has been increasing because of higher operating frequency and larger power consumption, which causes larger temporal power supply noise due to IR and Ldi/dt drops. Deeper in supply voltage intensifies the concern about noise induced performance fluctuation, since it makes the gate delay sensitive to the voltage fluctuation. Traditionally, the performance fluctuation due to these process and supply voltage variations are managed with timing margins empirically assigned in the conventional corner-based timing analysis, which often results in inaccurate and over-constrained designs. Coping with the key issue for the successful chip design in recent technologies.

For estimating the performance fluctuation due to process variation, SSTA (Statistical Static Timing Analysis) is expected to be a fundamental solution and intensively studied. SSTA calculates and propagates probability distributions of signal arrival times, instead of deterministic worst-case values, in a statistical manner according to the statistics of process parameter variations. It can eliminate excessive timing margin involved in conventional corner-based analysis, and then many researchers have focused on its gate delay modeling and estimation methods for the statistical distribution. Conventionally, linear sensitivities to the parameter variations are widely used in the gate delay modeling. On the other hand, the transition-times at gate inputs and outputs have not been discussed earnestly so far, though the input transition-time of a gate varies owing to process variation and the variation of the transition-time affects the gate delay distribution. To accurately estimate delay variations due to process variations, this research tackles with the variation of output transition-time under process variations. First, the variation of output transition-time is investigated under threshold voltage fluctuation as representative process parameters. The investigation shows that conventional linear sensitivity based modeling induces a considerable inaccuracy in the estimated transition-time variations, particularly for specific combinations of input transition-time and output load. Instead, the proposed estimation method combines the linear and quadratic relations. Experiments for accuracy clarification show that the proposed method could improve the estimation error at least 60% at maximum and 40% in contrast to the process variations, the impact of supply voltage fluctuations on gate delay has not been comprehensively studied, and its estimation method has not been well established yet. In current industrial design flow, the dynamic nature of the supply voltage fluctuation is ignored, and the average voltage within a cycle time, i.e. static IR drop, is used to take into account the impact of supply noise on circuit delay. However, the meaning of static noise based timing estimation has not been clarified. This work firstly discusses the effectiveness and limitation of IR drop based analysis and shows that it appropriately estimates the fluctuations for paths with large stages, i.e. setup critical paths. On the other hand, it is not appropriate for short paths. Thus, this thesis presents an estimation method of the stage delay fluctuation under given dynamic noise waveform, which overcomes problems found in reviewing conventional method at 45nm technology. The proposed method considers not only gate delay increase but also the decrease due to supply voltage drop, similarly to the conventional method, and the method is improved. The evaluation results show that the proposed method estimates stage delay fluctuations within 1% on average with 2.7% standard deviation. In digital CMOS circuits, setup and hold times of Flip-Flops, in addition to propagation delay of combinational gates, also play important roles in timing analysis, and hence the dependencies of setup and hold times on the dynamic voltage waveform are also investigated. Experimental evaluation shows that the setup time is sensitive to voltage drop waveform, and the dependence should be taken into consideration. On the other hand, it also reveals that the hold time is less sensitive as long as it is characterized with an ordinary configuration of industry practice, and the dependence is not necessary to be explicitly considered. According to these observations, this thesis also improves the proposed gate delay estimation so as to estimate Flip-Flop setup time and shows that the setup time fluctuations under the dynamic power supply noise can be estimated with 5% error on average.
だが、電源ノイズ下でのこれ等の見栄え方法は、従来検討されていなかった。本研究では、セットアップ・ホールドタイムの電源ノイズ依存性について調査し、セットアップタイムの電源波形に対する依存は高く、電源ノイズを考慮した見栄えが必要であること、および、ホールドタイムの依存は低く、標準電圧での値を使用可能との結果を得た。この結果に基づき、でのポート送信及複数手法をセットアップタイムに対して拡張し、平均対策を考慮する良好な結果を得た。

以上のように、プロセス・電圧による小さいタイミング解析に関する研究は、プロセス世代の進化に伴い増大する処理波形を変数する手段として非常に有用であり、これにより、深層化しつつあるタイミング依存性の向上に貢献するものと期待できる。従って、博士（情報科学）の学位論文として価値のあるものと認める。