Doctoral Dissertation

Studies on Thermal Characterization and Analysis of Packaged SiC Devices for High Temperature Applications

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Dedicated to my wife Yunhee

Abstract

Recently, silicon carbide (SiC) semiconductors, one of the wide band gap semiconductors, have received a great attention as a promising device to replace Si power devices in power conversion systems due to their superior material properties. The SiC devices offer high temperature operation capability of 200°C that is higher than the limitation temperature of the general Si devices, and it is expected to increase power density and to reduce a size of power conversion systems. In high temperature operation of the SiC devices, the thermal management is important, because the thermal margin of the packaged devices is shrunk. In addition, the thermal properties of the package materials such as thermal conductivity and specific heat are affected by temperature, and this effect results in variation of the thermal performance of the packaged semiconductor. In order to operate the SiC devices, stably, at high temperature environment, the accurate thermal analysis of the packaged device is necessary. In this dissertation, the thermal measurement and analysis of the packaged SiC devices is introduced for high temperature applications. This dissertation is organized as follows:

In chapter 1, background and related trend of research are reviewed. In addition, objectives and outline on this research are introduced.

In chapter 2, the fundamental theories for the thermal analysis of packaged SiC devices are presented. The heat transfer mechanism, the finite difference method (FDM), the compact thermal model, and the thermal measurement and characterization methods are described.

In chapter 3, thermal characteristics of a packaged SiC device for high temperature operation is investigated. The numerical thermal simulation of the packaged SiC SBD using finite difference method (FDM) is carried out considering the nonlinear thermal properties of the package materials. The transient thermal resistances of the packaged SiC SBD are experimentally measured, and compared with the simulated results. It is observed that the time constant of the transient thermal resistance and the steady state thermal resistance of the packaged SiC SBD are prolonged and increased for the temperature rise, respectively.

In chapter 4, the temperature dependence of partial thermal resistances of a packaged SiC SBD is analyzed at elevated temperature environment. The partial thermal resistances of the packaged SiC SBD are extracted from the transient thermal resistances using the cumulative and differential thermal structure functions. The extracted partial thermal resistances are compared to the results from the numerical simulation model, and the comparison results show good agreement. The temperature dependence of the partial thermal resistances of the SiC device and the Si_3N_4 substrate contribute to the overall thermal resistance variation of the packaged SiC SBD.

In chapter 5, new approach for the thermal measurement of a packaged SiC MOSFET is introduced.

In the thermal measurement, a relationship of gate-source voltage and temperature of the SiC MOSFET measured using constant current pulses is employed to measure junction temperature. The transient thermal resistance of the packaged SiC MOSFET is measured with the constant power injection in heating condition. A modified thermal resistance analysis by an induced transient (TRAIT) method is suggested for the thermal characterization of the packaged SiC MOSFET. The modified TRAIT method characterizes the measured transient thermal resistance with the discrete time constant spectrum and the thermal structure functions. The results from the modified TRAIT method showed good consistency with that of the network identification by deconvolution (NID) method. The thermal compact model of the packaged SiC MOSFET based on a Cauer equivalent thermal network is extracted and validated using the experimentally measured results in transient temperature response of the device. The partial thermal resistances of the packaged SiC MOSFET are compared and analyzed with results from the conventional NID and the numerical FDM simulation.

Chapter 6 concludes this dissertation with the achieved results, and future tasks are discussed.

Keywords: SiC, SBD, MOSFET, Thermal analysis, Finite difference method, TRAIT, Partial thermal resistance, Thermal structure function.

Contents

Chapter 1:
Introduction

1.1 SiC power devices

In recent years, the power conversion systems to increase the energy efficiency have received great attention due to environmental problems and exhaustion of fossil fuels [1],[2]. The power conversion systems such as DC-DC converters, AC-DC converters, and inverters convert the electrical power from one type into another type. In the power conversion system, one of the essential elements is power semiconductors. The power semiconductors are devices that have capability to handle the large current and high voltage to switch the high power, and the ideal power semiconductor is required to support the ability to flow the high power with zero power dissipation and fast switching speed [3].

Until recently, the main power devices are based on silicon (Si) technology. The Si based power devices have covered requirements of power conversion systems up to now, satisfactorily. However, the Si based power devices show limitation of technical development due to its physical limitations [4]. The Si based power devices are shown to not meet requirements for future power conversion systems that require fast switching and low power loss such as electric and hybrid vehicles, high power conversion systems for wind and photovoltaic power generation.

Silicon carbide (SiC) is one of the wide bandgap semiconductors, and is the most promising alternatives to Si in power devices due to its superior electrical, mechanical and thermal characteristic [5]-[7]. Among the SiC semiconductors, 4H-SiC has received the most attraction compared to other SiC materials due to their inherent material properties, quality of the crystal growth, and the maturity of manufacturing process [8],[9]. The 4H-SiC semiconductor exhibits about 10 times higher breakdown electric field strength, 3 times higher band gap, and 3 times higher thermal conductivity than Si. Table I shows the comparison of the electrical, material, and thermal properties between Si and 4H-SiC materials [7]-[10].

Currently, SiC schottky barrier diodes (SBDs), SiC junction field effect transistors (JFETs) and SiC metal oxide field effect transistors (MOSFETs) have been researched actively, and several SiC devices are commercially released by some manufactures. The SiC SBDs have ability of much lower reverse recovery current and recovery time compared to Si diodes, and the SiC SBDs have been employed in several power conversion system such as switch-mode power supplies,

photovoltaic power conversion system, and electric, hybrid vehicles [11-13]. As the switching power devices, SiC JFETs have been introduced, primarily, due to simple device structures [14],[15]. Although SiC JFET shows the fast switching speed, low power loss and high temperature operation capability, it is shown the limitation of the acceptance from the power conversion system due to the normally on characteristics. It has been reported that the research results about the SiC JFET with normally off characteristics [16-18].

SiC MOSFETs have been received attention as a promising device to replace Si IGBTs used for high voltage, high current power conversion applications in an industrial, consumer and automotive system, prevalently. Development of SiC MOSFETs has been reported through the several research results [19-22]. The SiC MOSFET have shown the various advantages such as high voltage, low on-resistance, fast switching speed, and high temperature operation compared to Si IGBTs. We expect to develop the power conversion system with improved efficiency, high reliability, and shrunk size with SiC devices.

Table 1.1 Comparison of the material properties between Si and 4H-SiC materials at room temperature.

Parameters	Si	4H-SiC
Energy band gap E_G (eV)	1.11	3.26
Intrinsic carrier concentration n_i (cm^{-3})	1.4×10^{10}	6.7×10^{-11}
Electron affinity X_s (eV)	4.05	3.7
Saturation drift velocity v_{sat} (cm/s)	1×10^{7}	2.1×10^{7}
Break down electric field E_B (V/cm)	2.5×10^{5}	2.2×10^{6}
Relative dielectric constant (ε_s)	11.7	9.7
Thermal conductivity (W/cm·K)	1.5	3.7

1.2 Thermal analysis of packaged SiC devices

1.2.1 Researches of thermal analysis of packaged SiC devices

In operation of the SiC devices, the static (conduction) and dynamic (switching) losses increase the device temperature due to the self-heating effect. The self-heating effect is well-known concern for the SiC devices, because the device temperature affects the electrical characteristic, life time, and reliability. The carrier mobility of the SiC semiconductor decreases with temperature rise, and it results in the increase of the drift region resistance required to support the blocking voltage [5]. The

forward voltage drops in *p-n* junction and schottky junction of SiC diodes and the threshold voltage of the SiC MOSFETs decrease with the temperature rise [14],[22]. The reverse leakage currents of the SiC devices increase with temperature rise [5]. These effects result in the variation of the electrical performance of the power conversion system such as the efficiency and noise characteristics. Furthermore, the operation of the semiconductors over the safe temperature range results in permanent damage or destruction [23],[24].

The temperature changes the mechanical characteristics of the package component materials. The variation of the temperature induces the mechanical stress of the package components such as the semiconductor devices, the solder, the bonding wires, and the substrates due to their different thermal coefficients [26],[27]. The cracks in interface parts inside the package are the typical example of such mechanical stress.

In order to operate the packaged SiC device, safely, the junction or device temperature must be managed under the safe operation region. Under the appreciated thermal management, the generated heat from the operation of the SiC devices can be transferred through the package and removed by the heat dissipation system such as a heat sink or the convection mechanism. The thermal characteristics of the packaged SiC devices such as the transient or static thermal resistances are very useful in the design of the thermal management system by providing the information on the thermal description inside the assembled package. Therefore, the analysis on the thermal characteristics of the packaged SiC devices is a fundamental issue in development of the power conversion system using the SiC devices.

Due to these reasons, the research on the thermal analysis for the packaged SiC devices has been carried out. Many researches have focused on the electro-thermal effect of the SiC devices. These researches have introduced the physical and analytical models of the electrical characteristics of the SiC devices that are combined with the thermal models that have the numerical type or the compact type that consist of the linear passive resistance-capacitance elements. They have tried to describe the electrical behavior variation of the SiC devices due to the self-heating in the device operation [28]-[30].

On the other hand, there are few researches that deal with nonlinear thermal characteristics of the SiC devices. The nonlinear thermal model of the SiC SBDs has been developed based on the temperature dependence in thermal conductivity and specific heat which have been extracted from the measured transient thermal responses in [31]. The nonlinear thermal compact models considering the dissipated power of the SiC devices have been introduced, and verified experimentally in [32]. Both research results have shown the significant differences in thermal responses between the linear and nonlinear models, and the nonlinearity should be considered to estimate the exact junction temperature of the SiC devices.

Since the SiC power devices in the mentioned researches have been packaged with a commercial transfer molding and can't be operated in high temperature environment. Currently, packaging technologies have been developed for high temperature operation of SiC power devices [33],[34]. These technologies include a copper bonded substrate with low thermal resistance, bonding materials and encapsulation materials with high temperature withstanding capability. In [35], the comparison of the static thermal performance of the packaged SiC SBD with the high temperature solders has been carried out with the experiment and numerically simulated results with finite element method (FEM). In addition, the evaluation on the electro-thermal responses of the SiC modules in high temperature environment has been carried out with comparison between the measured and numerically simulated results with finite difference method (FDM) [36].

1.2.2 The thermal properties of packaged SiC devices for high temperature operation

As previously mentioned, the generated heat from the power loss of the semiconductor device transfers through the package, and thermal properties are important factors to determine the heat transfer ability of the package: heat capacity and thermal conductivity. The solid substance is composed of free electrons and atoms bound in periodic structures termed lattice. The atoms bound in the lattices vibrate with frequencies and amplitudes, and these vibrations are coupled with that of adjacent atoms. Where, the vibrations of the atoms are termed with phonon. The vibrational movements of the atoms produce elastic waves that propagate though the lattices, and it results in atomic displacement.

The thermal properties are dependent on the energies of the free electrons and atoms. The thermal energy is represented by the energy of all phonons and all free electrons at given temperature. When heat is supplied into the substance, then the temperature of the substance increases with the rise of the internal thermal energy. Heat capacity means the ability of the material to store the thermal energy as it changes in temperature. The heat capacity is often replaced by the specific heat, the heat capacity per unit mass of a material [37].

The heat transfer is mainly carried out by the migration of the free electron and the phonon. In the solid substance that has temperature gradient, the net movement of phonons transfers the thermal energy from high to low temperature regions, and also, the free electrons gained a kinetic energy in high temperature region, migrate to the low temperature regions where, the free electrons transfer their kinetic energy to atoms through collision with phonons. Thermal conductivity is ability to transfer the thermal energy by both phonons and free electrons. For the conductors, the thermal conductivity is dominated by the effect of the migration of free electrons, because there are large number of the electrons participated in the transportation, while the heat conductivity of the

nonconductor is mainly depended on the phonon effects, because they are absence of the numbers of free electrons. Generally, the migration of the free electrons is much more efficient than phonons in thermal energy transportation because the free electrons have higher velocities and is less affected by phonons scattering by lattice imperfections, so that the thermal conductivities of the conductor have higher values than that of the nonconductor.

In temperature ranges of the semiconductor operation, for the package component materials such as the copper, the ceramics, and Si or SiC materials, the phonon scatterings increase with temperature so that the migration of the free electrons is interrupted. It results in the variation of their thermal conductivity [38]. The average thermal energy of the phonons and free electrons increases with the temperature rise, and it results in the increase of the heat capacity. The temperature dependence of the heat capacity can be represented by the Debye model [39].

The effect of the temperature dependent thermal properties may be particularly critical for the SiC devices compared to the Si devices, because the SiC device has the operation capability in the wide temperature range. The conventional Si devices have limitation operation temperature about 150°C ~ 170°C, but The SiC devices shows the operation ability in high temperature environment over 200°C [7],[36]. The wider temperature change induces the larger thermal properties variation. Consequently, the variation of the thermal properties of the package materials results in change of thermal characteristics of the packaged device such as thermal resistance and capacitance. Therefore, thermal characteristics analysis considering temperature effects is required for high temperature operation of the packaged SiC devices.

1.3 Research objectives and outline

This dissertation focuses on the thermal measurement and analysis of the packaged SiC devices for high temperature applications. The main objectives of this dissertation are transient and steady state thermal analysis on the packaged SiC SBD with temperature dependent thermal properties, and investigation of the temperature dependence of partial thermal resistances of the packaged SiC SBD for high temperature applications. In addition, new methodology for thermal measurement and characterization for the packaged SiC MOSFET is proposed. This dissertation is structured as follows:

Chapter 1 gives a background on this research. The electrical, material, and thermal properties of SiC materials are presented. In addition, researches on the thermal analysis of the SiC devices are briefly reviewed, and the research objectives and outline are described.

In chapter 2, the fundamentals for the thermal analysis of the packaged SiC devices are presented. The heat transfer mechanism, the finite difference method (FDM), the compact thermal model, and the thermal measurement and characterization method are explained.

In chapter 3, it is described that analysis of thermal characteristics of the packaged SiC SBD for high temperature operation. The finite difference thermal model considering the temperature dependent thermal properties is introduced. The measurement procedure for the transient thermal resistances of the packaged SiC SBDs is described, precisely. The comparisons between the numerically simulated and experimentally measured results are carried out, and the thermal performances of the packaged SiC SBD are discussed.

In chapter 4, the temperature dependence of partial thermal resistances of the packaged SiC SBD is investigated. The transient thermal resistances are measured at elevated temperature conditions and characterized using the cumulative and differential thermal structure functions. The extracted partial thermal resistances of the packaged SiC SBD are compared to the results from the finite difference thermal model. Finally, the partial thermal resistances of the packaged SiC SBD are analyzed and discussed.

In chapter 5, the new thermal measurement and characterization method for the packaged SiC MOSFET is introduced. The transient thermal resistance of the packaged SiC MOSFET are measured and compared with the results from the FDM numerical thermal simulation. Transient thermal characteristic of the packaged SiC MOSFET is modelled based on a Cauer network and validated with experimentally measured results. The analysis on partial thermal resistance of the packaged SiC MOSFET is carried out using the modified thermal resistance analysis by an induced transient (TRAIT) method, the network identification by deconvolution (NID) method, and the FDM thermal simulation.

Chapter 6 concludes this dissertation and the achieved results of the research are summarized.

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Chapter 2:

Fundamentals of thermal analysis for packaged SiC devices

2.1 Fundamentals of heat transfer theories

In the packaged semiconductor device, three heat transfer mechanisms play a role to determine the temperature of the package, namely, conduction, convection, and radiation [1],[2]. The heat from the power loss of the semiconductor device transfers through the package component materials by the conduction. The conduction is thermal energy transfer due to the temperature gradient by microscopic collision of particles and movement of electrons in the substance. The governing equation of the heat conduction is defined by:

$$\ddot{q}_{\text{cond}} = -\lambda \cdot \nabla T \tag{2.1}$$

where $\ddot{q}_{\text{cond}}$ is the heat flux (W/m^2), and λ is the material property known as the thermal conductivity of the substance (W/m·K), respectively. ∇T is the three-dimensional temperature gradient, and the negative sign means that the heat transfers is directed from high to low temperature, respectively.

The transferred heat that reaches the surface of the package is dissipated by the convection. The convection is the thermal energy transfer as a result of random motion of fluids from one place to another. The natural convection is caused by buoyancy forces due to the density variations that result from the temperature variation within the fluid. The forced convection results from the movement of the fluid forced by external sources such as fans, pumps, or atmospheric winds. The governing equation of the convection is defined by:

$$\ddot{q}_{\text{conv}} = h(T_s - T_\infty) \tag{2.2}$$

where $\ddot{q}_{\text{conv}}$ is the convective heat flux (W/m^2), and h is convective heat transfer coefficient (W/m^2·K). T_s and T_∞ are the surface temperature of the substance and the fluid temperature, respectively. The convective heat transfer coefficient is depended on the physical properties of the fluid and physical condition between the substance and the fluid.

All substances with temperature above absolute zero radiate the energy, and the heated semiconductor package transfers heat by the thermal radiation, too. The thermal radiation is the

energy transmission in the form of waves or particle from the surface of these substances. The heat flux ($\ddot{q}_{\text{rad}}$) emitted by the substance is defied by:

$$\ddot{q}_{\text{rad}} = \varepsilon\sigma(T_s^4 - T_\infty^4) \tag{2.3}$$

where ε is the radiative properties of the substance known as emissivity, and σ is the Stefan-Baltzmann constant (σ=5.67× 10^{-8}W/m^2·K^2).

2.2 Finite difference method

It is very difficult to solve the partial differential equations of the mathematical physic, directly, for most real cases that deal with nonlinearities, complicated geometries, and complex boundary conditions. Presently, the numerical methods are very frequently used to solve the partial differential equations for many real cases. Finite difference method (FDM) is one of the simplest methods to solve partial differential equations [3]. In FDM, the partial differential equations are replaced with the approximated discrete algebraic equation near the node, and are solved through analytical calculation. The FDM is easy to structure the formulation and has less computational work than other numerical analysis method such as finite element method (FEM), and can be helpfully applicable to solve the engineering and scientific problems that have partial differential equations with simple geometric models [4].

Generally, there are three types of the finite difference approximation: forward, backward, and central difference, and these approximations can be induced from Taylor's theorem. Figure 2.1 shows the finite difference approximation related to forward, backward, and central difference approximation at point x_i. Using the Taylor series expansion, the function $f(x)$ at x_i is expressed as follows:

$$\begin{aligned} f(x) = f(x_i) + f'(x_i)(x-x_i) + \frac{f''(x_i)}{2}(x-x_i)^2 + \frac{f'''(x_i)}{3!}(x-x_i)^3 + \\ \cdots + \frac{f^n(x_i)}{n!}(x-x_i)^n + \cdots = \sum_{n=0}^{\infty}\frac{f^n(x_i)}{n!}(x-x_i)^n \end{aligned} \tag{2.4}$$

By expanding the function $f(x)$ at x_{i+1} about the point x_i:

$$f(x_i + \Delta x) = f(x_i) + f'(x_i)\Delta x + \frac{f''(x_i)}{2}\Delta x^2 + \frac{f'''(x_i)}{3!}\Delta x^3 + \cdots \tag{2.5}$$

Equation (2.5) can be rearranged as follows:

$$f'(x_i) = \frac{f(x_i + \Delta x) - f(x_i)}{\Delta x} - \underbrace{\frac{f''(x_i)}{2}\Delta x - \frac{f'''(x_i)}{3!}\Delta x^2 + \cdots}_{\text{TruncationError}} \tag{2.6}$$

where the first term of the right hand side is definition of the first order derivate of the function $f(x)$ at the point x_i. If Δx is a sufficiently small quantity, then remaining of the series expansion after the first term in the right hand side of eq. (2.6) can be neglected in the calculation of the $f'(x_i)$, and this is referred to as the discretization error or the truncation error. This is known as a **forward difference** approximation because the derivate uses x_{i+1} that is a forwarded point from x_i by an increment Δx.

If the function $f(x)$ is expanded at x_{i-1} about the point x_i, then the derivate function $f'(x_i)$ can be written as:

$$f'(x_i) = \frac{f(x_i) - f(x_i - \Delta x)}{\Delta x} + \underbrace{\frac{f''(x_i)}{2}\Delta x - \frac{f'''(x_i)}{3!}\Delta x^2 + \cdots}_{\text{TruncationError}} \tag{2.7}$$

The first term of the right hand side of the Eq. (2.7) is called by the **backward difference** approximation.

The **central difference** approximation for the first derivative is obtained by combining eq. (2.7) and eq. (2.6), and it is expressed as follows:

$$f'(x_i) = \frac{f(x_i + \Delta x) - f(x_i - \Delta x)}{2\Delta x} + \underbrace{\frac{f'''(x_i)}{3!}\Delta x^2 - \frac{f^5(x_i)}{5!}\Delta x^4 + \cdots}_{\text{TruncationError}} \tag{2.8}$$

The orders of the first term in the truncation errors represent the order of the error magnitude. The forward and backward difference approximations have the error of the first order, while the central difference approximation has the error of the second order. Considering the order of the error magnitude, the central difference approximation has the better approximated result in the first derivative than the forward and backward difference approximations.

Based on the upper three approximations, the heat transfer partial thermal equation for the packaged SiC devices can be discretized. The heat transfer governing equation inside the packaged device, the discretized process, FDM equations, and thermal analysis are introduced in chapter 3.

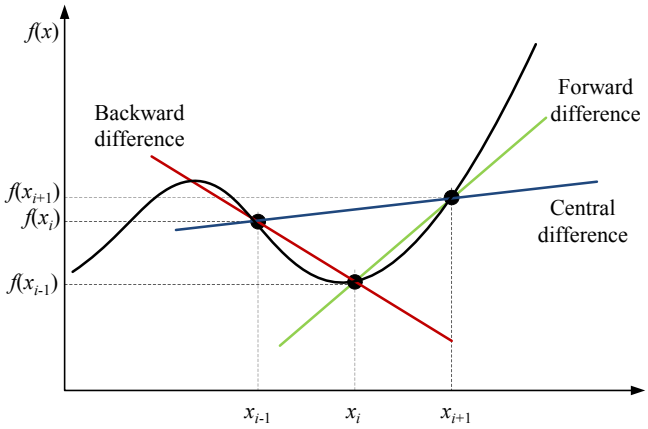

Fig. 2.1 Finite difference approximation related to forward, backward, and central difference approximation.

2.3 Compact thermal network model

2.3.1 Transient thermal resistance of packaged semiconductor device

Usually, transient thermal characteristics of the packaged semiconductor device are expressed by the transient thermal resistance [5],[6]. The transient thermal resistance of the packaged semiconductor device is defined as a ratio of the temperature difference between the junction and reference point to the dissipated power as a function of time, and means the one dimensional thermal characteristic of the package materials to oppose the generated heat flow from the device. The mathematical expression of the transient thermal resistance (Z_{th}) is represented as follows:

$$Z_{th}(t) = \frac{T_j(t) - T_r(t)}{P_d} \tag{2.9}$$

where T_j is the junction temperature of the semiconductor device, T_r is the reference temperature, and P_d is the dissipated power in the device, respectively. Generally, there are two reference points. One is a case that is the interface point between package and ambient, and another is ambient whose temperature is not affected by the semiconductor heating. The transient thermal resistance between the junction and case can be used to design a heat sink for a power electronics application, and can be used in thermal analysis on the inside of the package according to the heat path [7],[8]. While the transient thermal resistance between the junction and ambient can be used in operation of the power devices without any heat sink [9].

Traditionally, the junction temperature of the packaged semiconductor device can be calculated

using the estimated power from the electrical characteristics of the device and the transient thermal resistance between the junction and case, and the heat dissipation system can be designed considering the desired junction temperature. The measurement and analysis for transient thermal resistance is one of very interesting areas for the thermal and package engineer, and the many researches have been carried out [10]-[14].

Figure 2.2 shows the compact thermal network with the thermal resistances and capacitances to express the transient thermal behavior of the packaged semiconductor device between the junction and reference point. As described the previous chapter, the materials for the package components have the thermal properties: the thermal conductivity and specific heat, and the thermal characteristics of the packaged device are determined by these properties and the geometrical structure of the package for the heat flow path from the semiconductor.

The thermal resistance (R_{th}) and capacitance (C_{th}) are defined by:

$$R_{th} = \frac{L}{\lambda \cdot W} \tag{2.10}$$

$$C_{th} = m \cdot c = \rho \cdot V \cdot c \tag{2.11}$$

where λ, ρ, and c are the thermal conductivity, the density, and the specific heat of the package materials, respectively. L, W, m, and V are the length, the area, the mass and the volume of the package materials for heat flow path, respectively.

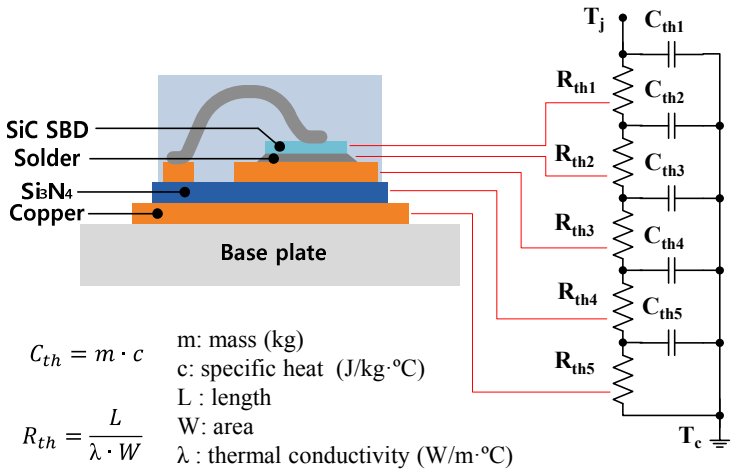

Fig. 2.2 The cross sectional view of the packaged semiconductor devices and the compact thermal network with the thermal resistances and capacitances.

Because the transient thermal resistance of the packaged semiconductor device between the junction and case represents a step response of the thermal characteristics including the thermal properties and the structure factors of the package, and the thermal system of the packaged semiconductor device can be obtained from the transient thermal resistance.

2.3.2 Foster and Cauer equivalent thermal network

The transient thermal resistance of the packaged semiconductor device can be modelled by resistances and capacitances passive component considering the analogy between electrical and thermal domains [5],[15]. The table 2.1 shows the contrast in thermal-electrical analogy.

Table 2.1 Contrast in thermal-electrical analogy

Electrical domain			Thermal domain		
Variable	Symbol	Unit	Variable	Symbol	Unit
Current	I	A	Power	P	W
Voltage	V	V	Temperature	T	°C
Electrical resistance	R	Ω	Thermal resistance	R_{th}	°C/W
Electrical capacitance	C	C	Thermal capacitance	C_{th}	J/°C

There are two canonical forms to describe the thermal system, namely, the Foster and the Cauer equivalent network [16],[17]. The Foster equivalent thermal network has a basic element that has a connection between the resistance-capacitance in parallel as shown in Fig. 2.3

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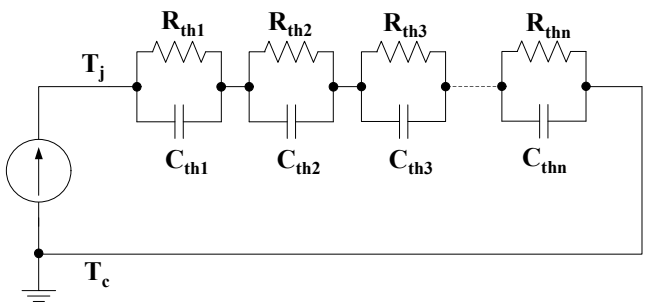


Fig.2.3 Description of the Foster equivalent thermal network.

The transient thermal resistance can be described by the following transfer function considering the Foster equivalent thermal network.

$$Z_{th}(s) = \sum_{i=1}^{n} \frac{1}{C_{thi}s + 1/R_{thi}} \tag{2.12}$$

The Foster equivalent thermal network can express directly the exponential term that describes the transient temperature change of the substance. Using the Foster equivalent thermal network, it is easy to express the complex thermal behavior of the packaged semiconductor device. However, the elements in this thermal network have no physical signification. The heat should flow through one direction from the source to the sink. However, the configuration of the resistance-capacitance elements permits the bidirectional heat flow in this thermal equivalent network.

The Cauer form is used to accord the physical signification to the elements in the equivalent thermal network. The Cauer equivalent thermal network has a basic element that has the connection between the resistance and capacitance connected to ground as shown in Fig. 2.4.

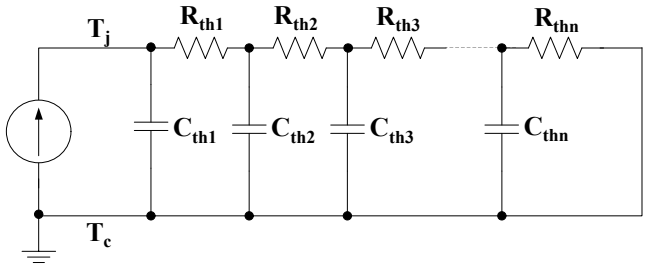


Fig.2.4 Description of the Cauer equivalent thermal network.

Considering the Cauer equivalent network, the transient thermal resistance can be described by the following transfer function.

$$Z_{th}(s) = \cfrac{1}{C_{th1}s + \cfrac{1}{R_{th1} + \cfrac{1}{C_{th2}s + \cdots + \cfrac{1}{R_{th,i}}}}} \tag{2.13}$$

In the Cauer equivalent thermal network, R_{thi} and C_{thi} represent the ability to interrupt the heat flows by the conduction and the thermal mass to store the thermal energy in the physical structures, respectively, and nodes express the interface points between the stacked structures. Using the Cauer equivalent thermal network, it is possible to monitor the thermal state of each part of the packaged

device, and to express the thermal behavior variation of the device with expansion of the thermal system due to the connection of the additional physical structures such as the heat sink.

The several identification methods can extract directly the values of the elements based on the Foster equivalent thermal network, and the configuration of the Cauer equivalent thermal network can be carried out through the Foster to Cauer network conversion [18],[19]. The basic algorithm of the Foster to Cauer conversion is described below. The transfer function in the Foster equivalent thermal network shown in Eq. (2.12) is expanded as follows:

$$Z_{th}(s)=\sum_{i=1}^{n}\frac{1}{C_{thi}s+1/R_{thi}}=\frac{a_{n-1}s^{n-1}+a_{n-2}s^{n-2}+\cdots+a_1s+a_0}{b_ns^n+b_{n-1}s^{n-1}+\cdots+b_1s+a_0} \tag{2.14}$$

Dividing the denominator by the numerator, Eq. (2.14) is expressed as follows:

$$\begin{aligned}Z_{th}(s)&=\frac{1}{\dfrac{b_ns^n+b_{n-1}s^{n-1}+\cdots+b_1s+a_0}{a_{n-1}s^{n-1}+a_{n-2}s^{n-2}+\cdots+a_1s+a_0}}=\frac{1}{\dfrac{b_n}{a_{n-1}}s+\dfrac{b'_{n-1}s^{n-1}+b'_{n-2}s^{n-2}\cdots+b_1s+a_0}{a_{n-1}s^{n-1}+a_{n-2}s^{n-2}+\cdots+a_1s+a_0}}\\&=\frac{1}{\mathrm{C}_{th1}s+Y(s)}\end{aligned} \tag{2.15}$$

where:

$$\mathrm{C}_{th1}s=\frac{b_n}{a_{n-1}}\text{, and }\ Y(s)=\frac{b'_{n-1}s^{n-1}+b'_{n-2}s^{n-2}\cdots+b_1s+a_0}{a_{n-1}s^{n-1}+a_{n-2}s^{n-2}+\cdots+a_1s+a_0} \tag{2.16}$$

From this calculation, the first capacitance of the Cauer equivalent thermal network as the quotient is obtained. The next step is dividing the denominator by the numerator of $Y(s)$ as follows:

$$\begin{aligned}Y(s)&=\frac{1}{\dfrac{a_{n-1}s^{n-1}+a_{n-2}s^{n-2}+\cdots+a_1s+a_0}{b'_{n-1}s^{n-1}+b'_{n-2}s^{n-2}\cdots+b_1s+a_0}}=\frac{1}{\dfrac{a_{n-1}}{b'_{n-1}}+\dfrac{a'_{n-2}s^{n-2}+a'_{n-3}s^{n-3}\cdots+a_1s+a_0}{b'_{n-1}s^{n-1}+b'_{n-2}s^{n-2}\cdots+b_1s+a_0}}\\&=\frac{1}{R_{th1}+Z'(s)}\end{aligned} \tag{2.17}$$

where:

$$R_{th1}=\frac{a_{n-1}}{b'_{n-1}}\text{, and }\ Z'(s)=\frac{a'_{n-2}s^{n-2}+a'_{n-3}s^{n-3}\cdots+a_1s+a_0}{b'_{n-1}s^{n-1}+b'_{n-2}s^{n-2}\cdots+b_1s+a_0} \tag{2.18}$$

As the quotient of this calculation, the first resistance of the Cauer equivalent thermal network is

obtained. After this calculation, the transfer function is expressed as follows:

$$Z_{th}(s) = \frac{1}{\mathrm{C}_{th1}s + \dfrac{1}{R_{th1} + Z'(s)}} = \frac{1}{\mathrm{C}_{th1}s + \dfrac{1}{R_{th1} + \dfrac{a'_{n-2}s^{n-2} + a'_{n-3}s^{n-3} \cdots + a_1 s + a_0}{b'_{n-1}s^{n-1} + b'_{n-2}s^{n-2} \cdots + b_1 s + a_0}}} \tag{2.19}$$

The next capacitance of the Cauer equivalent thermal network can be obtained using the repeat of the upper process, and this calculation is repeated until the remainder is zero, then elements values of the Foster equivalent thermal network turn into that of the Cauer equivalent thermal network.

2.3.3 Transient thermal characterization procedure

The thermal analysis of the packaged semiconductor with a compact model based on Cauer equivalent thermal network is very attractive, because it is simple and fast to estimate the thermal behavior of the packaged devices, and it can be figured out, intuitionally, that the thermal system for the heat flow path inside the packaged device. Several researches have been carried out to identify the compact thermal model [20]-[23]. Generally, it follows the procedures below.

(1) **Obtaining the transient thermal response of the packaged device**. The electrical switching method is generally used for the transient thermal response measurement [24]-[26]. This method has two phases: one is heating phase, and the other is cooling phase. In the heating phase, the high power is supplied into the device to heat up the device temperature. In cooling phase, the response of the junction temperature is measured using the temperature dependence of the electrical characteristics of the semiconductor device, namely, thermal sensitive electrical parameters (TSEPs) under low power operation. The reason that there are two phases in the measurement is difficult to measure the junction temperature using the conventional TSEPs with supplying power in the heating phase, consequently. It is challenging task to measure the junction temperature in the heating phase.

(2) **Identifying the thermal parameters for the thermal models.** The several research results have been introduced to identify the thermal parameters form the measured thermal response of the packaged device. The most widely used method is network identification by deconvolution (NID) method [27],[28]. The NID method tries to identify the thermal parameters by deconvolution of the thermal response and the thermal capacitance-resistance maps. This method can be applicable to other electronic applications and support the reliable results with spatial resolution, but the procedure to identify the thermal parameter is complicate. Thermal resistance analysis by induced transient (TRAIT) method

is a well-known method for this procedure, too [29],[30]. The TRAIT method obtains the thermal parameters by the curve fitting of the thermal response to the discrete multi-exponential function. This method has a simpler procedure compared to the NID method, but the help of the numerical simulation analysis is required in the complicate packaged structure. On the other hands, the other method can be applicable in this procedure such as a genetic algorithm [31],[32].

(3) **Configuration of the equivalent thermal circuit.** The measured thermal response represents the total thermal value for the whole packaged device, but it is possible to know the contribution of each layer for the thermal response of the packaged device through the configuration of Cauer based thermal network model. This equivalent thermal model can be implemented, simply, to several simulators such as several SPICE, Matlab, and etc., and can be combined with the electrical model of the semiconductor devices for more precise analysis. The thermal response of the packaged devices can be reconstructed in various operation conditions, and the results can be used to design the power conversion applications.

2.3.4 TRAIT method

The transient thermal response of the device is governed by an infinite series of exponential time constants that are affected by the thermal properties and structures of the various physical layers of the system. However, the thermal resistance analysis by induced transient (TRAIT) method has shown that the knowledge of the first *n*-terms of the time constant spectrum can express the whole transient thermal response of the device, sufficiently. In the TRAIT method, the cooling transient thermal response of the packaged semiconductor devices with a multi-layer structure after supplying a step input power can be described by a sum of exponential terms as follows [29],[30]:

$$T_j(0,t) = T_r + P_d \cdot \sum_{i=1}^{n} A_i \cdot \exp\left(-t/\tau_i\right) \tag{2.20}$$

where T_j is the junction temperature, T_r is the reference temperature, P_d is the dissipated power of the heat source, τ_i is the time constant and A_i is the corresponding amplitude factor to time constant. Eq. (2.20) can be rearranged as shown by Eq. (2.21), and transient thermal resistance at junction can be defined:

$$Z_{th}(t) = \frac{T_j(0,t) - T_r}{P_d} = \sum_{i=1}^{n} A_i \cdot \exp\left(-t/\tau_i\right) \tag{2.21}$$

In addition, the total thermal resistance of the packaged semiconductor device (R_{th}) at steady state can be expressed as follows:

$$R_{th}(t) = \frac{T_j(0,0) - T_r}{P_d} = \sum_{i=1}^{n} A_i(0) \tag{2.22}$$

The identification for the thermal parameters of the Eq. (2.21) can be carried out through the several curve fitting algorithms such as Gradient descent method, Newton-Rahpson method, Gauss-Newton method, and Levenberg-Marquardt method. The most widely used algorithm is the Levenberg-Marquardt method, because it is possible to find the solution compared to other methods, rapidly, and stably.

The thermal parameters identified from Eq. (2.21) can be modelled, directly, on the Foster equivalent thermal network using the following relation.

$$R_i = A_i(0) \tag{2.23}$$

$$C_i = \frac{\tau_i}{R_i} \tag{2.24}$$

Finally, the Cauer equivalent thermal model can be obtained through the Foster to Cauer network conversion. Generally, *n*-terms represent the number of the layers, and the Foster to Cauer network conversion generated the Cauer equivalent thermal network with *n*-layer that describes the thermal system inside the packaged device.

2.3.5 NID method

Considering the real system, the transient thermal response of the packaged device should be expressed by the distributed or infinite discrete system. Figure 2.5 shows the discrete and distributed time constant spectrum. In the network identification by deconvolution (NID) method, the thermal system is obtained by the deconvolution with the weigh function [27],[28],[33]. If the step response of the thermal system with the multi-layers is expressed as the distributed domain, the discrete exponential function shown in Eq. (2.21) can be expressed by:

$$Z_{th}(t) = \int_0^{\infty} R(\tau)\left[1 - \exp(-t/\tau)\right] d\tau \tag{2.25}$$

where $R(\tau)$ is the distribute time constant spectrum, and the thermal system can be known with obtaining $R(\tau)$. By introducing the logarithmic time variable $z = \ln(t)$ and the logarithmic time

constant $\zeta = \ln(\tau)$, Eq. (2.25) is expressed as:

$$Z_{th}(t) = \int_{-\infty}^{\infty} R(\zeta)\left[1 - \exp(-t/\exp(\zeta))\right]d\zeta \tag{2.26}$$

where the $R(\zeta)$ is the logarithmic time constant spectrum and defined as:

$$R(\zeta) = R(\exp(\zeta)) \cdot \exp(\zeta) \tag{2.27}$$

Equation (2.27) can be changed to:

$$Z_{th}(z) = \int_{-\infty}^{\infty} R(\zeta)\left[1 - \exp(-\exp(z-\zeta))\right]d\zeta \tag{2.28}$$

With differentiating Eq. (2.28) respect to *z*, Eq. (2.29) can be obtained.

$$\frac{d}{dz}Z_{th}(z) = \int_{-\infty}^{\infty} R(\zeta)\left[\exp(z-\zeta-\exp(z-\zeta))\right]d\zeta \tag{2.29}$$

By introducing the weight function $w_z(z) = \exp(z - \exp(z))$, Eq. (2.29) is changed to

$$\frac{d}{dz}Z_{th}(z) = \int_{-\infty}^{\infty} R(\zeta)w_z(z-\zeta)d\zeta \tag{2.30}$$

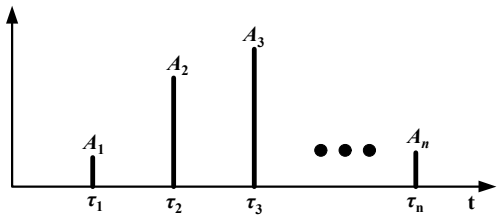
Equation (2.30) can be expressed by following convolution form:

$$\frac{d}{dz}a(z) = R(z) \otimes w_z(z) \tag{2.31}$$

where $\otimes$ is the convolution symbol. Finally, *R*(*z*) is obtained through the deconvolution of Eq. (2.31)

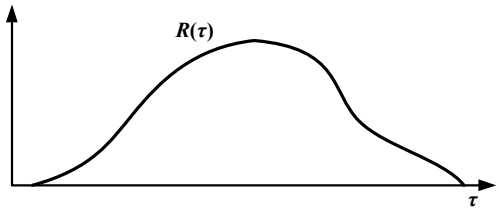
$$R(z) = \left[\frac{d}{dz}a(z)\right] \otimes^{-1} w_z(z) \tag{2.32}$$

The convolution can be carried out using the Bayesian iteration or Fourier domain inverse filtering. The obtained distributed thermal constant spectrum should be discretized to generate the thermal model based on the Foster equivalent network. After the Foster to Cauer network conversion, the differential and cumulative structure functions based on the Cauer equivalent thermal network can be obtained. The compact thermal model of the packaged semiconductor device can be obtained from these structure functions.



$$Z_{th}(t) = \sum_{i=1}^{n} A_i \cdot \left(1 - \exp\left(-t/\tau_i\right)\right)$$

(a) Discrete time constant spectrum



$$Z_{th}(t) = \int_{-\infty}^{\infty} R(\zeta)\left[1 - \exp(-t/\exp(\zeta))\right] d\zeta$$

(b) Distributed time constant spectrum

Fig. 2.5 Discrete time constant spectrum (a) and Distributed time constant spectrum based on RC equivalent thermal system.

2.4 Conclusion

In this chapter, the fundamentals for the thermal analysis of the packaged SiC devices were presented. The heat transfer mechanism for the thermal analysis of the package was described. The concept of the FDM, and the compact thermal model based on Foster and Cauer equivalent thermal network were described. The thermal measurement and characterization methods for the packaged semiconductor devices were presented and discussed.

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Chapter 3:

Analysis on steady state and transient thermal characteristics of packaged SiC SBDs

3.1 Introduction

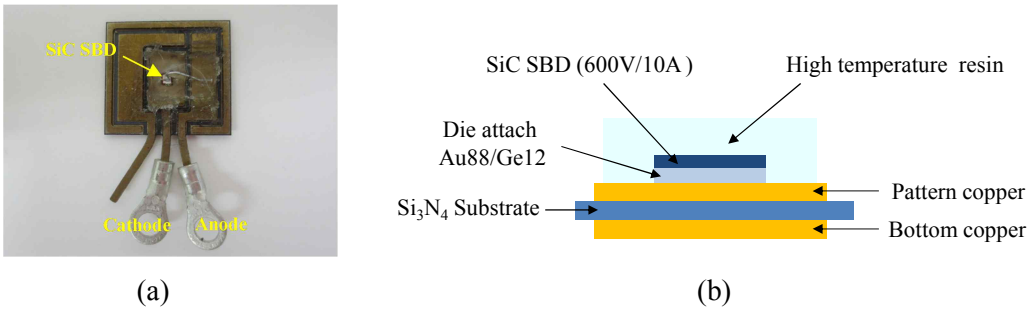
As described in chapter 1, the thermal properties of the package materials for the SiC semiconductor devices change with temperature due to the variation of the lattice vibration waves and the movement of electrons in materials with temperature [1],[2]. The thermal conductivity of the 4H-SiC material is decreased from 350.88 to 174.93 W/m·°C in the temperature rise from 27 to 300°C. In case of the specific heat of 4H-SiC material, the increasing trend is shown from 676.71 to 1018.45 J/kg·°C within the same temperature variation range [3]. In addition, the temperature dependence of the thermal properties of the other package materials such as the copper, the aluminum, and the ceramics (Al_2O_3, AlN and Si_3N_4) has been reported in several research results [4]-[6].

In the high temperature operation of the SiC devices, the thermal management is important, because the temperature margin to guarantee the electrical and physical performance of the packaged SiC devices is reduced [7],[8]. The thermal management allows the temperature of the SiC semiconductor device to be controlled under the safe operation condition. In the design of the thermal management of the packaged SiC devices for the high temperature operation, the accurate thermal information of the packaged devices considering the thermal characteristics variation with temperature is necessary.

This chapter presents the thermal analysis of the packaged SiC SBD for high temperature operation based on the experimental and numerical simulation results. The packaged SiC SBD for high temperature operation is introduced in section 3.2. The thermal modelling for the packaged SiC SBD with finite difference method considering the temperature dependence of the thermal properties, and the numerical simulation procedure are explained in section 3.3. The transient thermal resistance measurement of the packaged SiC SBD was carried out to validate the numerically simulated results. This experimental measurement details and results are shown in section 3.4. Then, the measured and simulated results are compared and analyzed through section 3.5. Finally, this chapter is concluded with a summary of the achieved results.

3.2 Structure of packaged SiC SBD

A 1.8 × 1.8mm^2 SiC SBD manufactured by "Rohm" was used as a DUT. The SiC SBD was soldered with 88Au/12Ge on an active metal brazed (AMB) Si_3N_4 substrate manufactured by "KYOCERA". The size of the AMB substrate, thickness of the wiring copper, the Si_3N_4 substrate and the backside copper metal were 20 × 20mm^2, 0.5mm, 0.35mm and 0.5mm, respectively. The anode of the SiC SBD was bonded with an Al wire (diameter of 300um), and the substrate was covered with a high temperature resin manufactured by "ADEKA". The packaged SiC SBD was attached on an Al heat-sink, and a thermal grease ("SUNHAYTO" SCH-30) was used to reduce the contact resistance between the package and the heat-sink. A K-type thermocouple was attached to the center position of the SiC SBD device in the bottom side of the packaged SiC SBD with the soldering contact to measure the temperature of the bottom copper layer. The overview and schematic cross sectional structure of the packaged SiC SBD is shown in Fig. 3.1.



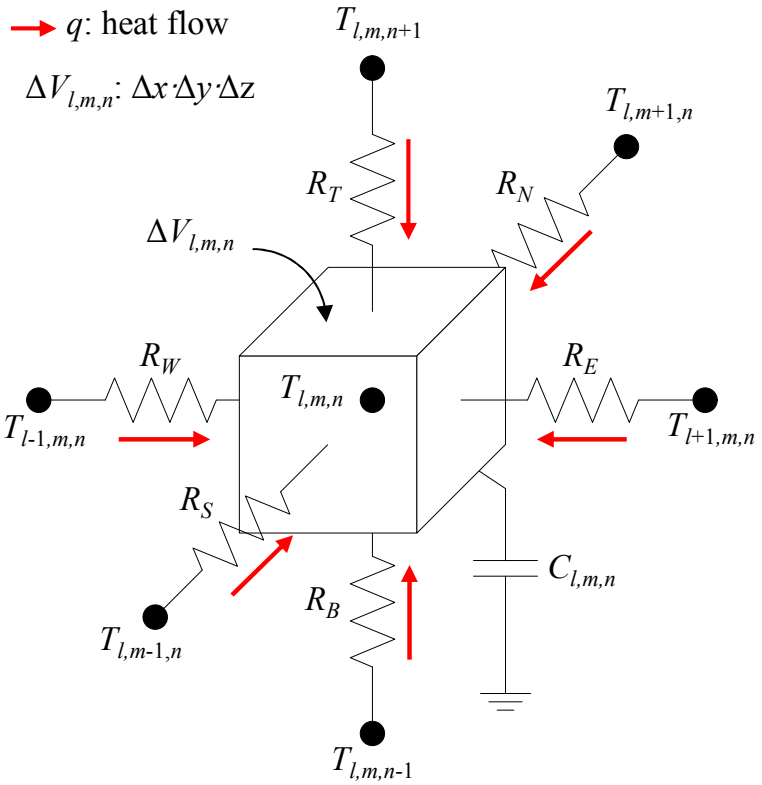
(a) (b)

Fig. 3.1 Overview of the packaged SiC SBD (a) and schematic cross sectional structure view of the packaged SiC SBD

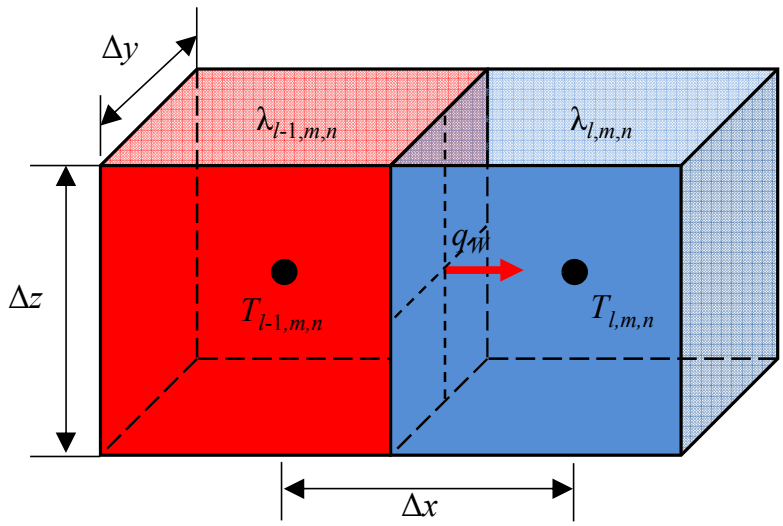
3.3 Finite difference thermal modeling

3.3.1 Finite difference equation

Although the three mechanisms described in chapter 2 affect the whole heat transfer of the packaged semiconductor device, the heat transfer inside the packaged devices is dominated by the heat conduction so that it can be assumed that the effects of the convection and radiation are negligible [9]. Therefore, the heat transfer inside the packaged SiC SBD can be expressed by the governing partial difference equation as follows:



(a)



(b)

Fig. 3.2. Thermal network with thermal resistance and capacitance (a), and the heat flow between (l-1, m, n) and (l, m, n) with the different thermal conductivities (b).

$$\rho c(T)\frac{\partial T(x,y,z,t)}{\partial t} = \nabla \cdot \left[\lambda(T)\nabla T(x,y,z,t)\right] + g(x,y,z,t) \tag{3.1}$$

where ρ is the density, $c(T)$ and $\lambda(T)$ are the specific heat and the thermal conductivity with temperature dependency, and g is the power density of the heat source.

As described in chapter 2, the finite difference method (FDM) is a widely used method to solve the partial difference equations, and it can be used for solving the heat conduction equation as shown in Eq. (3.1) [10]. In this research, the governing equation for Eq. (3.1) is changed into the explicit finite difference equation based on the forward approximation, and the energy balance method for each node.

Figure 3.2(a) shows the thermal network with the thermal resistance and capacitance in the three dimensional orthogonal coordinate for the finite difference method. The thermal network has a control volume that has the node (l, m, n) in the center, and has the lengths Δx, Δy, Δz. There are six adjacent nodes (l±1, m, n), (l, m±1, n), and (l, m, n±1) around the node (l, m, n), and the distances between the node (l, m, n) and the adjacent nodes are Δx, Δy, Δz, respectively. Assuming that all the heat flow goes into the node (l, m, n), the general energy conservation equation for the control volume $\Delta V=\Delta x\cdot\Delta y\cdot\Delta z$ is expressed as follows:

$$\sum_{i=1}^{\mathrm{n}} E_{in,i} = E_{stored} - E_{generaged} \tag{3.2}$$

where E_{in} is the input energy, E_{stored} is the stored energy, and $E_{generated}$ is the generated energy. The energy exchange is affected by the heat generation in the control volume, and by conduction between the node (l, m, n) and the adjacent nodes. The heat conduction can be represented by the heat flow q so that Eq. (3.2) is can be expressed:

$$\sum_{\mathrm{i}=1}^{6} q_{(i)\to(l,m,n)} + \dot{g}\Delta V_{l,m,n} = E_{stored} \tag{3.3}$$

where $\dot{g}$ is the rate of the heat generation per unit volume, and the subscripts l, m, n denote the grid point. As described in chapter 2, the heat flow can be expressed by Fourier's heat conduction equation. Considering the temperature dependence of the thermal conductivities, even if the nodes are in the same material, the thermal conductivities of each node change with the temperature variation of the nodes. Figure 3.2(b) shows the schematic heat flow from the node (l-1, m, n) to (l, m, n) with the different thermal conductivities. In Fig. 3.2(b), the heat flow q_W through the area $\Delta A=\Delta y\cdot\Delta z$ can be expressed as follows:

$$
\begin{aligned}
q_W &= -\lambda_W \Delta A \frac{\partial T}{\partial x} \\
&\approx \frac{\lambda_{l-1,m,n} + \lambda_{l,m,n}}{2} \left(\frac{\Delta y \Delta z}{\Delta x}\right)\left(T_{l-1,m,n} - T_{l,m,n}\right) \\
&\approx \lambda_{l-1/2,m,n} \left(\frac{\Delta y \Delta z}{\Delta x}\right)\left(T_{l-1,m,n} - T_{l,m,n}\right)
\end{aligned} \tag{3.4}
$$

where

$$
\lambda_{l-1/2,m,n} = \frac{\lambda_{l-1,m,n} + \lambda_{l,m,n}}{2} \tag{3.5}
$$

where $\lambda_{l\text{-}1,m,n}$, $\lambda_{l,m,n}$ are the thermal conductivities of the control volume with the node (l-1, m, n) and (l, m, n), respectively. A similar expression can be written for the other heat flows into the node (l, m, n).

The stored energy for the control volume is represented as follows:

$$
\dot{E}_{stored} = (\rho c)_{l,m,n} \Delta V_{l,m,n} \frac{\partial T}{\partial t} \approx (\rho c)_{l,m,n} (\Delta x \cdot \Delta y \cdot \Delta z) \frac{T_{l,m,n}^{p+1} - T_{l,m,n}^{p}}{\Delta t} \tag{3.6}
$$

where the superscript p represents the current time step, and Δt identifies the time interval between the current time p and the next time p+1.

It is required to discretize the temperature dependent thermal properties for the thermal simulation. Thermal conductivity λ^{p+1} at the time level p+1 can be expressed as follows:

$$
\lambda^{p+1} \cong \lambda^{p} + \left(\frac{\partial \lambda}{\partial t}\right)^{p} \Delta t \cong \lambda^{p} + \left(\frac{\partial \lambda}{\partial T}\right)^{p} \left(\frac{\partial T}{\partial t}\right)^{p} \Delta t \tag{3.7}
$$

where the term of the time derivative of the temperature is approximated by:

$$
\left(\frac{\partial T}{\partial t}\right)^{p} \cong \frac{T^{l} - T^{p-1}}{\Delta t} \tag{3.8}
$$

Substituting Eq. (3.8) into (3.7), the thermal conductivity with temperature dependence at the time level p+1 is determined as:

$$
\lambda^{p+1} = \lambda^{p} + \left(\partial \lambda / \partial T\right)^{p} \left(T^{p} - T^{p-1}\right) \tag{3.9}
$$

Using the similar procedure, the specific heat can be obtained as follows:

$$
c^{p+1} = c^{p} + \left(\partial c / \partial T\right)^{p} \left(T^{p} - T^{p-1}\right) \tag{3.10}
$$

Based on the equations of (3.4)-(3.10), the finite difference equation for the thermal simulation of the packaged SiC SBD at the internal node (l, m, n) is obtained as follows:

$$
\begin{aligned}
&(\rho c)_{l,m,n}\Delta x\Delta y\Delta z\frac{T_{l,m,n}^{p+1}-T_{l,m,n}^{p}}{\Delta t}\\
&=\left[\lambda_{l-1/2,m,n}\frac{\Delta y\Delta z}{\Delta x}\left(T_{l-1,m,n}^{p}-T_{l,m,n}^{p}\right)+\lambda_{l+1/2,m,n}\frac{\Delta y\Delta z}{\Delta x}\left(T_{i+1,j,k}^{p}-T_{l,m,n}^{p}\right)\right]\\
&+\left[\lambda_{l,m-1/2,n}\frac{\Delta x\Delta z}{\Delta y}\left(T_{l,m-1,n}^{p}-T_{l,m,n}^{p}\right)+\lambda_{l,m+1/2,n}\frac{\Delta x\Delta z}{\Delta y}\left(T_{l,m+1,n}^{p}-T_{l,m,n}^{p}\right)\right]\\
&+\left[\lambda_{l,m,n-1/2}\frac{\Delta x\Delta y}{\Delta z}\left(T_{l,m,n-1}^{p}-T_{l,m,n}^{p}\right)+\lambda_{l.m,n+1/2}\frac{\Delta x\Delta y}{\Delta z}\left(T_{l,m,n+1}^{p}-T_{l,m,n}^{p}\right)\right]\\
&+g(x_l,y_m,z_n,t)
\end{aligned}
\tag{3.11}
$$

3.3.2 Thermal model of packaged SiC SBD

Because the most of the heat generated from the SiC SBD flows through the center copper pattern inside the package, thermal model was built considering it. The schematic thermal simulation model and the dimensions of the packaged SiC SBD structure are shown in Fig. 3.3, and Table 3.1, respectively. The dimensions for the thermal simulation are accordance with the experimented real package structure.

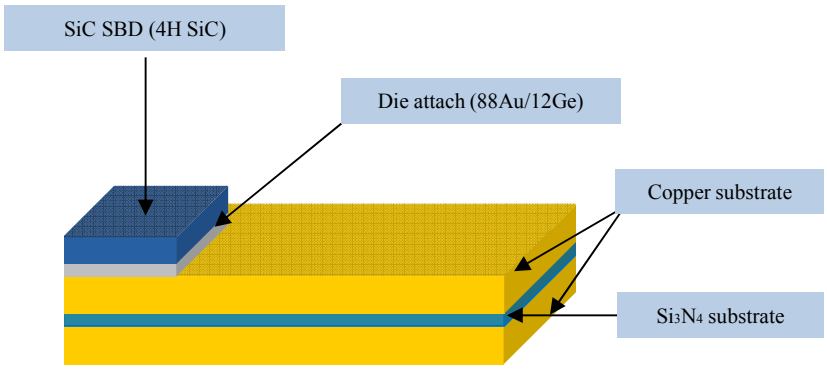


Fig. 3.3 Description of schematic thermal model for transient thermal response simulation of the packaged SiC SBD.

Table 3.1 Dimension of the thermal model of the packaged SiC SBD

Component		Surface area(mm^2)	Thickness (mm)
Chip		0.9 × 0.9	0.2
Die attach layer		0.9 × 0.9	0.17
Substrate	Copper	3 × 4.5	0.5
	Si_3N_4	3 × 4.5	0.35
	Copper	3 × 4.5	0.5

3.3.3 Simulation

In solving the governing equation, the boundary conditions were set as Fig. 3.4: The dissipated power of 5W in the SiC SBD was expressed by a uniform heat flux input at top side of the device. Because most of the generated heat flows to bottom direction for a heat sink, the lateral side is supposed to be thermally insulated and bottom side was clamped with the initial device temperature. Due to the symmetrical structure of the device, a quarter of the packaged SiC SBD was modeled and simulated.

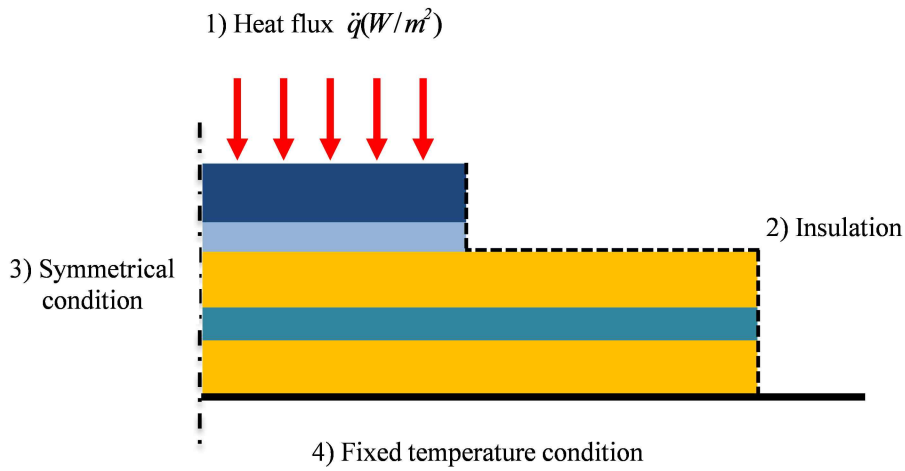


Fig. 3.4 Boundary conditions for FDM simulation

The main finite difference equations including the boundary conditions are shown as follows:

i) FDM equation with heat flux boundary condition

$$
\begin{aligned}
&(\rho c)_{l,m,n}\Delta x\Delta y\Delta z\frac{T_{l,m,n}^{p+1}-T_{l,m,n}^{p}}{\Delta t}\\
&=\left[\lambda_{l-1/2,m,n}\frac{\Delta y\Delta z}{\Delta x}\left(T_{l-1,m,n}^{p}-T_{l,m,n}^{p}\right)+\lambda_{l+1/2,m,n}\frac{\Delta y\Delta z}{\Delta x}\left(T_{i+1,j,k}^{p}-T_{l,m,n}^{p}\right)\right]\\
&+\left[\lambda_{l,m-1/2,n}\frac{\Delta x\Delta z}{\Delta y}\left(T_{l,m-1,n}^{p}-T_{l,m,n}^{p}\right)+\lambda_{l,m+1/2,n}\frac{\Delta x\Delta z}{\Delta y}\left(T_{l,m+1,n}^{p}-T_{l,m,n}^{p}\right)\right]\\
&+\left[2\lambda_{l,m,n-1/2}\frac{\Delta x\Delta y}{\Delta z}\left(T_{l,m,n-1}^{p}-T_{l,m,n}^{p}\right)+2\ddot{q}\Delta x\Delta y\right]
\end{aligned}
\tag{3.12}
$$

ii) FDM equation with insulation boundary condition

$$
\begin{aligned}
&(\rho c)_{l,m,n}\Delta x\Delta y\Delta z\frac{T_{l,m,n}^{p+1}-T_{l,m,n}^{p}}{\Delta t}\\
&=\left[2\lambda_{l-1/2,m,n}\frac{\Delta y\Delta z}{\Delta x}\left(T_{l-1,m,n}^{p}-T_{l,m,n}^{p}\right)\right]\\
&+\left[\lambda_{l,m-1/2,n}\frac{\Delta x\Delta z}{\Delta y}\left(T_{l,m-1,n}^{p}-T_{l,m,n}^{p}\right)+\lambda_{l,m+1/2,n}\frac{\Delta x\Delta z}{\Delta y}\left(T_{l,m+1,n}^{p}-T_{l,m,n}^{p}\right)\right]\\
&+\left[\lambda_{l,m,n-1/2}\frac{\Delta x\Delta y}{\Delta z}\left(T_{l,m,n-1}^{p}-T_{l,m,n}^{p}\right)+\lambda_{l.m,n+1/2}\frac{\Delta x\Delta y}{\Delta z}\left(T_{l,m,n+1}^{p}-T_{l,m,n}^{p}\right)\right]
\end{aligned}
\tag{3.13}
$$

iii) FDM equation with symmetrical boundary condition

$$
\begin{aligned}
&(\rho c)_{l,m,n}\Delta x\Delta y\Delta z\frac{T_{l,m,n}^{p+1}-T_{l,m,n}^{p}}{\Delta t}\\
&=\left[2\lambda_{l+1/2,m,n}\frac{\Delta y\Delta z}{\Delta x}\left(T_{i+1,j,k}^{p}-T_{l,m,n}^{p}\right)\right]\\
&+\left[\lambda_{l,m-1/2,n}\frac{\Delta x\Delta z}{\Delta y}\left(T_{l,m-1,n}^{p}-T_{l,m,n}^{p}\right)+\lambda_{l,m+1/2,n}\frac{\Delta x\Delta z}{\Delta y}\left(T_{l,m+1,n}^{p}-T_{l,m,n}^{p}\right)\right]\\
&+\left[\lambda_{l,m,n-1/2}\frac{\Delta x\Delta y}{\Delta z}\left(T_{l,m,n-1}^{p}-T_{l,m,n}^{p}\right)+\lambda_{l.m,n+1/2}\frac{\Delta x\Delta y}{\Delta z}\left(T_{l,m,n+1}^{p}-T_{l,m,n}^{p}\right)\right]
\end{aligned}
\tag{3.14}
$$

iv) FDM equation with fixed temperature boundary condition

$$
\begin{aligned}
&(\rho c)_{l,m,n}\Delta x\Delta y\Delta z\frac{T_{l,m,n}^{p+1}-T_{l,m,n}^{p}}{\Delta t}\\
&=\left[\lambda_{l-1/2,m,n}\frac{\Delta y\Delta z}{\Delta x}\left(T_{l-1,m,n}^{p}-T_{l,m,n}^{p}\right)+\lambda_{l+1/2,m,n}\frac{\Delta y\Delta z}{\Delta x}\left(T_{i+1,j,k}^{p}-T_{l,m,n}^{p}\right)\right]\\
&+\left[\lambda_{l,m-1/2,n}\frac{\Delta x\Delta z}{\Delta y}\left(T_{l,m-1,n}^{p}-T_{l,m,n}^{p}\right)+\lambda_{l,m+1/2,n}\frac{\Delta x\Delta z}{\Delta y}\left(T_{l,m+1,n}^{p}-T_{l,m,n}^{p}\right)\right]\\
&+\left[\lambda_{l,m,n-1/2}\frac{\Delta x\Delta y}{\Delta z}\left(T_{l,m,n-1}^{p}-T_{l,m,n}^{p}\right)+\lambda_{l.m,n+1/2}\frac{\Delta x\Delta y}{\Delta z}\left(T_{a}-T_{l,m,n}^{p}\right)\right]
\end{aligned}
\tag{3.15}
$$

The thermal properties for solving FDM simulation are shown in Table 3.2 [3], [6], [11], [12]. For simulation, the time interval Δt was set as 2.5μs, and the grid sizes of Δx, Δy, Δz were set as 150μm, 150μm and 10μm, respectively. This simulation conditions satisfied the stability criterion as follows:

$$\Delta t \le \frac{(\rho c)_{l,m,n}\Delta V}{\sum K} \tag{3.16}$$

where

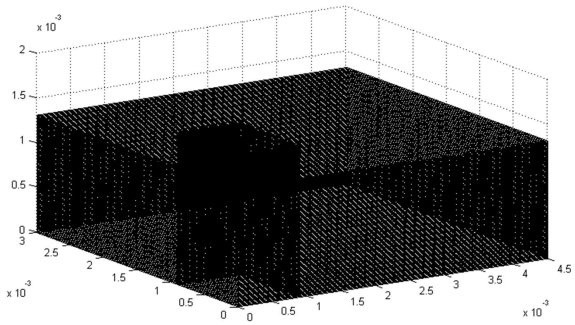
$$\sum K = (\lambda_{l-1/2,m,n} + \lambda_{l+1/2,m,n})\frac{\Delta y \Delta z}{\Delta x} + (\lambda_{l,m-1/2,n} + \lambda_{l,m+1/2,n})\frac{\Delta x \Delta z}{\Delta y} + (\lambda_{l,m,n-1/2} + \lambda_{l.m,n+1/2})\frac{\Delta x \Delta y}{\Delta z} \tag{3.17}$$

The numerical simulation was carried out in the reference temperatures of 27°C, 100°C, 175°C and 250°C, and the initial temperature conditions were same values with the reference temperatures.

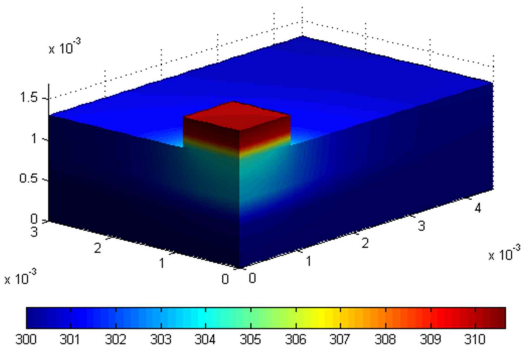
In the simulation results, it is shown that the maximum temperatures of the packaged SiC SBD are 37.6°C, 111.1°C, 186.5°C, and 261.9°C in different reference temperature conditions of 27°C, 100°C, 175°C, and 250°C. The drastic temperature change is shown in the 88Au/12Ge layer, and the heat spreads widely through the pattern copper layer. The heat spreading is interrupted in the Si_3N_4 layer. The variation in the temperature difference between the junction and bottom copper layer is 1.42°C as the reference temperature changes from 27°C to 250°C.

Table 3.2 Thermal properties for numerical FDM simulation

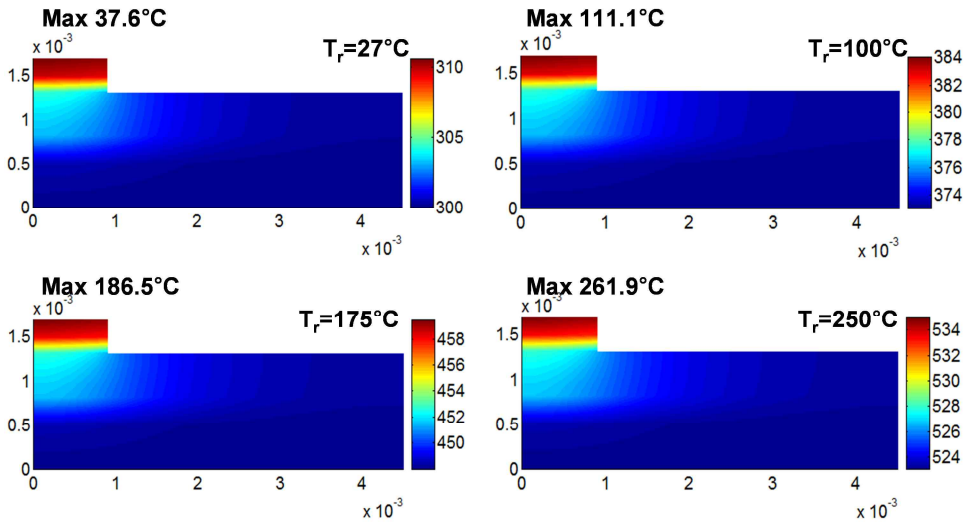
Materials	Thermal conductivity (W/m·K)	Specific heat (J/kg·K)	Density (kg/m^3)
4H-SiC	$(-0.0003+1.05\times10^{-5}T)^{-1}$	$925.65+0.3772T-7.9254\times10^{-5}T^2$ $-3.1946\times10^{-5}T^{-2}$	3215
88Au/12Ge	44.4	151.2	14670
Copper	$420.75-6.8493\times10^{-2}T$	$316.21+0.3177T-3.4936\times10^{-4}T^2$ $+1.661\times10^{-7}T^3$	8933
Si_3N_4	$74.359-0.082T+3\times10^{-5}T^2$	$61.576+2.4308T-0.0018T^2$ $+5\times10^{-7}T^3$	3500



(a)



(b)



(c)

Fig. 3.5 Mesh for the finite difference thermal simulation (a), the simulated three dimensional steady state temperature distribution of the packaged SiC SBD at reference temperature of 27°C (b), and three dimensional steady state temperature distribution of packaged SiC SBD in different reference temperature conditions of 27°C, 100°C, 175°C, and 250°C (c).

3.4 Experimental thermal measurement

There are several research results for the transient thermal resistance measurement of power semiconductors [13]-[15]. The junction temperature measurement should be carried out in these works. Directly, the surface temperature of the semiconductor device can be measured using the temperature measurement equipment such as an infrared camera and an optical fiber after encapsulation of the package [16]-[18]. This method is very simple, but needs the invasive process of the semiconductor device to detect the surface of the device. Currently, the temperature sensitive electrical parameters (TSEPs) are frequently used for the junction temperature measurement. TSEPs mean the electrical parameters of the semiconductors that change their values with the temperature variation such as parasitic *p*-*n* junction, on-state resistance, and saturation current [19]-[21]. This method allows measurement of the accurate junction temperature with a high time resolution without the external measurement system. In this research, the transient thermal resistance of the packaged SiC SBD was measured based on the electrical switching method [15],[22].

3.4.1 Thermal sensitive electrical parameter

The junction temperature of the SiC SBD can be measured using the forward voltage drop of the schottky junction as the thermal sensitive electrical parameters. In low forward current region, the voltage drop of the drift region is very small, so that it can be neglected in the model. Therefore, the forward characteristic of the SiC SBD can be modelled as follows [23]:

$$I_F \cong SA^* T_j^{\,2} \exp\left(\frac{q(V_F - \Phi_B)}{nk_b T_j}\right) \tag{3.18}$$

where S is the junction area of the SiC SBD, A^* is the Richardson constant, k_b is the Boltzmann constant, q is the electron charge, n is ideal factor, and Φ_B is the barrier height, respectively. Equation (3.18) can be rearranged for V_F as follows:

$$V_F = \frac{nk_b T_j}{q} \ln\left(\frac{I_F}{SA^* T_j^{\,2}}\right) + \Phi_B \tag{3.19}$$

With the derivative of Eq. (3.19) for the temperature, the temperature dependence of V_F in the constant current operation can be expressed as:

$$K = \left(\frac{dV_F}{dT_j}\right) = \frac{2nk}{q} + \frac{V_F - \Phi_B}{T_j} \tag{3.20}$$

The temperature dependence of V_F is called as the *K*-factor, and the junction temperature of the SiC SBD can be obtained using the following equation:

$$T_j = T_{ref} + \Delta T_j = T_{ref} + \Delta V_F / K \tag{3.21}$$

where T_{ref} is the reference temperature, and K is the *K*-factor. The sensing current for the forward voltage drop measurement of the SiC SBD should be small enough to suppress the junction temperature change due to the self-heating effect. In this measurement, the constant current of 1mA is used for the temperature sensing.

Prior to the transient thermal resistance measurement, temperature dependence of the forward voltage drop of the SiC SBD was measured to determine the *K*-factor from 27°C to 295°C, and the results are as shown in Fig. 3.6.

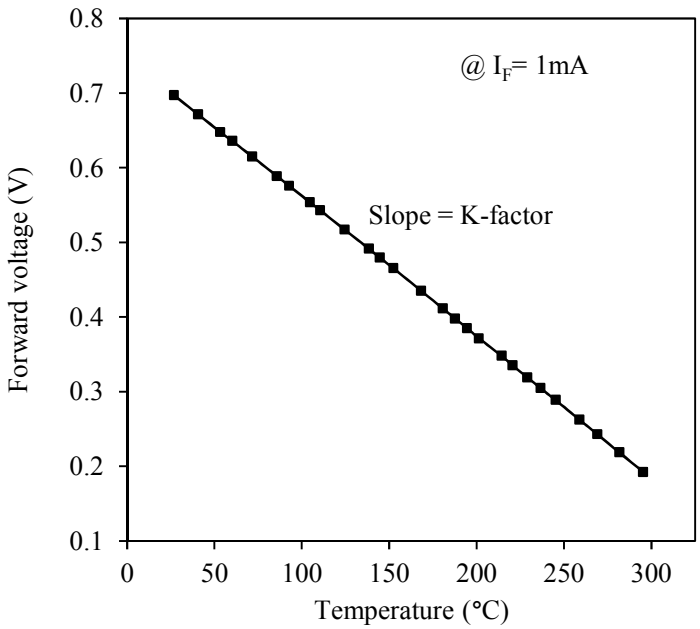


Fig. 3.6 Temperature dependence of forward voltage drop of SiC SBD measured from 27°C to 295°C.

3.4.2 Transient thermal resistance measurement

Figure 3.7 shows the schematic diagram of test circuit (a), the operation phases in thermal measurement (b), and the measurement system including the cross sectional view of the DUT (c). In forward conduction operation of the SiC SBD with high power, the dissipated power of the SiC SBD expressed by $P_d = I_F \cdot V_F$ changes due to temperature dependence of electrical characteristics.

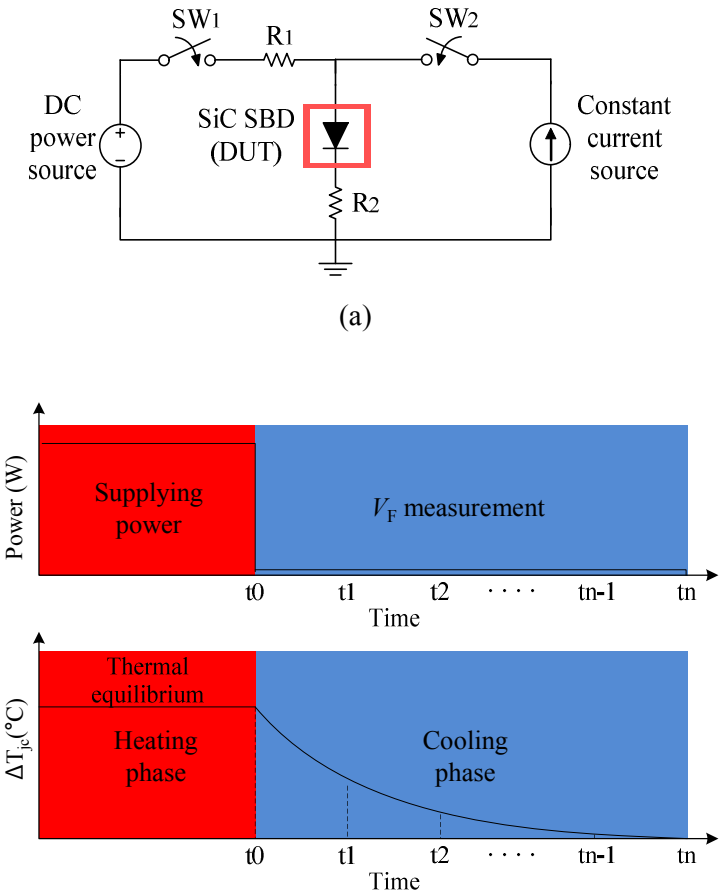


Fig. 3.7 Schematic diagram of the measurement circuit (a), schematic operation phases for the transient thermal resistance measurement (b), and schematic view of experimental setup for the transient thermal response measurement (c).

To achieve the power regulation for the SiC SBD, the load resistance R_L is inserted as shown in a left part of the test circuit of Fig. 3.7(a). In conduction operation of the SiC SBD connected with a load resistor in series and driven by a constant voltage source, the operation point is determined as the point of intersection between the forward characteristics of the SiC SBD and the load line represented in Eq. (3.22) [24].

$$I_F = -\frac{V_F}{R_L} + \frac{V_{DD}}{R_L} \tag{3.22}$$

where R_L is the load resistance and V_{DD} is the constant voltage source. The constant power curves expressed by Eq. (3.23) are calculated from the forward characteristics of the SiC SBD measured in difference temperatures.

$$I_F(V_F(T_j), T_j) = \frac{1}{R_S(T_j)}\left[V_F(T_j) - \Phi_B - \frac{nkT_j}{q}\ln\left(\frac{P_d(V_F(T_j), I_F(T_j))}{SA^* {T_j}^2 V_F(T_j)}\right)\right] \tag{3.23}$$

where R_s is the series resistance of the SiC SBD. The best fitted linear line can be obtained as the load line from the calculated constant power curve.

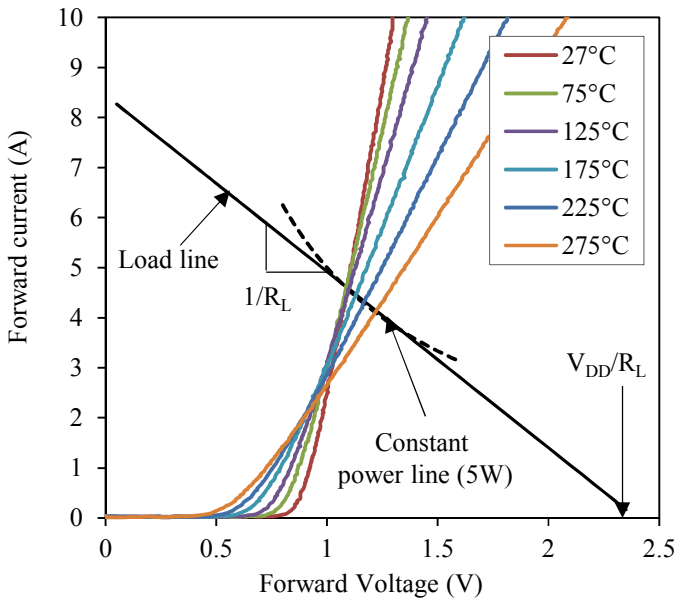


Fig. 3.8 Forward characteristics of SiC SBD in temperature range from 27°C to 275°C, and the load line from the equivalent power line of 5W to determine the load resistance and the voltage source.

Figure 3.8 shows the forward characteristics of the SiC SBD measured in the temperature range from 27°C to 275°C, the constant power curve of 5W and the load line. As can be seen from Fig. 3.8, the constant power curve is well matched with the straight load line within the measured temperature range.

In this measurement, the dissipated power in the SiC SBDs was set as 5W to limit the maximum difference between the junction and the reference temperature under 20°C due to the assurance for the linearity of each measurement [25]. The values of R_L and V_{DD} can be determined from a slope of the load line and the intersection point between the load line and x-axis, respectively. The value of R_L (0.28 Ω) and V_{DD} (2.36V) were determined from Fig. 3.8. In the test circuit, R_1 of 0.253 Ω was determined with consideration for on-resistance of the MOSFET (0.017 Ω) used as the switch SW_1, and R_2 of 0.01 Ω was used to measure the forward current of the DUT.

In the heating phase, the power of 5W is supplied into the DUT with closing the switch $SW1$ to heat up the DUT. The heating phase is continued until entrance of the thermal steady state of the DUT, and I_F and V_F are collected to calculate P_d. If the DUT reaches thermal steady-state, the switch $SW1$ is opened, and the measurement changes into the cooling phase. In the cooling phase, the constant current of 1mA is supplied into the DUT to measure V_F that varies with the decrease of the temperature of DUT. The power dissipation in the DUT due to the sensing current is so small that self-heating effect on the junction temperature can be neglected.

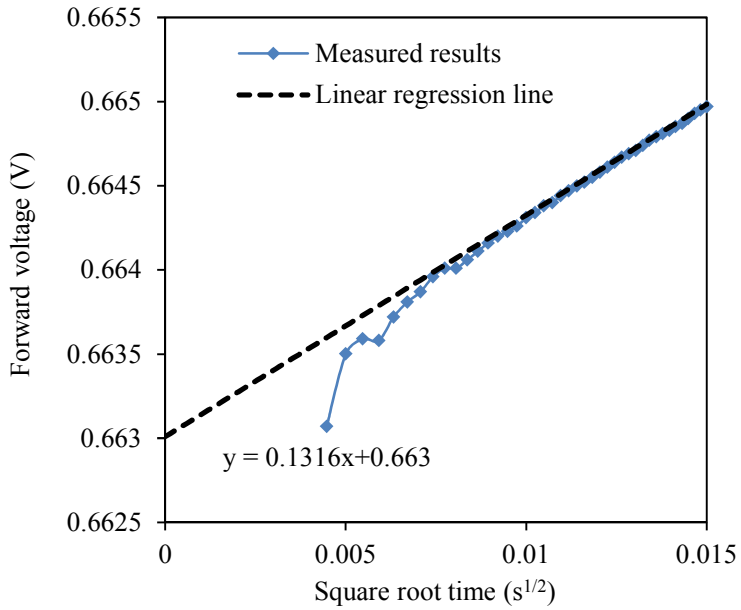


Fig. 3.9 Waveform of forward voltage of SiC SBD and the linear regression line against the square root of time at the reference temperature of 27°C.

There is transition time between the heating and cooling phase due to electrical switching. The cooling of the junction temperature of the packaged SiC SBD during the transition time results in V_F variation. Based on the heat transfer theory, V_F variation during the transition time can be estimated using the linearly fitted line against a square root of cooling time after stopping the supplied power [26]. The linear regression from the measured V_F at reference temperature of 27°C is shown in Fig. 3.9.

The junction temperature was calculated using the measured V_F and K-factor through Eq. (3.21). The temperature measurement of the bottom copper layer was carried out simultaneously with V_F measurement using the K-type thermocouple and an AD595aq thermocouple amplifier with cold junction compensation function [27]. Finally, the transient thermal resistance of the packaged SiC SBD was calculated using the obtained P_d, T_j, T_c and Eq. (3.24)

$$Z_{th}(t) = \frac{T_j(t) - T_c(t)}{P_d} \tag{3.24}$$

The transient thermal resistances were measured in reference temperature conditions from 27°C to 250°C with an incremental temperature step of 75°C. The reference temperature was controlled by a heat plate. The K-factors of the SiC SBD were obtained from the slope of the linearly fitted line from temperature dependence of V_F as shown in Fig. 3.6, and the K-factors at 27°C, 100°C, 175°C and 250°C were -1.84 mV/°C, -1.86 mV/°C, -1.88 mV/°C, and -1.90 mV/°C. All of the measured signals were acquired using a 16 bit AD converter (NI 9223) with sampling rate of 200 kHz, and were saved using the Labview program.

Figure 3.10 shows an example of the obtained waveforms for the transient thermal resistance measurement at reference temperature of 27°C. The dissipated power in the SiC SBD measured result in the heating phase is shown in Fig. 3.10(a). It is confirmed that the waveform of P_d is regulated to the constant value of about 5.01W. The forward voltage drop, the junction temperature, and the bottom copper layer temperature are acquired results in the cooling phase. It is shown that V_F increases as T_j decreases in the cooling phase in Fig. 3.10(b). The calculated T_j and the measured T_c are represented by the solid line and the dashed line, respectively in Fig. 3.10(c). Figure 3.10(d) shows the transient thermal resistance of the packaged SiC SBD between the junction and bottom copper layer.

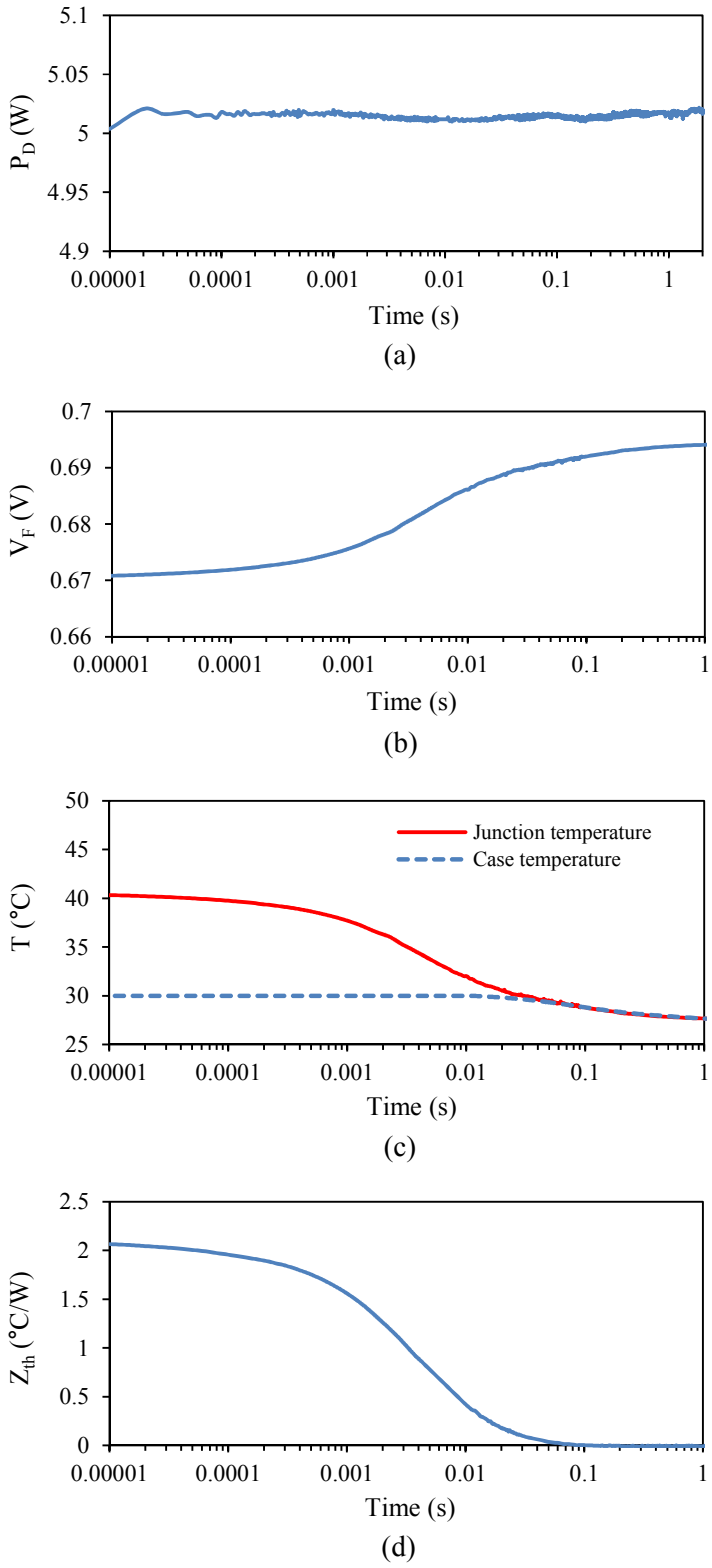
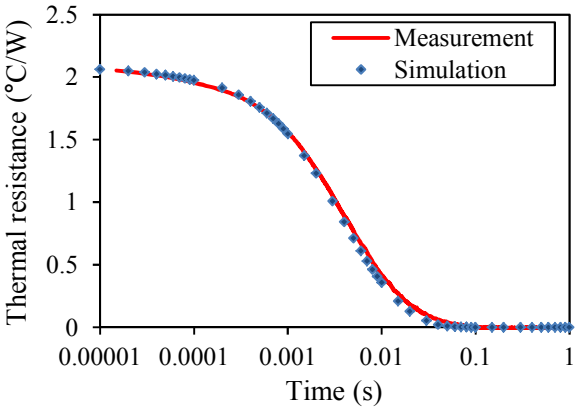


Fig. 3.10 Waveforms for the transient thermal resistance measurement at reference temperature of 27°C.

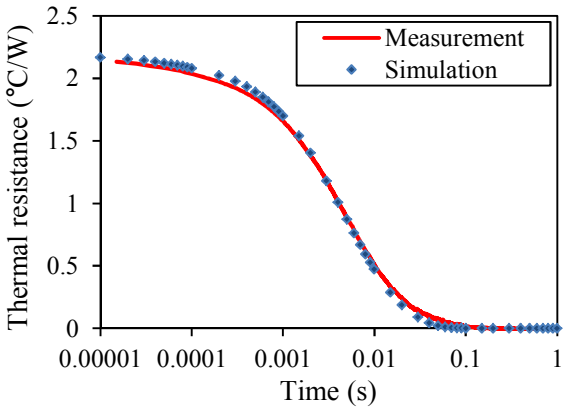
3.5 Comparison and discussion

The transient thermal resistances of the packaged SiC SBD from the numerically simulated results were calculated using Eq. (3.24). The surface average temperatures for the SiC SBD device were used as the junction temperature in this calculation. The comparison between calculated and the experimentally measured results are shown in Fig. 3.11 and Fig. 3.12.

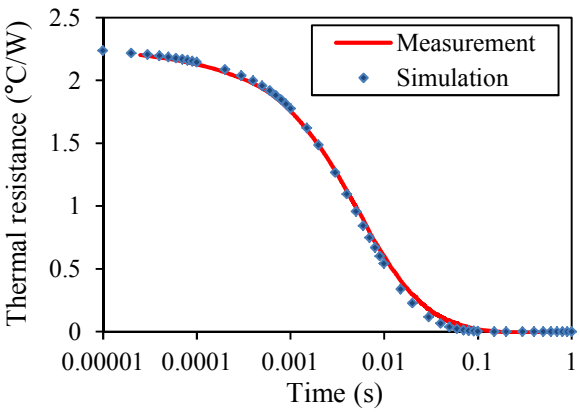
Figure 3.11 shows the transient thermal resistance of the packaged SiC SBD in the cooling phase. As can be seen from Fig. 3.11, the transient thermal resistances of the packaged SiC SBD start to decrease at 0s and reach the thermal steady state around 90ms.



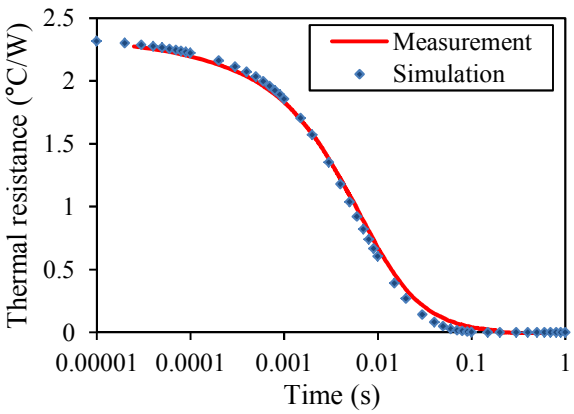
(a) Transient thermal resistance at 27°C



(b) Transient thermal resistance at 100°C



(c) Transient thermal resistance at 175°C



(d) Transient thermal resistance at 250°C

Fig. 3.11 Transient thermal resistances of the packaged SiC SBD between the junction and bottom copper layer during the cooling phase.

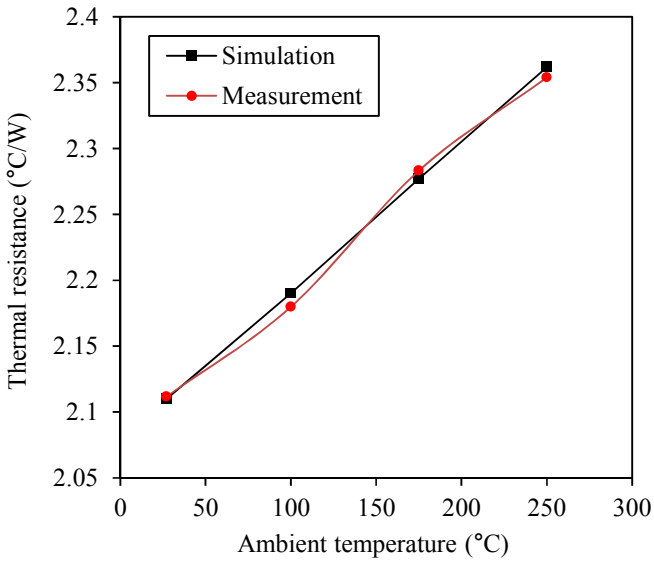


Fig. 3.12 Steady state thermal resistance of the packaged SiC SBD between the junction and bottom copper layer as a function of ambient temperature.

The measured and simulated results show same trends and good agreements, but, the simulation results have slightly faster responses than experimental results after about 10ms. The transient period in the transient thermal resistance is extended with temperature rise, and this represents the increase of the thermal time constant of the packaged SiC SBD.

Figure 3.12 shows the steady state thermal resistance of the packaged SiC SBD for the measured and simulated results in different ambient temperature conditions. The both results are in good agreement under maximum error of 0.76% of and average error of 0.36%. The thermal resistance increases by about 0.26°C/W (about 10%) while the ambient temperature increases from 27°C to 250°C.

In the experimentally measured temperature range, temperature rise increases the thermal conductivities and decreases specific heats of all of the package materials. The thermal simulation with the temperature dependent thermal properties was carried out, and the simulation results are well matched with the experimentally measured results. Thermal resistance rise represents the degradation of heat dissipation ability of the packaged device. It is recommended that heat dissipation system design with considering this point in the thermal management of the packaged SiC devices for high temperature operation. In addition, the FDM thermal model considering temperature dependent thermal properties introduced in this research can be applicable to design of the heat dissipation system of power electronics applications with SiC devices for high temperature environment.

3.6 Conclusion

In this chapter, thermal analysis of the packaged SiC SBD was carried out using the experiments and the numerical simulation for high temperature operation. The FDM thermal model for the packaged SiC SBD was built and simulated considering temperature dependence thermal properties. The steady state and transient thermal resistances of the packaged SiC SBDs were measured and compared with that for the numerically simulated results of FDM thermal model. Consequently, the comparison between both results showed good agreement.

The temperature affects the thermal characteristic of the packaged SiC SBDs. The steady state thermal resistance and thermal time constant of the packaged SiC SBD increased and extended with temperature rise, respectively. As a result, the consideration of the temperature effect on thermal characteristics of the packaged SiC devices is recommended for high temperature operation.

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Chapter 4:

Characterization and analysis of partial thermal resistances of packaged SiC SBDs

4.1 Introduction

In chapter 3, the transient and steady state thermal resistances between the junction and bottom copper layer of the packaged SiC SBD are characterized and analyzed using the experimentally measured and numerically simulated results. These results present the thermal characteristics of the whole package without any information about the thermal description of each layer of the packaged device.

The packaged SiC devices have a multi-layered structure that consists of different materials for electrical connection and insulation, and heat dissipation. Each layer of the packaged SiC devices has different thermal characteristics due to the different thermal properties and various structure shapes. The investigation of the thermal characteristics of each layer of the packaged device can be very helpful for the design, manufacturing, and failure analysis of the packaged device. The specific layer with the high thermal resistance can be modified in the design of the package, and the unpredictable increase of the thermal resistance values of the layer in the packaged device through the reliability test indicates the structural damage such as cracks, and it is possible to respond to such a failures.

As presented in chapter 1, the thermal properties of the packaged component materials change with temperature, and it results in the change of thermal characteristics of the packaged device. Especially, in case of the package materials such as the metals and the 4H SiC material, the thermal conductivities decrease with temperature above a room temperature [1]-[4]. As can be seen in chapter 3, this effect results in the degradation of the thermal performance of the packaged SiC devices in the high temperature operation. Through the detailed examination on the thermal resistances of the layers inside the packaged SiC device in wide temperature ranges, it can be observed that the contribution ratio of each layer to total thermal resistance, and the effects of the temperature for the thermal resistance of each layer.

In this chapter, the partial thermal resistances of the packaged SiC device and its temperature dependence are investigated. First, the concept of the partial thermal resistance of the packaged semiconductor device is described. In section 4.3, the transient thermal resistances of the packaged

SiC SBD are measured at elevated temperature conditions, and the partial thermal resistances of each layer for the packaged SiC SBD are extracted and analyzed using the cumulative and differential thermal structure functions. Section 4.4 shows the comparison and discussion of the partial thermal resistances of the packaged SiC SBD with the simulation results from the finite difference thermal model. Finally, this chapter is summarized in section 4.5.

4.2 Partial thermal resistance network of packaged SiC SBD

Figure 4.1 shows the schematic cross section of the packaged SiC SBD, and the partial thermal resistance network. The partial thermal resistances of the packaged SiC SBD are the thermal resistance of each layer in the heat flow path inside the package, and the total thermal resistance is the sum of all of the partial thermal resistances. In general case, the packaged device has the heat sink or the heat dissipated system in the case bottom to remove the generated heat from power loss of the semiconductor device. Therefore, the most of the generated heat flows into the bottom direction inside the packaged device, due to the low thermal resistance compared to the other direction. The generated heat from the semiconductor device flows through the die attach layer, and spreads in the substrate layer with the diffusion angle, and the thermal conductivities and the geometrical structure shapes of the stacked layers in this heat flow path are critical factors to determine the partial thermal resistance of the packaged SiC devices.

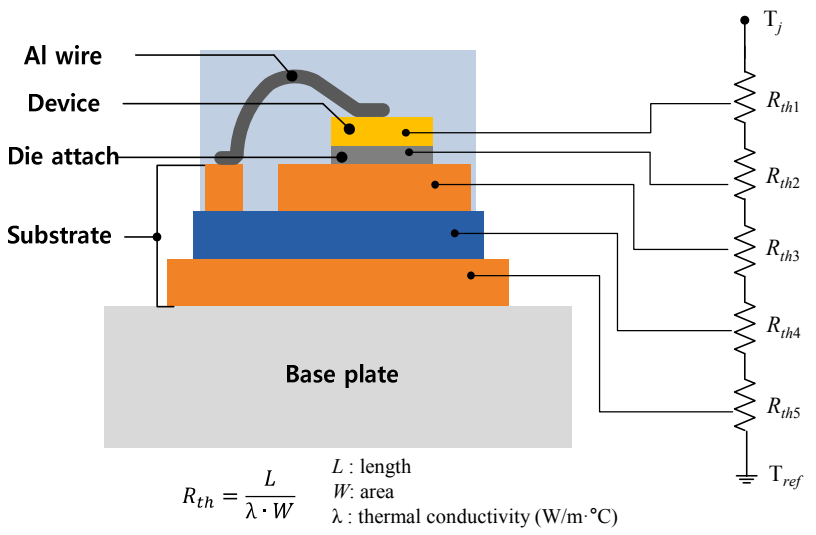


Fig. 4.1 Schematic cross sectional view of the packaged semiconductor device, and partial thermal resistance network.

In the Fig. 4.1, R_{th1}, R_{th2}, R_{th3}, R_{th4}, and R_{th5} represent the thermal resistance of the device, the die-attach layer, the pattern copper layer, the Si_3N_4 ceramic layer, and the bottom copper layer.

4.3 Thermal characterization of packaged SiC SBD

4.3.1 Experimental thermal measurement

The partial thermal resistances of the packaged SiC SBD can be extracted from the transient thermal resistance between the junction and bottom copper layer [5],[6]. Using the measurement system introduced in chapter 3, the transient thermal resistances were measured in reference temperature conditions from 27°C to 275°C with an incremental temperature step of 50°C.

For the junction temperature measurement, the *K*-factors of the SiC SBD were obtained from the slope of the linearly fitted line from temperature dependence of V_F measured using the forward current of 1mA as shown in Fig. 3.6. The *K*-factor at 27°C, 75°C, 125°C, 175°C, 225°C and 275°C were determined to be -1.84 mV/°C, -1.86 mV/°C, -1.87 mV/°C, -1.88 mV/°C, -1.89 mV/°C and -1.91 mV/°C.

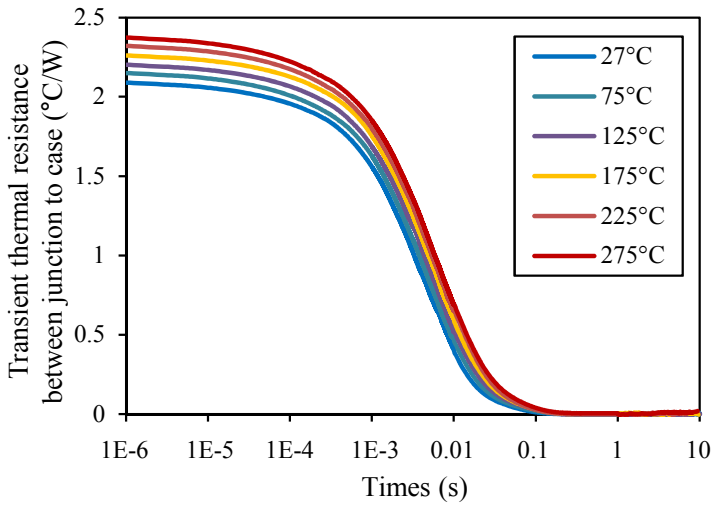


Fig. 4.2 Transient thermal resistances of the packaged SiC SBD in reference temperatures of 27°C, 75°C, 125°C, 175°C, 225°C, and 275°C

In the transient thermal resistance measurement, the device was heated with the supplied power of 5W in the heating phase, and the forward voltage drop of the SiC SBD was measured with supplying

the constant current of 1mA in the cooling phase. Using the measured dissipated power (P_d), junction temperature (T_j), and bottom copper layer temperature (T_c) and Eq.(4.1), transient thermal resistances of the SiC SBD in reference temperatures of 27°C, 75°C, 125°C, 175°C, 225°C, and 275°C were calculated as shown in Fig. 4.2.

$$Z_{th}(t) = \frac{T_j(t) - T_c(t)}{p_d} \tag{4.1}$$

4.3.2 Thermal structure functions

The measured transient thermal resistances were converted into the cumulative and differential thermal structure functions to obtain the partial thermal resistances of the packaged SiC SBD. This process was carried out using "T3ster master" that practices the network identification by deconvolution (NID) method and Foster to Cauer network conversion [7].

The converted thermal model was expressed on the cumulative and differential structure functions based on Cauer equivalent network to interpret the physical description along the one-dimensional heat flow path. The thermal structure functions show the thermal resistance-capacitance map along the heat flow path from the junction to reference point, and thermal partial resistances and capacitances can be determined on the structure functions [8]-[10]. The cumulative thermal structure function is a plot of the cumulative thermal capacitance as function of cumulative thermal resistances in the thermal system. On the other hand, the differential structure function is defined as the derivative of the cumulative structure function as follows:

$$K\left(\sum R\right) = \frac{d\sum C_{th}}{d\sum R_{th}} \tag{4.2}$$

In the horizontal axis of the structure functions, the origin and end point correspond to the junction and the reference point, respectively. In the cumulative structure function, the flat plateaus express the thermal mass of the region of the heat conduction path in the stacked material layers. In the differential structure function, the local peak points represent the interfaces between the stacked material layers in the heat flow path, and the distance between two peaks on the horizontal axis gives the partial thermal resistance values.

Figure 4.3 shows the converted differential (upper) and cumulative (below) thermal structure functions. Four peak points and the five plateau regions are observed in the differential and cumulative thermal structure functions, respectively, and the partial thermal resistances of the

packaged SiC SBD that has 5 stacked layers can be extracted from these results.

Figure 4.4 shows the first interface point between SiC SBD device and the die attach layer in the differential and cumulative thermal structure functions for SiC SBD (R_{th1}). In the differential structure functions, it can be observed that the peak points at the temperature of 27°C move to right side on the horizontal axis with temperature rise. It represents that the partial thermal resistance increases with temperature rise. From this result, the effect of temperature for the partial thermal resistance of the SiC SBD can be obtained, and the other partial thermal resistance can be obtained through the similar procedures.

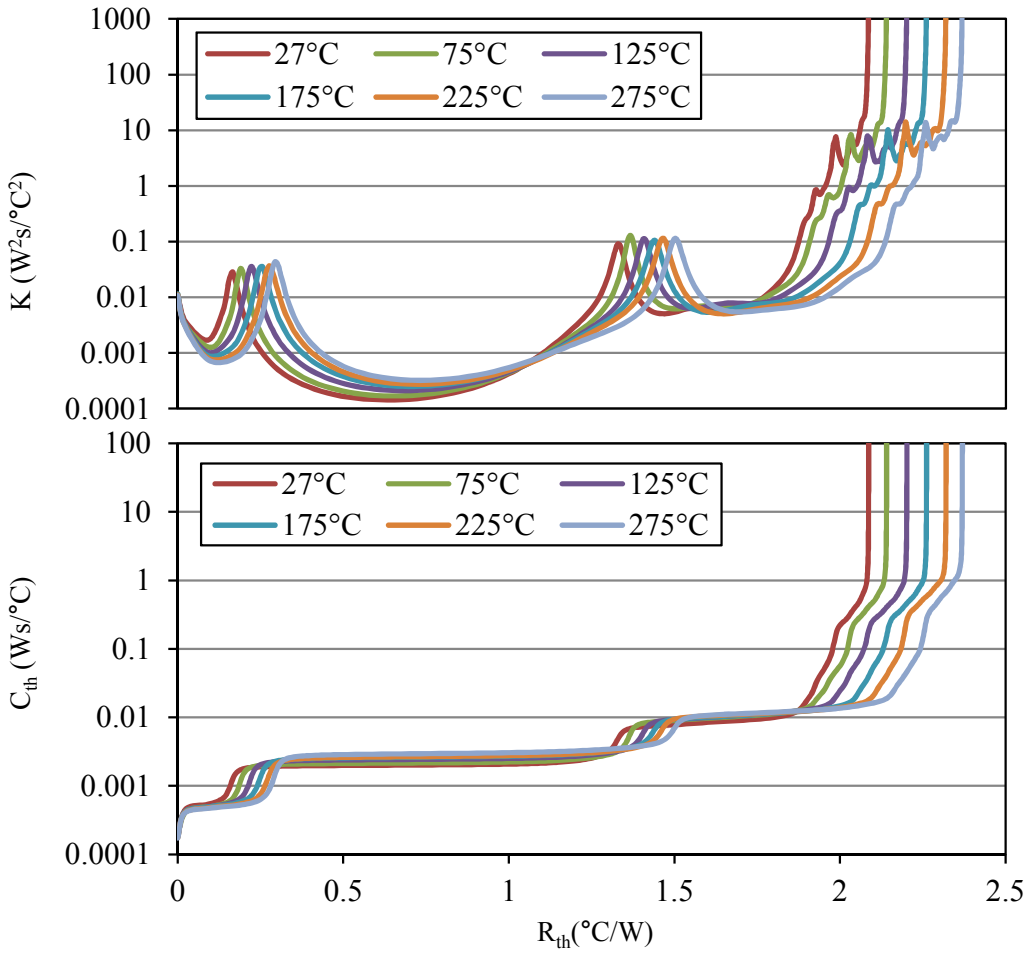


Fig. 4.3 Differential (upper) and cumulative (below) thermal structure functions of packaged SiC SBD in temperature range from 27°C to 275°C.

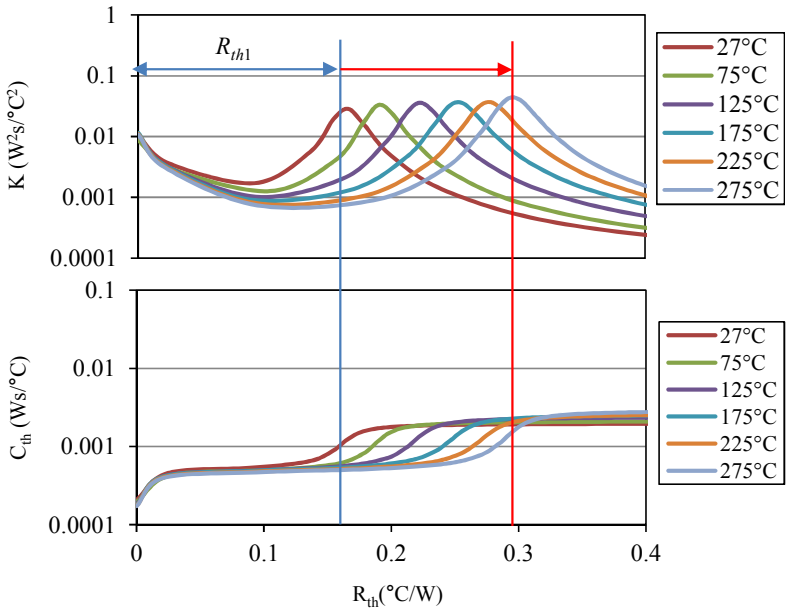


Fig. 4.4 Expansion of differential (upper) and cumulative (below) thermal structure functions around the first interface point between the SiC SBD device and the die attach layer.

4.4 Partial thermal resistance of packaged SiC SBD

4.4.1 Partial thermal resistance with FDM

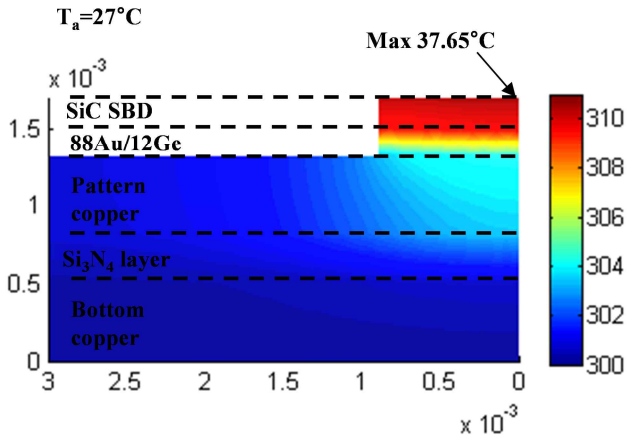
To present the validity of the extracted partial thermal resistances of the packaged SiC SBD, the numerical simulation was carried out using the finite difference thermal model with temperature dependent thermal properties introduced in chapter 3.

The thermal simulation was carried out with the condition of the supplied power of 5W in the reference temperatures that were same with the measured conditions. Figure 4.5 shows the steady-state temperature distribution of the simulated model at reference temperature of 27°C (a), and the profiles of temperature difference at the center position between the junction and bottom copper layer in different reference temperature conditions (b).

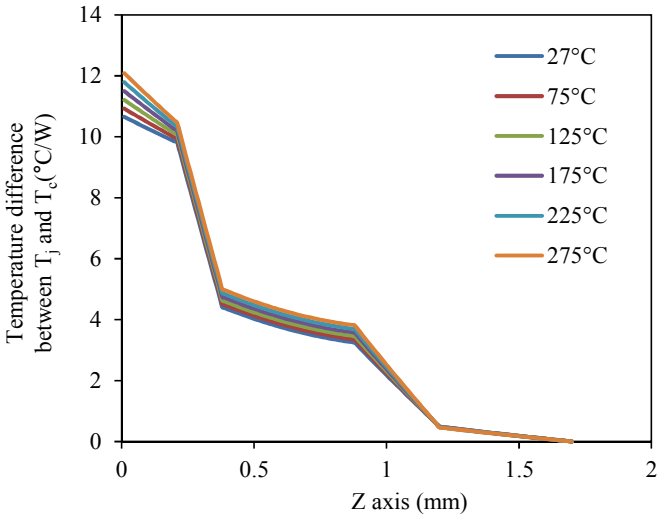
The partial thermal resistances of each layer of the packaged SiC SBD can be extracted from the simulated results. The steady state thermal resistance of the packaged semiconductor is defined by:

$$R_{th} = \frac{T_j - T_r}{P_d} \tag{4.3}$$

The partial thermal resistance calculation is based on the Eq. (4.3). The T_j and T_r are replaced by the surface temperatures of the interface of the two layers.



(a)



(b)

Fig. 4.5 Simulated results: steady state temperature distribution of packaged SiC SBD at ambient temperature of 27°C (a), and profiles of temperature difference between the junction and the bottom copper layer in the temperature range from 27 to 275°C.

Figure 4.6 shows the simulated two-dimensional temperature profiles of the packaged SiC SBD at reference temperature of 27°C. As can be seen from Fig. 4.6, the temperatures of the surfaces of the stacked layers are not really isothermal. The average surface temperatures of the interfaces of each stacked layer were used in the calculation of the partial thermal resistance. The partial thermal resistances of the experimentally measured and the numerically simulated results are shown in Fig. 4.7 and Fig. 4.8.

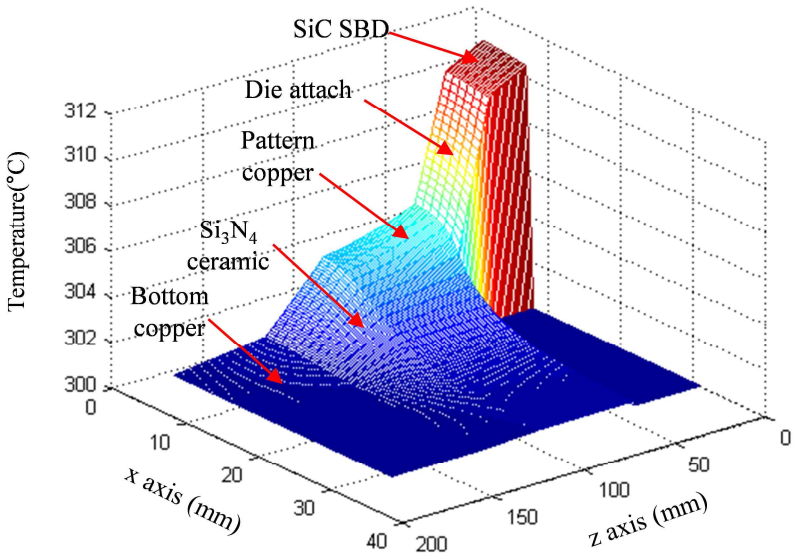


Fig. 4.6 Two-dimensional temperature profiles of the packaged SiC SBD at reference temperature of 27°C

4.4.2 Comparison and discussion

At case temperature of 27°C, the measured partial thermal resistances of the SiC SBD, die attach (88Au/12Ge), pattern copper, Si_3N_4 substrate and bottom copper are determined to be 0.168°C/W, 1.168°C/W, 0.252°C/W, 0.393°C/W, and 0.109°C/W, respectively.

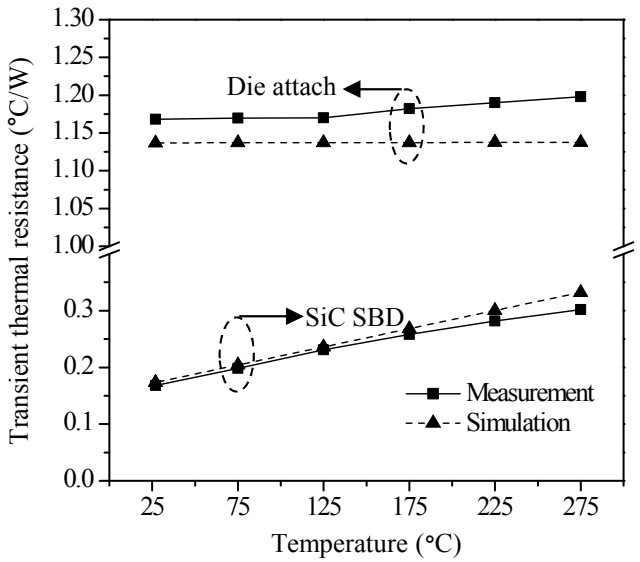


Fig. 4.7 Partial thermal resistances of the SiC SBD and the die attach layer.

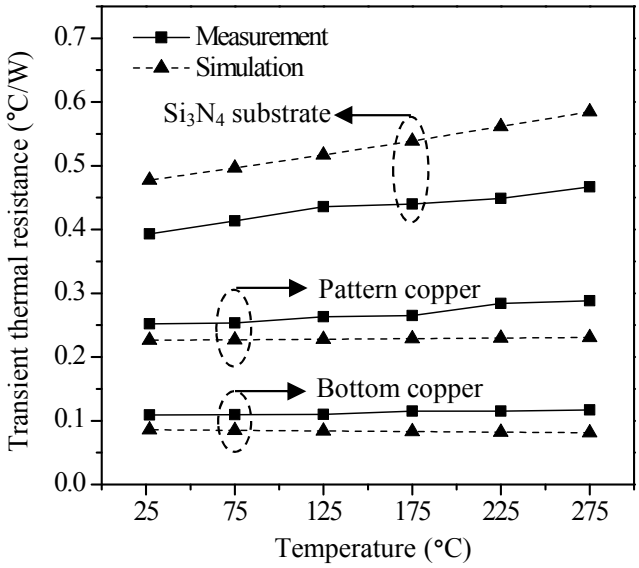


Fig. 4.8 Partial thermal resistances of the AMB substrate.

The thermal resistance of the SiC SBD device occupies 8% of the total thermal resistance. The die attach layer has the largest portion of the total steady state thermal resistance (about 56%). The bottom copper has the lower partial thermal resistance than the pattern copper due to the enlargement of the heat conduction area through the diffusion of the heat flow in the layer. From the simulated results, the partial thermal resistances of the SiC SBD, die attach, pattern copper, Si_3N_4 substrate and bottom copper are calculated to be 0.173°C/W, 1.137°C/W, 0.226°C/W, 0.477°C/W, and 0.086°C/W, respectively.

All of the measured partial thermal resistances increase with temperature. It is observed that the dominant partial thermal resistance variation is resulted from the SiC SBD. The partial thermal resistance of the SiC SBD increases from 0.168°C/W to 0.302°C/W in temperature increase from 27°C to 275°C. The partial thermal resistance of the Si_3N_4 substrate has increase of 19% with the whole temperature increase. The partial thermal resistances of the other layers increase with the temperature, slightly. The partial thermal resistance variation with temperature from the simulated results has similar trends with that of the measured results. In the comparison, the both partial thermal resistances of SiC SBD show good agreement, and the measured results of the other layers are acceptably consistent with the simulated results. The differences in the comparison results can be explained by the simplified thermal model of the packaged SiC SBD. The real packaged SiC SBD has the more complex shape, so that the heat in real situation diffuses through more various ways than that of the simulation condition. Apparently, the several terminal patterns that are not expressed in the

thermal model are attached on the Si_3N_4 substrate, and the Si_3N_4 substrate shows the big difference between the experimented and simulated results.

4.5 Conclusion

In this chapter, the partial thermal resistances of the packaged SiC SBD for high temperature operation have been investigated. The transient thermal resistances of the packaged SiC SBD between the junction and bottom copper layer were measured using the electrical switching measurement method under various temperature conditions, and the partial thermal resistances were determined using the cumulative and differential thermal structure functions. The extracted partial thermal resistances of the packaged SiC SBD were compared with that from the FDM simulation results, and the comparison showed good agreement.

It is confirmed that the steady state thermal resistance of the packaged SiC SBD were increased with temperature rise, and the SiC device and the Si_3N_4 substrate comprise a significant portion of the overall thermal characteristics variation of the packaged SiC SBD. The research results recommend the use of the thermal resistance model including temperature effect in design of the power electronics applications with the packaged SiC SBD for high temperature operation.

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Chapter 5:

Thermal measurement and characterization of packaged SiC MOSFETs

5.1 Introduction

Among the SiC devices, SiC MOSFETs are the attractive device to replace Si IGBTs used in various fields of the industrial, consumer and automotive. The comparison between the SiC MOSFETs and Si IGBTs has been reported through the several research results [1]-[4]. These researches have informed that SiC MOSFETs have the different electrical characteristics compared to Si IGBTs in the temperature variation condition. In the measurement of the transient thermal characteristics of the packaged SiC MOSFETs, the temperature sensitive electrical parameters (TSEPs) are required to measure the junction temperature, and these results offer the necessity for the researches of the TSEPs for the SiC MOSFETs.

On the other hand, the measured transient thermal results should be characterized and modeled to analyze the thermal performance of the packaged devices or to simulate the junction temperature of the device. There are several methods for these tasks [6]-[8]. The thermal-resistance analysis by induced transient (TRAIT) method introduced in chapter 2 is one of the frequently used methods to analyze the thermal resistance of the packaged semiconductors [9],[10]. The TRAIT method characterizes the thermal behavior of the packaged semiconductors using the finite terms of series of exponential time constants, and enables the thermal analysis inside the packaged semiconductors [11]-[13]. However, the TRAIT method shows some drawbacks. In the packaged system that has the unknown or complex internal structure, the determination of the number of the time constants is difficult, and the help of the numerically simulated thermal data is required for the accurate thermal analysis.

In this chapter, the procedure for the measurement and analysis of the transient thermal characteristics of a packaged SiC MOSFET has been presented. In this work, the relationship between the gate-source voltage and temperature of the SiC MOSFET is introduced as the TSEP to measure the junction temperature. The theoretical background, experiment setup and calibration process for TSEP are described. The transient thermal resistance of the packaged SiC MOSFET is measured and characterized using a modified TRAIT method. To carry out the accurate thermal analysis of the packaged device, a modified method for the TRAIT is suggested. The characterized transient thermal

resistance of the packaged SiC MOSFET using a modified TRAIT method is compared to the results from the network identification by deconvolution (NID) method. Finally, the thermal partial resistances of the packaged SiC MOSFET are extracted and compared with the results from the NID and the thermal model based on the finite difference method (FDM).

5.2 Thermal measurement of packaged SiC MOSFET

5.2.1 Structure of packaged SiC MOSFET

A 600V/10A SiC MOSFET manufactured by "ROHM" was used as a device under test (DUT). The SiC MOSFET was assembled on a ceramic package (manufactured by "Kyocera") that had a copper bonded Al_2O_3 substrate using 88Au/12Ge solder for high temperature operation. The electrical connection inside the package was completed with an Al wire (diameter of 300um). A K-type thermocouple was attached on the center position of the SiC MOSFET device in the bottom copper layer of the package with the soldering contact for the reference temperature measurement. The package was filled with a high temperature resin manufactured by "ADEKA". The packaged SiC MOSFET with the thermocouple is shown in Fig. 5.1.

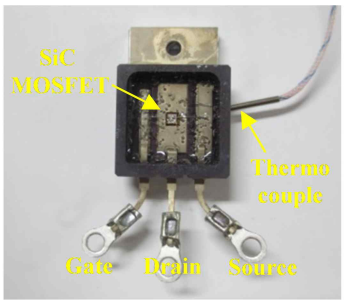


Fig. 5.1 Overview of the packaged SiC MOSFET with the attached thermocouple for reference temperature measurement

5.2.2 Thermal sensitivity electrical parameter for SiC MOSFETs

The output characteristics of the SiC MOSFETs in the saturation region under the supplied constant drain-source voltage (V_{DS}) can be expressed by the equation as follows:

$$I_D = \frac{1}{2}\mu_n(T)C_{OX}\frac{W}{L}\left[V_{GS} - V_{TH}(T)\right]^2 \tag{5.1}$$

where I_D is the drain current, μ_n is the electron mobility, C_{OX} is the intrinsic gate channel oxide capacitance, W/L is the gate width/length ratio, V_{GS} is the gate-source voltage, V_{TH} is the threshold voltage and T is the temperature. In Eq. (5.1), μ_n, and V_{TH} have the temperature dependence characteristics [14]. The electron mobility is limited by several scattering processes, and decreases with temperature. The temperature dependence of the electron mobility can be empirically modelled by given Eq. (5.2),

$$\mu_n = \mu_n(T_0)\left(T/T_0\right)^{\alpha} \tag{5.2}$$

where T_0 is the reference temperature. In case of the 4H silicon carbide, α is about -2.7. V_{TH} decreases with temperature due to the temperature dependence of the Fermi level in a channel region, and it is described by Eq. (5.3),

$$V_{TH} = V_{FB}(T) + 2\Psi_B(T) + \frac{\sqrt{4\varepsilon_{sic}qN_A\Psi_B(T)}}{C_{OX}} \tag{5.3}$$

where ε_{sic} is the dielectric constant of the silicon carbide, q is the electron charge, N_A is the doping density, V_{FB} is the flat band voltage and Ψ_B is the potential difference between the Fermi level and the intrinsic Fermi level.

For given constants I_D and V_{DS} across the SiC MOSFET, the Eq. (5.1) can be rearranged into an equation for V_{GS} as follows:

$$V_{GS} = \left[\frac{2I_D}{\mu_n(T)C_{OX}}\frac{L}{W} + V_{TH}(T)\right]^{1/2} \tag{5.4}$$

The right side of the Eq. (5.4) includes the temperature dependence parameters, and V_{GS} can be used as the temperature parameter to measure the junction temperature of the SiC MOSFET.

5.2.3 System for thermal measurement of packaged SiC MOSFETs

Figure 5.2 shows the measured transfer characteristics of the packaged SiC MOSFET under the fixed drain-source voltage condition using the conventional curve tracer in temperature range from 25 to 225°C. It can be observed that the gate-source voltage of the SiC MOSFET changes with the temperature variation under the constant current operation.

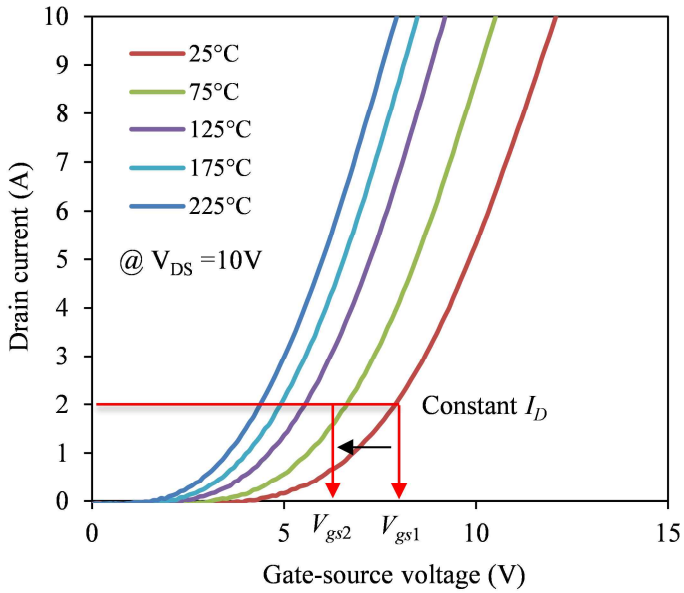
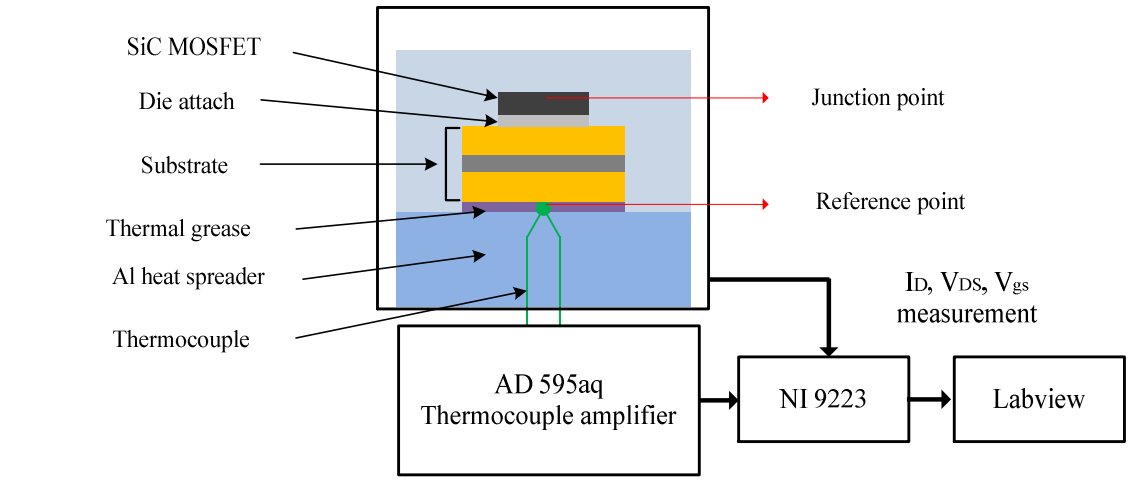


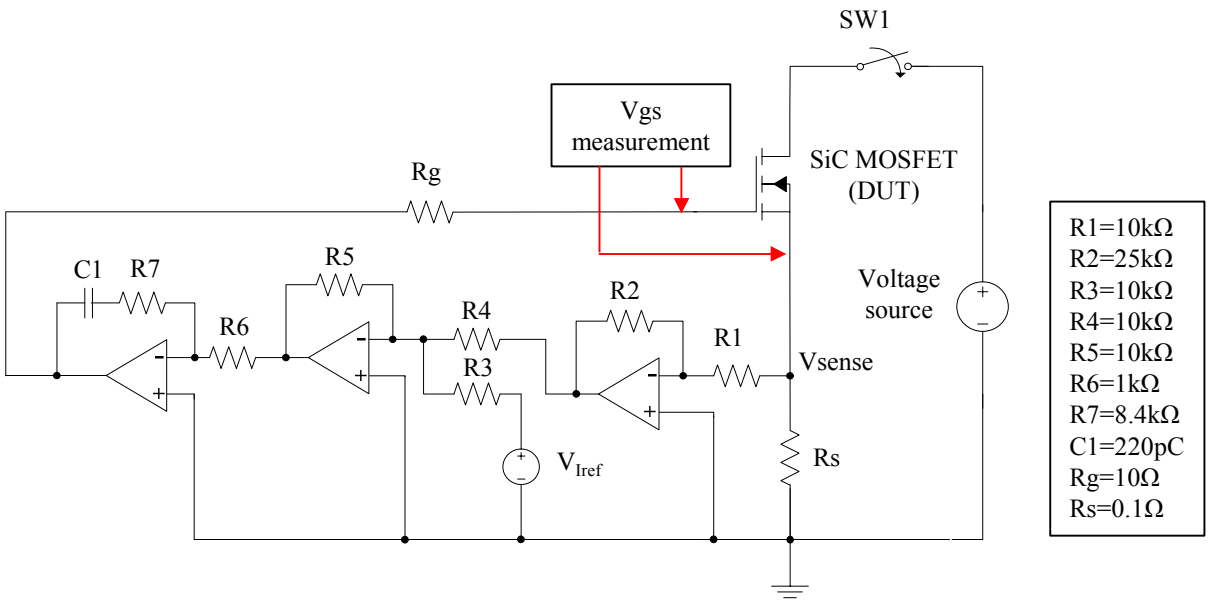
Fig. 5.2 Transfer characteristics of the SiC MOSFET

It is difficult to supply the constant current into the packaged SiC MOSFET under the fixed drain-source voltage using the conventional test circuit, because the on-resistance of the SiC MOSET changes with temperature rise in operation of the packaged SiC MOSFET due to the self-heating. For the transient thermal measurement with the temperature dependence of the gate-source voltage, the SiC MOSFET should be operated under the constant current and the fixed drain-source voltage condition.

For this thermal measurement, a test circuit with the current regulation function was developed as shown in Fig 5.3(a), and the schematic view of the measurement system is shown in Fig. 5.3(b). The operation of the test circuit is started with closing SW1 (SPW20N60S, Infineon). The SW1 is closed, and the current is injected into the SiC MOSFET. The injected current is sensed by the voltage drop of R_s, and this signal is amplified by an inverting amplifier. The amplified signal is input into a feedback loop with a PI controller. The feedback control loop adjusts the gate-source voltage of the SiC MSOFET to match the sensing voltage V_{sense} with reference voltage (V_{Iref}). The total voltage drop from the voltage source consists of the voltage drop of R_s, SW1 and the drain-source voltage of the SiC MOSFET. The variation of the voltage drop of SW1 due to self-heating was limited by the cooling system. As the feedback control drives voltage drop of R_s to be kept constant, the constant drain current flows into the SiC MOSFET. Consequently, the drain-source voltage of the SiC MOSFET keeps the constant value, and the dissipated power in the SiC MOSFET calculated by $P=I_D \cdot V_{DS}$ is regulated as the constant value.



(a)



(b)

Fig. 5.3 Experimental setup. (a) schematic view of the experimental measurement system (b) the test circuit to measure the transient thermal resistance of the packaed SiC MOSFETs.

The packaged SiC MOSFET was fixed on an air cooled aluminium heat sink. To reduce contact thermal resistance between the package and the aluminium heat sink, a thermal grease ("SUNHAYTO" SCH-30) was used. The supplied drain current, the gate-source voltage and the bottom copper temperature were measured and saved using AD converter (NI 9223) and Labview. Data sampling

rate was changed during the measurement process from 200kHz to 1kHz to save data for graphs with a logarithmic scale.

5.2.4 Measurement of temperature dependence of gate-source voltage

Prior to the measurement of the transient thermal resistance, the relationship between temperature and the gate-source voltage of the SiC MOSFET was calibrated with current pulses of 2A that have width of 200us. There was delay time (about 50μs) before the gate-source voltage measurement due to the switching period of the drain current of the SiC MOSFET. The self-heating during the measurement delay time increased the junction temperature that induces the gate-source voltage variation. After supplying power, the surface temperature rise of the device is expressed by [15]:

$$T_s(t) = T_{s0} + \frac{2\dot{q}}{\sqrt{\pi\lambda\rho c}}\sqrt{t} \tag{5.5}$$

where T_{s0} is initial temperature of the surface, $\dot{q}$ is the heat flux, λ is thermal conductivity, ρ is the density and c is the specific heat.

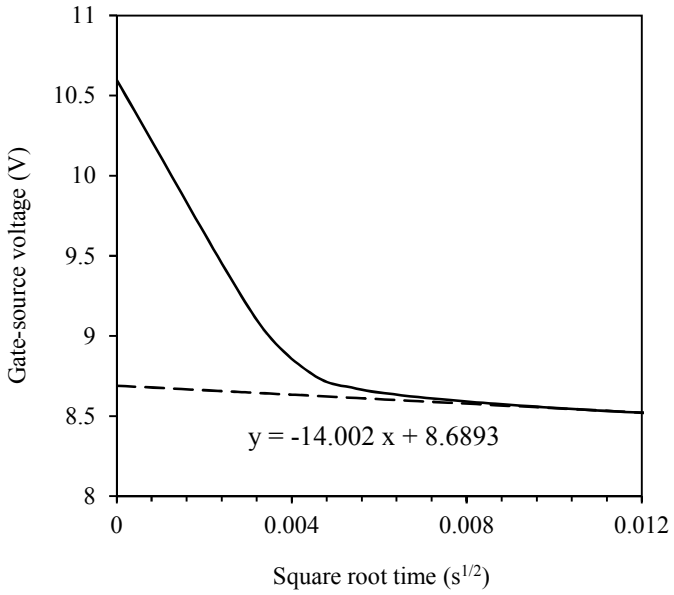


Fig. 5.4 Waveform of the gate-source voltage (solid line) and linear regression line (dashed line) as a function of the square root of time at room temperature.

From Eq. (5.5), it can be known that the surface temperature has the proportional relation with the square root of the time after supplying the power. The gate-source voltage at time t = 0s can be obtained using linear regression against the square root of the heating time as shown in Fig. 5.4.

The temperature of the packaged SiC MOSFET was raised by a hot plate, and was monitored with the thermocouple attached on the bottom copper layer. The calibration temperature range was from a room temperature to 210°C. The curve of the relationship between the temperature and the gate-source voltage of the SiC MOSFET is shown in Fig. 5.5. The relationship shown in Fig. 5.5 can be expressed by the following equation:

$$y = 0.00005\ x^2 - 0.0315\ x + 9.5043 \tag{5.6}$$

where x and y represent the temperature and the gate-source voltage, respectively.

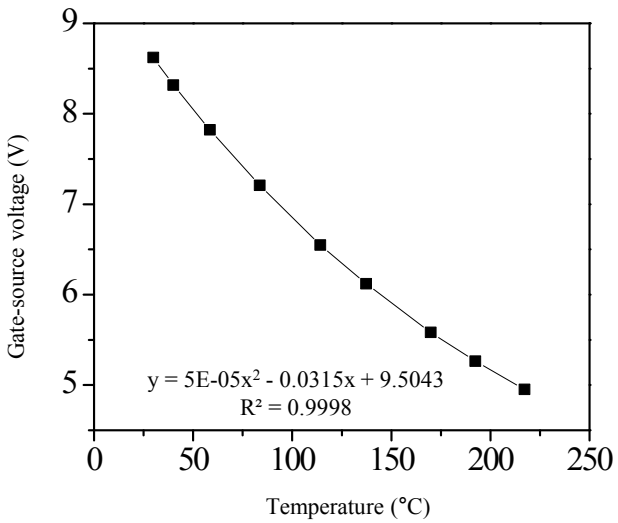


Fig. 5.5 Gate-source voltage and temperature calibration curve of the SiC MOSFET in temperature range from room temperature to 210°C.

5.2.5 Transient thermal resistance measurement

In the transient thermal measurement, the dissipated power of 20W in the SiC MOSFET was set with the drain current of 2A and the drain-source voltage of 10V, and the measured electrical and temperature waveforms of the packaged SiC MOSFET are shown in Fig. 5.6. As can be seen in Fig. 5.6, there is electrical transition region of about 50μs after switch-on, and waveforms of the drain current and drain-source voltage of the SiC MOSFET keep constant values with a function of time.

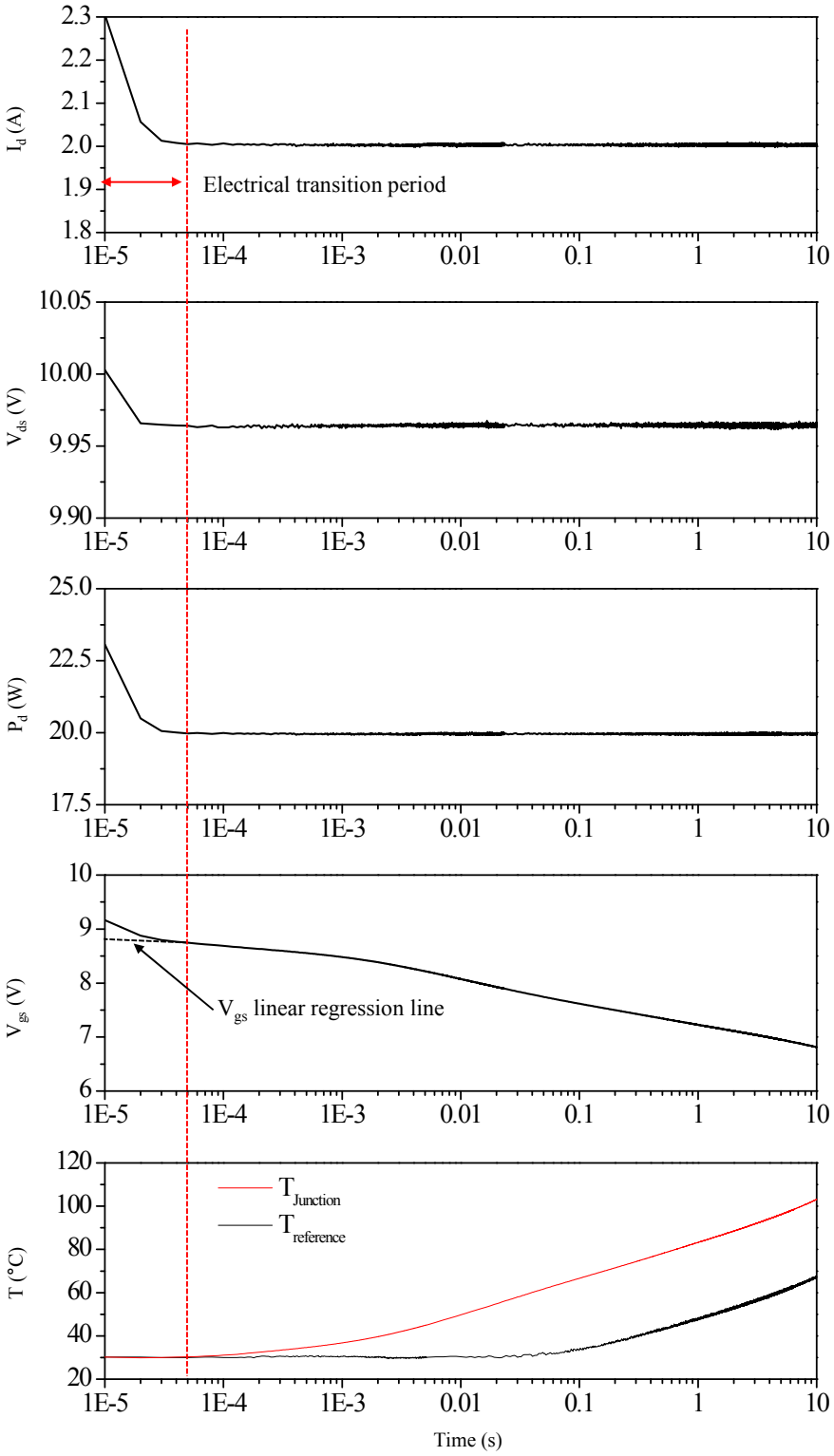


Fig. 5.6 Waveforms of the measured drain current, drain-source voltage, dissipated power, gate-source voltage, bottom copper layer temperature (reference temperature) and calculated junction temperature from the gate-source voltage of the packaged SiC MOSFET.

Consequently, it can be confirmed that the dissipated power in the SiC MOSFET was regulated to about 19.97W. Because the junction temperature increased with due to the self-heating, the gate-source voltage of the SiC MOSFET decreased. The gate-source voltage value of the SiC MOSFSET during transition region was estimated using the linear regression line against a square root of heating time after supplying the power as represented in Eq. (5.5). The junction temperature of the SiC MOSFET was calculated using the measured gate-source voltage and the Eq. 5.6, and the calculated result is shown by red line with the measured bottom copper layer temperature (reference temperature) by the thermocouple (black line).

The transient thermal resistance of the packaged SiC MOSFET was calculated using the measured results shown in Fig. 5.6 and Eq. (5.7), and calculated result is shown in Fig.5.7.

$$Z_{th}(t) = \frac{T_j(t) - T_r(t)}{P_d} \tag{5.7}$$

The transient thermal resistance increases slightly until about 1ms. The heat is conducted to the SiC MOSFET device in this region. The transient thermal resistance increases sharply between 1ms and 40ms due to effect of the lower thermal conductivity of the die attach material than that of the SiC material. After this region, the transient thermal resistance increases gradually, then, enters the steady state after 700ms. Total thermal resistance of the conduction path from the SiC MOSFET device to the bottom copper layer is 1.735K/W.

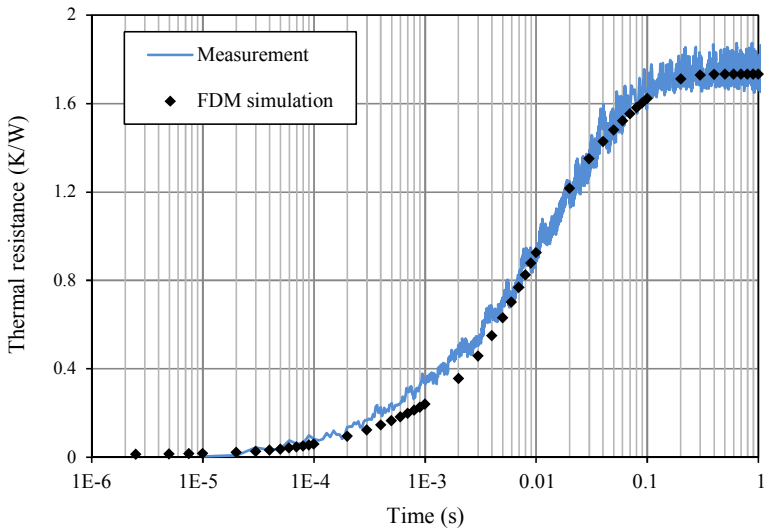


Fig. 5.7 The measured transient thermal resistance between the SiC MOSFET and bottom copper layer in the packaged SiC MOSFET.

5.3 Thermal characterization and modelling of packaged SiC MOSFET

5.3.1 Characterization of transient thermal resistance

Considering the transient thermal behaviour of the SiC MOSFET in heating condition when a step input power is supplied, the equation of the transient thermal resistance for the TRAIT method can be modified as follows:

$$Z_{th}(t) = \sum_{i=1}^{n} A_i \left[1 - \exp\left(-t/\tau_i\right)\right] \tag{5.8}$$

where, τ_i is the time constant and A_i is the amplitude factor.

The TRAIT method finds both the time constants and the amplitude factors corresponded to the time constants using the fitting process to the measured transient thermal resistance. The modified TRAIT method uses the fixed time constants in each region, and finds the only corresponded amplitude factors into the bound time constants in the fitting process. Figure 5.8 shows the concept of the modified TRAIT method. In this process, the real amplitude factors corresponded to the time constants are dispersed, and fitted into the adjacent time constants bound in each region. The fitted results generate the approximated transient thermal resistance to the original transient thermal resistance generated by the time constants and the corresponded amplitude factors to the time constants, and the accuracy of the approximated transient thermal resistance is determined by the number of the bound time constants.

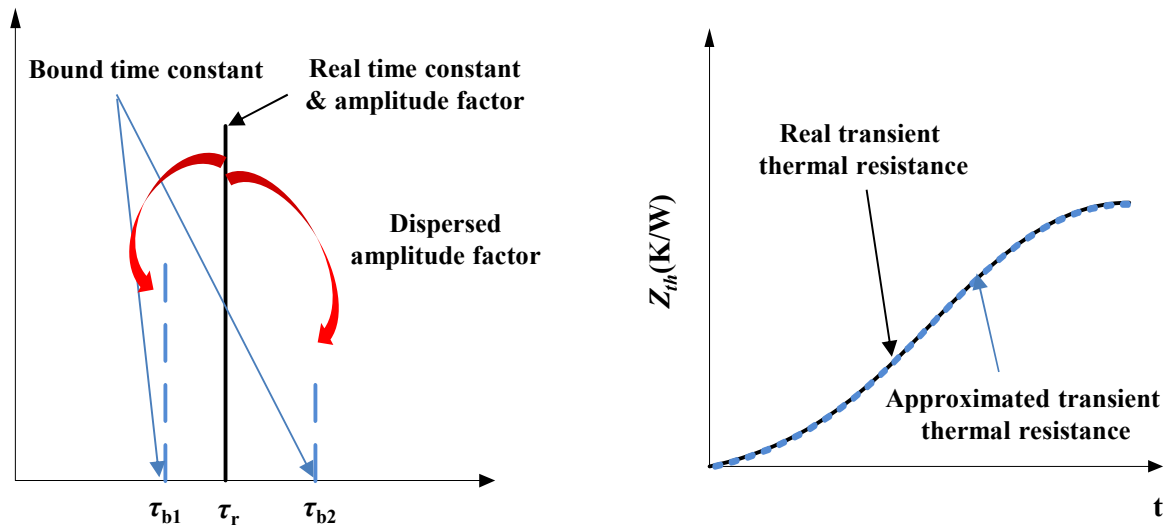


Fig. 5.8 The concept of the modified TRAIT method.

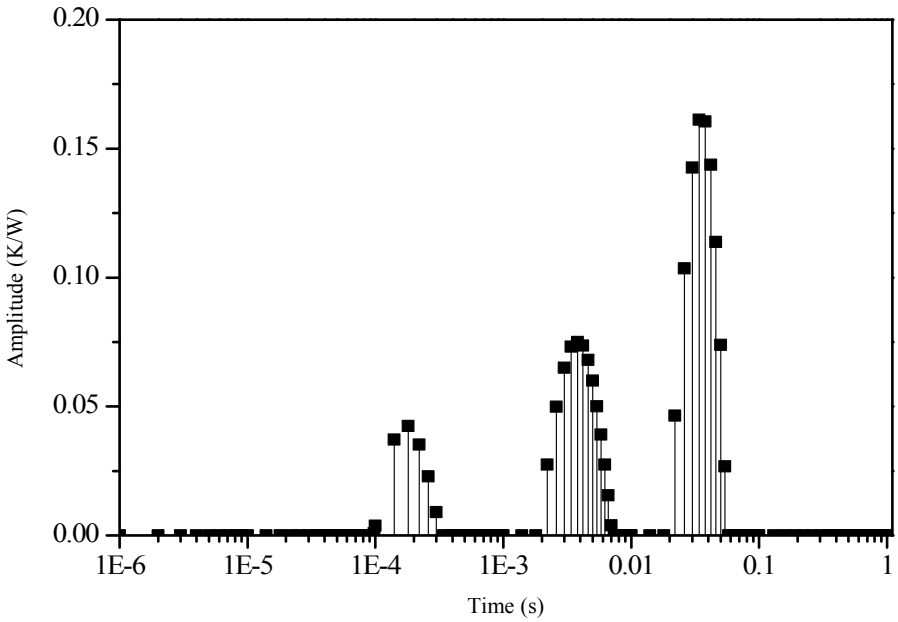


Fig. 5.9 Discrete time constant spectrum of the packaged SiC MOSFET through a modified TRAIT method.

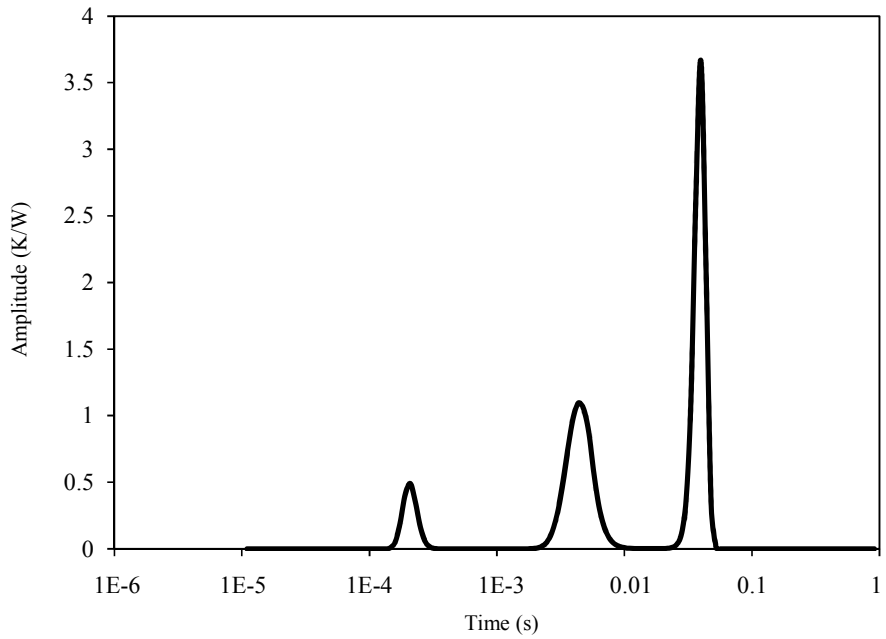


Fig. 5.10 Continuous time constant spectrum of the packaged SiC MOSFET from the NID method.

The measured transient thermal resistance was smoothed, and fitted using a nonlinear least square method using Eq. (5.8) and Levenberg-Marquardt algorithm [16],[17]. The total thermal response time was divided into 130 regions and time constants were bound to each region. The amplitude factors corresponded to each of the bound time constants were calculated in the fitting process. Using the extracted time constants and the amplitude factors, the discrete time constant spectrum was obtained as shown in Fig. 5.9.

The extracted thermal parameters were used to form the Foster equivalent thermal network with parallel configuration of resistance-capacitance given by $R_i=A_i$ and $C_i=\tau_i/A_i$. The Foster equivalent thermal network should be converted into the Cauer equivalent thermal network to obtain the physical description for the heat flow path from the junction to bottom copper layer (reference point). This conversion was carried out by the method described in [18],[19]. The differential (upper) and cumulative (bottom) structure functions based on the Cauer equivalent thermal network were calculated using the converted thermal parameters of the packaged SiC MOSFET. The calculated differential and cumulative structure functions of the packaged SiC MOSFET are shown as the blue lines in Fig. 5.11.

To compare the results from the suggested modified TRAIT method, the characterization of the transient thermal resistance of the packaged SiC MOSFET was carried out using the conventional network identification by deconvolution (NID) method. This characterization was carried out using "T3ster". The continuous time constant spectrum of the packaged SiC MOSFET from the NID method is shown in Fig. 5.10. In the time constant spectrum, the peak point represents the dominant time constant value. It can be observed that the number and position of the dominant time constant are same on the both time constant spectrums.

The converted cumulative and differential thermal structure functions of the packaged SiC MOSFET using the conventional NID method are shown as the yellow lines in Fig. 5.11. The comparison results show that both results are in good agreement. The small difference between both results in the cumulative and structure functions can be explained by the number and position of the fixed time constant.

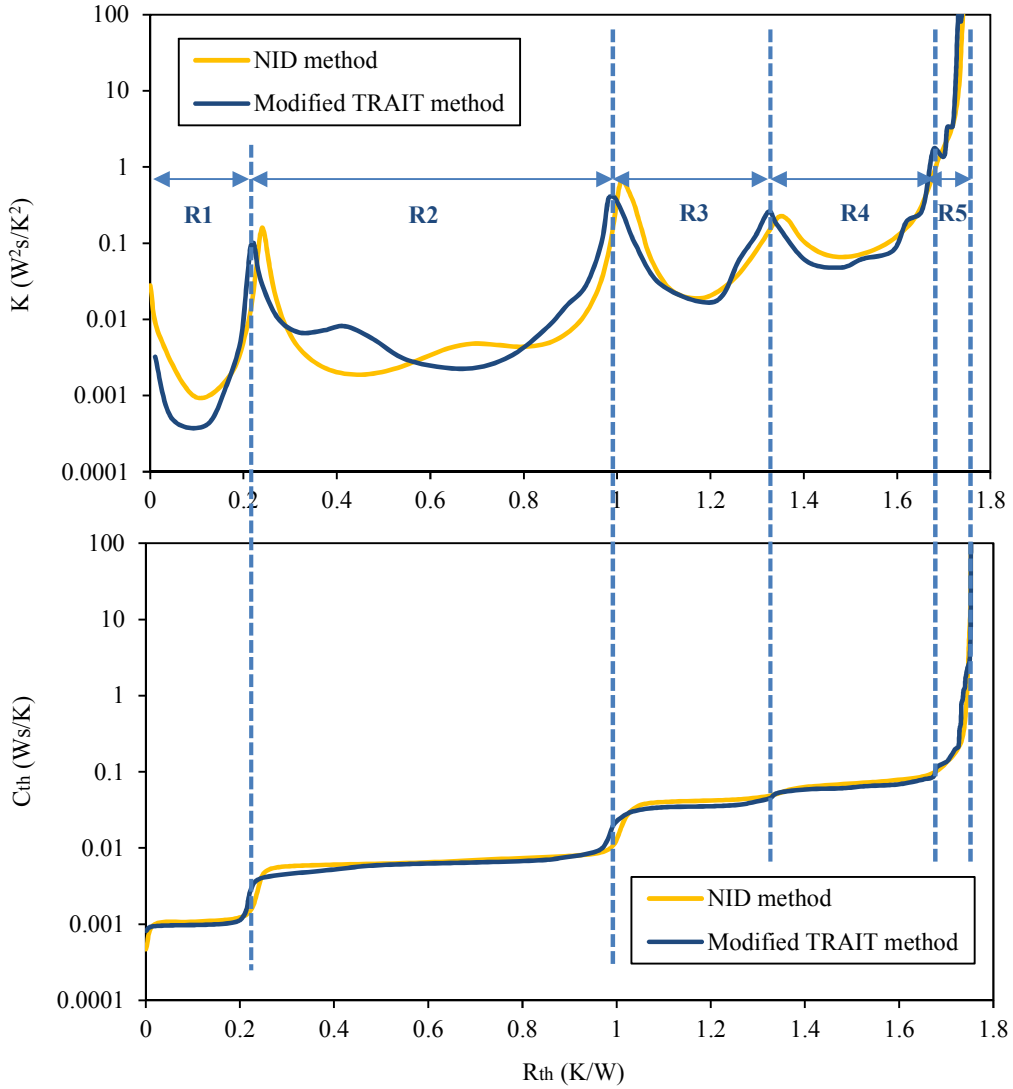


Fig. 5.11 Differential (upper) and cumulative (bottom) structure functions of the packaged SiC MOSFET.

5.3.2 Thermal model and validation

The precise descriptions of the cumulative and differential thermal structure functions are shown in chapter 4. The peak points in the differential structure function represent the interfaces between the stacked layers with the different materials, and the flat plateaus in the cumulative structure function express the thermal mass of the region for the heat conduction path in the stacked material layers. The 4 peak points and 5 flat plateaus are observed in Fig. 5.11.

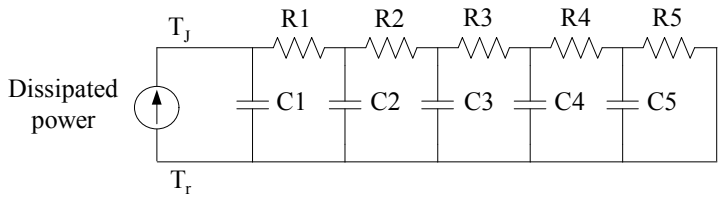


Fig. 5.12 Description of the 5th Cauer equivalent thermal circuit.

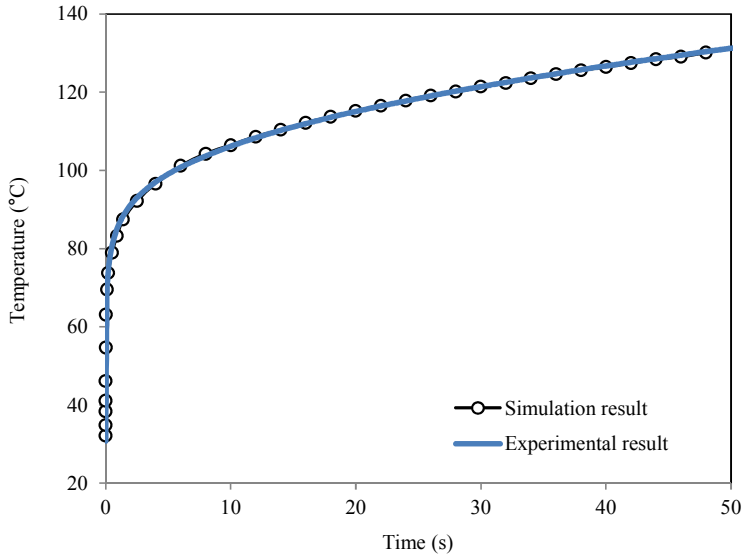


Fig. 5.13 Transient junction temperature responses of the packaged SiC MOSFETs at input power of 20W.

From these results, the stacked 5 layers of the packaged SiC MOSFET that consist of the SiC MOSFET, die attach layer (88Au/12Ge), pattern copper, Al_2O_3 substrate and bottom copper can be modelled in the 5th order Cauer equivalent circuit model as shown in Fig. 5.12. In Fig. 5.12, R_1, R_2, R_3, R_4, and R_5, and C_1, C_2, C_3, C_4, and C_5 are determined to be 0.222K/W, 0.744K/W, 0.358K/W, 0.355K/W, and 0.073K/W, and 0.0010Ws/K, 0.0051Ws/K, 0.028Ws/K, 0.030Ws/K and 0.152Ws/K, respectively.

The extracted thermal compact model of the packaged SiC MOSFET shown in Fig. 5.12 was validated with the comparison of the chip temperature responses between the experimentally

measured and numerically simulated results. After removing the high temperature resin on the SiC MOSFET device, the input power of 20W was supplied to the packaged SiC MOSFET, and the SiC MOSFET device temperature was measured with an infrared camera (NEC-Sanei TH9100MLN). In the numerical simulation of the compact thermal model of the packaged SiC MOSFET, the temperature variation of the bottom copper layer was expressed from the measured results. Fig. 5.13 shows the comparison between the measured and simulated responses of the device temperature of the SiC MOSFET, and the comparison results show good agreement within 0.7% error.

5.3.3 Thermal analysis of partial thermal resistance

In order to validate the measured transient thermal results, the numerical simulation for the transient thermal response of the packaged SiC MOSFETs was carried out using the finite difference thermal model introduced in chapter 3. As can be seen from Fig. 5.1, the center copper pattern that has the SiC MOSFET is isolated and most of the generated heat transfers through this pattern. The thermal modeling was carried out considering it. The schematically described simulation model of the packaged SiC MOSFET structure is shown in Fig. 5.14. The dimensions for the numerical thermal simulation shown in Table 5.1 corresponded with the measured real package structure.

In the thermal simulation, the dissipated power of 20W was supposed as a uniform heat flux at the top side of the SiC MOSFET device. The other boundary conditions were same with that of chapter 3.

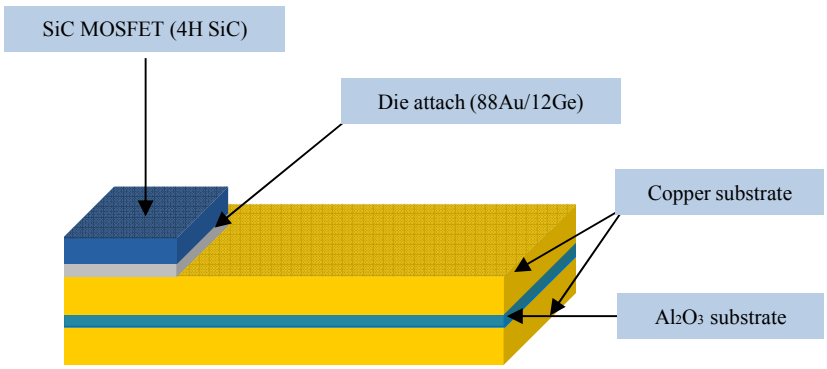


Fig. 5.14 Description of the schematic three-dimensional model for transient thermal resistance simulation of the packaged SiC MOSFET

The initial temperature condition is set as a room temperature, and the grid sizes of Δx, Δy, Δz and the time step were set as 50um and 2.5us, respectively. This simulation conditions satisfied the stability criterion introduced in chapter 3. The properties of the materials for simulation of the packaged SiC MOSFET are shown in Table 5.2 [20],[21],[22].

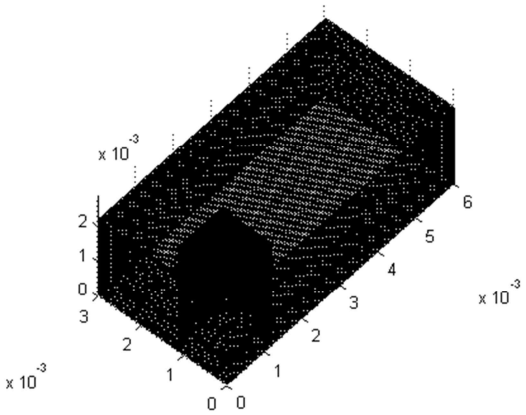
Table 5.1 Dimension of the thermal model of the packaged SiC MOSFET

Component		Surface area(mm^2)	Thickness (mm)
Chip		1.2 × 1.2	0.4
Die attach layer		1.2 × 1.2	0.2
Substrate	Copper	3 × 6	1
	Si_3N_4	3 × 6	0.25
	Copper	3 × 6	1

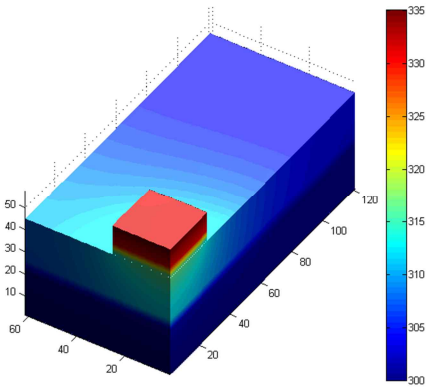
Table 5.2 Thermal properties of the materials used in the FDM numerical simulations

Component	Material	Thermal conductivity (W/m·K)	Specific heat (J/kg·K)	Density (kg/m^3)
Chip	4H SiC	$(-0.0003+1.05\times10^{-5}T)^{-1}$	$925.65+0.3772T-7.9254\times10^{-5}T^{2}$ $-3.1946\times10^{-5}T^{-2}$	3211
Die attach layer	88Au/12Ge	44.4	151.2	14670
Substrate	Copper	394	385	8930
	Al_2O_3	14	780	3600
	Copper	394	385	8930

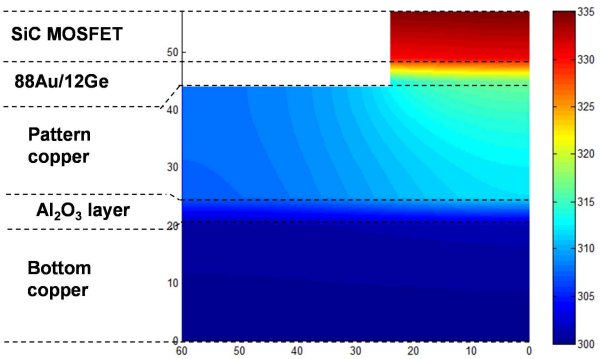
The simulation results are shown in Fig. 5.15 and 5.16. Figure 5.15(a) shows the three dimensional meshed thermal model of the packaged SiC MOSFET. The numerically simulated three-dimensional temperature distribution in the packaged SiC MOSET model under the constant dissipated power of 20W at thermal steady state is shown in Fig. 5.15(b), and the cross sectional temperature distribution of the packaged SiC MOSFET model at thermal steady state is shown Fig. 5.15(c).



(a)



(b)



(c)

Fig. 5.15 Simulated results: The three dimensional meshed thermal model of the packaged SiC MOSFET (a), Numerically simulated three dimensional temperature distribution in the packaged SiC MOSET model under the constant dissipated power of 20W at thermal steady state (b), the cross sectional temperature distribution of the packaged SiC MOSFET model at thermal steady state (c).

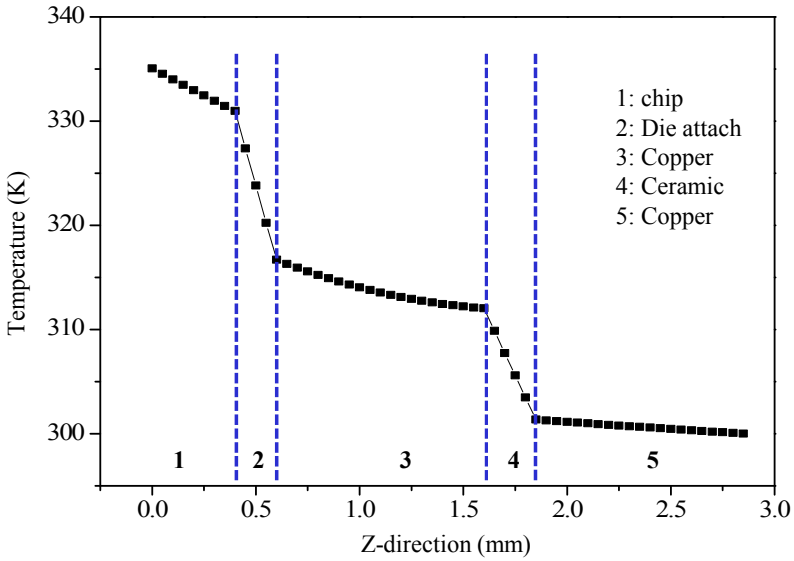


Fig. 5.16 Temperature profile from the SiC MOSFET device to the bottom copper layer.

Figure 5.16 shows the temperature profile from the SiC MOSFET device to the bottom copper layer in the center position. From the simulation results, it is observed that maximum temperature difference from the SiC MOSFET device to the bottom copper layer is 35.05°C, and drastic temperature variation is shown in the die attach layer and Al_2O_3 ceramic layer. The partial thermal resistances of the packaged SiC MOSFET were calculated from the simulated results.

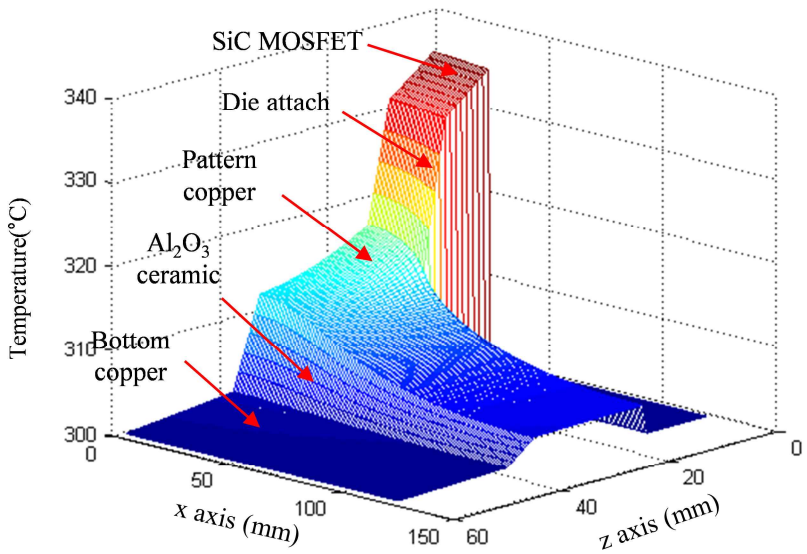


Fig. 5.17 Two-dimensional temperature profiles of the packaged SiC MOSFET

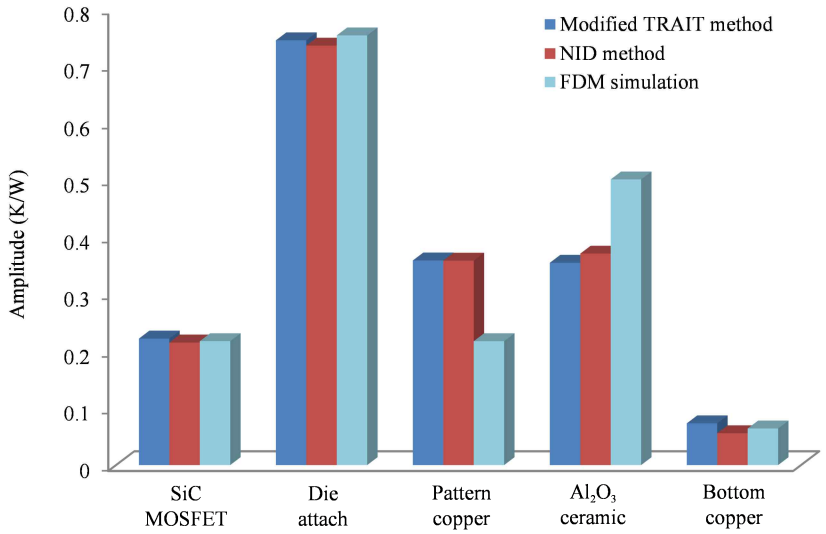


Fig. 5.18 Comparison of the partial thermal resistances of the packaged SiC MOSFET

Figure 5.17 shows the simulated two-dimensional temperature profiles of the packaged SiC MOSFET, and the calculation for the partial thermal resistance of the packaged SiC MOSFET was carried out using the introduced method in chapter 4.

Figure 5.18 shows the comparison results of the partial thermal resistances of the packaged SiC MOSFET from the modified TRAIT method, the conventional NID method, and the FDM simulation. As can be seen from Fig. 5.18, the partial thermal resistances from the modified TRAIT method shows good agreement with the results from the conventional NID method, and are similar to the results from the FDM simulation. Based on the results of the modified TRAIT method, it can be observed that the thermal resistance of the SiC MOSFET device is 0.222K/W, and it occupies about 12.6% of the total thermal resistance of the packaged SiC MOSFET. The die attach layer shows the largest value of the total thermal resistance, because the die-attach layer has relatively lower thermal conductivity compared to that of the other layers. The Al_2O_3 ceramic substrate layer has the lowest thermal conductivity in the configuration materials for the packaged SiC MOSFET and is thicker than the die attach layer, but the partial thermal resistance of the Al_2O_3 ceramic layer is lower than that of the die attach layer due to the heat diffusion in the ceramic layer. In spite of the large thickness, the copper layers have the low thermal resistance values due to the high thermal conductivity and the heat diffusion in the copper layers.

Finally, it is mentioned that the junction temperature measurement of the semiconductor device is challenging task in chapter 2, because it is difficult to measure the junction temperature of the

semiconductor device using the conventional TSEPs. The introduced method in this chapter draws the junction temperature measurement of the SiC MOSFET with the supplying constant power in the heating phase, successfully. This method can be applicable to the thermal reliability examination of the packaged SiC MOSFET such as the power cycling test through the on-line junction temperature estimation and the thermal health monitoring.

5.4 Conclusion

In this chapter, the transient thermal characteristics of the packaged SiC MOSFET have been measured and analyzed. In the transient thermal resistance measurement, a relationship of gate-source voltage and temperature of SiC MOSFETs measured using constant current pulses of 2A that have width of 200us, was employed to measure junction temperature. The transient thermal resistance of the packaged SiC MOSFETs was measured with the constant current injection of 2A in heating condition.

Using the suggested modified TRAIT method, the measured transient thermal resistance was characterized with a discrete time constant spectrum, and analyzed using thermal structure functions based on a Cauer equivalent network model. The partial thermal resistances of the packaged SiC MOSFETs were extracted and compared to the results from the conventional NID method and the thermal model based on FDM, and comparison results shows good agreement. The SiC MOSFET device, die attach layer, and substrate were accounts for 12.6%, 42.5% and 44.9% of the total thermal resistance of the packaged SiC MOSFET, respectively, and the die attach layer showed the dominant thermal resistance values of 0.744K/W.

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Chapter 6:
Conclusion

SiC power devices offer the operation ability in high temperature range. High temperature operation capability of SiC devices enables to increase the power density and reduce a size of a power electronics system. In high temperature operation of SiC devices, the thermal management is important work, because temperature margin to guarantee the electrical and mechanical reliability of the package is reduced. The temperature affects life time and failures as well as electrical characteristics of the semiconductor device. Therefore, the generated heat from the power loss of the device should be dissipated through the thermal management, appropriately. The thermal analysis means the evaluation of the thermal characteristics of the packaged devices, and the accurate thermal analysis is very useful for the thermal management of the packaged SiC devices. This dissertation focuses on the measurement and the analysis on thermal characteristics of the packaged SiC power devices, especially SBDs and MOSFETs, for high temperature applications. The major conclusions achieved in this research are summarized as follows:

Chapter 2 presented the fundamental theories on the heat transfer for the thermal analysis of the packaged SiC devices. In addition, the thermal compact models and thermal characterization methods for the packaged SiC devices are described.

In chapter 3, thermal analysis of the packaged SiC SBD was studied for high temperature operation. The thermal model was built and simulated using FDM with temperature dependence thermal properties. The transient and steady state thermal resistances from the thermal simulation were compared with the measured results, and comparison results were in good agreement. It was shown that the time constant of the transient thermal resistance was prolonged, and the steady state thermal resistance of the packaged SiC SBD increased with the temperature rise. From these results, it is recommended that the consideration of the temperature effect on thermal characteristics of the packaged SiC devices for high temperature operation, and the finite difference thermal model with temperature dependent thermal properties introduced in this chapter can be applicable to the development of the power conversion system with the SiC devices.

In chapter 4, the analysis of partial thermal resistances of the packaged SiC SBD was carried out to investigate the thermal characteristics inside the package. The partial thermal resistances of the packaged SiC SBD were extracted using the thermal structure functions from the measured transient thermal resistances between the junction and bottom copper layer under the various temperature

conditions, and compared with that of the results from numerically calculated FDM thermal simulation. It was shown that all of partial thermal resistances of the packaged SiC SBD increase with temperature, and the SiC device and the Si_3N_4 substrate comprised a significant portion of the overall thermal characteristics variation of the packaged SiC SBD. Above a room temperature, the decrease of the thermal conductivities of the package component materials with temperature rise affects the increase of the partial thermal resistances of the packaged SiC SBD. Especially, the increase of the thermal resistance means worsened heat dissipation ability of the package. For the high temperature operation of the packaged SiC SBD, thermal design is recommended considering temperature dependent thermal characteristics.

In chapter 5, the transient thermal characteristics of the packaged SiC MOSFET have been measured and analyzed. For the transient thermal resistance of the packaged SiC MOSFETs, the new measurement method was introduced. In the thermal measurement, the junction temperature of the SiC MOSFET was measured in the heating phase with supplying the constant power using the relationship between the gate-source voltage and temperature that was characterized using the high current pulses. The modified TRAIT method was suggested to characterize the transient thermal resistances of the SiC MOSFET, and the thermal characterized results were compared with that of the conventional method. The comparison results showed good agreement, and the suggested modified TRAIT method can be applicable to thermal characterization of the packaged power devices. The partial thermal resistance analysis was carried out from the modified TRAIT method, the conventional method, and FDM thermal simulation. Consequently, the partial thermal resistances from the modified TRAIT method agreed with the results from the conventional method, and were similar to the simulated results. It was shown that the die attach layer had a dominant portion in the total thermal resistance of the packaged SiC MOSFET.

In this dissertation, the thermal characterization and analysis of the packaged SiC devices were carried out, and the achieved results may contribute to the design of the package and the development of the power conversion system with the SiC devices for the high temperature operation. To apply these results, more usefully, the following tasks are expected to be solved in the future:

(1) **Electro-thermal modeling with temperature dependence thermal characteristics:** This research focuses on the thermal behavior of the packaged SiC devices. The main source of the temperature increase in the packaged SiC devices is the power loss in electrical switching and conduction operation. To analyze or estimate the thermal behavior of the packaged SiC devices, the consideration on the electro-thermal effect is required. By combining the electrical model and the thermal model, this task can be completed.

(2) **Determination of the bound thermal time constants in the modified TRAIT method:**

To increase the accuracy of the fitted results in the modified TRAIT method, it is necessary to increase the number of the time constant. However, it results in the expanded fitting time and the burdened calculation. The consideration for the appreciate determination of the number and the position of the bound time constant is required using the clues from the measured transient thermal resistance results.

(3) **Modified the FDM thermal model for the fast analysis:** Through this research, the precise thermal model was built, and validated considering the temperature dependent thermal properties. Thermal simulation with the temperature dependence thermal properties is a time consuming work. This is limitation point in applying this thermal model to other areas. For the fast calculation, the modification of the thermal model is required using the method such as the model order reduction.

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Publications

International Journals:

1. **Taehwa Kim**, Funaki Tsuyoshi, “Transient thermal analysis of packaged SiC SBDs for high temperature operation”, *IEICE Electron Express,* vol. 13, no. 6, pp. 1-6, Feb. 2016.

2. **Taehwa Kim**, Funaki Tsuyoshi, “Analysis on partial thermal resistances of packaged SiC schottky barrier diodes at elevated temperatures”, *Japanese Journal of Applied Physics*, Vol 55, 04ER18, March 2016

3. **Taehwa Kim**, Funaki Tsuyoshi, “Thermal Measurement and Analysis of Packaged SiC MOSFETs”, *Thermochimica Acta*, Vol. 633, pp. 31-36, June 2016.

International conferences:

1. **Taehwa Kim**, Funaki Tsuyoshi, “A simple thermal impedance measurement method of SiC JFET with constant current”, Extended Abstracts of the 2011 International Conference on Solid State devices and Materials (SSDM), Japan, 28-30 Sept. 2011.

2. **Taehwa Kim**, Funaki Tsuyoshi, “Characterization of Temperature Dependence of Parasitic Diodes of SiC JFETs for Transient Thermal Resistance Measurement”, Extended Abstracts of the 2012 International Conference on Solid State devices and Materials (SSDM), Japan, 25-27 Sept. 2012.

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