Doctoral Dissertation

A Study on All-Digital Phase-Locked Loop for Biomedical RF Transceivers

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Abstract

This dissertation addresses low-voltage and low-complexity design and implementation of fully integrated all-digital phase-locked loop (ADPLL) for biomedical radio frequency (RF) transceivers. It is organized into five chapters. The summary of each chapter is as follows:

Chapter 1

The background for this work and fundamentals of PLLs and the medical implant communication service (MICS) band are described.

Chapter 2

A phase noise reduction technique for low-voltage oscillator design is demonstrated. Phase noise is a key parameter for the design of RF transceivers and depends on many factors. In addition, the current biasing technique affects the phase noise. In this study, MOS current source and resistive biasing were considered as current biasing techniques. The current biasing technique, which has less noise contribution, was analyzed for low-voltage oscillators in terms of phase noise, and it was confirmed that top resistive biasing has good compatibility between phase noise and low-voltage operation. In addition, an LC oscillator with resistive biasing is presented to verify the implementation feasibility.

Chapter 3

A low-voltage design of a delta-sigma digitally controlled oscillator (DCO) for biomedical applications is demonstrated. The analog type of frequency tuning by voltage control has a limitation because of voltage scaling and linearity. Therefore, the digital approach is more suitable for low-voltage

operation because of its robustness and programmability. In this study, an 11-bit DCO controlled by digital logic blocks was designed. This architecture has fully digital control and a fractional tuning range using the delta-sigma modulator. In addition, dynamic element matching was used to reduce the capacitor mismatch. In the DCO core design, for low-voltage operation, the g_m/I_D methodology was used for optimizing the MOS size. For current biasing, top resistive biasing was applied for low voltage and low phase noise. The DCO was fabricated in a 130-nm CMOS process for a 0.7-V supply voltage. The fabricated DCO is controlled in a fully digital manner and has an active area of 0.41 mm^2. The total power consumption of the fabricated DCO is 740 μW. The fabricated chip was evaluated via a field-programmable gate array (FPGA)-based test bench. This DCO exhibited a phase noise of -115 dBc/Hz at an offset frequency of 200 kHz and a wide frequency tuning range with precise resolution of 18 kHz. Through chip evaluation, it has been demonstrated that the fabricated DCO satisfies the MICS band requirements and exhibits good performance compared with related works.

Chapter 4

A low-complexity ADPLL for biomedical RF transceivers is demonstrated. General time-to-digital converter (TDC)-based ADPLLs require highly complex systems to achieve high resolution, and thus have large power requirements. In this study, a TDC-less controller-based architecture was employed for a low-complexity ADPLL. In addition, to improve the phase acquisition performance, a phase selection scheme was applied that provided pre-settled operation of the phase of the ADPLL output signals. Through phase domain model analysis, it was confirmed that this architecture performs the PLL functionality, and its functionality was validated through the behavior model simulations. ADPLL circuits were implemented with a focus on low-voltage operation and high performance. Digital circuits were synthesized and implemented by using the standard cell library. This ADPLL was fabricated in a 130-nm CMOS process for a 0.7-V supply voltage. The fabricated ADPLL is controlled in a fully digital manner, and has an active area of 0.64 mm^2. During operation, the total power consumption of the fabricated ADPLL is 840 μW. In this study, the FPGA-based test bench was used to evaluate the chip performance. This ADPLL exhibited a settling time of 80 μs and phase noise of -114 dBc/Hz at an offset frequency of 200 kHz. In addition, it has precise channel selection based on the precise frequency resolution from the delta-sigma DCO. Through chip eval-

uation, it has been demonstrated that the fabricated ADPLL satisfies all MICS band requirements and shows better performance compared with related works. In addition, it is compatible with the various CMOS processes and supply voltages, and thus can be utilized in various fields that require high-performance, fully integrated RF transceivers with a low-voltage and advanced CMOS process.

Chapter 5

The achievements obtained in this study are summarized and this dissertation is concluded.

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Chapter 1

Introduction

1.1 Background

Biomedical radio frequency (RF) transceivers require miniaturized forms with a long battery life and low power consumption. It is usually preferable for implantable medical devices to be fully integrated on a single chip to realize easier surgery and encapsulation for high biocompatibility. The medical implant communication service (MICS) band in the frequency range of 402 MHz to 405 MHz is widely used for supporting biomedical RF transceivers because of its reasonable signal propagation characteristics in the human body and its suitability to achieve a favorable trade-off between chip size and power dissipation [1, 2]. There are many challenges associated with the implementation of the RF front-end in implantable medical devices such as pacemakers, implantable cardioverter defibrillators, and neurostimulators because their application requires extremely low power consumption, small size, minimal external components, and high reliability. The basic system requirements of RF transceivers for medical implantable devices are as follows [2]: To increase battery life, the RF transceiver current should be limited to below 6 mA during MICS band communication. The use of few external components provides higher reliability, lower cost, and smaller size. RF modules for pacemakers must be no more than approximately 3 mm $\times$ 5 mm $\times$ 10 mm. Pacemaker applications currently demand a reasonable data rate of over 20 kbps with higher data rates projected for the future. Their operating range is typically over 2 m because the MICS band is designed to improve upon the very short-range inductive link.

Figure 1.1 shows an example of the RF front-end structure for implantable biomedical applica-

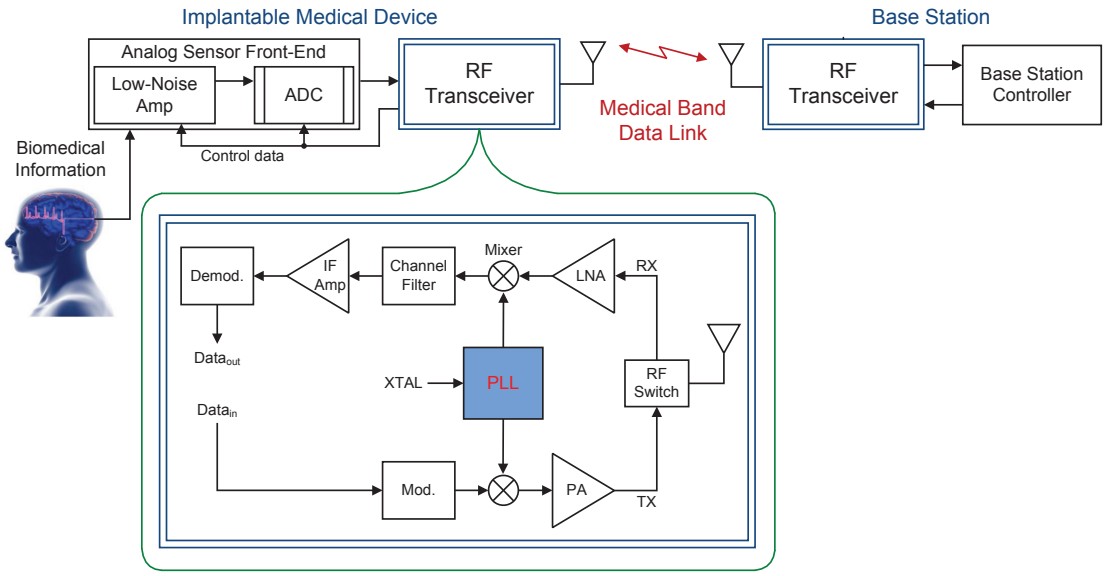

Figure 1.1: Structure of RF front-end for biomedical applications.

tions. The biomedical information in implantable devices is sensed through the analog sensor front-end and transmitted by RF transceivers. The modulated baseband signal is up-converted by the mixer using an RF frequency. The RF signal is amplified by a power amplifier (PA) to the required power level before transmission through the antenna. In the RF transceiver, the RF signal is received by the antenna and processed through a low-noise amplifier (LNA). After the LNA, the amplified RF signal is down-converted to an intermediate frequency (IF) by the mixer. The local oscillator (LO) generates the reference frequency necessary for the mixer, and the LO frequency is tuned to select the desired channel by using a frequency synthesizer. The IF signal is filtered to pass a specific frequency by using a channel selection filter and once more amplified by the IF amplifier. The channel select filter reduces interference from adjacent channels and spurious signals. Finally, the signal is demodulated in the digital domain before signal processing. The demodulated signal is used to control the analog sensor front-end.

In particular, the frequency synthesizer is one of the most important building blocks of the RF front-end because the quality of the LO signal plays a key role in the overall performance. Low power consumption and full integration are the most critical challenges for the design of implantable

RF transceivers. After rapid growth over a decade in CMOS technology scaling, digital circuits have become more preferable compared to analog circuits because of the aggressive improvements in cost, size, flexibility, and repeatability. The high level of integration demanded in wireless communication systems can be achieved with digital or digital-intensive approaches. Phase-locked loops (PLLs) are widely used in many wireless communication systems to perform frequency synthesis or clock and data recovery. The conventional PLLs are often designed using analog approaches, which usually consist of a phase and frequency detector (PFD), charge-pump, loop filter (LF), and voltage-controlled oscillator (VCO). However, analog PLLs are highly sensitive to process parameters and should be redesigned when a process is changed or the design migrates to the latest CMOS process.

Analog PLLs based on charge-pumps are still widely used, but all-digital PLLs (ADPLLs) have been attracting more attention because of their significant advantages over their analog counterparts. ADPLLs, which interface to enable peripheral circuitry to be digitally implemented, provide low-voltage operation compatibility under process and temperature variations with a shorter system turnaround time [3]. Therefore, ADPLLs provide several benefits to duty-cycled battery-operated systems, including MICS transceivers, wireless sensor nodes, and wireless telemetry devices. Realizing a low level of spurs and high-resolution is a challenge to achieve a fully integrated high-performance ADPLL architecture.

This chapter presents the fundamentals of PLLs and medical frequency band for a better understanding of the study and it also describes the motivation and structure of this dissertation. This chapter is organized as follows. Section 1.2 presents the fundamentals of PLLs and performance metrics. Section 1.3 explains the power consumption in CMOS digital circuits. Section 1.4 describes the medical frequency band and phase noise requirements for implantable biomedical RF transceivers. Section 1.5 presents the motivation of this study, and then Section 1.6 describes the structure of this dissertation.

1.2 Fundamentals of Phase-Locked Loops

1.2.1 Analog PLL

Analog PLLs have been investigated for the past several decades. As a result, various types of analog PLLs have been analyzed, and design procedures have been developed. Several references

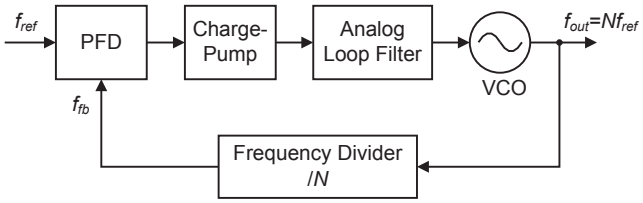

Figure 1.2: Block diagram of analog PLL.

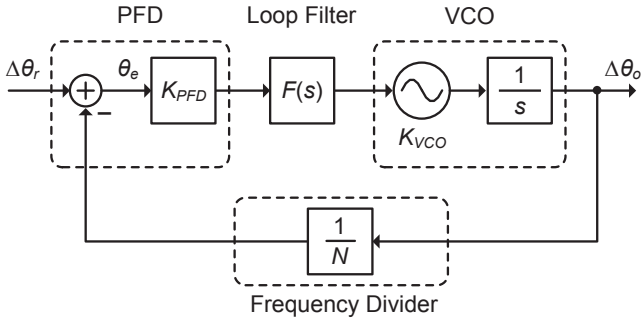

Figure 1.3: Linear s-domain model of analog PLL.

provide an analysis and design procedure for analog PLLs [4–7]. A PLL is a negative feedback system that aligns the phases of the input and output signals. In an analog PLL, as shown in Fig. 1.2, a PFD compares the phases between the reference signal frequency (f_{ref}) and feedback signal frequency (f_{fb}) from the divider and generates an output signal that includes the phase difference. The output signal of the PFD is converted to current by a charge-pump, and filtered by the analog LF and then used to control the frequency of a VCO. A divider is used in the feedback path for frequency multiplication. The negative feedback loop is needed to correct any phase misalignment resulting from internal or external noise sources. If the input and output phases match, the PLL is in a phase lock state (output frequency $f_{out} = Nf_{ref}$).

The block diagram of an analog PLL for linear s-domain phase model is shown in Fig. 1.3, where K_{PFD} is the gain of the PFD and charge-pump, $F(s)$ is the transfer function of the LF, and K_{VCO}

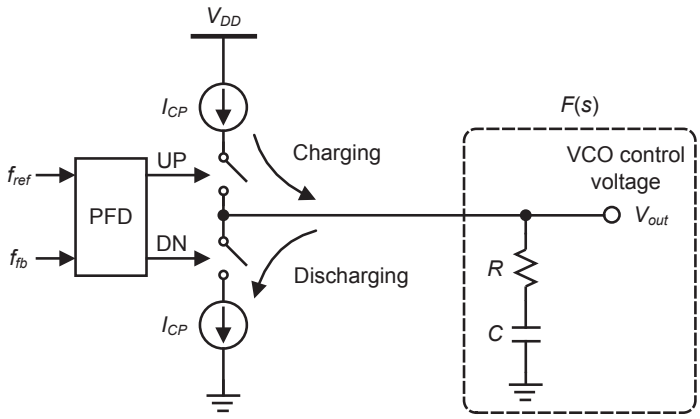

Figure 1.4: Structure of the LF based on charge-pump.

is the gain of the VCO. The open- and closed-loop transfer functions are given by

$$H_{ol}(s) = \frac{\Delta\theta_o(s)/N}{\theta_e(s)} = \frac{K_{PFD}F(s)K_{VCO}}{Ns}, \tag{1.1}$$

$$\begin{aligned} H_{cl}(s) &= \frac{\Delta\theta_o(s)}{\Delta\theta_r(s)} = \frac{NH_{ol}(s)}{1+H_{ol}(s)} \\ &= \frac{K_{PFD}F(s)K_{VCO}}{s+K_{PFD}F(s)K_{VCO}/N}. \end{aligned} \tag{1.2}$$

The phase error transfer function is expressed as

$$H_e(s) = \frac{\theta_r(s)}{\Delta\theta_r(s)} = 1 - \frac{H_{cl}(s)}{N}. \tag{1.3}$$

The PLL order is defined by the number of poles of the open-loop transfer function and equals the loop filter order plus one. The closed-loop stability can be obtained by analyzing the open-loop frequency response $H_{ol}(s)$. For this purpose, the open-loop gain information for amplitude and phase is needed.

Simple passive LFs can be used to implement a second-order PLL with zero static phase error. Figure 1.4 shows the second-order passive LF structure based on a charge-pump. In this case, $K_{PFD} = I_{cp}/2\pi$. The transfer function of the second-order passive LF is given by

$$F(s) = \frac{1+sRC}{sC}. \tag{1.4}$$

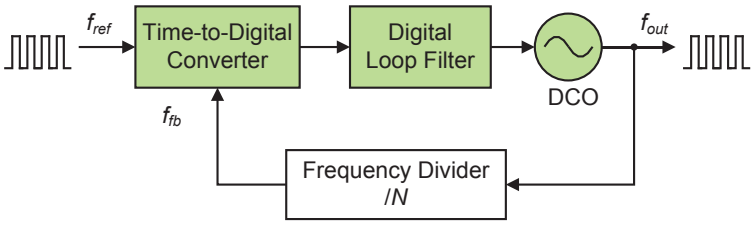

Figure 1.5: Block diagram of digital PLL.

From, Eq. (1.1), the open-loop transfer function of a second-order PLL with this loop filter is expressed as:

$$H_{ol}(s) = \frac{K_{PFD}K_{VCO}}{Ns} \cdot \frac{1+sRC}{sC}. \tag{1.5}$$

By using the final value theorem, the steady state phase error of this second-order PLL is zero when a step phase input is applied.

The closed-loop transfer function of this second-order PLL is:

$$\begin{aligned} H_{cl}(s) &= \frac{\frac{K_{PFD}K_{VCO}}{C}(1+sRC)}{s^2 + \frac{K_{PFD}K_{VCO}R}{N}s + \frac{K_{PFD}K_{VCO}}{NC}} \\ &= \frac{N\omega_n^2\,(1+2\zeta s/\omega_n)}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \end{aligned} \tag{1.6}$$

where

$$\begin{aligned} \omega_n &= \sqrt{\frac{K_{PFD}K_{VCO}}{NC}}, \\ \zeta &= \frac{\omega_n}{2}RC. \end{aligned} \tag{1.7}$$

This type is a popular structure for LF design because a second-order PLL may converge to zero phase error even with a frequency offset. It requires a zero in the loop filter for stability. This zero can cause extra peaking in the frequency response. Although it is an analog type PLLs, the PFD and divider can be implemented by using digital circuits.

1.2.2 All-Digital PLL

In the deep-submicron CMOS process, RF transceivers are adapted in order to reduce the cost, power consumption, and die area of the system. With the scaling of MOS device to submicron fea-

ture size, the supply voltage will also decrease. Analog PLLs are more sensitive to noise and process variations in low supply voltage. Although analog PLLs need to be redesigned as the process is changed, digital PLLs can be more easily changed for a new process. The power consumption of a digital circuit depends on the supply voltage. In voltage scaling, digital-based circuits can more efficiently reduce power consumption. Therefore, digital circuits are less susceptible to process and voltage variations. ADPLL is realized mostly from digital-intensive circuits. The components and functionality are similar to the analog PLL, but the implementation consists of digital components. ADPLLs consist of a time-to-digital converter (TDC), a digital LF, and a digitally controlled oscillator (DCO). A general block diagram of the ADPLL is shown in Fig. 1.5. The TDC measures the time difference between the reference and feedback clocks and converts it to a digital code. This digital code is filtered by the digital LF and then is used to control the DCO frequency. Recently, several digital PLLs for different applications have been reported [8–10]. They demonstrate the ability of a digital implementation by outperforming analog PLLs. The ADPLL has better portability, which can be used in fully integrated applications, and is independent of process variations. It also minimizes the design cost and time.

1.2.3 Performance Metrics

Phase Noise

Practical oscillators consist of both passive and active components, which cause noise in the system. This noise takes various forms, including shot noise, flicker noise, and thermal noise [11]. With regard to the frequency domain, the existence of phase noise in oscillators causes the output signals to contain significant energy at other frequencies. Considering the output signal of an ideal sinusoidal oscillator, shown in Fig. 1.6(a), operating at a given frequency f_0, the spectrum shape is characterized as an impulse. However, in a practical oscillator, the spectrum has power distributed around the desired oscillation frequency in addition to power located at harmonic frequencies. This undesired power distribution around the oscillation frequency is phase noise, and is depicted in Fig. 1.6(b).

Phase noise is expressed as the ratio of power at a specific offset frequency (Δf) from the carrier to the power at the center frequency. This power is measured in a unit bandwidth at a certain Δf.

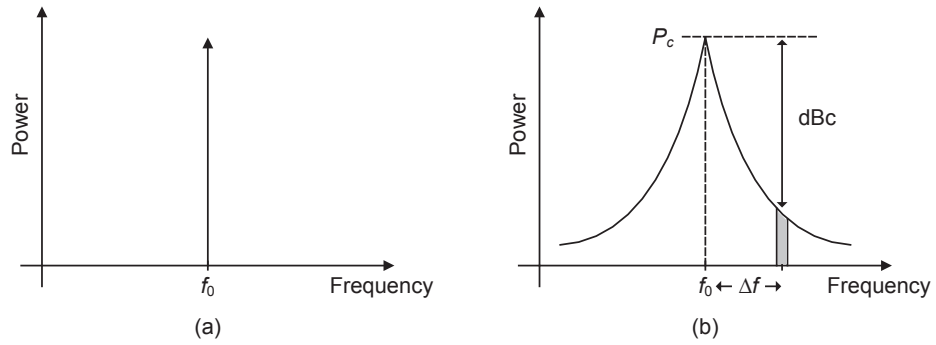

Figure 1.6: Frequency spectrum of (a) an ideal and (b) a practical oscillators.

The oscillator phase noise ($L\{\Delta f\}$) is mathematically defined by

$$L\{\Delta f\} = \frac{P_{sideband}(f_0 + \Delta f, 1\text{Hz})}{P_c}, \tag{1.8}$$

where P_c is the power in the fundamental carrier f_0 and $P_{sideband}$ is the power distributed around the carrier. From this simple definition, it may be confirmed that phase noise may be improved by increasing P_c at the cost of increased power dissipation.

The Leeson's semi-empirical phase noise model proposed in [12] is based on a linear time-invariant (LTI) assumption for the LC-tank oscillator. It quantitatively predicts the following behavior:

$$L\{\Delta f\} = \frac{2Fk_BT}{P_c}\left[1 + \left(\frac{f_0}{2Q\Delta f}\right)^2\right]\left(1 + \frac{\Delta f_{1/f^3}}{|\Delta f|}\right), \tag{1.9}$$

where F is a fitting parameter describing the noise of the circuit, k_B is the Boltzmann constant, T is the absolute temperature, and $\Delta f_{1/f^3}$ is the corner frequency between $1/f^3$ and $1/f^2$ regions. It is important that the empirical fitting parameter must be determined from measurements. Because Leeson's phase noise model is an LTI system, properties of the oscillator such as signal power, resonator Q factor, and noise factor, which do not change with time, are used to obtain an estimation of phase noise. In summary, the dominating phase noise in the $1/f^2$ region is improved by increasing the resonator Q factor or P_c. The main bottleneck of Leeson's model is the lack of knowledge about the fitting parameter F. The fitting parameter related to the noise remains as an unspecified value and strongly depends on the oscillator topology.

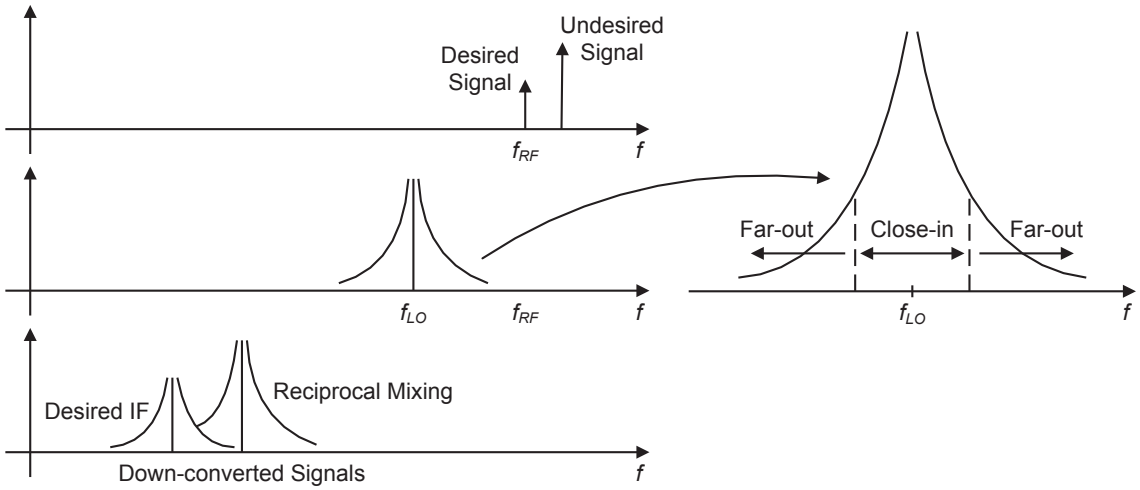

Figure 1.7: Influence of LO phase noise on RF receiver reciprocal mixing.

Phase noise degrades different aspects of the system depending on its applications. In RF transceivers, the LO phase noise degrades the received signal-to-noise ratio (SNR) by a reciprocal mixing. This effect is illustrated in Fig. 1.7. In addition to the direct superposition of the LO phase noise on the down-converted channel, the presence of a nearby interferer further degrades the SNR of the desired signal. Therefore, although close-in phase noise at offsets within the channel bandwidth is obviously important, far-out phase noise can also have a significant impact on system performance. In some applications, the LO phase noise specifications are the most difficult to meet at offsets far away from the carrier. Although close-in phase noise can be reduced to some extent by increasing the PLL loop bandwidth, far-out phase noise is typically dominated by the oscillator. Hence, the design of low-phase-noise oscillators is important for high-performance RF transceivers.

Settling Time

Settling time is the time interval to move from one frequency to another and settle on the new frequency. It depends on the frequency step and the PLL loop dynamics characteristics. The settling time is improved by using a wide LF bandwidth. If too wide an LF is used, it may cause degradation of phase noise and reference spurs because there is a trade-off between fast settling time and good spectrum performance. Because lock time often is a bottleneck in PLL implementations, various ap-

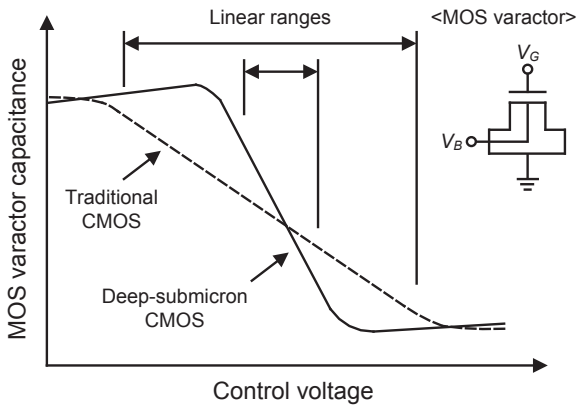

Figure 1.8: MOS varactor characteristic for both a traditional and a deep-submicron CMOS process.

proaches exist to improve the settling time. One method is to dynamically adapt the PLL bandwidth. Using a wide bandwidth during PLL lock results in a fast settling time. Once the PLL is locked to the correct frequency, a narrow bandwidth is used to provide good phase noise and spur performance.

Spurious Level

The undesired frequency components generated in the operating band of a device at some discrete frequency points are called spurs. Their power levels are described in a way similar to the phase noise power levels, namely by comparison with carrier power. Reference spurious signals are generated in a PLL system by a charge pump or amplifier leakage current. The spur generally can be reduced by using a high reference frequency and minimizing the charge-pump current mismatch.

Frequency Tuning Range

The operating frequency range is generally limited by the tuning range of the oscillators. Achieving high performance over a wide tuning range is challenging because the oscillator tuning range is always designed to have some margin in order to allow correct operation with noise and process variations. Frequency tuning of a low-voltage and deep-submicron CMOS oscillator is quite a difficult task because of its high non-linear characteristics and lack of low-voltage headroom. The oscillation frequency may be changed by using a varactor in the resonator. The capacitance of the varactor is

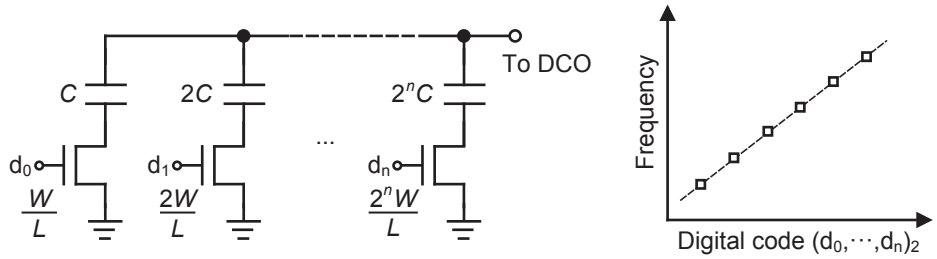

Figure 1.9: Discrete frequency tuning technique.

changed by controlling an external DC voltage that is applied to the varactor, and thus the oscillation frequency can be selected by changing the natural frequency of oscillation in the resonator. Figure 1.8 shows normalized curves of a MOS varactor capacitance versus control voltage (C-V) for both a traditional and a deep-submicron CMOS process. Obviously, a large linear range of the C-V curve can be applied for a precise and wide operational control of frequency. With a deep-submicron process, the linear range is quite narrow. This makes the operating point shifts because of its undesirable high gain. One technique is to use digitally controlled fixed capacitors to cover a larger frequency range, as conceptually shown in Fig. 1.9. The frequency range has linear trends, and the performance depends on the tuning capacitors and switch design. The digital-approach frequency tuning is more suitable for a low-voltage and deep-submicron CMOS process because of its inherent advantages of digital control.

1.3 Power Consumption in CMOS Digital Circuits

The power consumption of a CMOS circuit usually can be divided into three different components: dynamic ($P_{dynamic}$), short-circuit ($P_{short-circuit}$), and leakage ($P_{leakage}$) power consumption. Switching power, which includes both dynamic power and short-circuit power, is consumed when signals through CMOS digital circuits change their logic state. Leakage power is primarily due to the subthreshold currents in a CMOS transistor. Therefore, total power consumption is given by

$$P_{total} = P_{dynamic} + P_{short-circuit} + P_{leakage}. \tag{1.10}$$

Dynamic Power

The dynamic power consumption in CMOS digital circuits is due to the charging and discharging of load capacitance. The dynamic power consumption can be calculated by [13]

$$P_{dynamic} = \alpha C_L V_{DD}^2 f_{CLK}, \tag{1.11}$$

where α is the switching activity, C_L is the load capacitance, V_{DD} is the supply voltage, and f_{CLK} is the operating clock frequency. In CMOS digital circuits with high switching activity, the dynamic power accounts for most of the power used by CMOS circuits. Therefore, the dynamic power is dominant to the total power consumption. A simple way to reduce the dynamic power is by decreasing V_{DD}, because reducing V_{DD} causes a quadratic reduction.

Short-Circuit Power

Short-circuit power consumption occurs when a digital circuit switches [14]. During the transition, there is a short time when both the NMOS and PMOS transistor conduct. It is equivalent to shorting the supply and ground rails for a brief period time. Thus, this current flow consumes power. The short-circuit power consumption is simply given by

$$P_{short-circuit} = I_{sc} V_{DD}, \tag{1.12}$$

where I_{sc} is the short circuit current. The short-circuit power is proportional to the gate rise time and fall time. Therefore, reducing the input transition times will decrease the short-circuit current component.

Leakage Current Power

In deep-submicron CMOS, even though a transistor is in a stable logic state, it continues to leak small amounts of power, primarily because of subthreshold currents. The subthreshold leakage is the current between the drain and source of a transistor operating in the weak-inversion region [15]. The leakage current power consumption is simply given by

$$P_{leakage} = I_{leakage} V_{DD}, \tag{1.13}$$

where $I_{leakage}$ is the leakage current. Along with reducing V_{DD}, threshold voltage also must be scaled down, which results in an exponential increase in leakage power. As a result, leakage power has become a significant contributor in the total chip power dissipation according to the voltage and MOS scaling.

1.4 Medical Frequency Band

For implantable medical devices, full integration on a single chip is usually preferred to realize easier surgery and encapsulation for better biocompatibility. Many biomedical telemetry systems have used very short-range magnetic (inductive) links [16,17]. These systems require close coupling between the external unit and implanted device and can be easily affected by electromagnetic interference, which presents a risk to patient safety and medical effectiveness due to the increasing usage of electromagnetic energy radiating devices such as cell phones and security systems. To address these limitations, the Federal Communications Commission (FCC) allocated the MICS band in the frequency range of 402 MHz to 405 MHz with 10 channels in 1999 [1], as shown in Fig. 1.10. In the MICS band, each channel bandwidth is 300 kHz and located very close. In the transmit path, the phase noise will make the transmitter emit signals outside the allowed frequency band. So, the analysis of adjacent channel power ratio (ACPR) is important. ACPR covers all signal emission in adjacent bands, including phase noise and spurious tones. This band's signals have reasonable propagation characteristics in the human body and are well suited for achieving a good trade-off between size and power [2]. Furthermore, the use of the MICS band does not pose a significant risk of interference to other radio frequencies within or close to this band [1].

Extending battery lifetime without recharging is a challenge. Medical implantable devices must be optimized to consume as little energy as possible while achieving acceptable levels of performance. With the advance of CMOS technology, this frequency band promises high-level integration compared to inductive link designs, which results in miniaturization and low power consumption. In addition, penetration loss at these frequencies is relatively insignificant and is therefore suitable for implantable medical device applications.

Figure 1.11 shows the concept of the effect of phase noise and interference on an RF receiver reciprocal mixing [18]. Although the RF signal with power P_{sig} (dBm) is down-converted to an IF

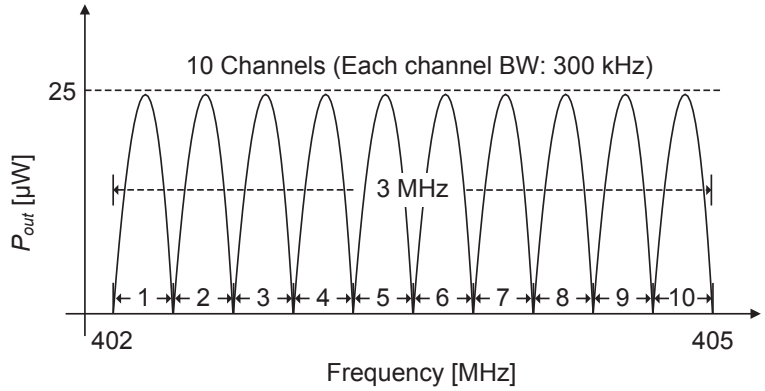

Figure 1.10: Frequency spectrum of MICS band.

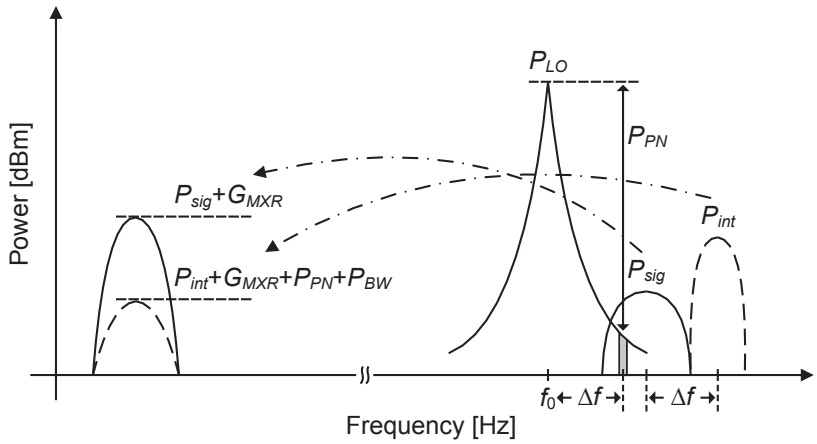

Figure 1.11: The effect of phase noise and interference on RF receiver reciprocal mixing.

by the LO with power P_{LO} (dBm), interference with power P_{int} (dBm) from adjacent channels is also down-converted to the same IF with the phase noise that has power P_{PN} (dBc/Hz). G_{MXR} (dB) is the conversion gain of switching mixing for sufficient large P_{LO} [19]. Because the phase noise is a random process, the effective bandwidth with power P_{BW} (dB) is considered in the total noise power calculation. The minimum SNR (dB) requirement that the IF signal should satisfy is given by

$$SNR = (P_{sig} + G_{MXR}) - (P_{int} + G_{MXR} + P_{PN} + P_{BW}) > SNR_{min}. \tag{1.14}$$

After re-arrangement focusing on the phase noise,

$$P_{PN} < P_{sig} - P_{int} - P_{BW} - SNR_{min}. \tag{1.15}$$

The phase noise requirement for an MICS-band oscillator that has been locked by PLL is relatively relaxed. For MICS-band receivers, because of the limited distance and upper bound of the equivalent isotropically radiated power, the dynamic range ($|(P_{sig} - P_{int})|$) is not too high and is determined by a path loss of approximately 30 dB at 2 m [1]. For this reason, the down-conversion of the phase noise in the adjacent channel is not a serious problem. The MICS band has 10 channels, and each channel occupies up to 300 kHz bandwidth [20]. If frequency shift keying (FSK) modulation is used, and the deviation of the two FSK tones is 50 kHz, then the closest adjacent-channel interferer is at 200 kHz away from the carrier. Assuming a SNR of 15 dB is required by the FSK demodulation [21] to obtain a bit error rate of 10^{-3}, the required phase noise at 200 kHz offset can be estimated by [22]

$$\begin{aligned} L\{200\text{ kHz}\} &= -15\text{ dB} - 30\text{ dB} - 10\log_{10}(300\text{ kHz}) \\ &= -100\text{ dBc/Hz}. \end{aligned} \tag{1.16}$$

The local oscillator signal should achieve a phase noise under -100 dBc/Hz at an offset frequency of 200 kHz while suffering from adjacent-channel interference. This value is the target phase noise requirement in the oscillator design.

1.5 Motivation

In ADPLLs, TDCs have been replacing conventional PFDs and charge-pumps [23]. The resolution of the TDC is critical to the performance of the ADPLL because low resolution causes in-band phase noise. TDCs require advanced CMOS technology and additional system complexity to achieve high-resolution and thereby have large power consumption. Additionally, TDCs are sensitive to process, voltage, and temperature variation. Such high sensitivity can cause poor linearity and non-uniform phase detector gain, resulting in widespread spur generation. Hence, a TDC-less controller-based ADPLL [24, 25] for high performance and low complexity is considered. The digital implementation of a controller reduces the silicon die area and eliminates external loop filter components. RF oscillators, which traditionally use an analog approach for frequency tuning, now have digital interfaces to allow the peripheral circuitry to be implemented in a digital manner. A DCO, which was

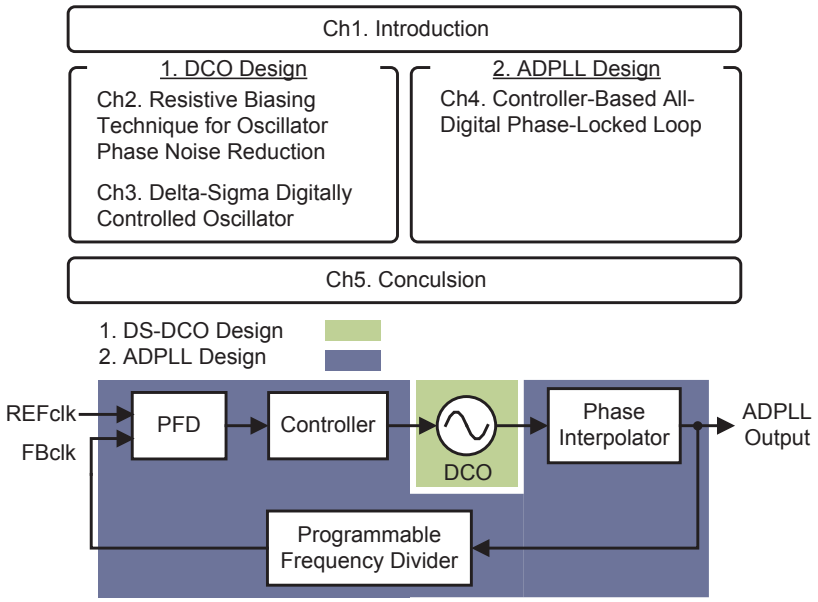

Figure 1.12: Structure of this dissertation.

proposed for wireless applications in [26], generates a signal whose frequency can be controlled with digital words. The DCO enables efficient implementation of the direct frequency modulation in an ADPLL. In the design of DCO, the low level of spurs and high resolution are challenges for implementations of the ADPLL. Low phase noise and precise frequency resolution are desirable for the high-performance fully integrated ADPLL architecture for wireless communications.

The goal of this study is to address and demonstrate a low-voltage and low-complexity fully integrated ADPLL for biomedical RF transceivers. ADPLLs are essential building blocks for biomedical RF transceivers, which require relatively high compatibility between complexity and performance. This causes difficulties in implementing low-voltage and low-complexity RF front-end chips. In addition, the conventional circuit topologies of fully integrated ADPLLs are quite complex, which implies that different topologies suitable for RF transceivers are required. Therefore, low-voltage and low-complexity ADPLLs can contribute to the implementation of biomedical RF transceivers.

1.6 Outline of This Dissertation

This dissertation describes a low-voltage and low-complexity fully integrated ADPLL for supporting biomedical RF transceivers. The structure of this dissertation is depicted in Fig. 1.12, and the dissertation is organized as follows:

Chapter 2 presents a phase noise reduction technique with top resistive biasing for low-voltage oscillator design. Phase noise analysis for current biasing methods is presented and an LC oscillator circuit design is described.

Chapter 3 presents the low-voltage design of a delta-sigma DCO, which is controlled in a fully digital manner. The circuit implementations for low-voltage operation are described and the chip evaluation results are presented.

Chapter 4 presents a low-complexity ADPLL for biomedical RF transceivers. The functionality of the considered ADPLL is analyzed and circuit implementations for low-voltage operation are described. The chip evaluation results are also presented.

Chapter 5 concludes the dissertation.

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Chapter 2

Resistive Biasing Technique for Oscillator Phase Noise Reduction

2.1 Introduction

One of the major challenges in the design of RF front-end modules is the implementation of fully integrated low-power, low-phase noise voltage-controlled oscillators (VCOs). CMOS devices operating in the weak-inversion region have the advantage of a higher transconductance to power dissipation ratio with satisfactory noise performance in comparison with the strong inversion region. Therefore, the subthreshold-biased VCO achieves low-power and low-phase-noise characteristics. The circuits designed with MOS transistors biased in the subthreshold region operate with reduced voltage headroom, resulting in lower supply voltage. However, the phase noise performance is degraded because of the small amplitude at low supply voltages, and it is recognized that the active current source for biasing purposes introduces noise performance degradation [1, 2]. There have been many efforts to improve the phase noise performance by improving the quality (Q) factor of the resonator or reducing the noise power [3, 4]. This study focuses on the current biasing technique in the weak-inversion region for better performance. The subthreshold-biased LC-VCO and resistive biasing technique are employed to achieve low-voltage operation and low phase noise.

This chapter presents the analysis of phase noise performance through various biasing techniques, and a low phase noise LC-VCO is designed using resistive biasing instead of the active current source scheme. Top resistive biasing is employed for low phase noise and low-voltage operation because of its inherent advantage of low effective noise and large voltage swing.

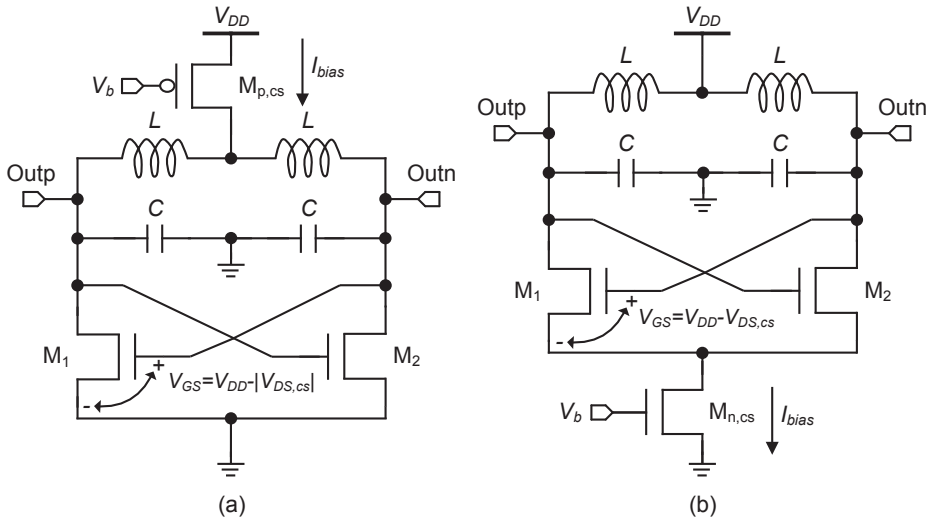

Figure 2.1: Active current biasing technique by (a) PMOS current source and (b) NMOS current source.

This chapter is organized as follows. Section 2.2 presents the resistive current biasing technique for low-voltage operation. Section 2.3 describes the analytical phase noise analysis for current biasing techniques. Section 2.4 presents the actual circuit design based on this analysis and describes its simulation results, and then Section 2.5 concludes the chapter.

2.2 Resistive Biasing Technique

Transistor biasing is the process of setting a transistor's DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor. Figures 2.1 and 2.2 show the biasing techniques in oscillator design. In this study, MOS current source and resistive biasing techniques are considered to provide the current of the core MOS devices. The active current source technique is widely used to supply current in integrated circuit technology. A current mirror is a circuit block that functions to produce a copy of the current in one active device by replicating the current in a second active device. Thus, it needs a reference circuit block to supply the constant current. In typical oscillators operating at high current levels with moderate-to-high resonator Q factors, the current source contribution dominates other sources of phase noise.

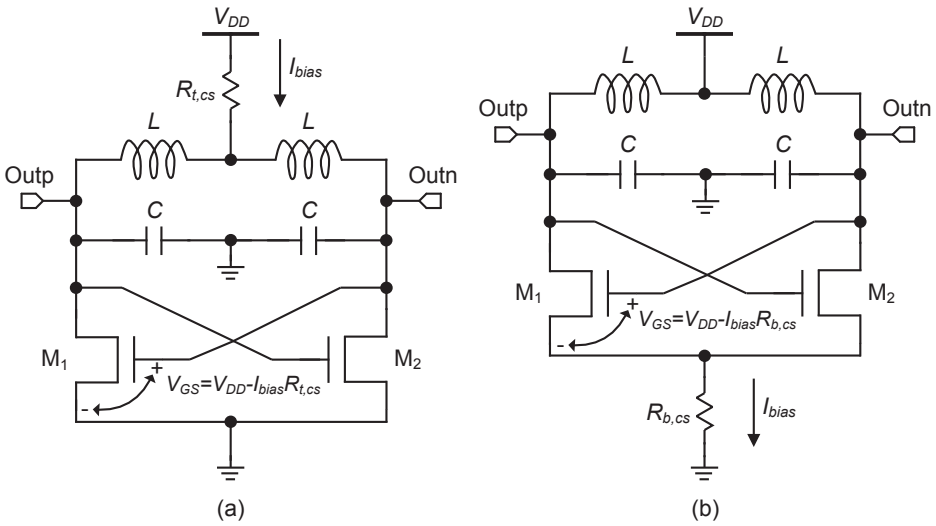

Figure 2.2: Passive current biasing technique by (a) top resistive biasing and (b) bottom resistive biasing.

In addition, it reduces voltage headroom, which is not suitable for low-voltage applications. There have been many efforts to improve phase noise performance by reducing the noise contribution from the current source [2, 5]. Resistive biasing is another approach to improve the phase noise and directly provides the current without extra reference circuits. The resistive biasing is simple and has a smaller noise contribution than active current source because of its low thermal noise. In this study, the mathematical analysis of phase noise according to biasing techniques is presented.

2.3 Phase Noise Analysis of Biasing Techniques

There are many ways to realize integrated LC-VCOs. For the analysis of the current biasing techniques, an NMOS cross-coupled differential pair is used for the core oscillator design, which has the advantages of common-mode noise suppression and low-voltage operation. The different cases of current biasing techniques in differential LC-VCO are shown in Figs. 2.1 and 2.2. In general, the active biasing with MOS current sources, $M_{p,cs}$ and $M_{n,cs}$ (Fig. 2.1), and passive biasing with resistors, $R_{t,cs}$ and $R_{b,cs}$ (Fig. 2.2), are used to supply the bias current.

The lack of completeness concerning the noise factor in Leeson's model still remains as the chal-

lenge of phase noise in oscillator design. A more accurate linear time-variant (LTV) model was developed by Hajimiri and Lee [6, 7]. The essential and key idea in this LTV approach is the introduction of a sensitivity function called the impulse sensitive function (ISF with symbol Γ). In [6], it was shown that the impact of stationary and cyclostationary noise sources on phase noise conversion varies across the oscillation period, and the ISF quantitatively exhibits these effects. ISF is a dimensionless, frequency- and amplitude-independent periodic function, and encodes information about the sensitivity of the oscillator to an injected impulse [6]. The detailed derivation of LTV phase noise is described in [6,7], and the phase noise in harmonic oscillators based on the LTV analysis approach is expressed as [6–8]

$$L\{\Delta f\} = \frac{1}{8\pi^2 \Delta f^2 C_{tot}^2 A_T^2} \cdot \sum_i N_{L,i}, \tag{2.1}$$

where Δf is the offset requency, $C_{tot}(= C/2)$ is the total capacitance of LC resonator, A_T is the oscillation amplitude across the LC resonator, and the effective noise power $N_{L,i}$ is given by [8]

$$N_{L,i} = \frac{\overline{|i_{n,i}(\Delta f)|^2}}{\Delta f} \cdot \frac{1}{T_p} \int_0^{T_p} \Gamma_i^2(t) dt, \tag{2.2}$$

where T_p is the oscillation time period, $\overline{|i_{n,i}(\Delta f)|^2}/\Delta f$ is the noise current power spectral density per unit frequency generated by the i-th device, and $\Gamma_i(t)$ is the ISF representing the time-varying sensitivity of the oscillator phase to perturbations. ISF describes how much phase shift occurs from applying a unit impulse at any point in time. The phase noise depends on the reciprocal of the oscillation amplitude. On the basis of a simple analytical model similar to [9], the oscillation amplitude A_T is given by

$$A_T \propto I_{bias} R_p, \tag{2.3}$$

where I_{bias} is the bias current and R_p is the equivalent parallel resistance of the LC resonator. Among the components of an LC resonator, the Q factor of the inductor is usually more dominant than that of the capacitor because the inductor has a lower Q factor than the capacitor. Thus, R_p can be calculated as

$$R_p \approx 2\pi f_0 L_{tot} Q_L, \tag{2.4}$$

where f_0 is the oscillation frequency, $L_{tot}(= 2L)$ is the total inductance, and Q_L is the Q factor of inductor. This is the reason that the usual design practices try to maximize both the available

oscillation amplitude and the Q factor in order to reduce the phase noise. In addition, the effective noise power proportionally links the phase noise performance and has relevance to the noise source, which depends on the biasing techniques.

2.3.1 Effective Noise

Lower effective noise improves phase noise performance, and it depends on the noise source. The total effective noise of LC-VCO using MOS current source (Fig. 2.1), $N_{L,CS}$, is expressed as [10]

$$\begin{aligned} N_{L,CS} &= N_{L,tank} + N_{L,gm} + N_{L,gmcs} \\ &= \frac{2k_BT}{R_p}\left(1+\gamma+\alpha_{n/p}\gamma g_{mn/p,cs}R_p\right), \end{aligned} \tag{2.5}$$

where $N_{L,tank}$, $N_{L,gm}$, and $N_{L,gmcs}$ are the effective noise of LC resonator, differential-pair MOS devices, and n/p-channel MOS current source, respectively. k_B is the Boltzmann's constant, T is the absolute temperature, $g_{mn/p,cs}$ is the transconductance of MOS current source, γ is the channel noise coefficient of MOS device, and $\alpha_{n/p}$ is a parameter related to the transition time interval between the switching action of differential-pair devices M_1 and M_2 in the case of n/p-channel MOS current source. In this work, $\alpha_{n/p}$ is different from the $4/9$ value in the literature [5] because of the weak-inversion region operation. The value of $\alpha_{n/p}$ is determined from the circuit simulation results of phase noise. From the circuit simulation results, α_n and α_p are obtained as 0.5 and 0.2, respectively. This equation describes three noise contributions. The first and second terms describe the noise contribution from the LC resonator loss and the differential-pair MOS devices, respectively. The third term describes the noise from the MOS current source. In typical LC-VCOs operating at high current levels with a moderate-to-high Q factor, the MOS current source noise dominates phase noise over other noise sources [1]. There have been many efforts to reduce the phase noise by using a high-value inductor in series with the current source in order to isolate the source node of differential-pair devices and the current source, thus obtaining a composite current generator [5, 11]. In such an approach, however, the noise of the tail transistor still affects at the source node of differential-pair MOS devices in spite of wasting the area for the added inductor.

To reduce the noise from the MOS current source, a low-value resistor is employed as a practical biasing technique for LC-VCOs. In the case of using a resistor as a current source, the thermal noise caused by the MOS current source can be replaced by the thermal noise of the bias-feeding resistor.

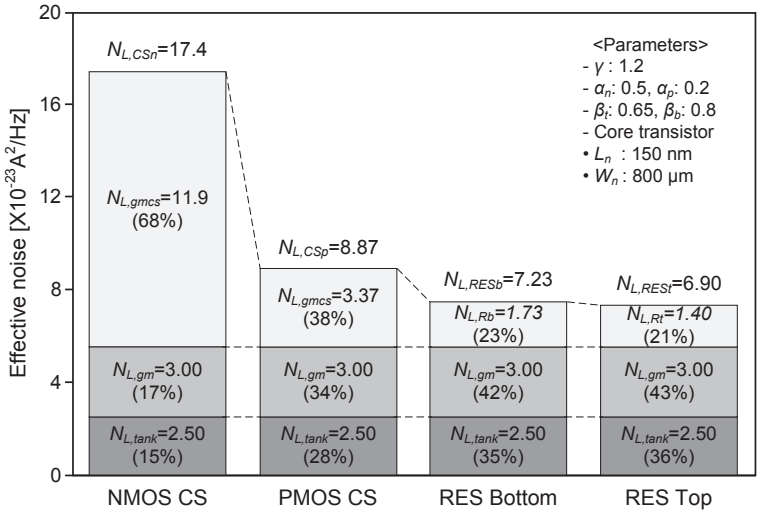

Figure 2.3: Effective noise contribution in current sources ("NMOS CS" and "PMOS CS") and resistive ("RES Top" and "RES Bottom") biasing techniques.

Here, considering the differential-pair MOS switching action in the resistive biasing case, the total effective noise for LC-VCO using resistive biasing (Fig. 2.2), $N_{L,RES}$, can be expressed as

$$\begin{aligned} N_{L,RES} &= N_{L,tank} + N_{L,gm} + N_{L,R_{t/b,cs}} \\ &= \frac{2k_BT}{R_p}\left(1+\gamma+\beta_{t/b}\frac{R_p}{R_{t/b,cs}}\right), \end{aligned} \tag{2.6}$$

where $N_{L,R_{t/b,cs}}$ is the effective noise of bias feeding resistor, $R_{t/b,cs}$ is the bias feeding resistance for each biasing position (top and bottom), and $\beta_{t/b}$ is a parameter related to the transition time interval between the switching action of differential-pair devices M_1 and M_2 in the case of resistive biasing. The value of $\beta_{t/b}$ is determined from the circuit simulation results of phase noise. From the circuit simulation results, β_t and β_b are obtained as 0.65 and 0.8, respectively. Similar to the MOS current source case, in the above equation the first and second terms of noise contribution are from the LC resonator loss and the differential-pair MOS devices, respectively. The third term indicates the contribution from the thermal noise of the bias-feeding resistor.

Figure 2.3 represents the simulated effective noise contribution for different biasing techniques. Typically, an NMOS transistor has a larger drain noise current than a PMOS transistor under the

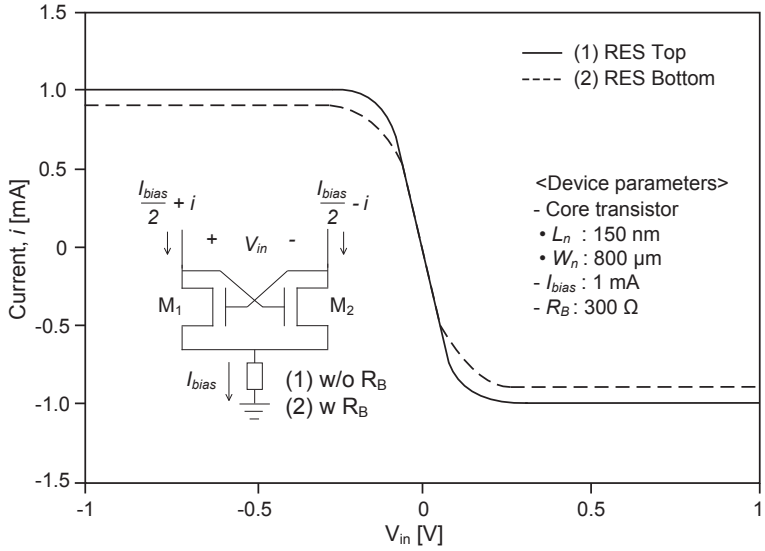

Figure 2.4: Characteristics of current i and different voltage V_{in} in the differential-pair part.

same drain current. Thus, the choice of using PMOS transistors as a current source reduces the effective noise. However, a PMOS current source case still has a large effective noise. Contrarily, resistive biasing techniques show low effective noise because they avoid the use of a noisy MOS current source. Thermal noise from the bias feeding resistor as a current source is low, and therefore it has a small influence on phase noise.

2.3.2 Oscillation Amplitude

From the preceding discussion, increasing oscillation amplitude reduces the phase noise. In Eq. (2.1), the oscillation amplitude in LC-VCO is proportional to the equivalent parallel resistance of the LC resonator R_p and bias current I_{bias}. Because the LC-VCOs shown in Figs. 2.1 and 2.2 have the same LC resonator, the current in each VCO dominates the improvement of oscillation amplitude.

Figure 2.4 shows the I-V characteristic of the differential-pair part of the LC-VCO, which realizes small-signal negative resistance. In the bottom resistive biasing, this part is equivalent to a couple of common-source MOS devices with a source degeneration resistor. The instantaneous gate-source voltage of the common-source MOS devices for bottom and top resistive biasing techniques ($V_{GS,b}$

and $V_{GS,t}$) have a relationship as follows:

$$V_{GS,b} = V_{GS,t} - \Delta V_{R_B}, \tag{2.7}$$

where ΔV_{R_B} is the voltage change of bottom resistor from a biasing point. $V_{GS,t}$ and $V_{GS,b}$ are the instantaneous gate-source voltage of top biasing and bottom biasing, respectively. MOS drain current in the weak-inversion region is proportional to the exponential of the gate-source voltage. The gate-source voltage in bottom biasing is attenuated by the voltage drop across the bottom resistor. The subthreshold drain currents for the two resistive biasing techniques have the following relationship:

$$\begin{aligned} I_{D,b} &\approx I_0 \frac{W}{L} e^{\frac{V_{GS,b}-V_{TH}}{nU_T}} \\ &= I_{D,t} e^{-\frac{\Delta V_{R_B}}{nU_T}}, \end{aligned} \tag{2.8}$$

where $I_{D,t}$ and $I_{D,b}$ are the drain current of top biasing and bottom biasing, respectively. I_0 is the technology current factor, L and W are the effective channel length and width, V_{TH} is the threshold voltage, n is the substrate factor, $U_T = k_B T/q$ is the thermal voltage, and q is the electronic charge ($U_T = 25.9$ mV at room temperature). This equation explains that top biasing has more current than bottom biasing as shown in Fig. 2.4. Considering this phenomenon, instead of Eq. (2.3), the oscillation amplitude can be modified as $A_T \propto iR_p$, where i is the instantaneous current in the differential-pair part. The simulated oscillation amplitude by biasing technique is shown in Fig. 2.5. Top biasing has a larger oscillation amplitude than bottom biasing according to the current at the peak of the differential oscillation voltage characteristics of the differential-pair, and thereby improves the phase noise performance.

2.3.3 Comparison and Discussion

Figure 2.6 shows the simulated phase noise comparison for different biasing techniques. The phase noise results are obtained from the periodic steady-state circuit simulation with various current conditions. In the aspect of a biasing source, through the effective noise analysis, the resistive biasing techniques, which do not use a noisy MOS current source, have 60% less effective noise than the NMOS current source case. The low thermal noise introduced by a biasing resistance lower than nearly 1 kΩ does not influence the oscillator's spectral purity. In the aspect of a biasing position, the

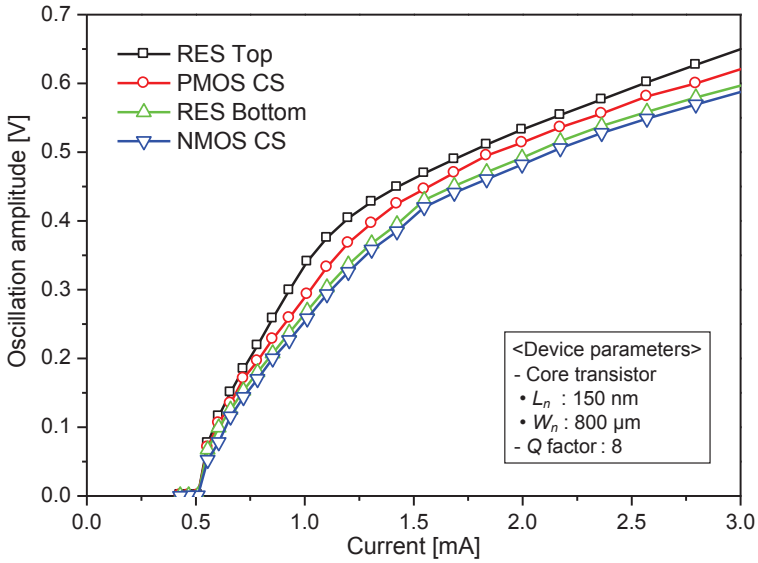

Figure 2.5: Oscillation amplitude.

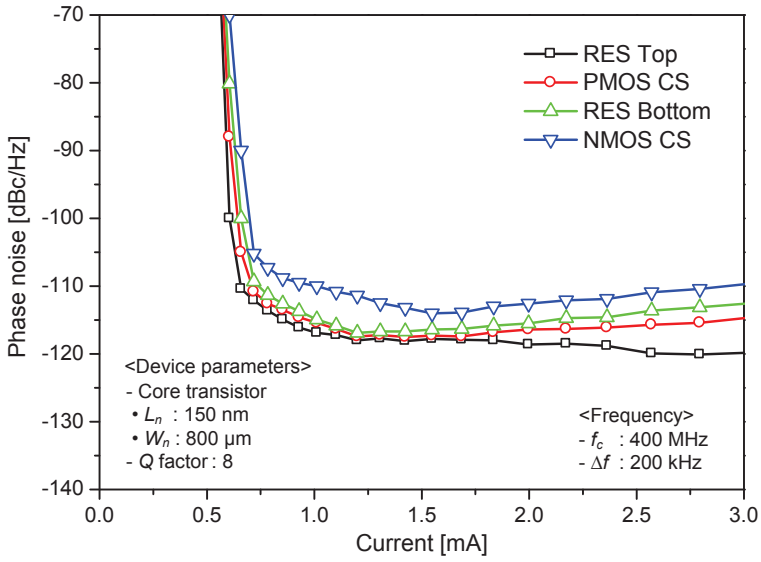

Figure 2.6: Phase noise comparison.

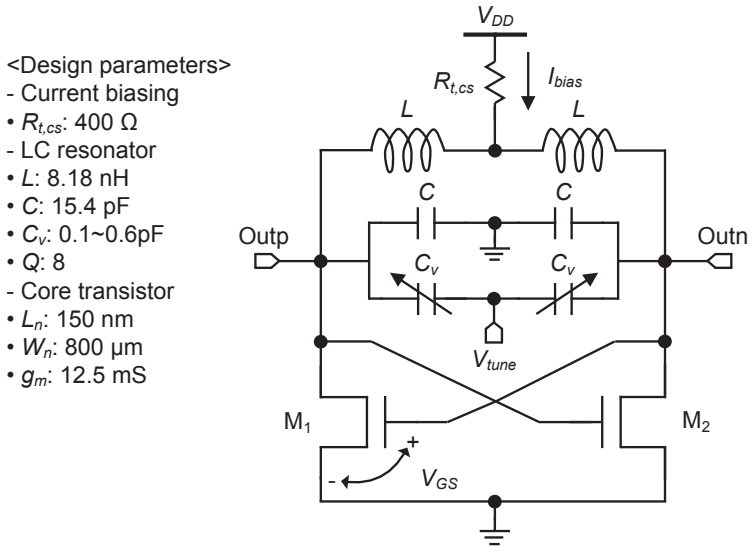

Figure 2.7: Schematic of LC-VCO with top resistive biasing.

bottom biasing technique degrades the oscillation amplitude because of the degradation of drain current. As a result, the top position biasing technique has a higher oscillation amplitude of 1.15 to 1.35 times that of the other biasing techniques. All things considered, the top resistive biasing technique has better phase noise performance because of its smaller effective noise and large output swing. In low-voltage and deep-submicron CMOS technologies, achieving low phase noise is becoming more difficult. In spite of supplying stable current, the MOS current source is not appropriate as current biasing for applications requiring high signal purity, because it operates as a high noise source and needs extra circuits for the reference stable current. In the case of requiring low phase noise, the resistive biasing technique may be efficiently utilized to supply the current in oscillator designs. It is a passive type and thus does not require extra reference circuits. Therefore, this technique has good compatibility in terms of phase noise and implementation complexity.

2.4 Circuit Design and Simulation Results

In this study, the top resistive biasing is applied to design the LC-VCO operating at a 0.7-V supply for the medical implant communication service (MICS) band. The structure of the NMOS cross-

coupled differential LC-VCO with top resistive biasing is shown in Fig. 2.7. The MOS transistors optimally biased in the weak-inversion region ($V_{GS}-V_{TH} \approx -80$ mV) are utilized to provide enough transconductance for a given bias condition, resulting in a reduction of the power dissipation of the LC-VCO. Additionally, a lower gate bias voltage would increase the maximum achievable oscillation amplitude [8] and thereby improves the phase noise performance. The dual-layer spiral inductor and varactor are used for the LC resonator. A dual-layer spiral inductor has a high Q factor value because of its lower series resistance [12]. The inductance of the spiral inductor is 8.18 nH. The capacitance corresponding to inductance is 15.4 pF, and the varactors have a capacitance range of 0.1 pF to 0.6 pF. The Q factor value of the LC resonator is approximately 8 at 400 MHz. Figure 2.8 shows the phase noise and current consumption in accordance with top biasing resistance. With the increase in current consumption, the phase noise performance is improved. However, it is a trade-off between power consumption and performance. For low power consumption, the target of current consumption is set under 1 mA, and the top bias-feeding resistance is approximately 400 Ω, which has a small influence on the phase noise performance. The power consumption of the designed LC-VCO is 700 μW with a 0.7-V supply voltage. Figure 2.9 shows the phase noise performance. The designed LC-VCO using top resistive biasing oscillating near 400 MHz has a phase noise of -116 dBc/Hz at 200 kHz offset frequency, meeting the MICS band phase noise requirement of less than -100 dBc/Hz at 200 kHz offset frequency. The tuning range of the designed LC-VCO is 398 MHz to 408 MHz, covering the MICS band (402 MHz∼405 MHz).

2.5 Conclusion

A phase noise reduction technique using resistive biasing in a low-voltage oscillator design is presented. Phase noise is a key parameter for RF transceivers, and it demands the low-phase noise condition for better spectral purity. Oscillator phase noise is affected by many factors, and the current source is one of the main parameters. In typical oscillators, the current source contribution dominates other sources of phase noise. In this chapter, the phase noise by current biasing techniques is analyzed, and a low-voltage design of LC-VCO using a phase noise reduction technique is presented. Through the phase noise analysis by various current biasing techniques, resistive biasing has the smallest effective noise power because of the elimination of the noisy MOS current source, and

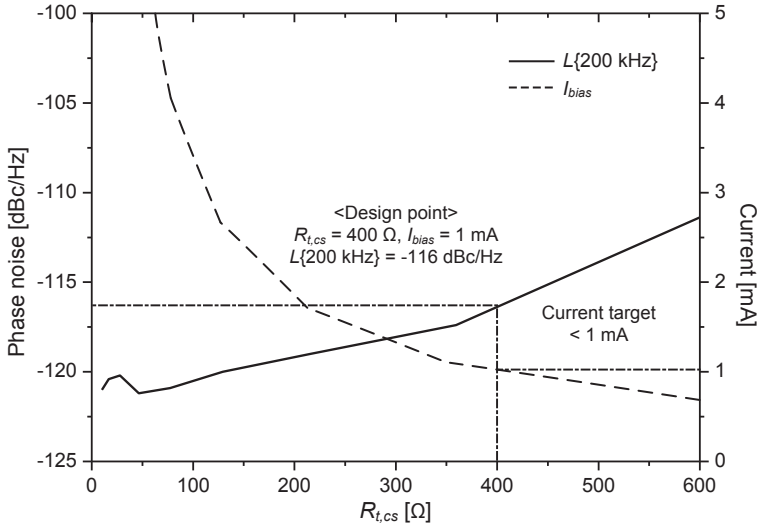

Figure 2.8: Phase noise and current consumption in accordance with top resistance.

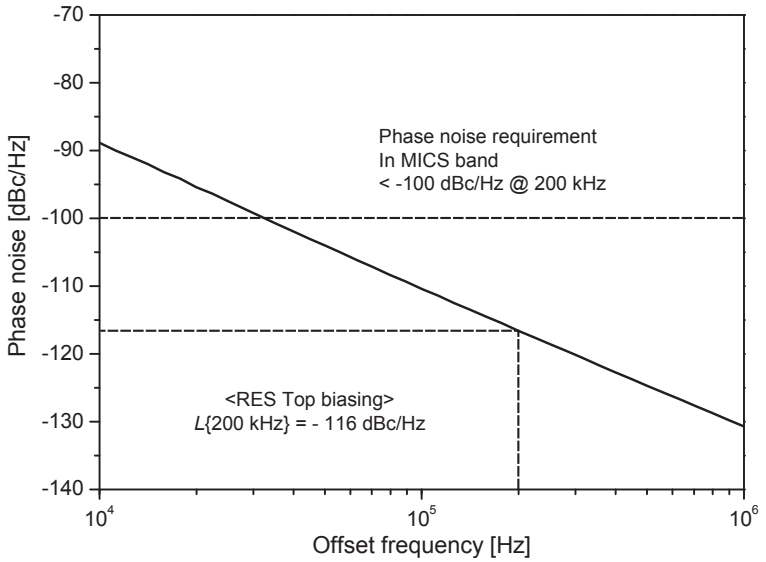

Figure 2.9: Phase noise performance.

top position basing has a large output swing because it has no current degradation. Therefore, the top resistive biased LC-VCO realizes low-voltage operation with better phase noise performance. The designed LC-VCO using top resistive biasing operates from 398 MHz to 408 MHz and exhibits a phase noise of -116 dBc/Hz at 200 kHz offset frequency with an improvement of 1 dB to 6 dB compared to other biasing techniques at similar conditions. In addition, it consumes 700 μW from a 0.7-V supply. From this result, it is confirmed that the top resistive biasing provides a good phase noise performance, and is more proper to low-voltage oscillator designs.

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Chapter 3

Delta-Sigma Digitally Controlled Oscillator

3.1 Introduction

The aggressive scaling of CMOS technology has allowed not only the reduction in the physical size of integrated circuits (ICs) but also the ability to include more components onto a single die. In RF transceivers for medical implantable devices, low power consumption and full integration are the most significant challenges for the design of implantable RF transceivers. After rapid growth over a decade in technology scaling, digital circuits have become preferable compared to analog circuits because of the aggressive improvements in cost, size, flexibility, and repeatability. The high level of integration demanded in wireless systems can be achieved with digital or digital-intensive approaches. RF oscillators traditionally use an analog type for frequency tuning, and now have digital interfaces to allow the peripheral circuitry to be implemented in a digital manner. A digitally controlled oscillator (DCO) generates a signal whose frequency can be controlled with digital words [1]. The DCO enables efficient implementation of the direct frequency modulation in an all-digital phase-locked loop (ADPLL). In the design of a DCO, the low level of spurs and high frequency resolution are challenges for implementation of the ADPLL. Low phase noise and precise frequency resolution for channel selection are desirable for the high-performance fully integrated ADPLL architecture for wireless communications. There have been many efforts to improve the phase noise performance by improving the Q factor of the oscillator, and to increase the frequency resolution by using a large number of capacitors. However, the method of using a large number of capacitors has a trade-off

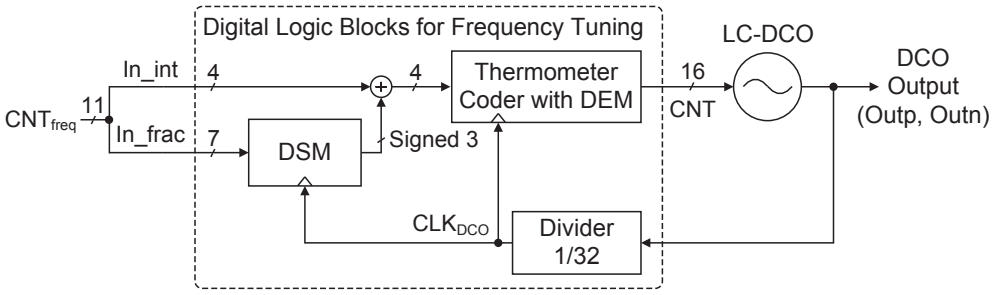


Figure 3.1: Architecture of the DCO with digital logic blocks.

relationship between the size and frequency resolution, and it also suffers from capacitor mismatch.

In this study, an LC-DCO operating in the weak-inversion region and delta-sigma modulator (DSM) are employed for better performance. CMOS devices operating in the weak-inversion region have the advantage of a higher transconductance to power dissipation ratio with satisfactory noise performance in comparison with the strong-inversion region. Therefore, an LC-DCO operating in the weak-inversion region achieves low-power and low-phase-noise characteristics. The DSM is used to achieve precise resolution. It provides a fractional tuning range with a small number of capacitors. In addition, dynamic element matching (DEM) is used to reduce the capacitor mismatch.

This chapter describes the DSM-based LC-DCO design using a 130-nm CMOS process for low-voltage operation. The architecture of a DCO operating in the MICS frequency band is shown in Fig. 3.1. It is composed of an LC-DCO core and digital logic blocks for frequency tuning. The oscillation frequency is controlled through the digital logic blocks with two types of digital word (In_int and In_frac). A thermometer coder with DEM is used for the conversion of an input digital bit. In addition, for high frequency resolution, the DSM is employed and is clocked with the high-frequency signal derived from the DCO output using a divide-by-32 circuit.

This chapter is organized as follows. Section 3.2 presents the phase noise analysis, including the DSM effect. Section 3.3 explains the digital frequency tuning logic circuit. Section 3.4 describes the low-voltage DCO circuit design and implementation. Section 3.5 presents the chip measurement results and discussion, and then Section 3.6 concludes the chapter.

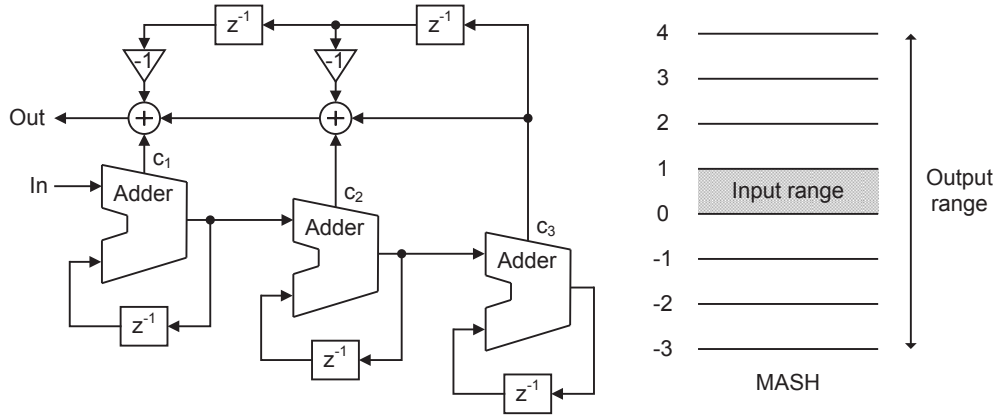


Figure 3.2: Structure of the 3rd-order MASH DSM.

3.2 Phase Noise Analysis

3.2.1 Influence of DSM on Phase Noise

In this section, the extra phase noise introduced by the quantization effects of a finite DSM is analyzed. To analyze the DSM effects on phase noise, a multi-stage noise shaping (MASH) DSM with a simple configuration is considered. The MASH DSM as shown in Fig. 3.2 uses adders in a cascade configuration, and the quantized output of each stage is processed by the noise cancellation logic circuit [2, 3]. Generally, the noise transfer function (NTF) of an N_m-th order MASH DSM is given by [4]

$$NTF\left(z\right) = \left(1 - z^{-1}\right)^{N_m}. \tag{3.1}$$

The extra phase noise for the DSM, $L_{DSM_{N_m}}\left\{\Delta f\right\}$, is calculated as follows [5]:

$$L_{DSM_{N_m}}\left\{\Delta f\right\} = \frac{1}{12 f_{DSM}} \cdot \left(\frac{\Delta f_{res}}{\Delta f}\right)^2 \cdot \left|NTF(z)\right|^{2N_m}, \tag{3.2}$$

where f_{DSM} is the clock frequency of the DSM ($z = exp(j2\pi\Delta f / f_{DSM})$), and Δf_{res} is the frequency resolution associated with the effective capacitance switched by the DSM output. From this formula, it can be seen that both small frequency resolution and high clock frequency of the

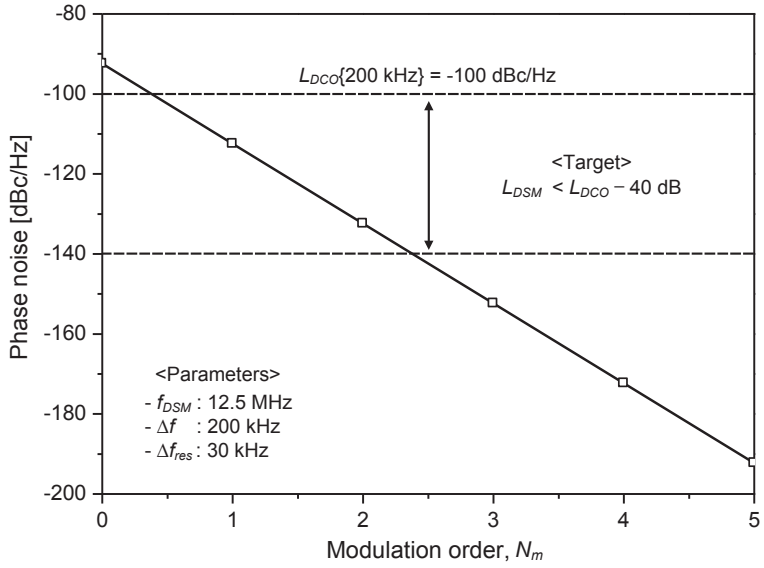


Figure 3.3: Phase noise due to a modulation order.

DSM are desirable for a low phase-noise contribution. In case of N_m-th order DSM,

$$L_{DSM_{N_m}}\{\Delta f\} = \frac{1}{12 f_{DSM}} \cdot \left(\frac{\Delta f_{res}}{\Delta f}\right)^2 \cdot \left|2 \sin \frac{\pi \Delta f}{f_{DSM}}\right|^{2N_m}. \tag{3.3}$$

Figure 3.3 shows the expected extra phase noise of the DSM as a function of modulation order N_m. The spurious tones can be reduced for the high-order DSM. However, the high-order DSM also increases the hardware complexity. To avoid the influence of the DSM on phase noise performance, the target of extra phase noise is set to -40 dB below the main oscillator phase noise. Thus, a third-order DSM is employed.

3.2.2 Employed 3rd-Order DSM

In this design, to avoid overflow and have a small output range, the single-loop feed-forward structure shown in Fig. 3.4 is used instead of the MASH structure. The shaded area in Figs. 3.2 and 3.4 represents the fractional input range. The number of output levels is only four whereas that of the MASH modulator is eight. Therefore, the single-loop feed-forward structure is useful to prevent drastic changes to the number of selected capacitors. The maximum quantization noise is also much

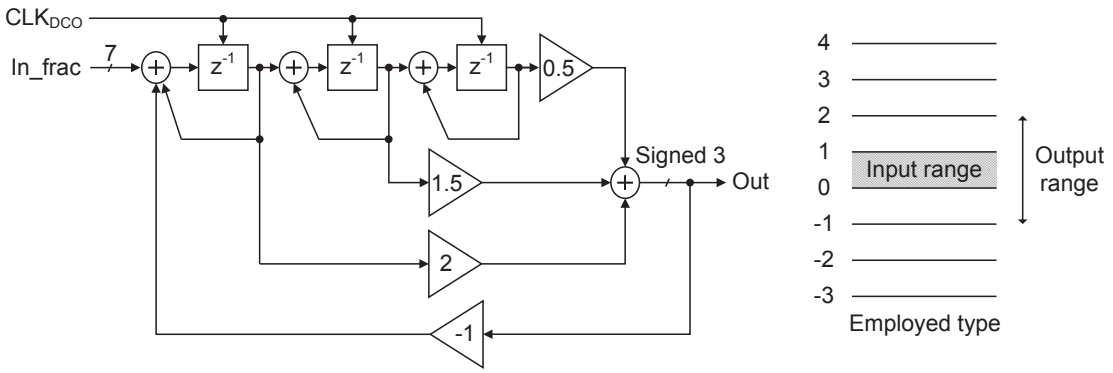


Figure 3.4: Structure and output range of the 3rd-order DSM.

less than that of the conventional MASH modulator. The DSM input is a fractional 7-bit. However, in the DSM implementation, the input data type is used the signed 10-bit to overcome the overflow. The NTF of the employed modulator is given by [6]

$$NTF(z) = \frac{(1 - z^{-1})^3}{1 - z^{-1} + 0.5z^{-2} - 0.1z^{-3}}. \tag{3.4}$$

To avoid digital multiplication, the coefficients of $\{2, 0.5, 1.5\}$ are used to implement using shift operations. This constraint slightly modifies the original NTF, but it still maintains the causality and stability conditions. Substituting Eq. (3.4) in Eq. (3.2), the final extra phase noise for the 3rd-order DSM is given by

$$L_{DSM_{3rd}}\{\Delta f\} = \frac{(\Delta f_{res}/\Delta f)^2}{12\ f_{DSM}} \cdot \frac{(2\sin(\pi\Delta f/f_{DSM}))^6}{1.06 - 2.5\ \rho + 2.4\ \rho^2 - 0.8\ \rho^3}, \tag{3.5}$$

where $\rho = \cos(\pi\Delta f/f_{DSM})$. The calculated extra phase noise by the DSM is -150 dBc/Hz at condition of $\Delta f = 200$ kHz, $f_{DSM} = 12.5$ MHz, and $\Delta f_{res} = 30$ kHz. The overall phase noise including the DSM is expressed as follows:

$$L_{DS-DCO}\{\Delta f\} = L_{DCO}\{\Delta f\} + L_{DSM_{3rd}}\{\Delta f\}, \tag{3.6}$$

where $L_{DCO}\{\Delta f\}$ is the phase noise of the DCO core without the DSM at an offset frequency Δf. This gives $L_{DS-DCO}\{200\text{ kHz}\} = -99.9$ dBc/Hz. Clearly, the DSM introduces extra phase noise through quantization noise. However, it does not significantly affect the overall phase noise because it is sufficiently as low as only 0.1 dB difference for MICS frequency band applications.

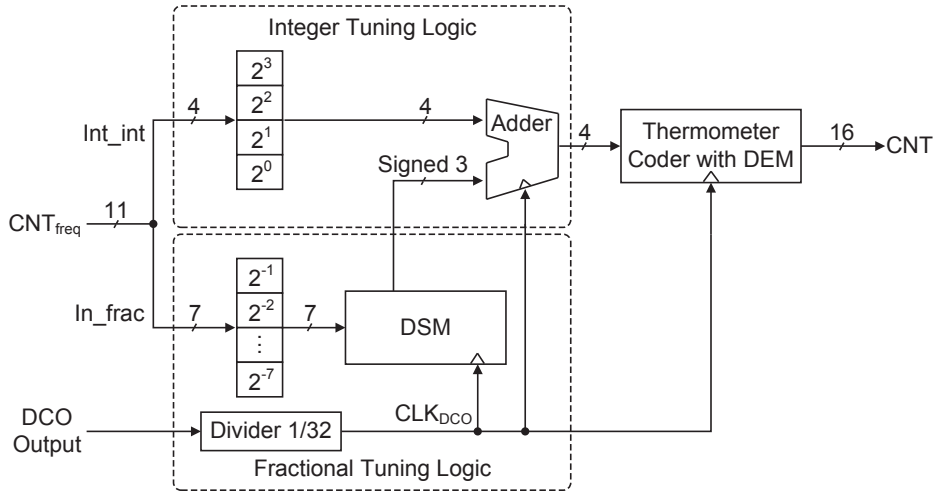


Figure 3.5: Structure of digital logic blocks.

3.3 Digital Frequency Tuning

In a low-voltage and deep-submicron CMOS process, the analog type of frequency tuning, which uses varactor, is a challenging design task because of its nonlinear characteristics and low voltage headroom. The varactor has a narrow linear range and thereby reduces the frequency tuning range. This approach has limits for wideband oscillator design in voltage scaling and a deep-submicron process. The digital approach provides a more efficient solution for frequency tuning in the latest design trends. In this study, the digital logic block as shown in Fig. 3.5 is considered for fully digital frequency tuning. The input control word to the digital block is an 11-bit digital word with a 4-bit integer part and a 7-bit fractional part. In the digital blocks, the fractional part is fed to a DSM, which is clocked by the high-frequency signal CLK_{DCO} derived from a DCO output using a divide-by-32 circuit. The 4-bit integer and signed 3-bit fractional codes are merged by the adder. Then, the merged 4-bit part is converted to a 16-bit thermometer code, where a DEM scheme is also implemented to improve the linearity of the DCO. The 16-bit thermometer output controls the capacitor bank for frequency tuning and performs high-speed capacitance dithering to produce high frequency resolution.

The frequency tuning specifications for the DCO are derived from the intended application with

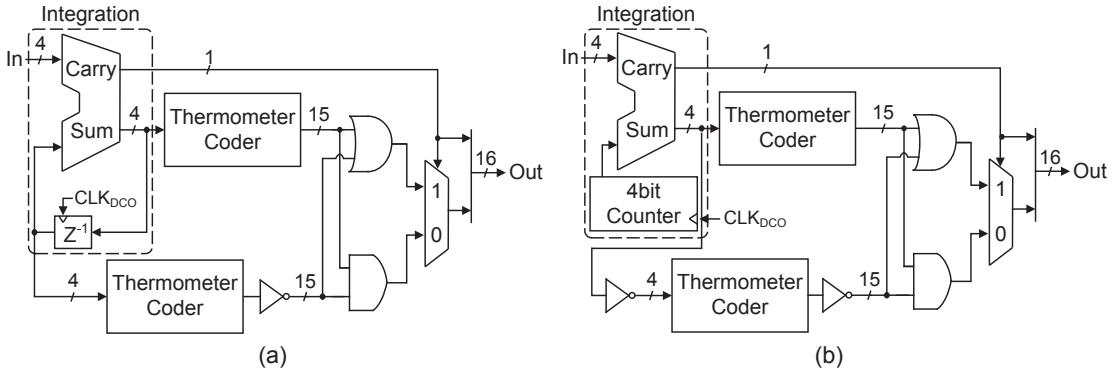


Figure 3.6: Block diagram of (a) DWA and (b) CLA.

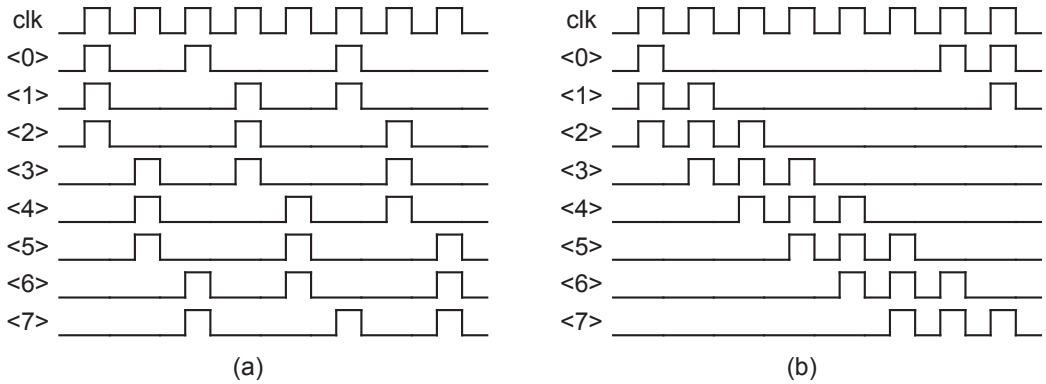


Figure 3.7: Bit-shift operation of (a) DWA and (b) CLA (Input: 3_{10}).

a periodic calibration, where the MICS reference tolerance is 100 ppm [7]. Accordingly, the target frequency resolution considering margin is set below 30 kHz. The oscillation frequency is decided by the integer and fractional frequency tuning codes. The integer tuning step with 4-bit resolution covers a large frequency range with a calibration of the large frequency uncertainty due to process, voltage, and temperature variations. The frequency resolution of the integer step Δf_I is 2 MHz. For precise channel selection, the fractional tuning step is utilized, which is realized by the DSM. The fractional tuning step with 7-bit resolution satisfies the target frequency resolution ($<$ 30 kHz) to cover a narrower band range. The frequency resolution of the fractional step Δf_F is 18 kHz.

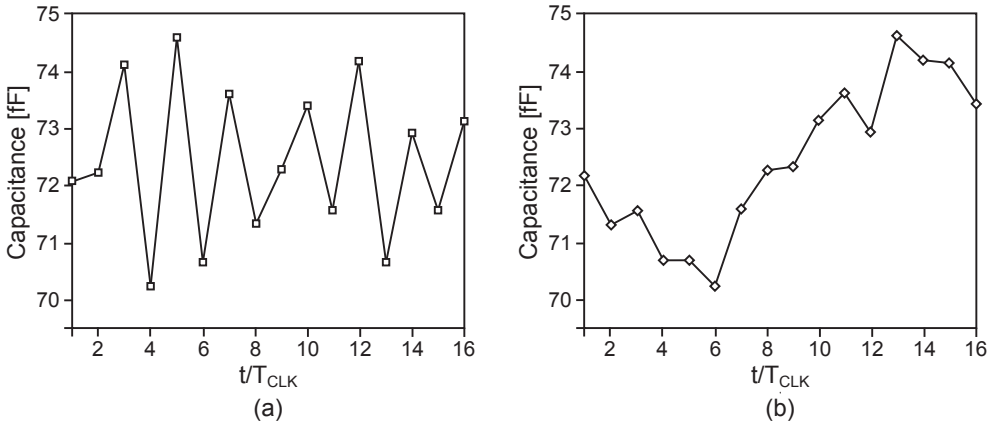


Figure 3.8: Capacitor variation of (a) DWA and (b) CLA.

3.3.1 Dynamic Element Matching

The effect of a capacitor mismatch in the switchable capacitor bank causes distortion in the oscillation signal. The DEM effectively eliminates component mismatches [8]. This technique rearranges the interconnections of the mismatched components to nearly equalize the time averages of the equivalent components at each of the component positions. The influence of the capacitor mismatch can be reduced by changing the capacitor selection during each time in DEM techniques [9]. Accordingly, the oscillation frequency is more stable because of a reduction in the capacitor mismatch. There are many ways to realize DEM. In this work, data-weighted averaging (DWA) and clocked averaging (CLA) are considered for the DEM technique.

The designed DWA and CLA structures are shown in Figs. 3.6(a) and (b). DWA is the most widely used DEM technique because of its simplicity and low hardware overhead [10]. As shown in Fig. 3.7(a), DWA guarantees that each of the elements is used with an equal probability for each digital input code. To realize this, selecting elements sequentially begins with the next available unused element. On the other hand, CLA is realized by sequentially selecting elements shifted by one element, and thereby the influence of previous selected capacitance remains, as shown in Fig. 3.7(b).

Figure 3.8 shows the behavior simulation results of capacitor variation in accordance with DEM

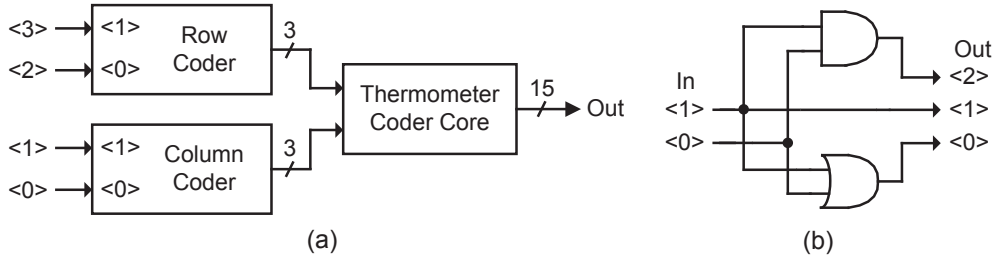


Figure 3.9: (a) Structure of 4-bit thermometer coder and (b) equivalent circuit of 2-bit row/column coder.

techniques. Generally, the capacitor variation can be expressed as $\Delta C/C = 2A/\sqrt{C}$, where A is the process dependent constant. However, analyzing the effect of capacitor mismatch is difficult from actual circuits because it is affected by various parameters. It may be assumed that the capacitor mismatch approximately follows the normal distribution. In this simulation, the standard deviation is set to 5% for the normal distribution of capacitor mismatch. Compared with CLA, the instantaneous capacitance in DWA has a sudden change. Thus, the noise power from the mismatch is distributed at high-frequency components as shown in Fig. 3.8(a). Moderate change of the instantaneous capacitance in CLA causes the noise power from the mismatch at low-frequency components as shown in Fig. 3.8(b). In this study, the DEM effect on the capacitor bank is compared between the DWA and CLA.

3.3.2 Thermometer Coder

The thermometer coder converts a binary number into a thermometer vector where the number of bits set to 1 equals the input binary starting at the first bit 0. In this design, a 4-bit thermometer coder as shown in Fig. 3.9(a) is used to convert the input digital bits. Row-column decoding is most widely used in digital-analog converter design because of its simplicity in design and layout [11]. The digital inputs are decoded in the row and column coder. The equivalent circuit of 2-bit row/column coder is shown in Fig. 3.9(b). On the basis of the 2-bit coder logic circuits, a 4-bit thermometer coder is composed of two 2-bit row-column coders and thermometer coder core shown in Fig. 3.10. The employed thermometer coder converts the 4-bit input to the 15-bit thermometer code. A 4-bit binary to thermometer coder is given in Table 3.1.

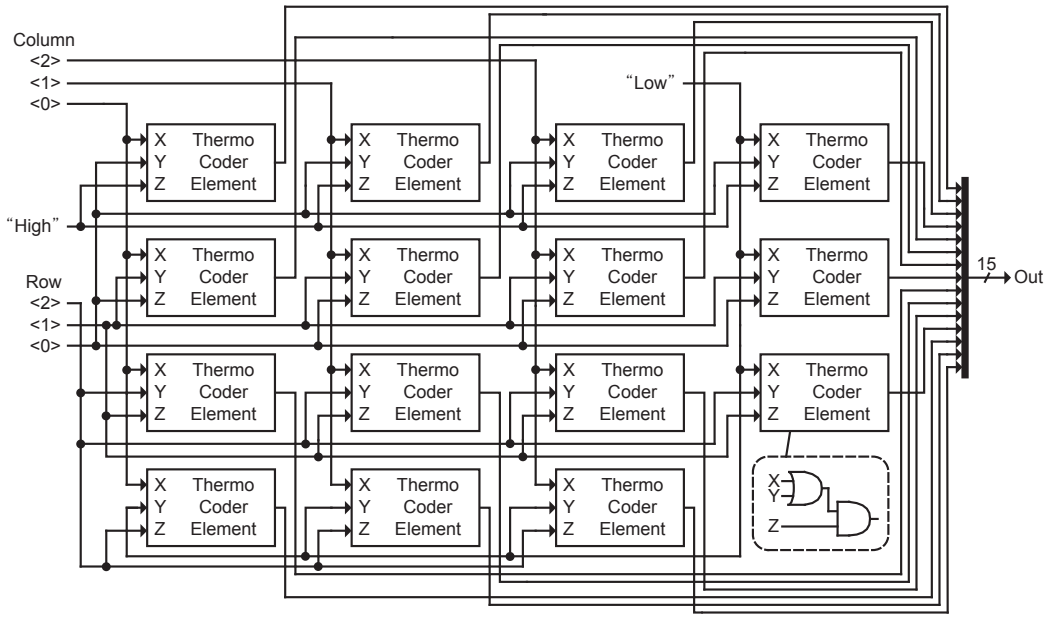


Figure 3.10: Structure of thermometer coder core.

Table 3.1: 4-Bit Binary to Thermometer Coder Logic Truth Table

Decimal	Binary				Thermometer Code							
	B3	B2	B1	B0	T15	T14	T13	···	T4	T3	T2	T1
0	0	0	0	0	0	0	0	···	0	0	0	0
1	0	0	0	1	0	0	0	···	0	0	0	1
2	0	0	1	0	0	0	0	···	0	0	1	1
3	0	0	1	1	0	0	0	···	0	1	1	1
4	0	1	0	0	0	0	0	···	1	1	1	1
≀			≀					≀				
13	1	1	0	1	0	0	1	···	1	1	1	1
14	1	1	1	0	0	1	1	···	1	1	1	1
15	1	1	1	1	1	1	1	···	1	1	1	1

3.4 Circuit Design and Implementation

In this section, the circuit design methodology and parameters are discussed. Table 3.2 shows the design target specifications based on the MICS band requirements. Between the low-frequency

<Design parameters>

1) LC-DCO
- Current biasing
• R_T: 380 Ω (I_{bias}: 0.9 mA)
• R_B: 10 Ω
- LC tank
• L: 8.18 nH
• C_a: 14.3 pF
• C_{bank}: 0.1~1.6 pF (C_u: 100 fF)
• Q: 8
- Core transistor
• L_n: 150 nm
• W_n: 800 μm
• g_{mn}: 12.5 mS

2) Output Buffer
• A_v: 18 dB
• f_{3dB}: 800 MHz

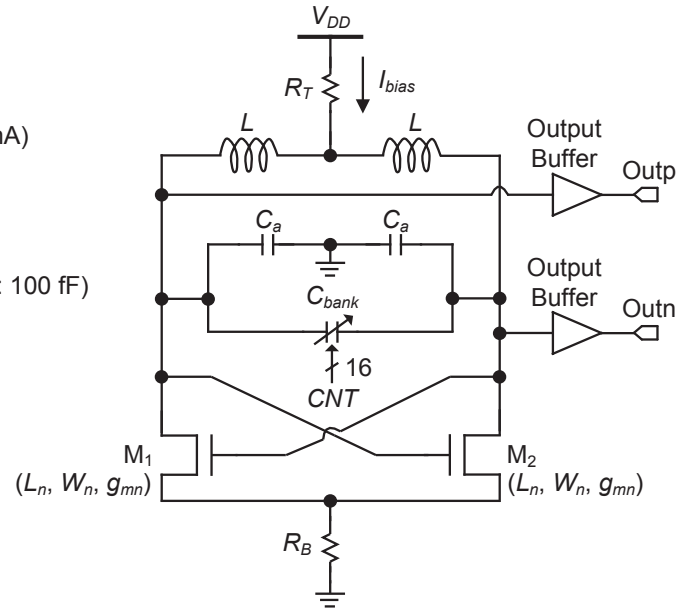


Figure 3.11: Schematic of the LC-DCO.

oscillator and high-frequency oscillator with a frequency divider, the oscillator designs have a trade-off relation between area occupation and power consumption, as shown in the literature [12]. In this design, the direct 400-MHz LC-DCO structure is considered for low power consumption, as shown in Fig. 3.11. An NMOS cross-coupled pair is chosen for the core oscillator design operating at a 0.7-V supply voltage because it has the advantage of common-mode noise suppression and low-voltage operation. For current biasing, top resistive biasing is applied to achieve lower phase noise at low-voltage operation. The switchable capacitor bank controlled by digital blocks is employed for frequency tuning. In the output stage, CMOS buffers are employed to isolate the oscillator from output load variations and to provide the required output signal. The oscillator design procedure can be illustrated as follows:

- LC-tank

  - Determine the inductor with large Q factor at center frequency.

  - Design the capacitor bank in accordance with the inductance to cover the frequency tuning range.

Table 3.2: DCO Design Considerations

CMOS Technology	130-nm
Supply Voltage [V]	0.7
Operating Frequency [MHz]	$402 \sim 405$ (MICS band)
Tuning Range [MHz]	> 3
Frequency Resolution [kHz]	< 30
Phase Noise [dBc/Hz]	< -100 @ 200 kHz offset
Power Consumption [mW]	< 1

- Oscillator core

  - Determine the bias current from the target power dissipation for a given supply voltage.

  - Calculate the target transconductance (g_m) specification from the equivalent parallel resistance of the LC-tank.

  - Determine the transistor gate length from the unity-current-gain cut-off frequency f_T and current efficiency g_m/I_D (I_D: drain current).

  - Determine the transistor gate width to meet the required g_m from the g_m/I_D.

3.4.1 LC-Tank

Oscillators based on LC-tank are the most popular configurations in RF transceivers because of their relatively good phase noise performance and ease of implementation. In this design, a dual-layer spiral inductor and switchable capacitor bank are used for the LC-tank circuit.

Integrated Inductor

The LC-tank resonator is implemented by an on-chip inductor for a fully integrated oscillator. The phase noise associated with the oscillator can be minimized by maximizing the Q factor of the resonator; the inductor plays a key role in determining the resonator Q factor. Thus, maximizing the Q factor of the tank inductor is an efficient way of reducing the phase noise through increasing the oscillation amplitude. In the inductor design, the dual-layer spiral inductor as shown in Fig. 3.12(a) is used to achieve a high Q factor because of its lower series resistance. Figure 3.12 shows the structure of two inductor types. The dual-layer parallel device wires M7 and M8 are coils in parallel. This

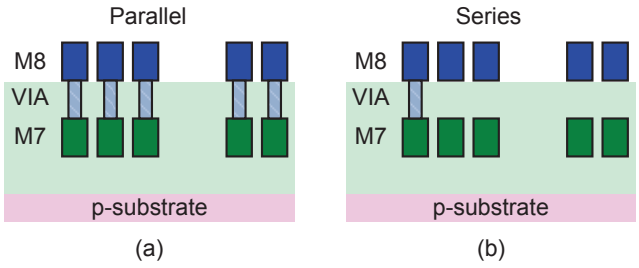


Figure 3.12: Structure of (a) parallel and (b)series inductors.

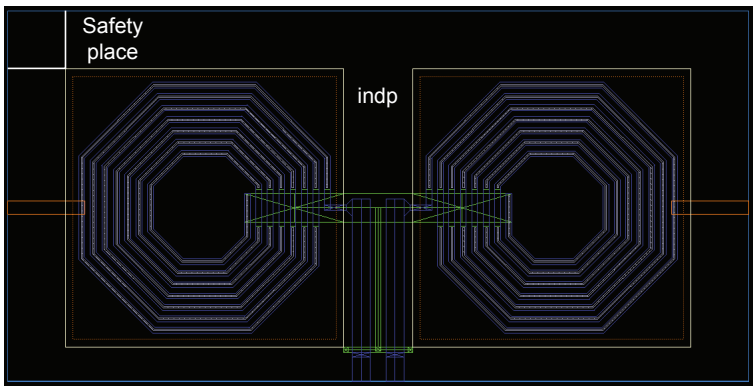


Figure 3.13: Layout of integrated inductor.

layer structure increases the effective metal thickness, and thereby reduces the series resistance [13]. Thus, this inductor has high Q factor. Figure 3.13 shows the layout of the integrated inductor. To isolate the signal line from the ground plane, a safety place is located outside the inductor and a guard ring is used around the inductor. Figure 3.14 shows the simulated inductance and Q factor. The inductance and Q factor of the spiral inductor are 8.18 nH and approximately 8 at 400 MHz, respectively.

Capacitor

The oscillation frequency of an LC-tank is calculated as follows:

$$f_0 = \frac{1}{2\pi\sqrt{L_{tot}C_{tot}}}, \tag{3.7}$$

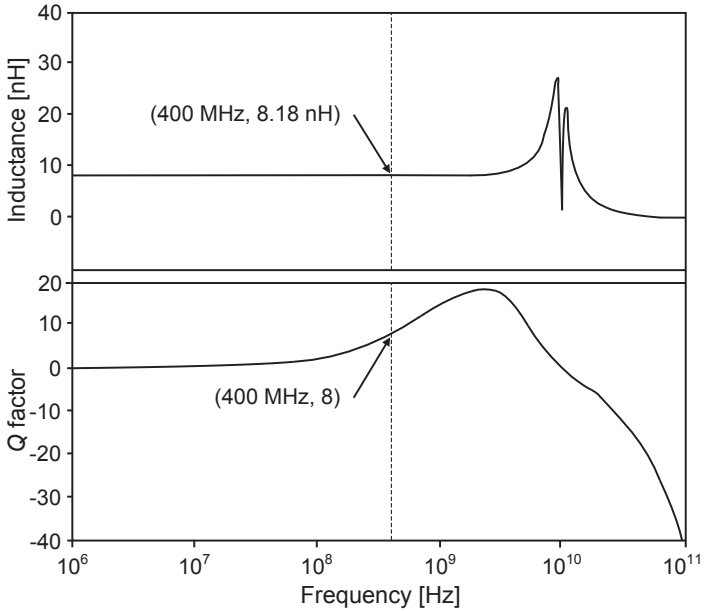


Figure 3.14: Simulated inductance and Q factor.

where $L_{tot}(= 2L)$ and C_{tot} are total inductance and total capacitance, respectively. For the low-voltage operation, the frequency tuning of the LC-DCO using MOS varactors is an extremely challenging task due to its highly nonlinear characteristics [1]. In this design, the switchable capacitor bank is utilized instead of the MOS varactor because it has a high Q factor, linear characteristics, and lower temperature coefficients than the varactor. Although low-cost, high-density metal-oxide-metal capacitors [14] can be fabricated, stacked metal-insulator-metal (MIM) capacitors are used in this design considering the predictability of a capacitor mismatch. The stacked MIM capacitor with a dual-layer design can achieve high capacitance density. Figure 3.15 shows the schematic of the switchable capacitor bank. Each capacitor is switched by using an NMOS switch (M_3) that has a small parasitic capacitance because the on-state conductance can be enhanced even for a small gate width by controlling its source and drain voltages by M_4 and M_5 [15].

Frequency tuning with the switchable capacitor bank enables a fully digital implementation. Because the main capacitors have a small capacitance because of the employed large inductor, the unit capacitors should have much smaller capacitance. The issue is that both small frequency steps and a

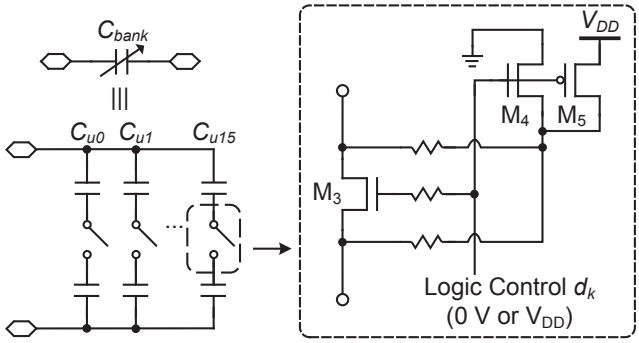


Figure 3.15: Schematic of the switchable capacitor bank.

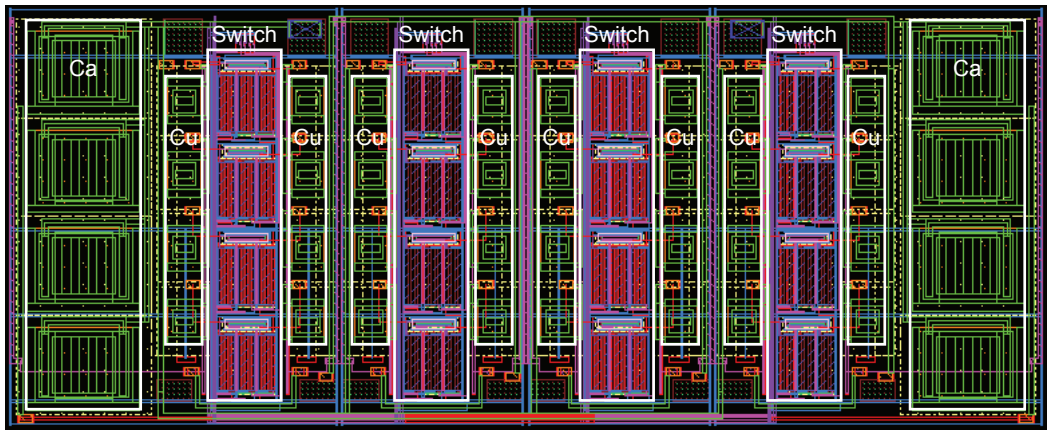


Figure 3.16: Layout of switchable capacitor back.

wide frequency range must be realized with many bits. Because classical implementations of capacitor arrays would require impractically tiny capacitors in the CMOS process, the DSM is utilized to achieve small effective capacitor step sizes. The total instantaneous capacitance can be expressed as below

$$C_{tot} = \frac{1}{2}\left[C_a + \left(\sum_{k=0}^{N_C-1} d_k\right) \cdot C_u\right], \tag{3.8}$$

where C_a is the main capacitance and C_u is the unit capacitance per control code. N_C represents the number of unit capacitors. The codes $\{d_k\}$ are generated in the thermometer coder with DEM, and d_k

indicates the deselection and selection of the k-th unit capacitor for $d_k = 0$ and 1, respectively. The main capacitance corresponding to the inductance is 14.3 pF, and the unit capacitance corresponding to the tuning range is 100 fF. Figure 3.16 shows the layout of the switchable capacitor bank. This layout structure is symmetrically configured. In the MIM capacitor, the width is smaller than the length for lower parasitic resistance.

3.4.2 Oscillator Core

CMOS devices operating in the weak-inversion region provide high transconductance for a given bias condition. This property may be utilized to design low-power circuits. Because the transconductance g_m increases at the expense of lower unity-current-gain cut-off frequency f_T under constant drain current I_D, the weak-inversion region operation is desirable for low-frequency applications. With 130-nm CMOS technology, the device can be driven in the weak-inversion region to achieve the highest transconductance for 400-MHz operation. To satisfy the oscillation condition, the required device transconductance g_{mn} that satisfies unity loop gain at the oscillation frequency f_0 is obtained from the following equations:

$$G_M \geq 1/R_p, \tag{3.9}$$

$$R_p \approx 2\pi f_0 L_{tot} Q_L, \tag{3.10}$$

where R_p is the equivalent parallel resistance of an LC-tank, Q_L is the Q factor of an inductor, and $G_M (= g_{mn}/2)$ is the transconductance of the NMOS differential-pair M_1 and M_2 in Fig. 3.11. In practice, a loop gain of 1.5 to 3 is often used to ensure oscillation start-up. The required transconductance overcoming equivalent parallel tank resistance of an LC-tank ($R_p \approx 330\ \Omega$) is set to 6 mS with a safety factor of 2 for stable oscillation including the start-up condition, and the actual transconductance for NMOS devices M_1 and M_2 (g_{mn}) is set to 12 mS. The NMOS devices are designed in the weak-inversion region to satisfy the required transconductance specification.

The drain current in the weak-inversion and saturation regions is proportional to the exponential of the gate-source voltage V_{GS}, which is expressed as

$$I_D \approx I_{D0} \frac{W_n}{L_n} e^{\frac{V_{GS}-V_{TH}}{nU_T}}, \tag{3.11}$$

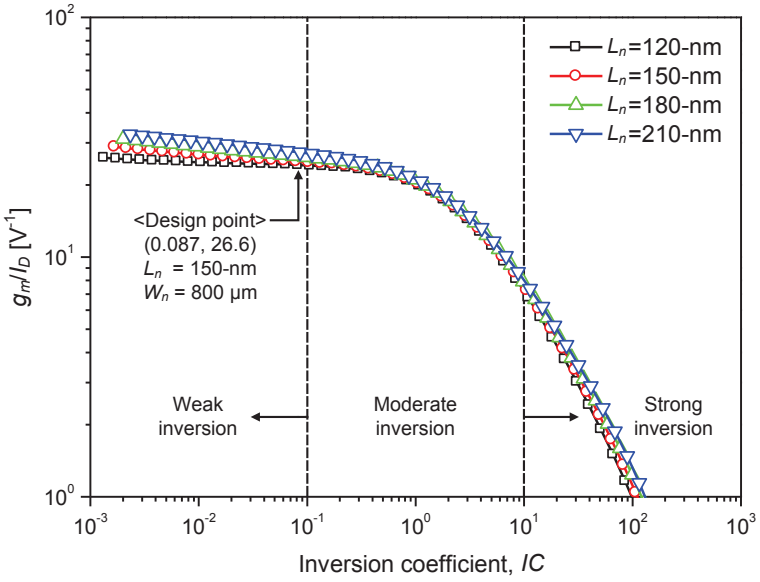


Figure 3.17: Plot of g_m/I_D versus IC for difference channel lengths.

where W_n/L_n is the device aspect ratio, I_{D0} is the technology current, V_{TH} is the threshold voltage. n is the subthreshold slope factor, $U_T = k_BT/q$ is the thermal voltage, k_B is the Boltzmann's constant, T is the absolute temperature, and q is the electronic charge ($U_T = 25.9$ mV at room temperature). The transconductance in this region is expressed as

$$g_m = \frac{I_D}{nU_T}. \tag{3.12}$$

In this region, the drain current is mainly diffusion current and the device works like a bipolar transistor. In fact, the drain current of a given device in any region of operation may be normalized to I_{D0}, producing the inversion coefficient (IC), which provides a measure of the level of inversion for a given set of bias conditions and is given by [16]

$$IC = \frac{I_D}{I_0(W_n/L_n)}. \tag{3.13}$$

Weak, moderate, and strong-inversion correspond to $IC < 0.1$, $0.1 < IC < 10$, and $IC > 10$, respectively. The weak-inversion operation is especially useful because g_m/I_D is nearly constant.

The g_m/I_D methodology has been an attractive technique as a transistor sizing tool for low-power designs because the current efficiency g_m/I_D indicates a measure of efficiency to generate g_m from

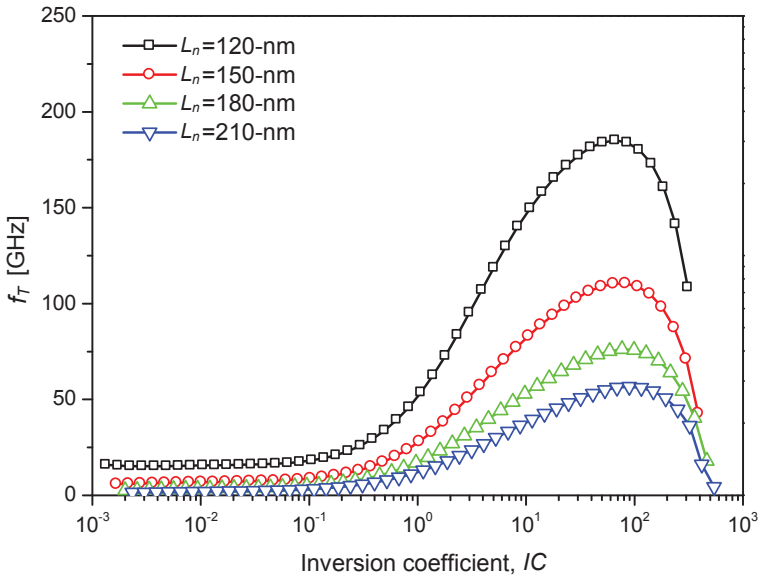


Figure 3.18: Unity-current-gain cut-off frequency f_T versus IC ratio for different channel lengths.

a given I_D. The g_m/I_D can specify all device operation regions including the strong, moderate, and weak-inversion regions [17]. The fundamental design parameters, the unity-current-gain cut-off frequency f_T and current efficiency g_m/I_D, are calculated as a function of IC. The f_T corresponds to $g_m/2\pi C_{gg}$, where C_{gg} is the total capacitance at gate node, and depends on the device size.

Figure 3.17 demonstrates the simulated value of g_m/I_D plotted against the IC ratio for different channel lengths. It is observed that the g_m/I_D gradually decreases with the IC ratio. This plot demonstrates that g_m/I_D increases with decreasing IC. From the square-law device model in strong-inversion, the g_m/I_D can be derived as $2/V_{OV}$ where the overdrive voltage $V_{OV} = V_{GS} - V_{TH}$. The reduced IC enhances the g_m/I_D through the decreased V_{OV}. In the weak-inversion region, the longer channel lengths yield higher values of g_m because longer devices have more ideal subthreshold slope factors. In addition, the g_m/I_D degrades with the reduction of the gate length L_n, which originates from the degradation of the sensitivity of the surface potential to gate voltage [18], or in other words, an increase in n in Eq. (3.12). From this result, it can be seen that longer lengths provide more transconductance in the weak-inversion region because the longer devices have a more ideal subthreshold slope factor (closer to 1). Therefore, a channel length (L_n) of 150-nm is used in this

design.

Figure 3.18 demonstrates the f_T for various channel lengths against the IC. It is confirmed that the f_T decreases with reduced IC and increased channel length because of the gate node capacitance ($C_{gg} \propto L_n W_n C_{ox}$, C_{ox} is the gate-oxide capacitance per unit dimension). In the weak-inversion region, it has a low f_T, which is associated with low-frequency applications.

Equipped with the g_m/I_D methodology, the analog design procedure could be simplified as follows: once the target is set, one could determine the amount of DC bias current that is required in the targeted region, as well as the desired device aspect ratio for the given value of IC. Then, one could determine the device channel length and width on basis of the area requirement. This design procedure is especially useful in the weak-inversion region operation where the transconductance efficiency is nearly constant and the simulated g_m/I_D values could be sufficiently accurate in the weak-inversion region. Considering the required transconductance, the channel length L_n as 150 nm and width W_n as 800 µm are used for NMOS pair transistors. In this design point, the g_{mn} and f_T are approximately 12 mS and 8.5 GHz, respectively. It has enough f_T to operate in the MICS frequency band.

For current biasing, resistive biasing with the top resistor R_T is applied. As discussed in Chapter 2, this technique is more suitable than the active current mirror biasing technique because of the inherent advantages of low noise and large output voltage swing. In addition, the noise performance is improved by eliminating the noise from the active current mirror source. For low power consumption, the target of current consumption is set below 1 mA. The top bias feeding resistance is approximately 380 Ω and its thermal noise has a small influence on phase noise. In addition, to obtain common-mode rejection, a bottom resistor with a small value ($R_B = 10\ \Omega$) is also utilized.

3.4.3 Digital Logic Blocks

Digital logic blocks are implemented in all-digital architecture and expressed in a hardware description language (HDL). It can be synthesized from standard digital cells and automatically placed and routed (P&R) using digital design tools. Between conventional analog and digital-intensive implementations, synthesizable digital implementations significantly reduce the design cost and time. In addition, synthesizable architectures enhance the portability and scalability of analog circuits for various applications and different process technologies because the functionality of standard digital

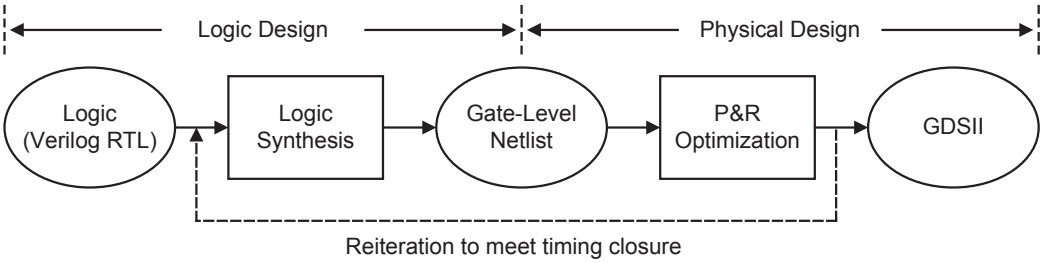


Figure 3.19: The digital design flow for fully synthesizable digital blocks.

cells remains unaltered between different process technologies. In addition, design rules in deep-submicron CMOS technology become much more complex and allow only restricted forms of circuit layout [19], which degrades the productivity of conventional analog design, whereas synthesizable analog design has the potential to circumvent such restrictions on circuit layout.

Figure 3.19 shows the design procedure using standard cell library automated digital design flow. Gate-level Verilog netlists of digital logic blocks can be obtained directly from circuit schematics designed entirely from the standard cell library. Digital logic blocks are described by Verilog code, which can be used to generate gate-level netlists using commercially available logic synthesis tools such as Synopsys Design Compiler. Once all separate netlists are integrated to one netlist, the layout of digital logic blocks can be directly obtained by using commercial P&R tools, including Cadence SoC Encounter. During this step, the P&R tools assume that the whole block is a fully digital system and it might try to optimize the circuit by replacing/removing some of the logic gates, or even changing the whole circuit while maintaining the identical digital functions. Digital logic blocks for frequency tuning are designed and implemented on the basis of Verilog HDL, and detailed synthesizable codes are described in Appendix A.

3.5 Measurement Results and Discussion

3.5.1 LabVIEW-Based Test Bench

Testing and evaluation of the fabricated ASIC are carried out. This chip was evaluated through a field programmable gate array (FPGA)-based test bench. The FPGA enables simple and rapid evaluation of chip performance. The LabVIEW design environment is also used to facilitate FPGA-

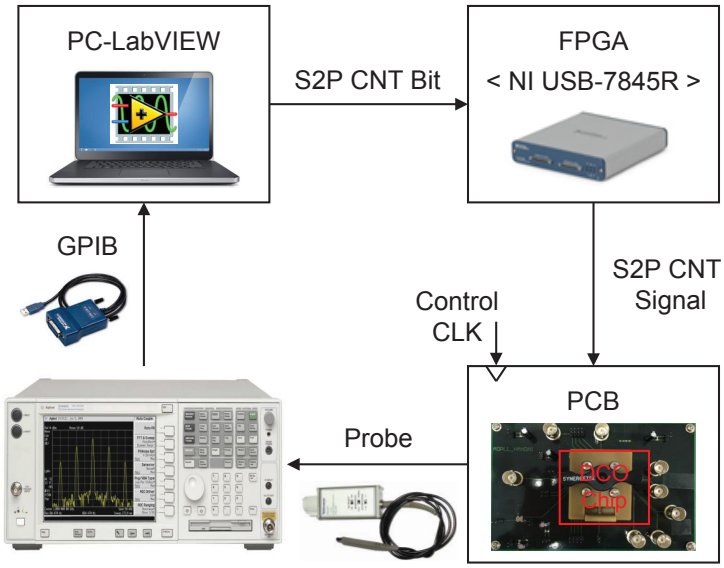


Figure 3.20: FPGA-based DCO chip evaluation environment.

assisted chip testing. Figure 3.20 shows the environment of the LabVIEW-based test bench. In this evaluation, an NI USB-7845R was used as the FPGA board. This board is based on the Kintex-7 70T FPGA module through LabVIEW programming, and has eight analog inputs/outputs and 32 digital inputs/outputs. The control bits are generated through the LabVIEW programming. The procedure of LabVIEW-based chip evaluation is as follows. The control bits for the S2P converter are generated through the LabVIEW programming. In the FPGA, the control bits are translated to an electric signal for the ASIC input. These control signals activate the chip on the printed circuit board (PCB). The instrument measures the chip performance and sends the measured data to LabVIEW through a GPIB cable. Finally, from these measured data, the chip performance is evaluated through the LabVIEW evaluation programming. In this evaluation, the Tektronix P6247 differential probe was used for signal transmission. The phase noise and tuning range were measured using the Agilent E4448A spectrum analyzer. The DC results were checked by the Advantest R6243 DC voltage current source/monitor. The output signal was measured by the Tektronix TDS6604 oscilloscope.

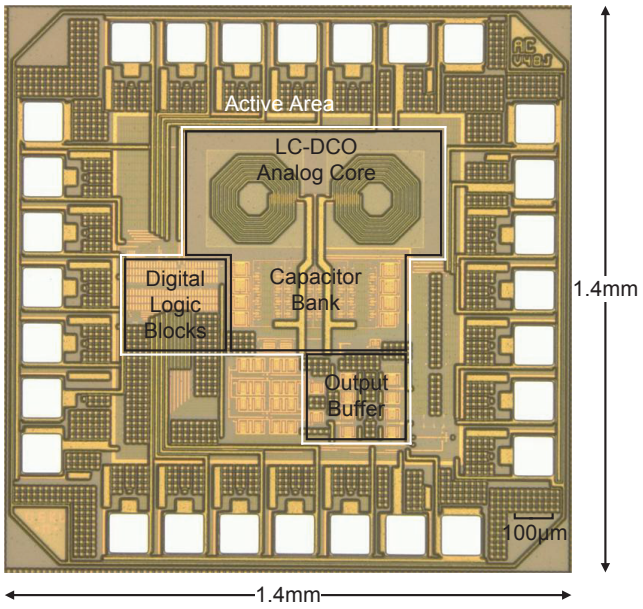


Figure 3.21: Die micrograph (active area of 0.41 mm^2).

3.5.2 Measurement Results

Figure 3.21 shows the die micrograph of the delta-sigma DCO fabricated in a 130-nm CMOS process for a 0.7-V supply voltage, which is the minimum voltage for stable operation of the employed digital standard cell circuits. The chip micrograph includes all ADPLL blocks, and the DCO is fabricated for use in the ADPLL. This section focuses its discussion only on the DCO block. A detailed discussion of ADPLL is presented in Chapter 4. The total chip area including pads is 1.96 mm^2, and the active DCO chip area is approximately 0.41 mm^2. The total power consumption of the fabricated DCO is 700 µW, where the DCO core and the digital block consume 630 µW and 70 µW, respectively. The IC-chip with a 44-pin QFN package is mounted on a PCB. In the board design, the power (VDD) and ground (GND) lines are separated between digital and analog to avoid signal interference. Figure 3.22 shows the measured power dissipation of both the analog and digital parts for different supply voltages. The fabricated DCO has a wide supply voltage compatibility (0.7–1.2 V).

Figure 3.23 shows the measured phase noise performance of the DSM-based LC-DCO by DEM techniques. The digital logic block for frequency tuning introduces spurious signals based on the

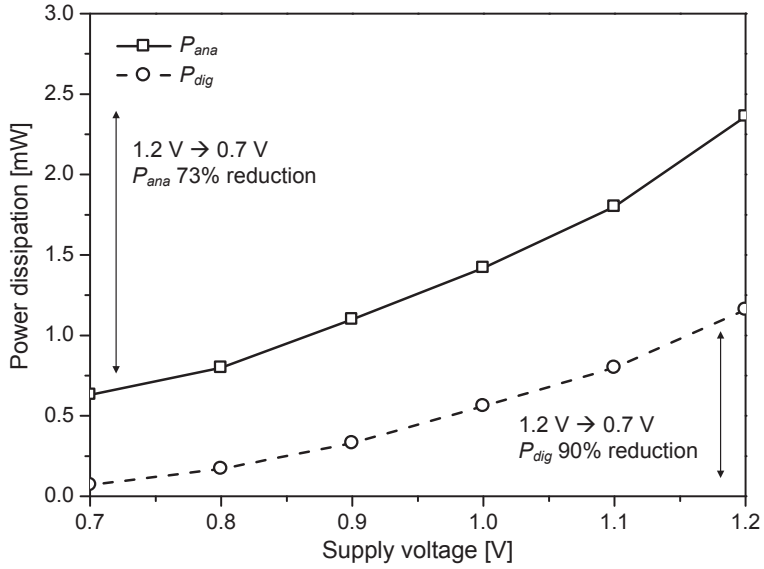


Figure 3.22: Measured power dissipation of each part for different supply voltages.

quantization noise. Thus, the total phase noise of the DCO includes both the DCO core noise and spurious signals from the digital logic block. In the digital logic block, the DSM and DEM generate spurious tones at an offset similar to and lower than the CLK_{DCO} frequency shown in Fig. 3.5, respectively. Therefore, the DEM spur more strongly affects the phase noise performance in the MICS band. Compared with DEM techniques, the CLA spur is generated at a lower frequency offset than DWA (DWA spur: -75 dBc/Hz @ 6 MHz offset, CLA spur: -73 dBc/Hz @ 800 kHz offset). Even if the spurious tone is introduced, it does not affect the phase noise performance because the spurious tone is generated at a large offset frequency out of the MICS channel bandwidth (300 kHz). In addition, the generated spurious tone satisfies the permitted spurious emission level, which is 30 dB lower than the transmitter power [7]. The measured phase noise results are -96.9, -115.3, and -118.6 dBc/Hz at 100 kHz, 200 kHz, and 1 MHz offsets, respectively. This satisfies the MICS band requirement ($L\{200\text{ kHz}\} < -100$ dBc/Hz).

The oscillator is tuned by two types of digital control words: integer and fractional codes. Figure 3.24 shows the measured DCO frequency of the integer tuning range. The implemented LC-DCO has an integer frequency tuning range from 382 MHz to 412 MHz. It has a wide tuning range and

covers the MICS frequency band. The frequency resolution of integer tuning by 4-bit is approximately 2 MHz. Figure 3.25 shows the measured DCO frequency of the fractional tuning range. The fractional frequency tuning range is achieved by using DSM. To obtain the precise fractional tuning range, the measured data for the same codes are averaged. The fractional frequency resolution is roughly 18 kHz, which satisfies the target of the MICS band frequency tolerance.

3.5.3 Comparison and Discussion

To evaluate this study, well-known figure-of-merits (FoMs) are employed as shown below [20]

$$\mathrm{FoM} = L\{\Delta f\}\,[\mathrm{dBc/Hz}] - 20\log_{10}\frac{f_0}{\Delta f} + 10\log_{10}\left(\frac{P_{diss}}{1\ \mathrm{mW}}\right), \tag{3.14}$$

$$\mathrm{FoM_T} = \mathrm{FoM} - 20\log_{10}\left(\frac{\mathrm{FTR}}{10\%}\right), \tag{3.15}$$

where f_0 is the oscillation frequency, P_{diss} is the power dissipation, and FTR is the frequency tuning range in percent. The FoMs are normalized by an offset frequency Δf. Table 3.3 shows performance summary and the comparison of this work with respect to the oscillators in the MICS frequency band reported in the literature. Compared with related works, this work has better phase noise performance and a wide tuning range with high frequency resolution. Low phase noise is realized by the weak-inversion region operation and resistive biasing technique. The wide frequency tuning range with precise frequency resolution is achieved through a switchable capacitor bank controlled by the digital logic blocks. This technique also improves the linearity and resolution. The DSM is often used to realize a fractional range, and is usually applied in the divider for the fractional division ratio in PLL designs [25–27]. In this study, it is applied to digital logic blocks for frequency tuning to achieve the fractional frequency range. Generally, the digital frequency tuning technique requires many tuning capacitors in order to obtain high frequency resolution. In this case, the capacitor bank occupies a large size and is more affected by process mismatch. By using the DSM for frequency tuning, the fractional tuning range can be realized within a small number of capacitors, and it can also reduce the chip size. Moreover, the employed DSM structure is the single-loop feed-forward type, and thus has smaller output variation than the MASH structure. For better performance improvement, the DEM technique is used to suppress the capacitor mismatch effects.

In the aspect of power consumption, the power consumption of the analog and digital circuits is reduced by supply voltage scaling as shown in Fig. 3.22. This means that the digital-based circuits

Table 3.3: Measured Performance and Comparison of MICS Band Oscillators

	This Work	[21]	[22]	[23]	[24]
CMOS Technology	130-nm	180-nm	65-nm	130-nm	180-nm
Supply [V]	0.7	0.7	1.0	1.2	1.5
Oscillator Type	LC-DCO	LC-DCO	LC-VCO	LC-VCO	LC-VCO
Frequency (f_c) [MHz]	397	403	403	403	395
FTR [%]	7.6	2.5	1.2	1.2	22
Phase Noise [dBc/Hz]	-115 @ 200 kHz	-118 @ 1 MHz	-102 @ 200 kHz	-96 @ 100 kHz	-98 @ 160 kHz
Power [μW]	700	400	430	720	1870
FoM [dBc/Hz]	-182.8	-174.1	-171.8	-169.5	-163.3
FoM_T [dBc/Hz]	-180.4	-161.9	-153.7	-151.4	-170.2

may reduce dynamic power consumption in the voltage scaling. Because digital logic blocks are based on fully digital circuits, it has the possibility of low power consumption according to decreasing supply voltage. If V_{DD} is decreased to 0.5 V, the dynamic power of digital logic blocks may reduce by approximately 40%. In this study, a low clock frequency for digital logic blocks is applied through the divide-by-32 circuits. This also reduces the power consumption of the digital blocks.

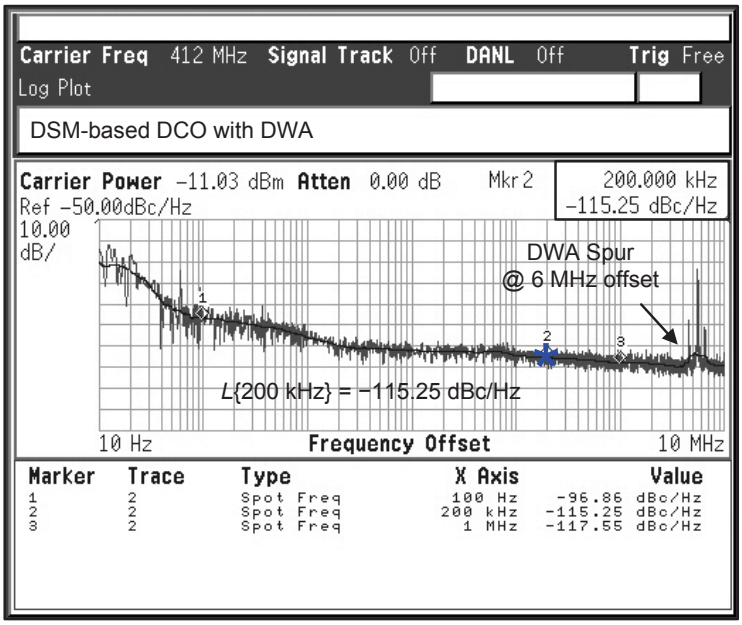
Despite the low power consumption in the digital blocks, this fabricated DCO has higher power consumption compared with [21, 22]. The main reason is the MOS device in DCO core, which consumes most of the power. In the DCO core design, the transconductance g_m target is set up to focus on stable oscillation and superior signal purity because this DCO is used as an oscillator for the ADPLL. In the MOS device in DCO core design, the target g_m generally has a safety factor of 1.5 to 3 to ensure oscillation start-up. In this study, a safety factor of 2 is used for stable oscillation.

A higher g_m usually demands higher current consumption. Therefore, decreasing the g_m provides the possibility of current reduction. A g_m boosting circuit is a solution for reducing the current consumption, but it requires extra circuits [28, 29]. In addition, the resonator design with high Q is a good approach for achieving low power and low phase noise. Through the optimization of on-chip inductor design at the oscillation frequency, high Q can be achieved. This structure has the possibility of low power consumption and can be utilized in various applications in accordance with target performance.

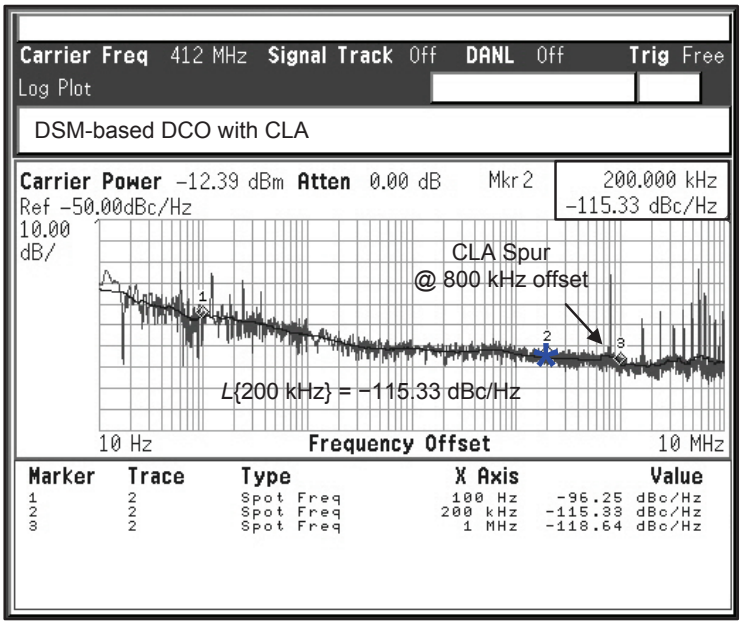
To sum up, the fabricated DCO satisfies all MICS band requirements, has the best FoMs according to the design techniques introduced in this study, and is controlled in a fully digital manner. It also provides the feasibility of low-voltage and high-performance designs for RF oscillators.

3.6 Conclusion

A low-voltage design of a DSM-based LC-DCO for MICS band application is presented. In low-voltage and deep-submicron CMOS technology, analog type frequency tuning is quite a challenging task because of its highly nonlinear varactor characteristics and low-voltage headroom. Digital frequency tuning with a switchable capacitor bank provides a large frequency tuning range and is more robust in low-voltage and deep-submicron CMOS technology. In this study, digital frequency tuning with precise frequency resolution is implemented in the digital logic blocks, such as a thermometer coder with the DEM (DWA and CLA) and DSM. The precise frequency is achieved by using DSM, and it is realized by using a small number of capacitors. In addition, capacitor mismatch is decreased through the DEM technique. Through the digital logic blocks, a large frequency tuning range with precise resolution is achieved within less number of capacitors. The design of the DCO core is optimized by the g_m/I_D methodology for low-voltage operation, and the resistive biasing technique is employed for its advantages of low noise and large voltage swing. From the chip evaluation, it is confirmed that the fabricated DCO has low phase noise and precise frequency resolution. It satisfies the MICS band requirements and shows good performance compared with those of related works.



(a)



(b)

Figure 3.23: Measured phase noise of DSM-based DCO with (a) DWA and (b) CLA.

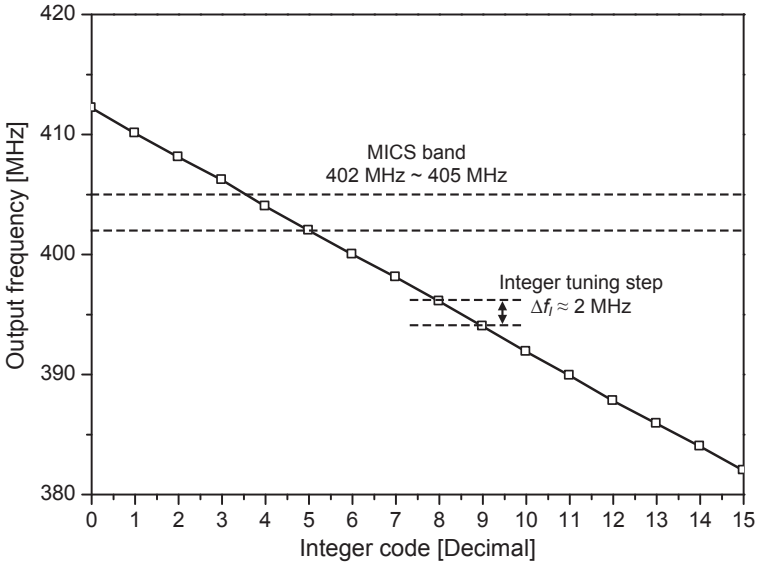


Figure 3.24: Measured DCO frequency range of integer tuning.

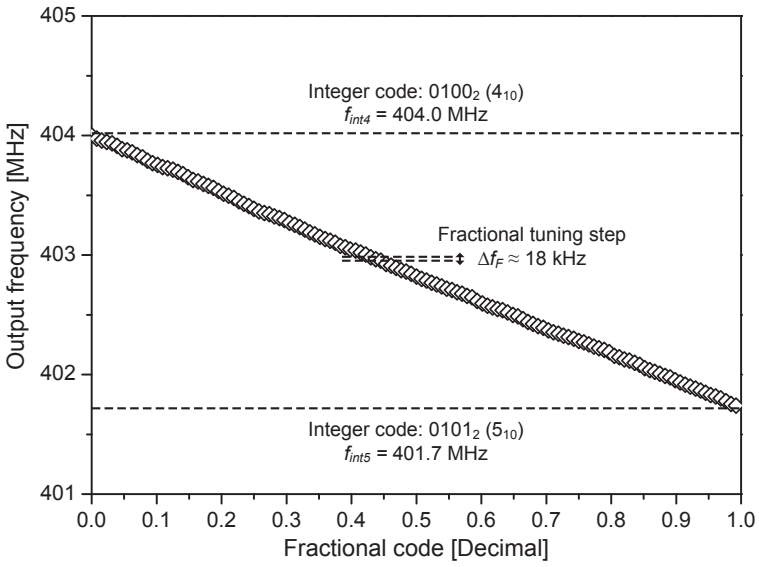


Figure 3.25: Measured DCO frequency range of fractional tuning.

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Chapter 4

Controller-Based All-Digital Phase-Locked Loop

4.1 Introduction

RF transceivers for medical implantable devices require miniaturized forms with long battery life and low power consumption. The frequency synthesizer is one of the most critical building blocks of the RF front-end. Phase-locked loops (PLLs) are widely used in many communication systems to perform frequency synthesis or clock and data recovery. Analog PLLs based on charge-pumps are still widely used, but all-digital PLLs (ADPLLs) have been attracting more attention because of their significant advantages over their analog counterparts. ADPLLs, which interface to allow peripheral circuitry to be digitally implemented, provide low-voltage operation compatibility under process and temperature variations with a shorter system turnaround time [1]. Hence, ADPLLs provide several benefits to duty-cycled battery-operated systems, including MICS transceivers, wireless sensor nodes, and wireless telemetry devices. In the design of an ADPLL, realizing a low level of spurs and high resolution are challenges to achieving a fully integrated high-performance ADPLL architecture.

An important issue in frequency synthesis for recent wireless applications is the acquisition or settling time to a new channel frequency from the trigger event to the instance when the wireless terminal is ready to transmit or receive with the specified low level of frequency error, phase noise, and spurious tones. In ADPLLs, time-to-digital converters (TDCs) have been replacing conventional phase-frequency detectors (PFDs) and charge-pumps [2]. The resolution of the TDC is highly im-

portant in the performance of the ADPLL because low resolution causes in-band phase noise. TDCs require advanced CMOS technology and additional system complexity to achieve high resolution and thereby have high power consumption. Additionally, TDCs are sensitive to process, voltage, and temperature variation. Such high sensitivity can cause poor linearity and non-uniform phase detector gain, resulting in widespread spur generation. Hence, in this study, a TDC-less controller-based architecture is employed for a low-complexity ADPLL [3, 4]. The controller has a counter-based structure. Thus, it has easier implementation with less complexity. The digital implementation of a controller reduces the silicon die area and eliminates loop filter components. To improve phase acquisition, the phase interpolator is employed. It provides pre-settled operation of the ADPLL output phase through the phase selection schemes.

This chapter describes the architecture and circuit implementation of a controller-based ADPLL. The circuit is intended for medical implantable transceivers operating in the MICS band and is based on a programmable integer-N PLL. The system functionality of the controller-based ADPLL is analyzed through phase-domain modeling. Additionally, the phase-domain model has been validated against Verilog-HDL simulations. The ADPLL circuits are designed with a focus on low-voltage operation. The chip was fabricated using a 130-nm CMOS process with eight-level metals. The fabricated ADPLL is controlled in a fully digital manner, and all target specifications are based on the MICS band requirements. The ADPLL designed in this study was verified through on-board evaluation from an FPGA-based test bench. Using the FPGA-based test bench facilitates the evaluation of chip performance. The chip was packaged in a 44-pin QFN package and tested on the evaluation board. From the chip measurement, the fabricated ADPLL performance was evaluated. It was also verified by comparison with related studies.

This chapter is organized as follows. Section 4.2 presents the architecture of ADPLL including modeling analysis. Section 4.3 describes the circuit design and implementation of ADPLL blocks for low-voltage operation, and then Section 4.4 concludes the chapter.

4.2 Architecture of All-Digital Phase-Locked Loop

Figure 4.1 shows the top-level architecture of the designed ADPLL. It consists of a PFD, controller, digitally controlled oscillator (DCO), phase interpolator (PI), phase selector (PS), and programmable

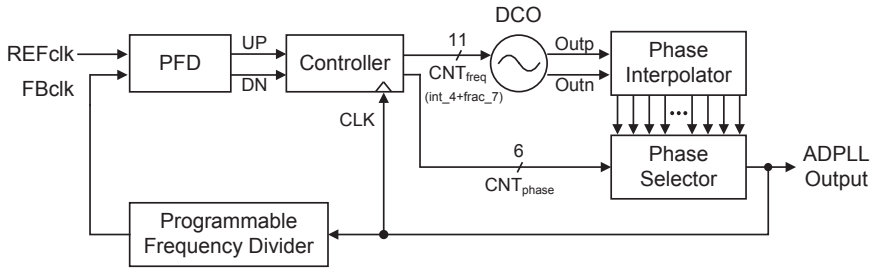


Figure 4.1: Architecture of the controller-based ADPLL.

frequency divider. In addition to phase modulation path in the DCO, the proposed ADPLL has a secondary phase selection path to select the phase with the least error from the phases generated by the PI. Furthermore, the phase of the ADPLL output signal is pre-settled by the phase selection, thereby reducing the phase acquisition time of the ADPLL. The feedback path includes a programmable frequency divider that divides the output signal for comparison with a reference signal. The PFD detects both the phase and frequency differences between the reference and feedback signals (REFclk and FBclk, respectively, in Fig. 4.1). The pulse widths of the PFD outputs (UP and DN) indicate the phase difference. The controller then measures the UP and DN pulses to digitize the phase differences. The accumulator in the controller counts the phase error using the time resolution of the CLK of the controller. From the phase and frequency errors, the controller adjusts the digital control words. The frequency and phase control words are generated by the division (/) and modulo ($\%$) operations, respectively. The DCO generates a signal whose output frequency is tuned with the frequency control word CNT_{freq} from the controller. On the basis of phase control word $\text{CNT}_{\text{phase}}$, the PS selects one of the multi-phase signals generated by the PI with the least phase error. The phase of the output signal is pre-settled by phase selection, as described previously.

4.2.1 Discrete Time z-Domain Model

The controller-based ADPLL is a discrete-time sampled system implemented with all digital components. Therefore, the z-domain representation is the most accurate without requiring approximations [5]. Figure 4.2 shows the discrete-time z-domain model of the ADPLL, where K_{dco} is the gain of the DCO and K_{pi} is the gain factor from the PS. The variables $\Delta\theta_r$ and $\Delta\theta_0$ are the excess

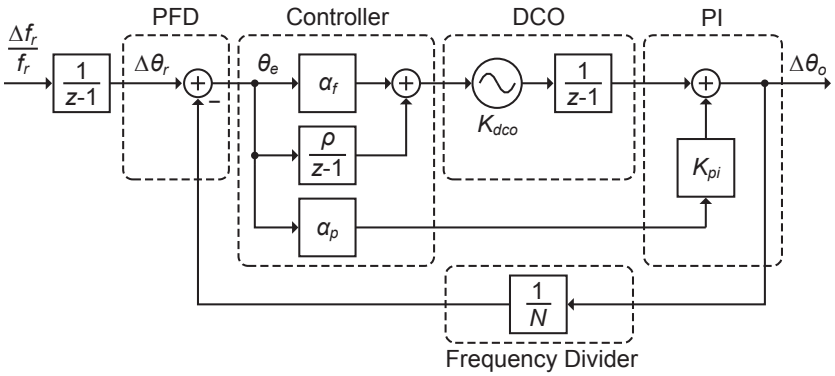


Figure 4.2: z-domain model of the controller-based ADPLL.

reference and feedback phases, respectively, and the sampling rate is the reference frequency f_r.

The controller has two types of digital control words based on the counter operation, and its two transfer functions, $K_{cnt,dco}$ and $K_{cnt,ps}$ for the DCO and PS in the discrete-time z-domain, are respectively given by [3, 4]

$$K_{cnt,dco}(z)\theta_e(z) = 2^{-b_{frac}} \left\lfloor \frac{1}{M_{PI}} \frac{1}{z-1} \left\lfloor \frac{N \cdot \theta_e(z)}{2\pi} \right\rfloor \right\rfloor, \tag{4.1}$$

$$K_{cnt,ps}(z)\theta_e(z) = \frac{1}{M_{PI}} \frac{1}{z-1} \left\lfloor \frac{N \cdot \theta_e(z)}{2\pi} \right\rfloor - \left\lfloor \frac{1}{M_{PI}} \frac{1}{z-1} \left\lfloor \frac{N \cdot \theta_e(z)}{2\pi} \right\rfloor \right\rfloor, \tag{4.2}$$

where $\lfloor x \rfloor$ is the floor function, and yields the largest integer not greater than x, θ_e is the phase error, b_{frac} is the number of digits of a fractional part of the DCO input, N is the frequency division ratio, M_{PI} is the number of phases generated through the PI, and $z = exp(s/f_r)$. The expressions on the right-hand sides of Eqs. (4.1) and (4.2) correspond to the Verilog-hardware description language (HDL) description of the controller in this study. Within a small-signal analysis, to simplify the ADPLL analysis, $K_{cnt,dco}(z)$ and $K_{cnt,ps}(z)$ are approximated as $\alpha_f + \rho/(z-1)$ and α_p, respectively. The multiplication factors α_f and ρ are the loop parameters, and α_p is the phase compensation factor. To simplify the mathematical expressions, the scaled factors are given as $\alpha_{fn} = K_{dco}\alpha_f/N$, $\rho_n = K_{dco}\rho/N$, and $\alpha_{pn} = K_{pi}\alpha_p/N$.

According to the control theory, the open-loop phase transfer function can be expressed as

$$\begin{aligned} H_{ol}(z) &= \frac{\Delta\theta_o(z)/N}{\theta_e(z)} \\ &= \frac{\alpha_{pn}(z-1)^2+\alpha_{fn}(z-1)+\rho_n}{(z-1)^2}. \end{aligned} \tag{4.3}$$

The closed-loop transfer function of the z-domain of the controller-based ADPLL is written as

$$\begin{aligned} H_{cl}(z) &= \frac{\Delta\theta_o(z)}{\Delta\theta_r(z)} = \frac{NH_{ol}(z)}{1+H_{ol}(z)} \\ &= N\frac{\alpha_{pn}(z-1)^2+\alpha_{fn}(z-1)+\rho_n}{(\alpha_{pn}+1)(z-1)^2+\alpha_{fn}(z-1)+\rho_n}. \end{aligned} \tag{4.4}$$

4.2.2 Linear s-Domain Approximation

Although the z-transform is the natural description of a discrete-time system, it is common to approximate it with a linear continuous-time system in the s-domain. It is common to approximate the z-transform as a linear continuous-time system in the s-domain. The sampling rate f_r must be at least 10 times the PLL bandwidth [6], such that the approximation $z = exp(s/f_r) \approx 1 + s/f_r$ is valid. Figure 4.3 shows the s-domain linear model of ADPLL. It is a continuous-time approximation of a discrete-time z-domain model and is valid as long as the frequencies of interest are much smaller than the sampling rate, which equals f_r in this case.

The open-loop transfer function of controller-based ADPLL is expressed as

$$\begin{aligned} H_{ol}(s) &= \frac{\Delta\theta_o(s)/N}{\theta_e(s)} \\ &= \frac{\alpha_{pn}}{s^2}\left[s^2+2\left(1+\frac{1}{\alpha_{pn}}\right)\zeta\omega_n s+\left(1+\frac{1}{\alpha_{pn}}\right)\omega_n^2\right] \\ &= \frac{(1+\alpha_{pn})\,\omega_n^2}{s^2}\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right). \end{aligned} \tag{4.5}$$

The open-loop transfer function shows two poles at origin and two zeros at ω_{z1} and ω_{z2}, which are expressed as

$$\begin{aligned} \omega_{z1} &= \left(1+\frac{1}{\alpha_{pn}}\right)\zeta\omega_n\left[1-\sqrt{1-\frac{4\alpha_{pn}\rho_n}{\alpha_{fn}^2}}\right], \\ \omega_{z2} &= \left(1+\frac{1}{\alpha_{pn}}\right)\zeta\omega_n\left[1+\sqrt{1-\frac{4\alpha_{pn}\rho_n}{\alpha_{fn}^2}}\right]. \end{aligned} \tag{4.6}$$

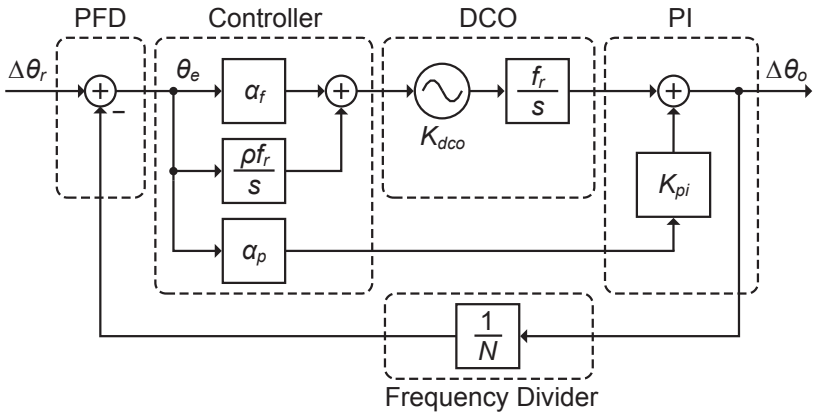


Figure 4.3: Linear s-domain model of the controller-based ADPLL.

The controller-based ADPLL has an additional zero from the phase selection path. Thus, the system parameters depend on the phase compensation factor α_{pn}. In this model, the system characteristics can be controlled by adjusting the phase compensation factor α_{pn}. For the case where $\alpha_{pn} = 0$, the open-loop transfer function is obtained as follows:

$$\begin{aligned} H_{ol}(s) &= \frac{\omega_n^2}{s^2}\left(1 + \frac{2\zeta}{\omega_n}s\right) \\ &= \frac{\omega_n^2}{s^2}\left(1 + \frac{s}{\omega_z}\right), \end{aligned} \tag{4.7}$$

where $\omega_z = \omega_n/2\zeta$. This open-loop expression follows the general second-order PLL system. Comparison shows that the phase compensation factor α_{pn} can enhance tunability of zero in the open-loop transfer function.

The closed-loop transfer function of the s-domain linear model of the controlled-based ADPLL is obtained as follows:

$$\begin{aligned} H_{cl}(s) &= \frac{\Delta\theta_o(s)}{\Delta\theta_r(s)} = \frac{NH_{ol}(s)}{1 + H_{ol}(s)} \\ &= N\frac{\alpha_{pn}s^2 + \alpha_{fn}f_r s + \rho_n f_r^2}{(\alpha_{pn}+1)s^2 + \alpha_{fn}f_r s + \rho_n f_r^2}. \end{aligned} \tag{4.8}$$

The ADPLL has been mathematically analyzed as z-domain and linearly approximated s-domain models in [3, 4, 7]. Generally, the closed-loop function of the ADPLL exhibits the classical two-pole

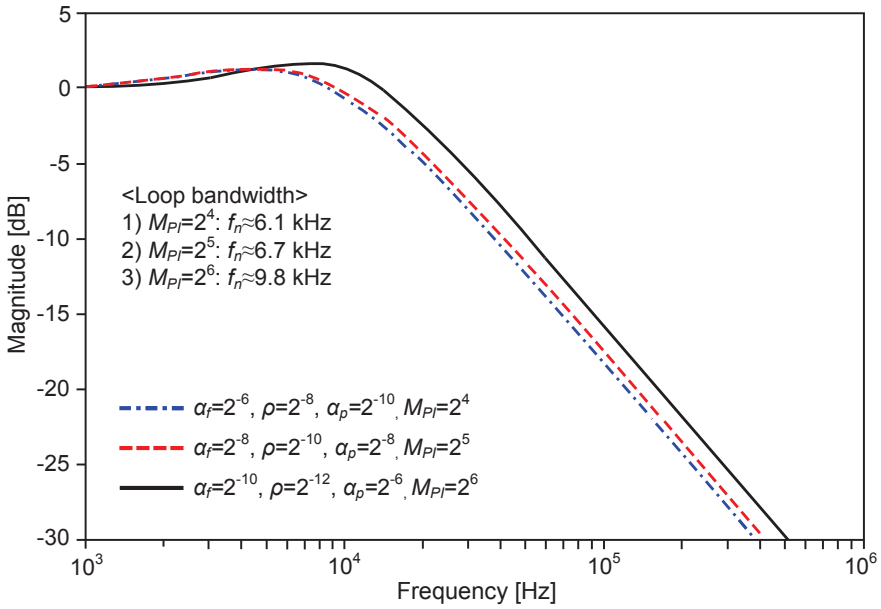


Figure 4.4: Magnitude response $H_{cl}(s)/N$.

system behavior. The system characteristics are determined through the damping factor ζ and natural frequency ω_n calculated by the sampling rate f_r and loop parameters. For this phase model to be compared with the classical two-pole system transfer function, the phase error transfer function is expressed as

$$\begin{aligned} H_e(s) &= \frac{\theta_e(s)}{\Delta\theta_r(s)} = 1 - \frac{H_{cl}(s)}{N} \\ &= \frac{1}{\alpha_{pn}+1} \cdot \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \end{aligned} \tag{4.9}$$

where $f_n = \omega_n/2\pi = \sqrt{\rho_n/(1+\alpha_{pn})}f_r/2\pi$ is the natural frequency and $\zeta = \alpha_{fn}/2\sqrt{(1+\alpha_{pn})\cdot\rho_n}$ is the damping factor. The additional phase compensation factor α_{pn} affects factors ζ and f_n. The phase and frequency errors are eliminated by the closed-loop system. The inclusion of the phase compensation factor reduces the residual phase error of the system.

Figure 4.4 shows the simulation results of the phase-domain model for the s-domain approximation. The modeling parameters α_f, ρ, and α_p can be approximately expressed using M_{PI}, b_{frac}, and N. In this simulation, the gains K_{dco} and K_{pi} are 2 MHz/code-change ($= 4\pi$ Mrps/code-change)

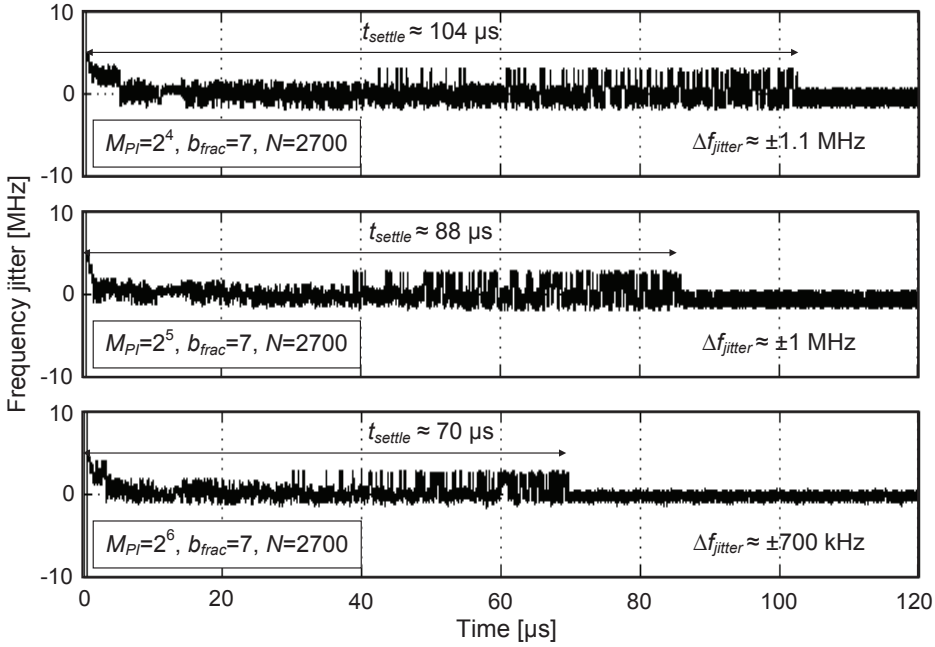


Figure 4.5: Frequency jitter response for one-integer frequency step in the behavior-level simulation.

and $2\pi/M_{PI}$ rad/code-change, respectively. From Fig. 4.4, as M_{PI} increases, the phase domain model simulation of the ADPLL shows that the loop bandwidth increases.

4.2.3 Behavior Model Simulation

The s-domain model has been validated against Verilog-HDL simulations in the previous studies [3, 4]. From the behavior-level simulation shown in Fig. 4.5, as M_{PI} increases, the settling time and frequency jitter variation both decrease. In this study, with $f_r = 150$ kHz, $N = 2700$, $b_{frac} = 7$, and $M_{PI} = 2^6$ ($\alpha_f = 2^{-10}$, $\rho = 2^{-12}$, and $\alpha_p = 2^{-6}$), f_n and ζ are 10 kHz and 0.85, respectively. Note that $f_n \ll f_r$. The settling time ($= 4/\zeta\omega_n$) is less than 70 µs.

From similar behavior-level simulation results for $N = 27$–2700 and $M_{PI} = 2^4$, 2^5, and 2^6 and their comparison with the s-domain analytical model, the empirical approximations for α_f, ρ, and

Table 4.1: ADPLL Design Considerations

CMOS Technology	130-nm
Supply Voltage [V]	0.7
Operating Frequency [MHz]	$402 \sim 405$ (MICS band)
Tuning Range [MHz]	> 3
Frequency Resolution [kHz]	< 30
Phase Noise [dBc/Hz]	< -100 @ 200 kHz offset
Power Consumption [mW]	< 1
Settling Time [μs]	< 100

α_p were obtained in this study as

$$\begin{aligned} \alpha_f &\approx 4\,\rho \\ &\approx \frac{1}{5} \cdot \frac{2^{-b_{frac}}}{2\pi} \cdot \frac{N^{1.25}}{M_{PI}^2}, \end{aligned} \tag{4.10}$$

$$\alpha_p \approx \frac{1}{2} \cdot \frac{1}{2\pi} \cdot \frac{M_{PI}^2}{N^{1.25}}. \tag{4.11}$$

The variables α_f and ρ depend on the maximum number of digitized phase differences (N) and the phase resolution ($\propto 1/M_{PI}$). Equation (4.11) implies that α_p depends on the range of the modulo of M_{PI} (0, 1, $\cdots$, $M_{PI} - 1$) and the time resolution of the CLK ($\propto 1/N$).

4.2.4 Design Considerations

Table 4.1 shows the design considerations of the ADPLL based on the MICS band requirements. In this ADPLL, digital circuits are implemented on the basis of standard cell library for low-voltage operation. To ensure low power consumption, a supply voltage of 0.7 V is applied, which is the minimum voltage for the stable operation of the employed digital standard cell circuits. The DCO structure is same as Chapter 3, and the detailed specifications are described in Section 3.4. The settling time is set to less than 100 μs for low start-up energy. From behavior-level simulations, the phase interpolation technique with 64 phases is used considering the margin, and it yields a phase deviation of $2\pi/64$.

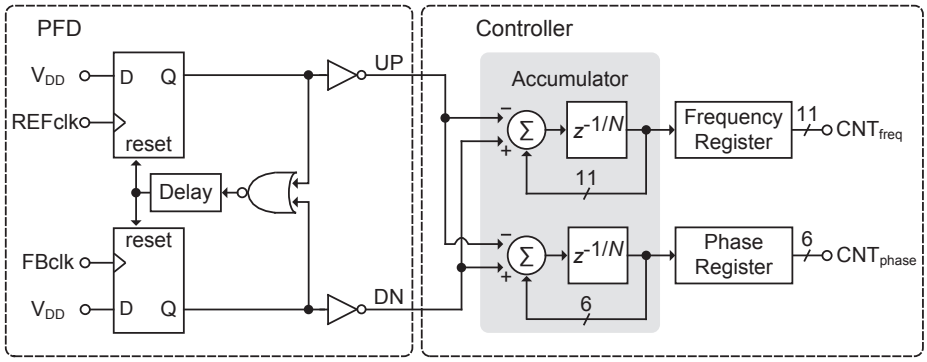


Figure 4.6: Structure of the PFD and controller.

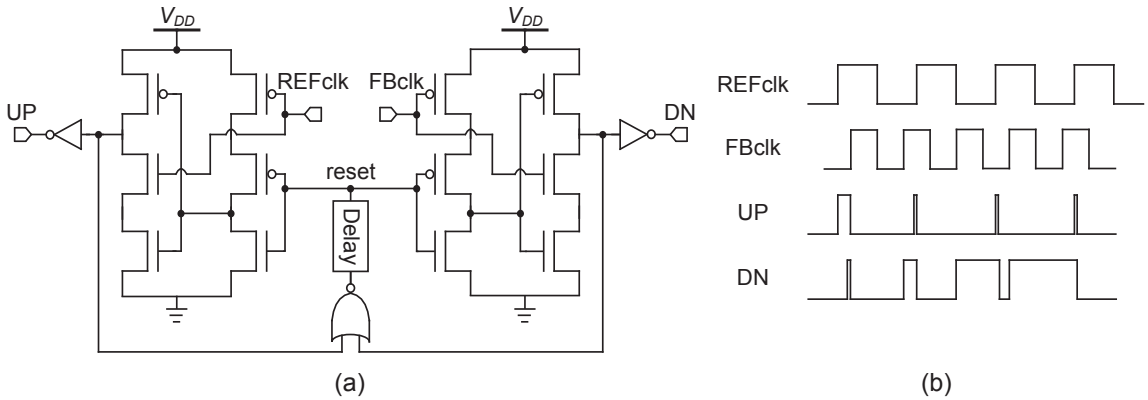


Figure 4.7: (a) Schematic of TSPC DFF-based PFD and (b) its timing diagram.

4.3 Circuit Design and Implementation

4.3.1 Phase Frequency Detector and Controller

Figure 4.6 shows the structure for combination logic of the PFD and the controller. In place of the TDC, this combination logic is used to convert the phase difference to digital control words for frequency and phase adjustment.

The employed PFD consists of D-flip-flops (DFFs), a NOR gate, and a delay element. As shown in Fig. 4.7(a), the DFFs are implemented by the true-single-phase-clock (TSPC) [8] for low-voltage

operation. It consists of two TSPC DFFs and a NOR gate in the feedback path for the reset. This type of circuit can operate normally in high frequency [9–11]. The PFD compares the edges of the reference clock (REFclk) and feedback clock (FBclk) from the frequency divider. As shown in Fig. 4.7(b), when REFclk leads FBclk, the pulse width of UP signal corresponds phase difference. On the other way, when FBclk leads REFclk, the pulse width of DN signal corresponds phase difference. On the reset path, the delay element is inserted to prevent the dead-zone problem. This improves the phase adjustment and reduces the phase noise of the oscillator. Furthermore, compared with PFDs using an RS-type FFs, this structure has low power consumption because of the small number of gates and a large operating frequency range because of short gate delays in the critical reset path.

The controller consists of an accumulator and registers to generate the digital control words as shown in Fig. 4.6. It uses a high CLK frequency to achieve high resolution as shown in Fig. 4.1. The delay element in the accumulator in Fig. 4.6 is expressed as $z^{-1/N}$. The controller measures the UP and DN pulses to digitize the phase difference, and then accumulates the PFD outputs with the resolution of the CLK. The frequency and phase control words are generated by divide and modulo operations on the basis of the accumulation data. From the frequency control word ($\mathrm{CNT_{freq}}$), the digital logic blocks tune the DCO output frequency. In addition, from the phase control word ($\mathrm{CNT_{phase}}$), the phase selector selects one of the 64 phase signals with the least phase error and it provides the pre-settled operation of the phase of the ADPLL outputs. In this study, Verilog-HDL is used to design the controller, and the detailed synthesizable codes are described in Appendix B. The logic synthesizer is used to synthesize the module for gate-level circuits with a standard cell library following the digital design flow. It follows the same procedure as mentioned previously. in 3.4.3.

4.3.2 Phase Interpolator

Figure 4.8 shows the structure of the PI. It consists of a polyphase filter (PPF), a resistive PI, and a PS. A two-stage combination of the PPF and PI is used to generate the 64-phase signal. First, the quadrature signals are generated by the PPF from the DCO differential outputs. In this study, as shown in Fig. 4.9(a), a two-stage RC network PPF was employed because of its wide bandwidth [12]. A two-stage PPF is useful for enhancing the robustness of the process variations in the passive elements [13, 14]. This structure is balanced input signal type, and two-stage PPF transfer functions are

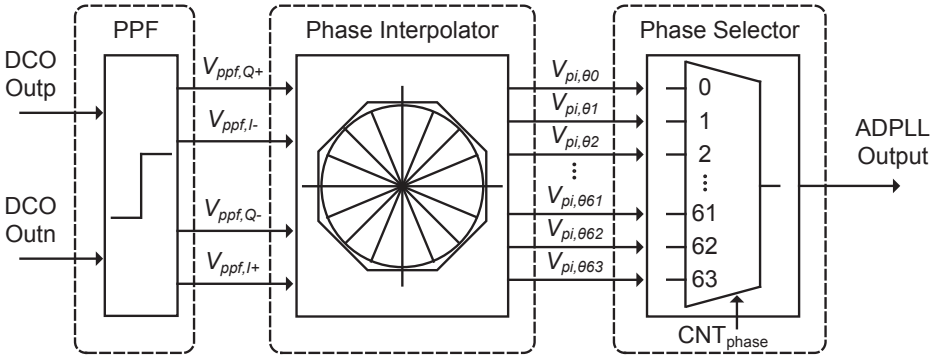


Figure 4.8: Structure of the PI.

given by [12]

$$\begin{aligned} H_I(s) &= \frac{V_{ppf,I+}(s) - V_{ppf,I-}(s)}{V_{dco,p}(s) - V_{dco,n}(s)} \\ &= \frac{1 - s^2\left(R_{p1}C_{p1}R_{p2}C_{p2}\right)}{1 + s\left(R_{p1}C_{p1} + R_{p2}C_{p2} + 2R_{p1}C_{p2}\right) + s^2\left(R_{p1}C_{p1}R_{p2}C_{p2}\right)}, \\ H_Q(s) &= \frac{V_{ppf,Q+}(s) - V_{ppf,Q-}(s)}{V_{dco,p}(s) - V_{dco,n}(s)} \\ &= \frac{s\left(R_{p1}C_{p1} + R_{p2}C_{p2}\right)}{1 + s\left(R_{p1}C_{p1} + R_{p2}C_{p2} + 2R_{p1}C_{p2}\right) + s^2\left(R_{p1}C_{p1}R_{p2}C_{p2}\right)}. \end{aligned} \tag{4.12}$$

Assume that the PI has high input impedance. The ratio between the I- and Q-output signals has an imaginary of $s = j\omega$. Thus, the phase balance is always 90° at all frequencies, R_p and C_p values. The resistor and capacitor values of the two-stage PPF are $R_{p1} = 100\ \Omega$, $R_{p2} = 82\ \Omega$, and $C_{p1} = C_{p2} = 4.42$ pF. The designed PPF has a bandwidth of 350 MHz to 450 MHz and a phase error of 0.1°.

Second, an additional 15 signals are generated by the PI element, which consists of a resistor ladder between quadrature signals, as shown in Fig. 4.9(b), resulting in the 64-phase signal. The resistive voltage-mode interpolator generates the interpolation outputs with a symmetric zero crossing [15,16]. Moreover, the resistive interpolator reduces the power consumption compared with a current-mode interpolator [17].

Nonlinear resistor values were used to achieve equal phase differences. Figure 4.10 shows a

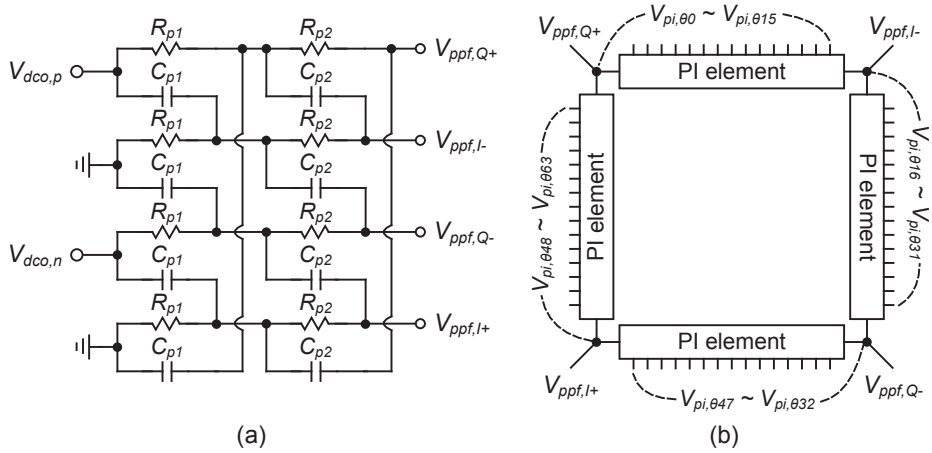


Figure 4.9: Schematic of (a) the two-stage PPF and (b) the PI.

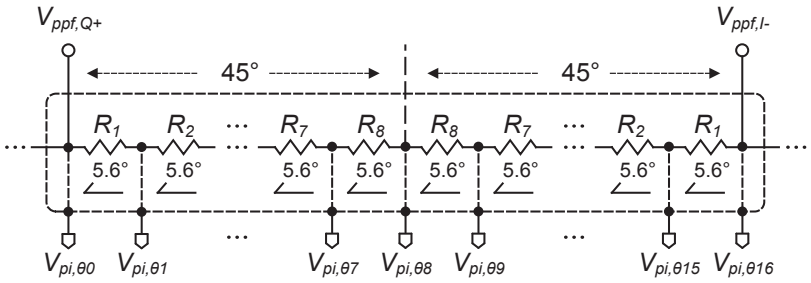


Figure 4.10: PI element ($M_{PI} = 2^6$).

schematic of the resistor ladder-based PI element. The interpolated signals are defined by the resistance ratio. The resistance ratio k_i ($= R_i / \sum_{k=1}^{M_{PI}/8} R_k$, $i = 1, \cdots, M_{PI}/8$) of the resistor ladder can be obtained from the following equation:

$$\sum_{j=1}^{i} k_j = 1 - \tan\left\{(M_{PI}/8 - i)\ \phi\right\}, \tag{4.13}$$

where $\phi = 45°/(M_{PI}/8)$ is the phase difference. In the 64-phase interpolator ($M_{PI} = 2^6$), $\phi = 5.625°$. In this study, a resistance scale on the order of kΩ was used for the actual implementation of the resistor ladders. Based on the resistance ratio, the resistance of each branch resistor is $R_1 =$

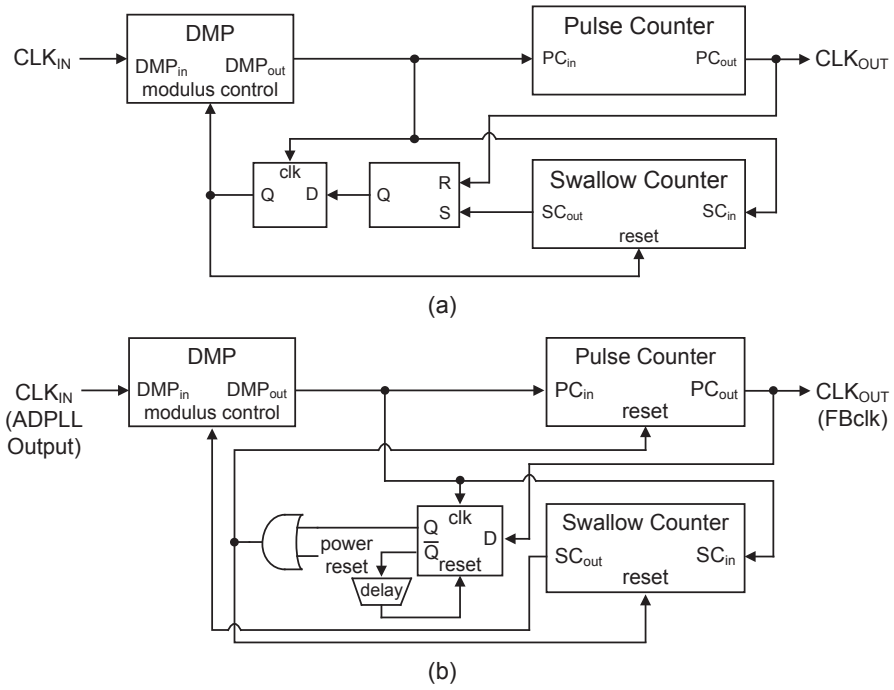


Figure 4.11: Structure of (a) conventional pulse-swallow divider and (b) programmable frequency divider with modified MC re-timing.

1.8 kΩ, $R_2 = 1.53$ kΩ, $R_3 = 1.34$ kΩ, $R_4 = 1.2$ kΩ, $R_5 = 1.1$ kΩ, $R_6 = 1.04$ kΩ, $R_7 = 1$ kΩ, and $R_8 = 985$ Ω.

The PS selects one of them as an output signal from the 64-phase signal according to the phase control word from the controller. This scheme ensures reliable operation and always presents 64 stabilized interpolated signals after the phase interpolation is settled. Because the output signal lock is selected among the 64 pre-settled signals generated by the PI, the output signal is always stabilized for small reference phase fluctuations. In this study, the phase selector is designed by Verilog-HDL, and the detailed synthesizable code is described in Appendix B. The logic synthesizer is used to synthesize the module for gate-level circuits with a standard cell library following the digital design flow as mentioned in 3.4.3.

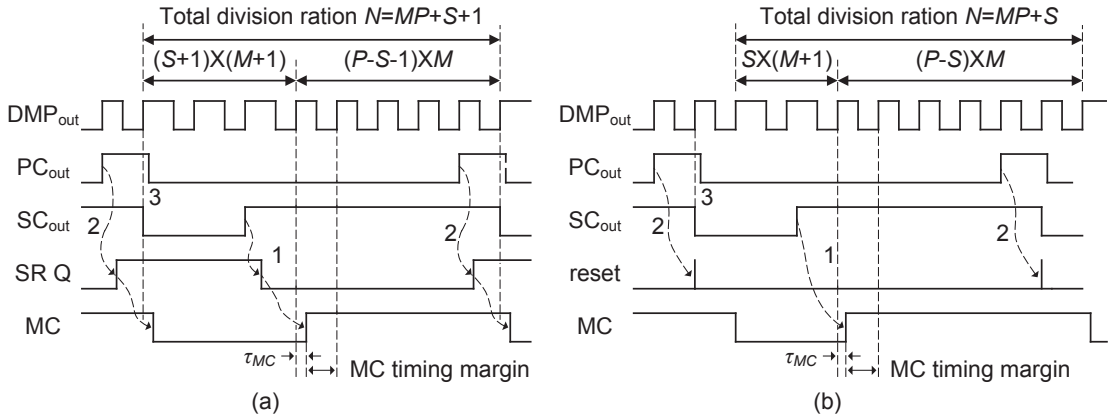


Figure 4.12: Timing diagram of (a) conventional and (b) modified types.

4.3.3 Programmable Frequency Divider

The conventional structure of the programmable frequency divider for PLLs is a pulse-swallow type system based on a dual-modulus prescaler (DMP), as shown in Fig. 4.11(a). It consists of a DMP ($M/(M+1)$), a pulse counter (P), and a swallow counter (S). The division ratio is determined by changing the control words of either P or S. The fundamental speed limitation of this structure usually arises from the critical delay path of the modulus control (MC) signal. When the MC delay is longer than the DMP output period, the total division ratio becomes wrong and the PLL operation goes to a failure. In this study, a modified MC re-timing scheme using a DFF as shown in Fig. 4.11(b) is adopted to effectively resolve the delays [18]. The gate count and critical delay path of the MC signal extending the timing margin are reduced, which provides a high-frequency operating range in low-voltage operation.

Figure 4.12 shows the timing diagram of each scheme. In the employed divider, unlike conventional complex reset circuitry with a set-reset latch and FF, the MC signal is set and reset by a single triggering signal to eliminate the unwanted offset of the total division ratio. As a result, the division ratio of the first half of each period is given by $S(M+1)$, and the second half of each period has a division ratio of $(P-S)M$. Thus, the total division ratio is simply $MP+S$, The reset circuitry is designed by tapping the divider output CLK_{out} and feeding it as an input to the DFF clocked with DMP_{out}. An OR gate is used to turn off the entire divider as an external power reset.

Table 4.2: Division Ratios for MICS Band Channel Selection

Channel	CLKin [MHz]	P code [Decimal]	S code [Decimal]	Division ratio D=$MP + S$, M=32
1	402.15	83	25	2681
2	402.45	83	27	2683
3	402.75	83	29	2685
4	403.05	83	31	2687
5	403.35	83	33	2689
6	403.65	83	35	2691
7	403.95	83	37	2693
8	404.25	83	39	2695
9	404.55	83	41	2697
10	404.85	83	43	2699

Usually, the P code is fixed, and the S code is varied to allow the selection of successive channel values. In this study, M, P, and S are set to 32, 83, and 25–43, respectively, to select the 10 channels of the MICS band. Therefore, the total division ratio is 2681–2699 for the reference CLK of 150 kHz. Table 4.2 summarizes the required division ratios for MICS band channel selection.

4.4 Measurement Results and Discussion

4.4.1 Measurement Results

Testing and evaluation of the fabricated ASIC are carried out. This chip was evaluated through a field programmable gate array (FPGA)-based test bench. The FPGA enables simple and rapid evaluation of chip performance. The LabVIEW design environment is also used to facilitate FPGA-assisted chip testing. This test-bench is similar to DCO evaluation which is described in Section 3.5.1. The output spectrum and phase noise were measured using the Agilent E4448A spectrum analyzer. The DC results were checked by the Advantest R6243 DC voltage current source/monitor. The settling time and channel selection were measured by the Tektronix TDS6604 oscilloscope.

Figure 4.13 shows a die micrograph of the ADPLL fabricated in a 130-nm CMOS process with a supply voltage of 0.7 V. The total chip area including pads and electrostatic discharge (ESD) protection circuits is 1.96 mm^2, and the active chip area is approximately 0.64 mm^2. The DCO in this

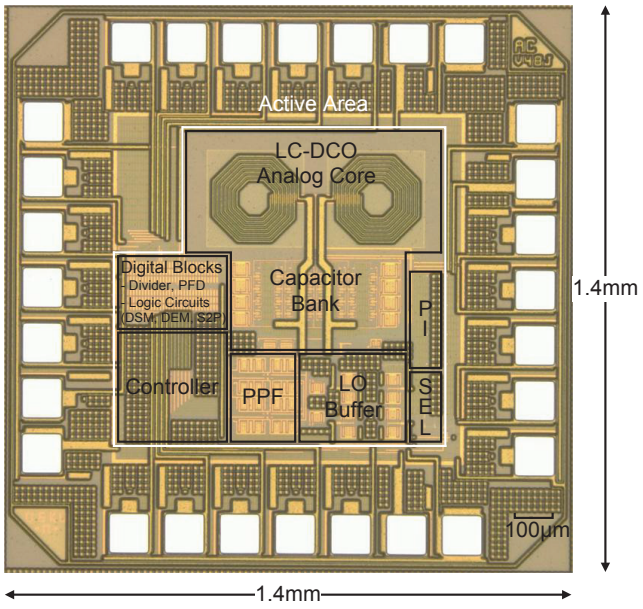
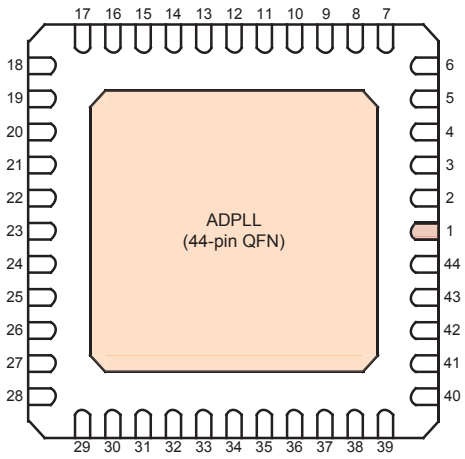


Figure 4.13: Die micrograph (active area of 0.64 mm^2).

chip is same as in Chapter 3. The total power consumption of the fabricated ADPLL is 840 µW, where the DCO including the frequency-tuning and other digital blocks consume 700 and 140 µW, respectively, as described in Section 3.5.2. The IC chip with the 44-pin QFN package was mounted on a printed circuit board (PCB), and its pin assignment is shown in Fig. 4.14. Additionally, the chip was tested on the FR-4 evaluation board. The evaluation PCB, with a size of 15 cm $\times$ 10 cm, is shown in Fig. 4.15. In the board design, the power (VDD) and ground (GND) lines are separated between digital and analog to avoid signal interference. This chip has only an external crystal (XTAL) for the reference CLK. The XTAL is a Silicon Labs Si510 product. It provides a stable reference CLK of 150 kHz and has a stability of $\pm$25 ppm. This fabricated chip was evaluated through the LabVIEW-based test bench.

Figure 4.16 shows the measured MICS band channel selection results. The MICS band has 10 channels, and each channel's bandwidth is 300 kHz. In this ADPLL, XTAL at 150 kHz is used for a reference CLK. The channel is decided by changing the division ratio of the programmable frequency divider. Through the DSM technique in DCO, the fine frequency resolution is achieved. On



no	Pin Name	no	Pin Name	no	Pin Name	no	Pin Name
1	DCO output - outp	12	S/P divider - rst1	23	P/S output - psout1 (div)	34	S/P DSM - rst2
2	DCO output - outn	13	S/P divider - enb1	24	P/S output - psout2 (dsm)	35	Divider - rst_div
3	Analog VSS - gnd_a: 0V	14	S/P divider - clk1: 400M	25	XTAL - 150 kHz	36	Digital VSS - gnd_d: 0V
4	Analog VDD - vdd_a: 0.7V	15	S/P divider - in_div	26	VSS - 0V	37	Digital VSS - vdd_d: 0.7V
5	-	16	-	27	-	38	-
6	-	17	-	28	-	39	-
7	-	18	-	29	-	40	-
8	-	19	-	30	-	41	-
9	VDD - 0.7V	20	Divider - vdd_div: 0.7V	31	S/P DSM - in_dsm	42	t2
10	Divider - gnd_div: 0V	21	Divider - pw_rst	32	S/P DSM - clk2: 12.5M	43	t1
11	Divider - clkout	22	Divider - in_clk: 400M	33	S/P DSM - enb2	44	ADPLL output - adpll

Figure 4.14: Package pin assignments (44-pin QFN).

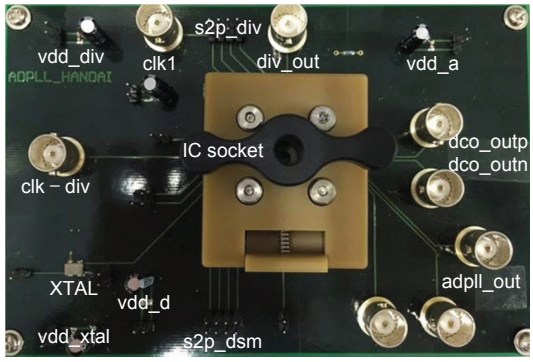


Figure 4.15: Evaluation PCB board (Size of 15 cm $\times$ 10 cm).

the basis of this resolution, it is possible to precisely select the MICS band channels. From the measured channel selection results, the fabricated ADPLL has a precise channel selection. In addition, it has a frequency stability of 0.45 kHz.

Figure 4.17 shows the output spectrum of the ADPLL. The measured reference spur is approximately -52 dBc at an offset frequency of 150 kHz from the carrier frequency; this obtained value is similar to those obtained in related studies. Because many medical applications typically operate in isolated and protected environments with relatively short communication distances, the requirement

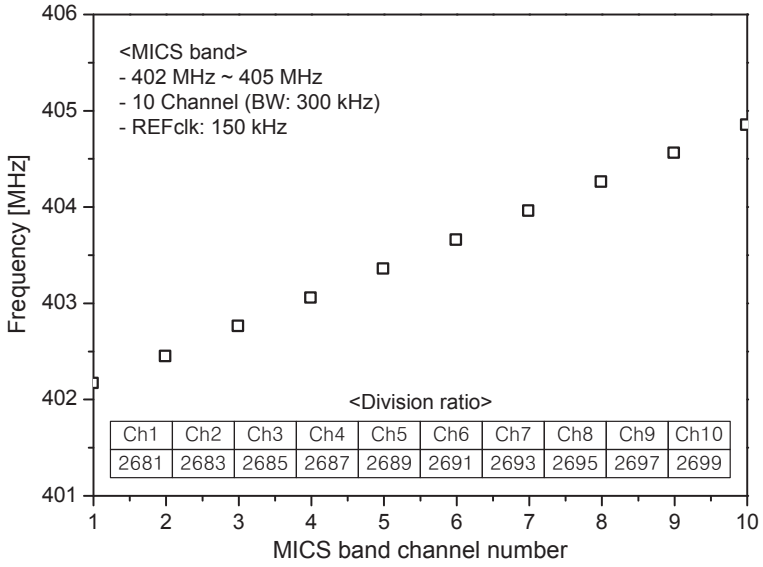


Figure 4.16: Measured MICS band channel selection.

for the reference spurs is less stringent than other requirements.

Figure 4.18 shows the measured phase noise of the ADPLL at an operating frequency of 405 MHz. Close-in phase noise depends on the PLL loop bandwidth, and far-out phase noise is dominated by the DCO. Digital blocks for frequency tuning introduce a spurious tone based on the quantization noise. A DWA spur of -120 dBc/Hz is generated at an offset frequency of 6.8 MHz. Furthermore, the DSM generates a spur at a large offset of 12.5 MHz, which is nearly equal to the clock frequency. However, the generated spur has no influence on the phase noise because it is generated at a large offset frequency outside of the MICS channel bandwidth. The measured phase noise at an offset frequency of 200 kHz is -114 dBc/Hz, which satisfies the MICS band requirement. The phase noise is suppressed at a loop bandwidth of less than approximately 15 kHz and has an in-band noise of -90 dBc/Hz.

Figure 4.19 shows the settling time response of the ADPLL from one locked state to another, which was taken from the integer tuning of the DCO. In this study, the phase selection scheme provides a pre-settled operation for the phase of the ADPLL output signal and thereby reduces the phase acquisition time. The settling time is approximately 80 μs with $\pm 1\%$ accuracy.

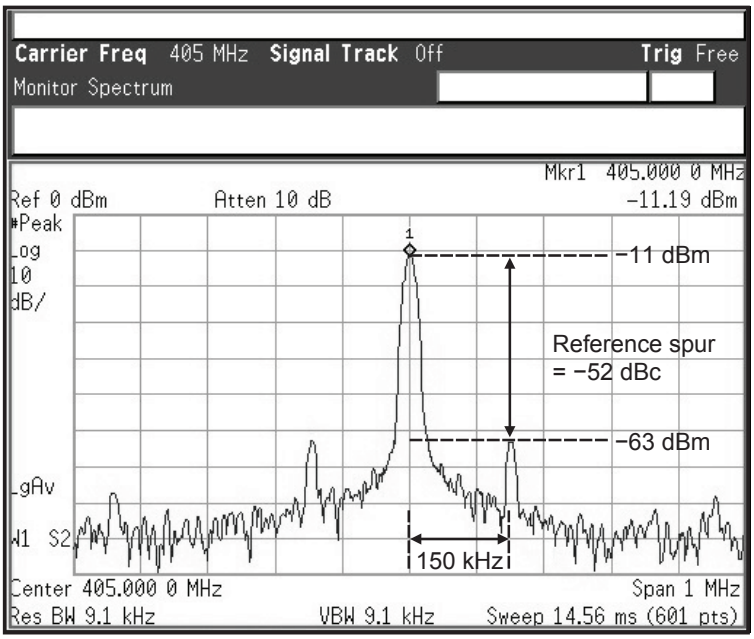


Figure 4.17: Measured output spectrum of the ADPLL.

Figures 4.20 and 4.21 show the measured power dissipation and phase noise for different supply voltages. The fabricated ADPLL has wide supply voltage compatibility (0.7–1.2 V). The supply voltage scaling provides reduction of power consumption. In Fig. 4.21, the phase noise becomes saturated at over 1.0-V supply voltage because the oscillation amplitude is limited by the bias current.

4.4.2 Comparison and Discussion

To evaluate the fabricated ADPLL through this study, the well-known figure-of-merits (FoMs) are employed [19]:

$$\text{FoM} = L\{\Delta f\}\,[\text{dBc/Hz}] - 20\log_{10}\frac{f_c}{\Delta f} + 10\log_{10}\left(\frac{P_{diss}}{1\text{ mW}}\right), \tag{4.14}$$

$$\text{FoM}_\text{A} = \text{FoM} + 10\log_{10}\left(\frac{\text{Area}}{1\text{ mm}^2}\right), \tag{4.15}$$

where $L\{\Delta f\}$ is the phase noise at an offset frequency of Δf, f_c is the oscillation frequency, P_{diss} is the power dissipation, and area is the overall chip size. The FoMs are normalized at an offset fre-

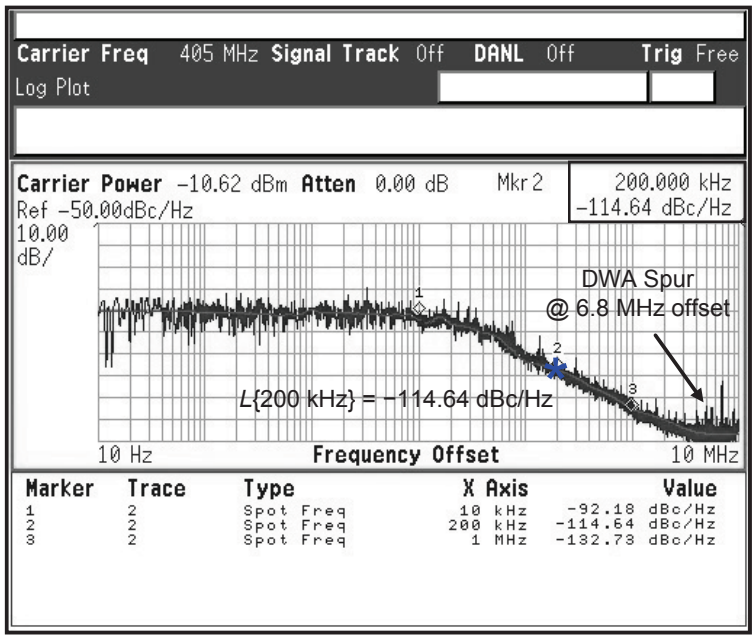


Figure 4.18: Measured phase noise of the ADPLL.

quency Δf. Table 4.3 summarizes the measured performance of the proposed ADPLL and compares this device with other PLLs in the MICS frequency band that have been reported in the literature. In comparison with the devices in the related works, the proposed ADPLL demonstrates better phase noise performance and faster settling time. Low phase noise is realized by weak-inversion operation and a resistive biasing technique. The wide frequency tuning range is achieved through the switchable capacitor bank controlled by digital logic blocks. The DSM is adopted to achieve precise frequency resolution with a small number of capacitors. Additionally, the ADPLL is rapidly settled through phase selection with the PI.

With regard to power consumption, the fabricated ADPLL has more power dissipation than [20,21] because the DCO core consumes most of the power; its detailed description is dealt with in the DCO discussion of Section 3.5.3. The power consumption of digital circuits is decreased by supply voltage scaling as shown in Fig. 4.20, and thus digital-based circuits may have reduced dynamic power consumption by voltage scaling. Because this ADPLL is almost digital-based circuits, it has

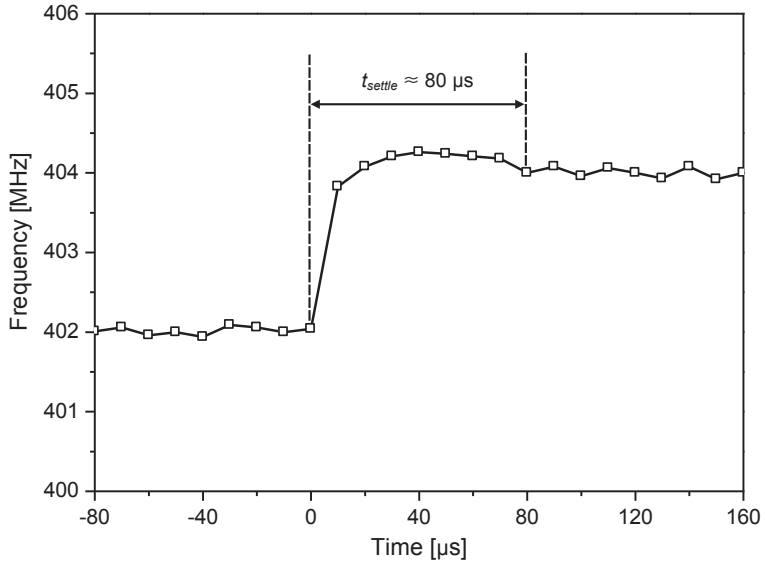


Figure 4.19: Measured settling time of the ADPLL.

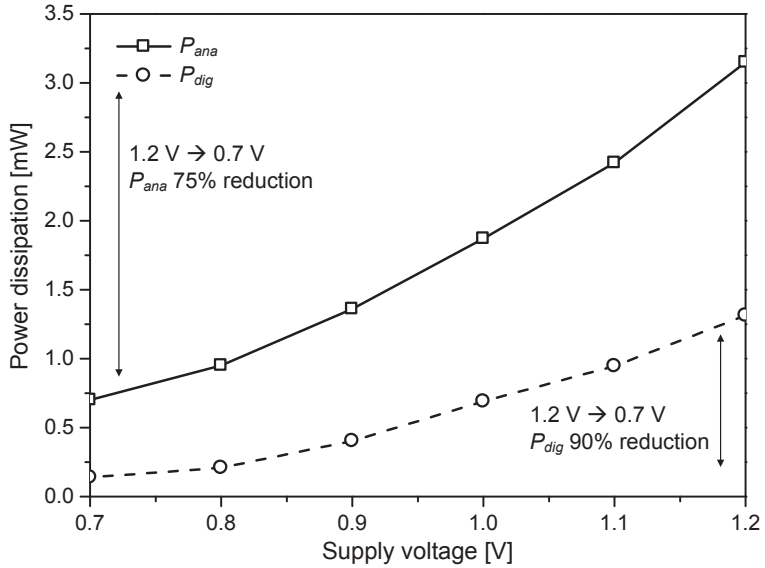


Figure 4.20: Measured power dissipation of each part for different supply voltages.

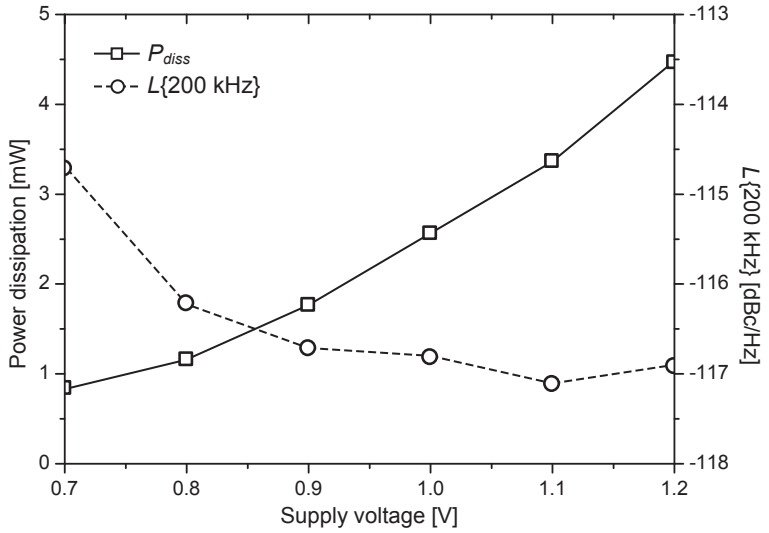


Figure 4.21: Measured power dissipation and phase noise for different supply voltages.

the possibility of reduced power consumption by decreasing the supply voltage. If V_{DD} is decreased to 0.5 V, the dynamic power of digital blocks may be reduced by approximately 40%. With regard to chip area, this ADPLL has a similar or smaller area compared with the same LC-based topology studies in [20, 22]. However, compared with the ring oscillator studies in [21, 23], it occupies quite a large area. Generally, an LC-based oscillator has a much larger size than a ring oscillator as a cost of having better phase noise performance. The oscillator topology may be selected according to the target application. In this study, the LC-based oscillator is used to achieve good phase noise performance. By optimizing the integrated inductor, the size may be decreased. This area result satisfies the medical implantable devices requirement as described in Section 1.1. In addition, most of the ADPLL blocks are implemented on the basis of digitally intensive circuits. Therefore, it has good compatibility with different processes and supply voltages.

To sum up, the fabricated ADPLL satisfies all MICS band requirements, has the best FoMs according to the design techniques introduced in this study, and is controlled in a fully digital manner. It also provides the feasibility of low-voltage and high-performance design for adoption in biomedical RF transceivers.

Table 4.3: Measured Performance and Comparison of MICS Band PLLs

	This Work	[20]	[22]	[21]	[23]
CMOS Technology	130-nm	65-nm	130-nm	130-nm	180-nm
Supply [V]	0.7	1.0	1.2	0.5	1.8
PLL Type	Integer-N	Integer-N	Integer-N	Integer-N	Fractional-N
Oscillator Type	LC-DCO	LC-VCO	LC-VCO	Ring Oscillator	Ring Oscillator
Frequency [MHz]	382∼412	400∼405	640∼650	400∼433	400∼410
Phase Noise [dBc/Hz]	−114 @ 200 kHz	−102 @ 200 kHz	−99 @ 100 kHz	−92 @ 1 MHz	−84 @ 300 kHz
Settling Time [μs]	80	350	500	90	110
Reference Spur [dBc]	−52	−45	−52	−38	−55
Area [mm^2]	0.64	0.54	1.0	0.072	0.135
Power [μW]	840	430	1200	440	1260
FoM [dBc/Hz]	−181.4	−171.8	−174.4	−147.5	−145.2
FoM_A [dBc/Hz]	−185.8	−177.9	−174.4	−173.8	−165.2

4.5 Conclusion

A low-complexity ADPLL architecture for biomedical RF transceivers is presented. General TDC-based ADPLLs require advanced CMOS technology and additional system complexity to achieve high resolution and thereby have high power consumption. In addition, such high sensitivity can cause poor linearity and non-uniform phase detector gain, resulting in widespread spur generation. In this study, a TDC-less controller-based architecture is employed for a low-complexity ADPLL.

In addition, a phase selection scheme is used to decrease the phase acquisition time. It provides fast settling operation of the ADPLL output signals. Through the phase domain modeling analysis, it is confirmed that this architecture performs the PLL functionality. That functionality was validated through behavior model simulations. In the circuit implementation, it was designed with a focus on low-voltage operation. For low-voltage operation and high performance, a TSPC DFF-based PDF and controller are used to generate the digital control words. The controller is implemented through logic synthesis using the standard cell library. In addition, passive-type PPF and PI are used for low power consumption. The ADPLL circuits were implemented with a 130-nm CMOS process for a 0.7-V supply voltage. Digital circuits were synthesized and implemented by using the standard cell library. The controller-based ADPLL has good compatibility between performance and complexity. Therefore, this ADPLL architecture is most suitable for low-voltage biomedical RF transceivers.

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Chapter 5

Conclusion

In this dissertation, a low-voltage and fully integrated ADPLL for biomedical RF transceivers was presented and demonstrated.

Chapter 1 described the purpose of this study. It gave some basic theory for better understanding of this study; the motivation and structure of the dissertation were also presented.

Chapter 2 demonstrated the phase noise reduction technique in oscillator design for low-voltage operation. Phase noise is a key parameter for RF oscillators, which demand low phase noise for better spectral purity. In typical oscillators, the current source contribution dominates other sources of phase noise. Therefore, in this chapter, the phase noise by current biasing techniques was analyzed, and the design feasibility was confirmed through the circuit implementation of a low-voltage LC-VCO with the resistive biasing technique. Through the phase noise analysis by various current biasing techniques, the resistive biasing has the least effective noise power because of the elimination of the noisy MOS current source, and top position basing has a large output swing because it has no current degradation. As a result, the top resistive biasing technique realizes good phase noise performance in low-voltage operation. The designed LC-VCO using top resistive biasing operated from 398 MHz to 408 MHz and exhibited a phase noise of -116 dBc/Hz at an offset frequency of 200 kHz with an improvement of 1 dB to 6 dB compared to other biasing techniques at similar conditions. From this study, it has been demonstrated that the top resistive biasing provides a good phase noise performance, and is more suitable to low-voltage oscillator designs.

Chapter 3 demonstrated the low-voltage delta-sigma DCO for MICS band applications. In low-voltage and deep-submicron CMOS technology, analog type frequency tuning using a varactor is

quite a challenging task because of its highly nonlinear characteristics. Therefore, digital frequency tuning with a switchable capacitor bank provides a large frequency tuning range. In this study, the oscillation frequency was controlled in a fully digital manner through the digital logic blocks. The precise frequency was achieved by using DSM, and it was realized by using a small number of capacitors. In addition, capacitor mismatch was decreased through the DEM technique. Through the control of digital logic blocks, a large frequency tuning range with precise resolution was achieved within low complexity. The DCO core was optimized by the g_m/I_D methodology for low-voltage operation, and the resistive biasing technique was employed for its advantage of low phase noise. The DCO was fabricated in a 130-nm CMOS process for a 0.7-V supply voltage and evaluated through an FPGA-based test bench. Digital logic blocks were implemented on the basis of the standard cell library. The fabricated DCO had an active area of 0.41 mm^2, and consumed 700 μW. The DCO chip achieved a phase noise of -115 dBc/Hz at an offset frequency of 200 kHz with the tuning range of 382 MHz to 412 MHz for the MICS band. It had a high frequency resolution of 18 kHz. Measured results satisfy the MICS band requirements and had the best FoMs compared with those of related studies. This study confirmed that the fabricated DCO operates in fully digital control and provides good performance. In addition, it provides a solution for achieving precise frequency resolution in RF oscillator design.

Chapter 4 demonstrated the low-voltage and low-complexity fully integrated ADPLL for biomedical RF transceivers. General TDC-based ADPLLs demand an advanced CMOS technology and additional system complexity to achieve high resolution, thus causing large power consumption. In this study, a TDC-less controller-based architecture was employed for low-complexity ADPLL. In addition, to improve the output phase acquisition, the phase selection schemes combined by PS and PI were applied, which provided pre-settled operation. Through the phase domain modeling analysis, it was confirmed that this architecture performs the PLL functionality, and its functionality was further validated through the behavior model simulations. In the circuit implementation, the device was designed with a focus on low-voltage operation. For low-voltage and high-performance operation, a TSPC DFFs-based PDF and controller were used to generate the digital control words. The passive type PPF and PI were used for generating the 64-phase reference signal. Controller was implemented through the logic synthesis using the standard cell library. Digital circuits were synthesized and implemented by using the standard cell library. The designed ADPLL was fabricated

in a 130-nm CMOS process for a 0.7-V supply voltage. The fabricated ADPLL is controlled in a fully digital manner, and all target specifications were based on the MICS band requirements. The fabricated ADPLL has an active area of 0.64 mm^2. During operation, the total power consumption of the fabricated ADPLL was 840 μW. In this study, an FPGA-based test bench was used to evaluate the chip performance. The ADPLL had a settling time of 80 μs and phase noise of -114 dBc/Hz at an offset frequency of 200 kHz. In addition, it had precise channel selection based on the high-frequency resolution from the delta-sigma DCO. Through the chip evaluation, it was demonstrated that the fabricated ADPLL satisfies all MICS band requirements and shows better performance compared with those of related studies. It is compatible with the CMOS process and supply voltage, and thus can be utilized various fields that require high-performance fully integrated RF transceivers in low-voltage deep-submicron CMOS technology.

In summary, a low-voltage fully integrated ADPLL for supporting biomedical RF transceivers was achieved. It was realized through the low-voltage design methodology and proposed techniques. Low phase noise was achieved by top resistive biasing as shown in Chapter 2. Wide tuning range with precise frequency resolution was achieved by fully digital tuning logic as shown in Chapter 3. Fast settling time was achieved by phase selection schemes based on the controller logic as shown in Chapter 4. From the chip evaluation, it was confirmed that the fabricated DCO and ADPLL satisfy the MICS band requirements and exhibit good performance as shown in Chapters 3 and 4. Biomedical devices are an emerging market, and will be more attractive in the future. This trend demands fully integrated high-performance devices. This study demonstrated the feasibility of a 0.7-V fully integrated ADPLL controlled in a digital manner with high performance. In addition, because of the implementation of the digitally intensive approach, it is compatible with the CMOS process and supply voltage and thus can be utilized in various applications. The presented circuit techniques for ADPLL contribute to the design of low-voltage and low-complexity CMOS RF transceivers.

Appendix A

Verilog HDL Codes: Delta-Sigma DCO

A.1 3rd-Order DSM

```
//Verilog HDL for “ds_ dco”, “Delta_sigma_3rd” “functional”
module Delta_sigma_3rd(clk,reset,In,Out);
input clk,reset; input signed [9:0] In; // Signed 10-bit(sign:1-bit,integer:2-bit,fractional:7-bit)
output signed [2:0] Out; parameter [1:0] Gain2_gainparam = 2’b11;
wire signed [2:0] Data_Type_Conversion_out1; wire signed [9:0] Gain4_out1;
reg signed [9:0] Unit_Delay1_out1; wire signed [9:0] Sum_out1;
reg signed [9:0] Unit_Delay2_out1; wire signed [9:0] Sum1_out1;
reg signed [9:0] Unit_Delay3_out1; wire signed [9:0] Sum2_out1;
wire signed [9:0] Gain3_out1; wire signed [9:0] Gain2_out1; wire signed [9:0] Gain1_out1;
wire signed [9:0] Sum3_out1; wire signed [3:0] unaryminus_temp; wire signed [9:0] sum_1;
wire signed [10:0] add_temp; wire signed [10:0] add_temp_1; wire signed [10:0] add_temp_2;
wire signed [10:0] add_temp_3; wire signed [12:0] mul_temp; wire signed [9:0] sum_1_1;
wire signed [10:0] add_temp_4; wire signed [10:0] add_temp_5;
assign unaryminus_temp = (Data_Type_Conversion_out1==3’b100) ?
$signed({1’b0, Data_Type_Conversion_out1}) : -Data_Type_Conversion_out1;
assign Gain4_out1 = $signed({unaryminus_temp[2:0], 7’b0000000});
assign add_temp = In + Gain4_out1; assign sum_1 = add_temp[9:0];
always @ (posedge clk or posedge reset)
```

```
begin: Unit_Delay1_process
if (reset) begin Unit_Delay1_out1 <= 0; end
else begin if (clk) begin Unit_Delay1_out1 <= Sum_out1; end end
end // Unit_Delay1_process
assign add_temp_1 = sum_1 + Unit_Delay1_out1; assign Sum_out1 = add_temp_1[9:0];
always @ (posedge clk or posedge reset)
begin: Unit_Delay2_process
if (reset) begin Unit_Delay2_out1 <= 0; end
else begin if (clk) begin Unit_Delay2_out1 <= Sum1_out1; end end
end // Unit_Delay2_process
assign add_temp_2 = Unit_Delay1_out1 + Unit_Delay2_out1; assign Sum1_out1 = add_temp_2[9:0];
always @ (posedge clk or posedge reset)
begin: Unit_Delay3_process
if (reset) begin Unit_Delay3_out1 <= 0; end
else begin if (clk) begin Unit_Delay3_out1 <= Sum2_out1; end end
end // Unit_Delay3_process
assign add_temp_3 = Unit_Delay2_out1 + Unit_Delay3_out1;
assign Sum2_out1 = add_temp_3[9:0];
assign Gain3_out1 = $signed({{1{Unit_Delay3_out1[9] }}, Unit_Delay3_out1[9:1] });
assign mul_temp = Unit_Delay2_out1 * $signed({1'b0, Gain2_gainparam });
assign Gain2_out1 = mul_temp[10:1];
assign Gain1_out1 = $signed({Unit_Delay1_out1[8:0], 1'b0});
assign add_temp_4 = Gain3_out1 + Gain2_out1;
assign sum_1_1 = add_temp_4[9:0];
assign add_temp_5 = sum_1_1 + Gain1_out1;
assign Sum3_out1 = add_temp_5[9:0];
assign Data_Type_Conversion_out1 = Sum3_out1[9:7];
assign Out = Data_Type_Conversion_out1;
endmodule
```

A.2 Dynamic Element Matching

A.2.1 DWA/CLA Integration

```
//Verilog HDL for "ds_dco", "DWA_integration" "functional"
module DWA_integration(clk,reset,In,Out_to_Compare,Out_to_Therm1,Out_to_Therm2);
input clk,reset; input [3:0] In; output Out_to_Compare;
output [3:0] Out_to_Therm1; output [3:0] Out_to_Therm2; wire [3:0] Extract_Bits_out1;
reg [3:0] Unit_Delay2_out1; wire [4:0] Sum1_out1;
wire Compare_To_Constant_out1; reg [3:0] add_cast;
always @(posedge clk or posedge reset)
begin : Unit_Delay2_process
if (reset) begin Unit_Delay2_out1 <= 0; end
else begin if (clk) begin Unit_Delay2_out1 <= Extract_Bits_out1; end end
add_cast <= In; end
assign Sum1_out1 = add_cast + Unit_Delay2_out1; assign Extract_Bits_out1 = Sum1_out1[3:0];
assign Compare_To_Constant_out1 = (Sum1_out1 >= 5'b10000) ? 1'b1 : 1'b0;
assign Out_to_Therm1 = Extract_Bits_out1; assign Out_to_Therm2 = Unit_Delay2_out1;
assign Out_to_Compare = Compare_To_Constant_out1;
endmodule

//Verilog HDL for "ds_dco", "CLA_integration" "functional"
module CLA_integration(clk,reset,In,Out_to_Compare,Out_to_Therm1,Out_to_Therm2);
input clk,reset; input [3:0] In; output Out_to_Compare;
output [3:0] Out_to_Therm1; output [3:0] Out_to_Therm2;
wire [3:0] Extract_Bits_out1; wire [3:0] Extract_Bits_out2;
reg [3:0] Unit_Delay2_out2; wire [3:0] Sum1_out1; reg [3:0] Sum1_out2;
reg [3:0] Sum1_out3; wire [4:0] Sum1_out4; wire Compare_To_Constant_out1;
always @(posedge clk or posedge reset)
begin : Unit_Delay2_process
if (reset) begin Sum1_out2 <= 0; Sum1_out3 <= 0; Unit_Delay2_out2 <= 0; end
```

```
else begin Unit_Delay2_out2 <= (Unit_Delay2_out2 + 1) % 16;
Sum1_out2 <= Unit_Delay2_out2; Sum1_out3 <= In; end end
assign Sum1_out1 = Sum1_out2 + Sum1_out3; assign Sum1_out4 = Sum1_out2 + Sum1_out3;
assign Compare_To_Constant_out1 = (Sum1_out4 >= 5'b10000) ? 1'b1 : 1'b0;
assign Extract_Bits_out1 = Sum1_out1; assign Extract_Bits_out2 = Sum1_out2;
assign Out_to_Therm1 = Extract_Bits_out1; assign Out_to_Therm2 = Extract_Bits_out2;
assign Out_to_Compare = Compare_To_Constant_out1;
endmodule
```

A.2.2 Bitwise AND/OR

```
//Verilog HDL for "ds_dco", "Bitwise_AND" "functional"
module Bitwise_AND(In1,In2,Out);
input [14:0] In1; input [14:0] In2; output [14:0] Out;
assign Out[0] = In1[0] & In2[0]; assign Out[1] = In1[1] & In2[1];
assign Out[2] = In1[2] & In2[2]; assign Out[3] = In1[3] & In2[3];
assign Out[4] = In1[4] & In2[4]; assign Out[5] = In1[5] & In2[5];
assign Out[6] = In1[6] & In2[6]; assign Out[7] = In1[7] & In2[7];
assign Out[8] = In1[8] & In2[8]; assign Out[9] = In1[9] & In2[9];
assign Out[10] = In1[10] & In2[10]; assign Out[11] = In1[11] & In2[11];
assign Out[12] = In1[12] & In2[12]; assign Out[13] = In1[13] & In2[13];
assign Out[14] = In1[14] & In2[14];
endmodule

//Verilog HDL for "ds_dco", "Bitwise_OR" "functional"
module Bitwise_OR(In1,In2,Out );
input [14:0] In1; input [14:0] In2; output [14:0] Out;
assign Out[0] = In1[0] | In2[0]; assign Out[1] = In1[1] | In2[1];
assign Out[2] = In1[2] | In2[2]; assign Out[3] = In1[3] | In2[3];
assign Out[4] = In1[4] | In2[4]; assign Out[5] = In1[5] | In2[5];
assign Out[6] = In1[6] | In2[6]; assign Out[7] = In1[7] | In2[7];
```

```
assign Out[8] = In1[8] | In2[8]; assign Out[9] = In1[9] | In2[9];
assign Out[10] = In1[10] | In2[10]; assign Out[11] = In1[11] | In2[11];
assign Out[12] = In1[12] | In2[12]; assign Out[13] = In1[13] | In2[13];
assign Out[14] = In1[14] | In2[14];
endmodule
```

A.2.3 DEM Switch

```
//Verilog HDL for "ds_dco", "DEM_switch" "functional"
module DWA_switch(Compare_To_Constant_out1,Bitwise_or_out,Bitwise_and_out,Switch_out1);
input Compare_To_Constant_out1; input [14:0] Bitwise_or_out;
input [14:0] Bitwise_and_out; output [15:0] Switch_out1;
assign Switch_out1[0]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[0]:Bitwise_and_out[0];
assign Switch_out1[1]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[1]:Bitwise_and_out[1];
assign Switch_out1[2]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[2]:Bitwise_and_out[2];
assign Switch_out1[3]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[3]:Bitwise_and_out[3];
assign Switch_out1[4]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[4]:Bitwise_and_out[4];
assign Switch_out1[5]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[5]:Bitwise_and_out[5];
assign Switch_out1[6]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[6]:Bitwise_and_out[6];
assign Switch_out1[7]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[7]:Bitwise_and_out[7];
assign Switch_out1[8]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[8]:Bitwise_and_out[8];
assign Switch_out1[9]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[9]:Bitwise_and_out[9];
assign Switch_out1[10]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[10]:Bitwise_and_out[10];
assign Switch_out1[11]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[11]:Bitwise_and_out[11];
assign Switch_out1[12]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[12]:Bitwise_and_out[12];
assign Switch_out1[13]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[13]:Bitwise_and_out[13];
assign Switch_out1[14]=(Compare_To_Constant_out1==1'b1)?Bitwise_or_out[14]:Bitwise_and_out[14];
assign Switch_out1[15]=Compare_To_Constant_out1;
endmodule
```

A.2.4 Row/Column Coder

```
//Verilog HDL for “ds_dco”, “Row_coder” “functional”
module Row_coder(In,Out);
input [1:0] In; output [2:0] Out; reg [2:0] Combinatorial_Logic;
always @(In) begin case (In)
2’b00: Combinatorial_Logic <= 3’b000; 2’b01: Combinatorial_Logic <= 3’b001;
2’b10: Combinatorial_Logic <= 3’b011; 2’b11: Combinatorial_Logic <= 3’b111;
endcase end
assign Out = Combinatorial_Logic;
endmodule

//Verilog HDL for “ds_dco”, “Column_coder” “functional”
module Column_coder(In,Out);
input [1:0] In; output [2:0] Out; reg [2:0] Combinatorial_Logic;
always @(In) begin case (In)
2’b00: Combinatorial_Logic <= 3’b000; 2’b01: Combinatorial_Logic <= 3’b001;
2’b10: Combinatorial_Logic <= 3’b011; 2’b11: Combinatorial_Logic <= 3’b111;
endcase end
assign Out = Combinatorial_Logic;
endmodule
```

A.2.5 Thermometer Coder Element

```
//Thermometer coder is configured using the thermometer coder element module, as shown in Fig. 3.10.
//Verilog HDL for “ds_dco”, “Thermometer_element” “functional”
module Thermometer_element(X,Y,Z,Out);
input X,Y,Z; output Out; wire Logical_Operator1; wire Logical_Operator2;
assign Logical_Operator1 = X | Y;
assign Logical_Operator2 = Z & Logical_Operator1;
assign Out = Logical_Operator2;
endmodule
```

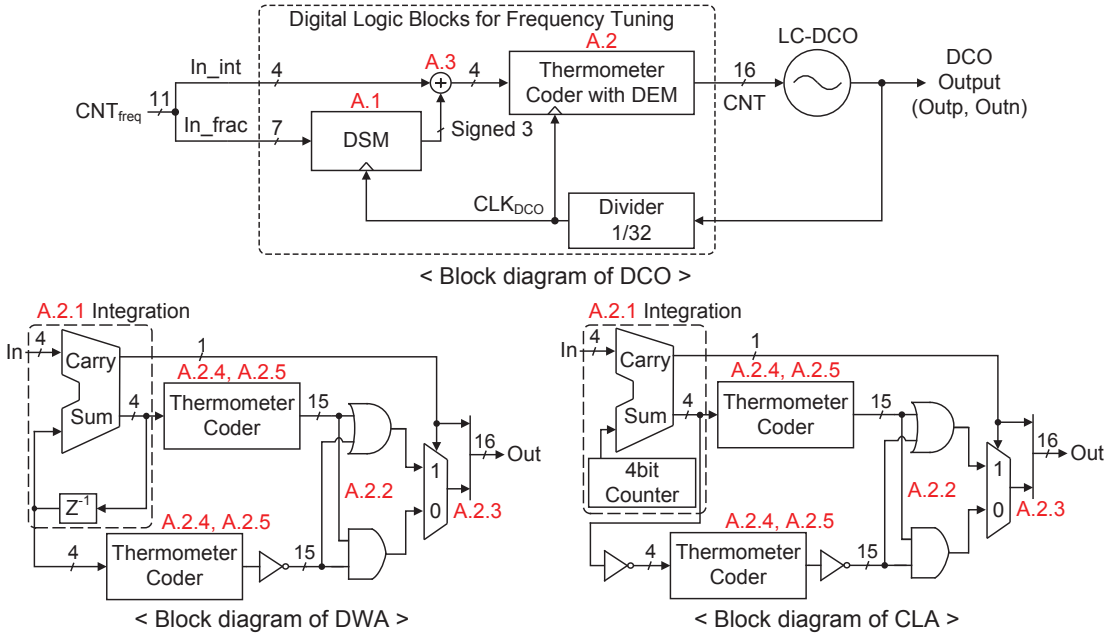

Figure A.1: Block diagram of digital logic blocks for DCO corresponding to Appendix codes.

A.3 Adder

```
//Verilog HDL for “ds_dco”, “Adder_4bit_3bit” “functional”
module Adder_4bit_3bit(clk,reset,In_fr_int,In_fr_ds,Out,co);
input clk; input reset; input [3:0] In_fr_int; input [2:0] In_fr_ds;
output [3:0] Out; output co; reg [3:0] Out; reg co;
always @(posedge clk or posedge reset)
begin if(reset) begin Out <= 0; end
else begin if(clk) begin if (In_fr_ds ==3’b111) begin Out <= In_fr_int - 4’b0001; end
else begin co,Out <= In_fr_int + In_fr_ds ; end end end
end
endmodule
```

Appendix B

Verilog HDL Codes: ADPLL

B.1 Controller

```
//Verilog HDL for “adpll”, “Controller” “functional”
module Controller(up,dn,clk,out,PI);
input up,dn,clk; output [13:0] out; reg [13:0] temp; output [5:0] PI; reg [5:0] PI_temp;
integer flag_ave,flag,flag_PI; integer temp_up,temp_dn;
always @(posedge clk) begin if(up == 1’b1) temp_up=1; else temp_up=0;
if(dn == 1’b1) temp_dn=1; else temp_dn=0; flag=flag-temp_up+temp_dn; flag_ave=flag/64; flag_PI=flag%64;
case(flag_ave)
-832:temp <= 14’b00010000000000;
-831:temp <= 14’b00010000000001;
-830:temp <= 14’b00010000000010;
. . .
830:temp <= 14’b11010001111110;
831:temp <= 14’b11010001111111;
endcase end
assign out = temp;
case(flag_PI)
-32:PI_temp <= 6’b111111;
-31:PI_temp <= 6’b111110;
```

```
-30:PI_temp <= 6'b111101;
...
30:PI_temp <= 6'b000001;
31:PI_temp <= 6'b000000;
endcase end
assign PI = PI_temp;
endmodule
```

B.2 Phase Selector

```
//Verilog HDL for "adpll", "Phase_selector" "functional"
module Phase_selector(in,cnt,out);
input [63:0] in; input [5:0] cnt; output out; reg [63:0] in_t; reg out_t;
integer flag0,flag1,flag2,flag3,flag4,flag5,temp;
always @ * begin
if(cnt[0] == 1'b1) flag0=1; else flag0=0; if(cnt[1] == 1'b1) flag1=1; else flag1=0;
if(cnt[2] == 1'b1) flag2=1; else flag2=0; if(cnt[3] == 1'b1) flag3=1; else flag3=0;
if(cnt[4] == 1'b1) flag4=1; else flag4=0; if(cnt[5] == 1'b1) flag5=1; else flag5=0;
temp=flag0+flag1*2+flag2*4+flag3*8+flag4*16+flag5*32; in_t = in;
case (temp)
0:out_t = in_t[0];
1:out_t = in_t[1];
2:out_t = in_t[2];
...
62:out_t = in_t[62];
63:out_t = in_t[63];
endcase end
assign out = out_t;
endmodule
```

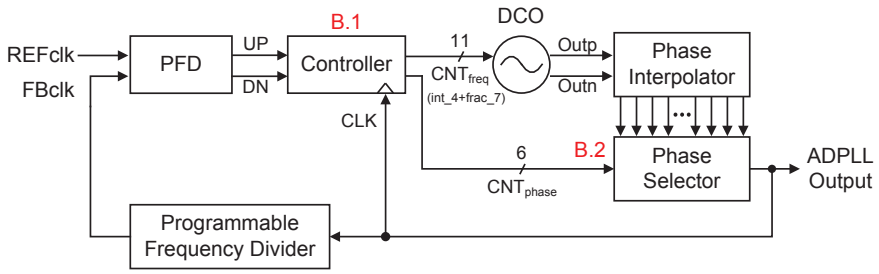

Figure B.1: Block diagram of digital logic blocks for ADPLL corresponding to Appendix codes.

B.3 Serial-to-Parallel Converter

//This is a block for chip test bench, as shown in Fig. 3.20.
//Verilog HDL for “chip_test”, “s2p_15” “functional”
module s2p_15(si,clk,rst,en,q1,q2);
input si,clk,rst,en; output [14:0] q1,q2; reg [14:0] q1,q2;
always @(posedge clk) begin if (rst == 1’b0) q1 <= 14’h00; else if (en == 1’b1) q1 <= q1[14:0], si;
if (rst == 1’b0) q2 <= 14’h00; else if (en == 1’b1) q2 <= q2[14:0], si; end
endmodule

//Verilog HDL for “chip_test”, “p2s_15” “functional”
module p2s_15(d,clk,rst,ld,so); input [14:0] d; input clk,rst,ld; output so; reg [14:0] q;
always @(posedge clk) begin if (rst == 1’b0) q <= 15’h000; else if (ld == 1’b1) q <= d;
else q <= q[13:0], 1’b0; end assign so = q[14];
endmodule

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5. Saichandrateja Radhapuram, Jungnam Bae, Ikkyun Jo, Weimin Wang, and Toshimasa Matsuoka, "Analysis of a controller-based all-digital phase-locked loop," *Far East Journal of Electronics and Communications*, vol. 15, no. 1, pp. 57-73, Sep. 2015.

DOI:10.17654/FJECSep2015_057_073
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DOI:10.1587/transele.E98.C.1179

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DOI:10.1109/RFIT.2015.7377929

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