Resistance modulation by strongly correlated oxide transistor with high-*k* Ta_2O_5/organic parylene-C hybrid gate insulator

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SEPTEMBER 2016

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A dissertation submitted to

THE GRADUATE SCHOOL OF ENGINEERING SCIENCE

OSAKA UNIVERSITY

in partial fulfillment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY IN SCIENCE

BY

TINGTING WEI

SEPTEMBER 2016

Thesis advisor Author

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Abstract

As one of the most promising candidates for next generation electronics, strongly correlated oxide, vanadium dioxide VO_2, has drawn widespread concerns due to their intriguing features, which exhibits drastic metal-insulator transition (MIT) in the vicinity of room temperature with four orders of magnitude in resistance variation. Field-triggered electrical transport modulation utilizing a three-terminal field-effect transistor device facilitates the research on control of MIT functionality, and provides the potential for exploiting novel devices based on strongly correlated oxides.

In this thesis, I have investigated the electronic transport modulation properties in VO_2 films and nanowires by applying an electric field utilizing a hybrid solid gate insulator consisting of inorganic high-*k* oxide Ta_2O_5 and organic polymer material parylene-C, which provides less effects of lattice defects at gate/channel interface and sufficient carrier doping.

My achievements are listed as follows:

(1) I successfully fabricated a hybrid gate insulator to verify the series connection mode of capacitors in this structure. Through being applied to the band semiconductor $KTaO_3$, the hybrid gate dielectric was demonstrated to possess outstanding characteristics: excellent gate/channel interface due to the suppression of formation of oxygen vacancies and charge trapping levels, providing higher breakdown fields, and giant induced carrier density to sufficient electrostatic modulation resulting from the high effective dielectric constant compared with only parylene-C gate insulator.

(2) I achieved electrostatic effect tailoring reversible and prompt resistance switch in VO_2 thin films *via* hybrid gate insulator. Moreover, I observed the maximum resistance modulation occurred near the transition temperature. Simultaneously, I clarified that five-fold higher resistance change (～0.6%) induced by hybrid gate insulator rather than parylene-monolayer gate originated from the promoted carrier density. Additionally, I obtained a pronounced shift of transition temperature by applying positive/negative gate bias.

(3) I further enhanced sensitivity in resistance modulation through decreasing the channel scale close to nanometer scale size (100 nm) in the nanowire-based field-effect transistors (FETs) constructed by nanoimprint lithography. I accessed the enhanced maximum resistance modulation (～8.6%) near transition temperature. This value was ten-fold higher than that in VO_2 film-based devices. Such enhancement in resistance modulation was well explained by the giant mobility modulation in the edge part of nanowire-based FETs. Even though the stronger field strength (1.5 folds stronger) distributed in the edge part yielded little enhancement of carrier density, it would make the mobility enhance logarithmically on the basis of Brinkman-Rice picture for correlated system. The achieved transport modulation ratio in nanowire-based FETs is the highest one in the all-solid-gated devices so far.

This research provides a new avenue for pure electrostatic modulation in strongly correlated oxides, and simultaneously supplies potential possibilities for exploiting nano-devices based on strongly correlated oxides for next generation electronics.

CONTENTS

CHAPTER 1

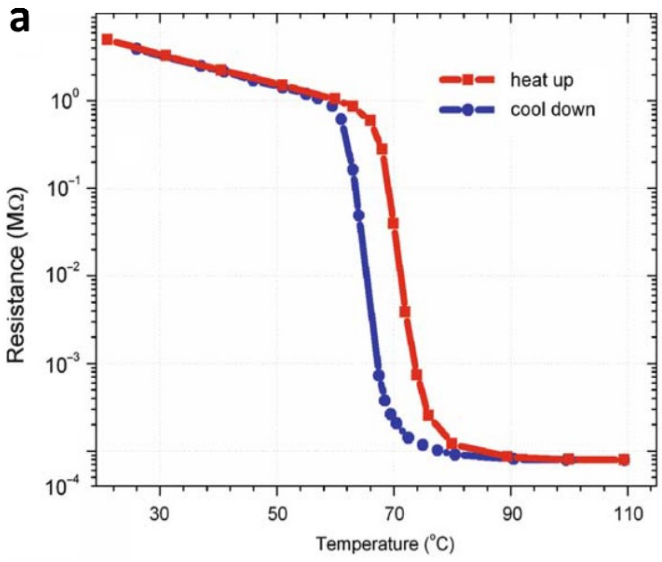
General introduction

1.1 Strongly correlated oxide vanadium dioxide

Over 10^{18} of MOSFETs have been manufactured every year, which are ubiquitous as the most common electronic devices in our life [1]. Recently, the development of electronics industry has been hampered by miniaturization. According to the Moore's Law, the gate length of MOSFET has a logarithmic scaling because of the limit carriers in conventional semiconductors [2-4]. In order to breakthrough this problem, a number of recent efforts have been devoted to probe new replacements for silicon devices [5-8]. As one of the most promising candidates, strongly correlated materials have drawn much attention. A slight perturbation would induce electronic phase transition due to change of strong electron-electron repulsive interactions in this system. The consequence is the fascinating phenomena, such as high-temperature superconductivity [9-10], colossal magneto-resistance (CMR) [11-12], metal-insulator transition (MIT) [13-14], etc. Such system cannot be explained well by conventional free electron band theory. Therefore, many attempts have been performed to reveal the fundamental nature of strongly correlated system. In addition, the study on strongly correlated system is inevitably regarded as the most important part in condensed matter physics.

Vanadium dioxide (VO_2) is one of the standard materials among the strongly

correlated materials, which has attracted widespread concerns due to the many intriguing features. It is well known that not only possesses drastic metal-insulator transition behavior in the vicinity of room temperature 340 K in bulk crystals, but also exhibits four orders of magnitude in resistance change [15-17]. Figure 1.1 a. shows the electrical resistance of a VO_2 thin film. This transition is a first-order phase transition accompanied by a structural change from high-temperature tetragonal lattice with half-filled conduction band to low-temperature monoclinic structure with a band gap of e_g = 0.6 eV [18-19] as plotted in Figure 1.1 b.



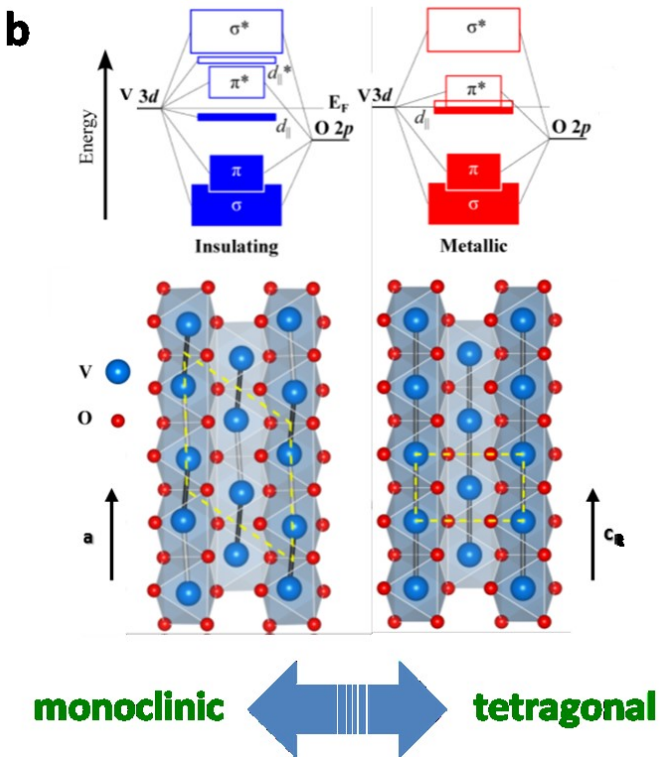


Figure 1.1 (a) MIT property in a typical VO_2 thin film [20]; **(b)** The corresponding monoclinic (M1) in insulating state and rutile (R) lattice in metallic state. The unit cells are shown (dashed yellow lines) to indicate the effective doubling of the M1 cell compared to the R phase [19].

Otherwise, the timescales of optical switching upon transition is typically picosecond or faster [21-22]. These abundant characteristics make VO_2 suitable for practical applications in various fields such as smart windows [23], switches [24], memory [25], infrared detectors [26], and thermal sensors [27]. Among the numerous applications of VO_2, a field-triggered phase transition near room temperature provides the potential for novel electronics. The earliest research on field-driven MIT can be traced back to the early 1970s [28]. The continuous resistance switching behavior was

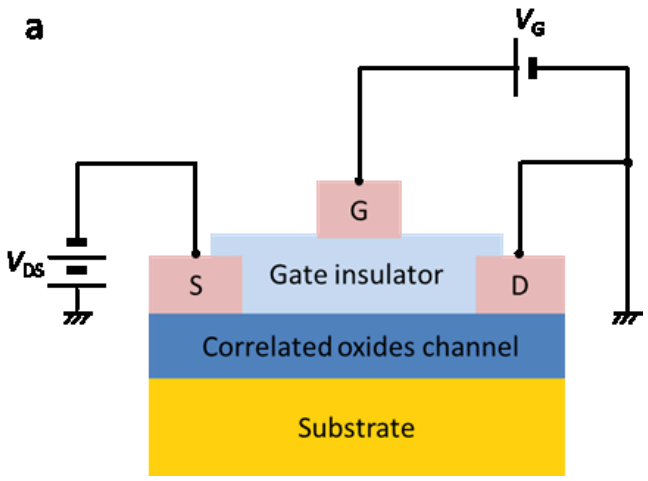
reported with nonlinear I-V characteristics. This phenomenon perhaps doesn't coincide with electrical triggering MIT, but the possibility of a current-induced heating effect was regarded as the primary [29-30]. In recent years, a three-terminal device field-effect transistor (FET) facilitates the research on clarifying electrical triggered or heating induced MIT through an introduced field by external gate voltage to minimize the current-induced heating [31-33].

1.2 Electrostatic carrier doping

An electrostatic carrier doping utilizing a FET is a powerful tool to probe their fundamental nature in correlated electron oxides. In terms of chemical doping, using metal element dopants to change the properties is an irreversible process [34-35]. In contrast, electrostatic doping provides continuous and reversible changes of carrier density without introducing any chemical impurity or disorder [36]. Moreover, the electronic, magnetic and optical properties can be controlled by an electric field, which offers high potential for practical application based on strongly correlated system. Figure 1.2 a. depicts a typical FET schematic. A classic FET is a three-terminal device, in principle, which works depending on the conductivity control of the channel layer between source and drain electrodes. A gate insulator inserted between channel layer and gate electrode is responsible for carrier modulation. When a positive/negative gate voltage is applied, the charges will be induced at the channel surface, and the number of the accumulation charges is depended on the operating gate bias V_{G} and capacitance of gate insulator C, $Q = \mathrm{C}V_{\mathrm{G}}$. Such a three-terminal device is regarded as to effectively suppress the current-induced heating effect.

The electrostatic carrier doping is descripted by typical band structure. Figure 1.2 b. plots the classic MOSFET energy band diagram for *n*-type channel structure. For

gate voltage V_G=0 V, majority and minority carriers are equilibrium. Majority carriers (electrons) will be accumulated on the surface of channel layer by a transverse electric field induced by a positive gate voltage, and the band bends down to the Fermi level E_f. This process is called accumulation. When a small negative voltage is applied, majority carriers (electrons) will be depleted. At this moment, the band is bending up and the intrinsic energy is close to the Fermi level E_f, which is depletion. With the rise of negative bias, the band bends continuously even upward. The intrinsic level E_i crosses the Fermi level E_f. In other words, minority carriers (holes) would be accumulated on the surface rather than majority carriers (electrons), so it is called inversion. For *p*-type channel materials, the majority carriers and minority carriers will exchange each other.



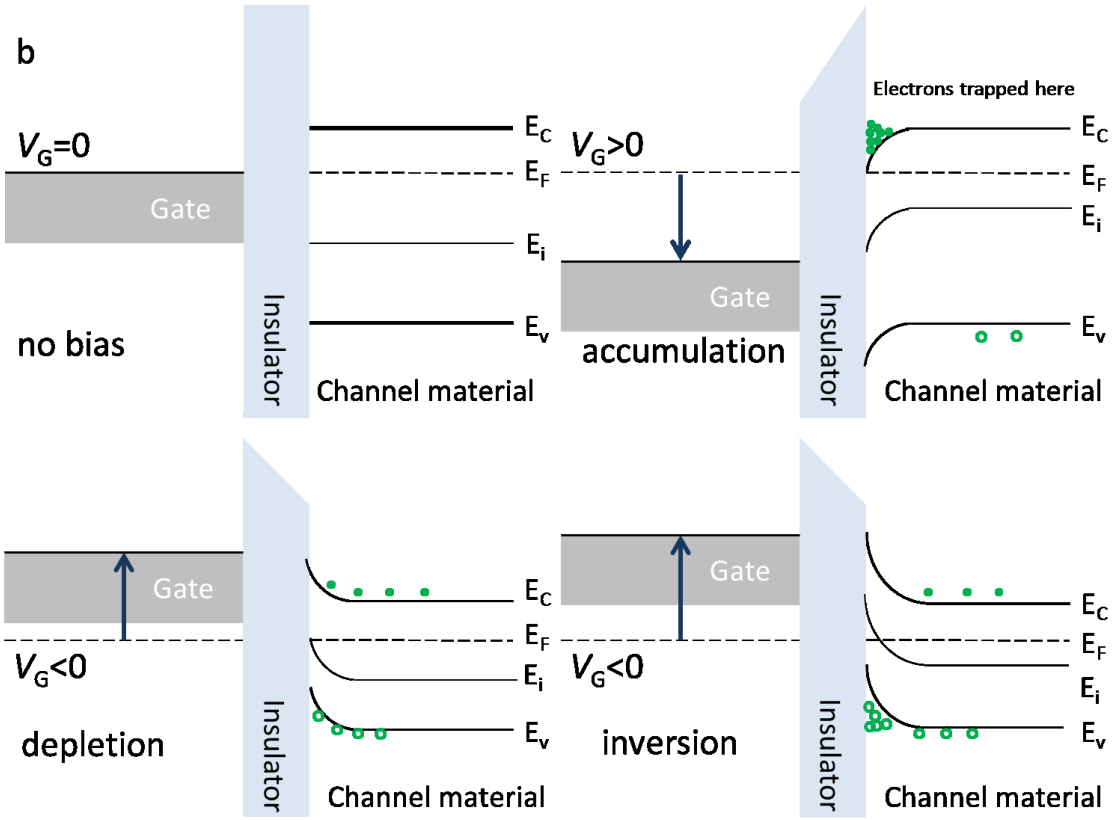


Figure 1.2 (a) cross-section of a typical FET schematic; **(b)** Energy band diagram of a classic MOSFET for *n*-type channel structure.

In principle, electrostatic carrier doping using FETs in correlated system is the same as MOSFET. However, quite thin charge accumulation or depletion layers will form at the interface, limited less than 10-nm-thick by high carrier density (~10^{20} cm^{-3}), corresponding to Thomas-Fermi screening length λ_{el}. Thus, to effectively utilize this thin interfacial layer, the smooth interface without defect and impurity between channel layer and gate insulator should be required. If sufficient carrier density can be induced by an electric field, unprecedented physical properties, namely, electric phase transition

would appear in the range of 10^{19}-10^{22} cm^{-3} accumulation carriers as descripted in Figure 1.3.

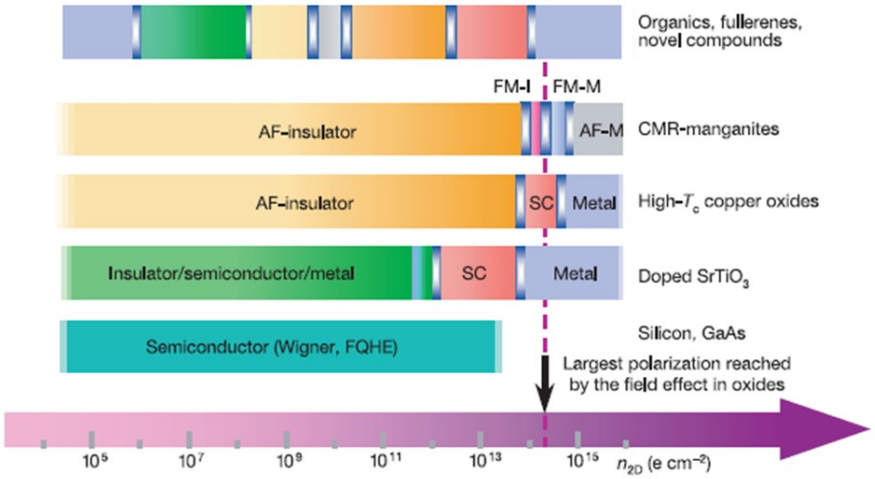


Figure 1.3 Nontrivial properties of the materials as a function of their sheet charge density [1].

According to these two factors, the large modulation should be tailored by gate insulator, which can offer a low density of charge trapping at the interface with the oxide channel, and possess high dielectric constant and large breakdown field. However, to date, the conventional dielectrics have been always restricted by large leakage current, and emergence of oxygen defects yielded during the gate dielectrics deposition [37]. As a powerful means, electrolyte gating with ionic liquid has triggered approximately 10^{14} cm^{-2} sheet carrier density [38-39]. Actually, it has been indicated not suitable for integration of semiconductor technology; and in some cases, an irreversible and slow conductance modulation indicates the presence of electrochemical reaction in EDLT

[40-41]. With a perspective towards electronic devices, there has been an enduring appeal to replace the ionic liquid with a solid gate dielectric and realize the functional phenomena in all-solid structures [42]. Most spectacular was focused on an organic polymer dielectric, parylene-C, which can be deposited on various materials at room temperature by a friend fabrication approach chemical vapor transport technique. $SrTiO_3$ FETs fabricated with parylene-C were reported to show better FET characteristics especially at low temperatures than those fabricated with oxide-based gate dielectrics [43]. The less effect of lattice defects due to the suppression of oxygen vacancy formation and charge trapping at the gate/channel interface are considered to be the origin of the improved FET characteristics. One of the important steps to utilize parylene-C for other oxide systems is to increase the induced carrier density, which remains as small as 10^{12} cm^{-2} due to its low relative dielectric constant of ~3.15. Recently, A. B. Eyvazov *et al.* demonstrated that the overlay deposition of a high-*k* oxide onto parylene-C results in an enhancement in the carrier density up to ~10^{13} cm^{-2} for $SrTiO_3$ FETs [44]. This new gate design can be potentially used for various oxides, and it is worth investigating the electrostatic charging mechanism in the hybrid structure.

1.3 Scope of this dissertation

The originality of this study is to investigate the electrostatic modulation in strongly correlated oxide VO_2 thin films and nanowires by synthesizing a hybrid gate insulator consisting of inorganic high-*k* material Ta_2O_5 and organic polymer material parylene-C. This thesis is divided into six chapters. The general introduction of this research is presented in Chapter 1, including the fundamental characteristics of strongly correlated oxide VO_2 and the feature of electrostatic carrier density control. The experimental and analysis methods employed in this work, such as pulse laser deposition, chemical vapor deposition, nanoimprint lithography, electrical measurement means and so on, are introduced in Chapter 2. In this dissertation, we have addressed three issues in the following ways: First, a hybrid gate structure is fabricated to evaluate its dielectric properties through being applied in the band semiconductor $KTaO_3$ as described in Chapter 3. Subsequently, the transport modulation of strongly correlated oxide VO_2 thin films was studied by employing such hybrid gate insulator, reported in Chapter 4. About the third part, as Chapter 5 described, the enhancement of transport modulation of VO_2 *via* decreasing channel scale size to nanometer was discussed. In addition, analysis of the origin in enhanced transport modulation for nanowire-based device was performed using an electric field distribution simulation and Brinkman-Rice

pictures [45]. Finally, I summarized all the achievements, and gave the prospective for application of hybrid gate insulator and exploitation of novel devices based on strongly correlated oxides in the last chapter.

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CHAPTER 2

Fabrication and characterization

2.1 Sample preparation

In this study, the channel oxide VO_2 thin films were fabricated by pulsed laser deposition (PLD), and combined with nanoimprint lithography to synthesize VO_2 nanowire channels. In addition, the first layer of hybrid gate insulator, parylene-C was grown onto the substrate held at room temperature by chemical vapor deposition. The overlay Ta_2O_5 was prepared using rf-sputtering. The electrodes for device were patterned utilizing two methods: stencil mask and photolithography. The details of these methods are introduced in following parts.

2.1.1 Pulsed laser deposition method

Pulsed laser deposition (PLD) has become popular in research laboratories as an extremely simple technique of producing thin films of materials. Using laser to ablate material can be traced back to 1962. Breech and Cross vaporized and excited atoms from a solid surface by ruby laser [1]. And three years later, Smith and Turner recognized high-powered pulsed laser could be used for fabricate films, which marked the beginning of the development of pulsed laser deposition technique [2]. Factually, this method has attracted much attention after the success of high-temperature superconducting films $YBa_2Cu_3O_7$ in 1987 [3]. According to the requirement for exploiting novel material, pulsed laser deposition has been employed to fabricate single

crystalline thin films with epitaxy quality, such as ceramics, nitrides, metallic multilayers, even supper-lattices in recent years [4-7].

Figure 2.1 shows a schematic for a typical experimental arrangement for pulsed laser deposition technique. A high-powered pulsed laser beam is focused on a target in a vacuum chamber to vaporize material used as an external energy source. Atoms vaporized from the target are deposited to form a film on a substrate. Laser parameters, such as wavelength, pulse repetition frequency or duration affects the deposition rate and the quality of films. The substrate temperature is influential to the diffusion length of atoms. The introduction of ambient gas, such as oxygen which is commonly used for oxides deposition, is also an important factor for stoichiometry of films.

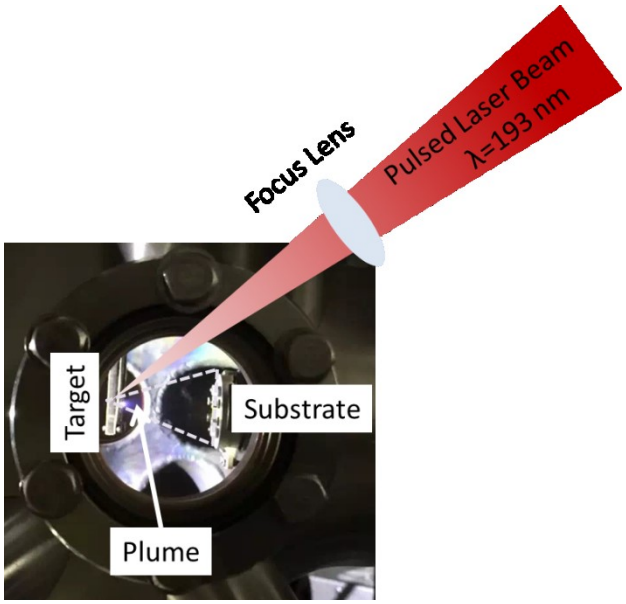

Figure 2.1 An image for a typical experimental arrangement for pulsed laser deposition technique.

In my research, VO_2 thin films have been epitaxial grown on TiO_2 (001) single crystal substrates by pulsed laser deposition method (ArF excimer laser, λ=193 nm) with pulse repetition frequency of 2 Hz. The substrate temperature was kept around 450°C in an oxygen flow of 1 Pa. The deposition rate was about 15～40 nm per hour. The thickness, surface morphology and crystallization were investigated by atomic force microscopy (AFM) and x-ray diffraction, which was depicted in section 4.2.

2.1.2 Chemical vapor deposition

Chemical vapor deposition (CVD) is a materials synthesis process through chemically reaction of a volatile reactant, with other gases, to produce nonvolatile solid films that deposits on a substrate [8-9]. A feature of CVD is versatile for fabricating simple and complex compounds at relative low temperatures.

In this research, the first layer of hybrid gate structure, parylene-C, was synthesized by chemical vapor deposition. The parylene-C deposition process follows Gorham's method [10]. It consists in three steps: 1) vaporization of dimer (the raw dix-C is sublimated to a dimer vapor by heating it up to a temperature of about 120°C); 2) pyrolysis (the dimer vapor is then passed through the quartz tube and broken to reactive monomers at 700°C); 3) polymerization (the monomer is introduced onto the substrate held at room temperature to form polymer structure). By taking advantage of

this friendly synthetic method, organic polymer parylene-C has been synthesized on the channel oxides to suppress the surface damage.

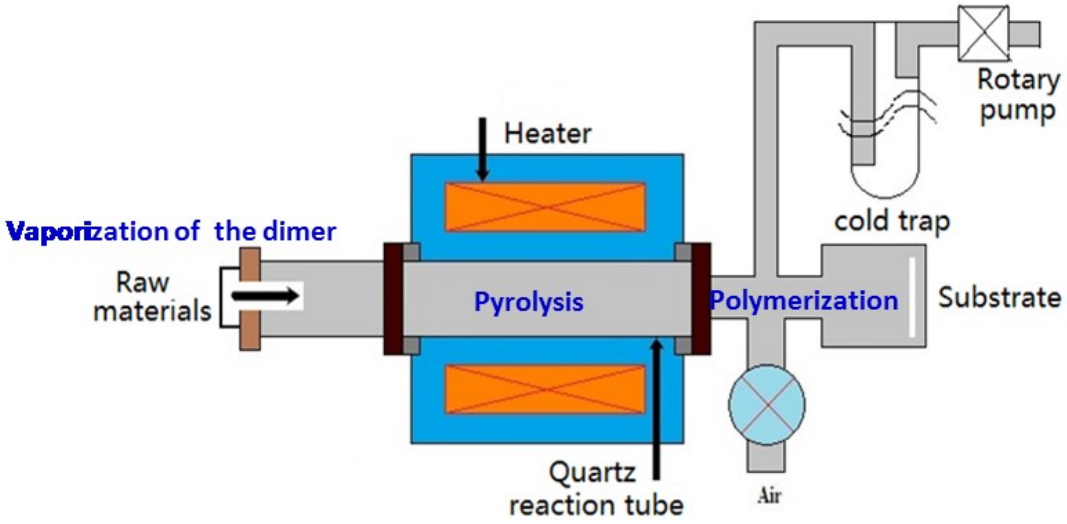

Figure 2.2 Schematic illustration of CVD technique.

2.1.3 Radio frequency sputtering

Radio frequency sputtering (rf-sputtering) is also one kind of popular manufacturing equipment to fabricate films. This method is alternative to evaporation first discovered in 1852 [11], and was developed as a thin film deposition technique by I. Langmuir and K. H. Kingdon in 1920. Figure 2.3 shows a typical set-up of rf-sputtering equipment. The sputtering gas such as argon, oxygen, and so on, is inserted into the chamber directly. Through yielded plasma to ionize the gas atoms, ions break the target material into small particles, and accumulate onto the substrate. An important advantage of rf-sputtering is not to be confined in laboratory research, always applied into large industry. Recent years, it has been reported to advanced technique, such as epitaxial

growth [12-13].

In this study, overlay Ta_2O_5 of hybrid gate insulator was fabricated by rf-sputtering from a ceramic target Ta_2O_5 doped with 10at% Y_2O_3. The Y-doping was employed to enhance the breakdown field without dielectric constant change [14]. The deposition was carried out at argon ambient, and rate was controlled at 15 nm / min.

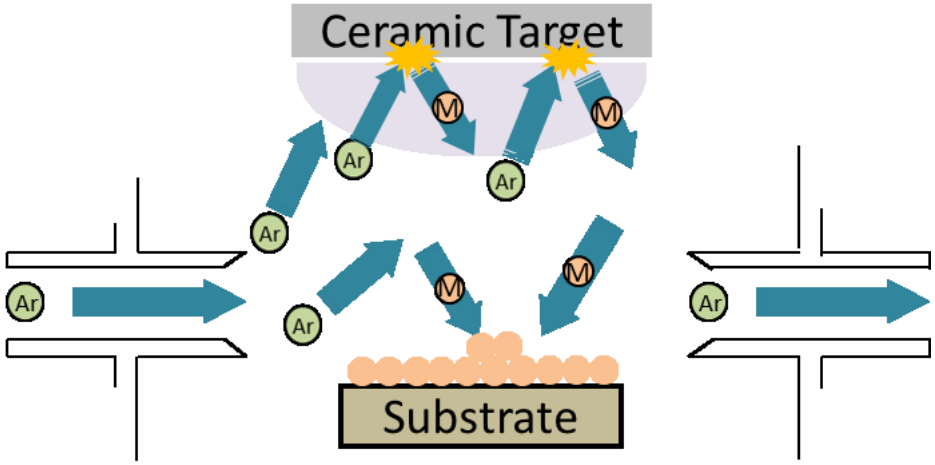

Figure 2.3 A typical set-up of rf-sputtering equipment.

2.1.4 Nanoimprint lithography

Nanoimprint lithography (NIL), first invented in 1995 [15], is a nonconventional lithographic technique as a high throughput, great precision and low cost alternative to photolithography and e-beam lithography. Unlike the traditional lithographic methods, NIL is based on the principle of mechanically modifying a thin polymer film using a template (mold) containing the micro/nanopattern, in a thermo-mechanical or ultra violet (UV) curable process [16-17].

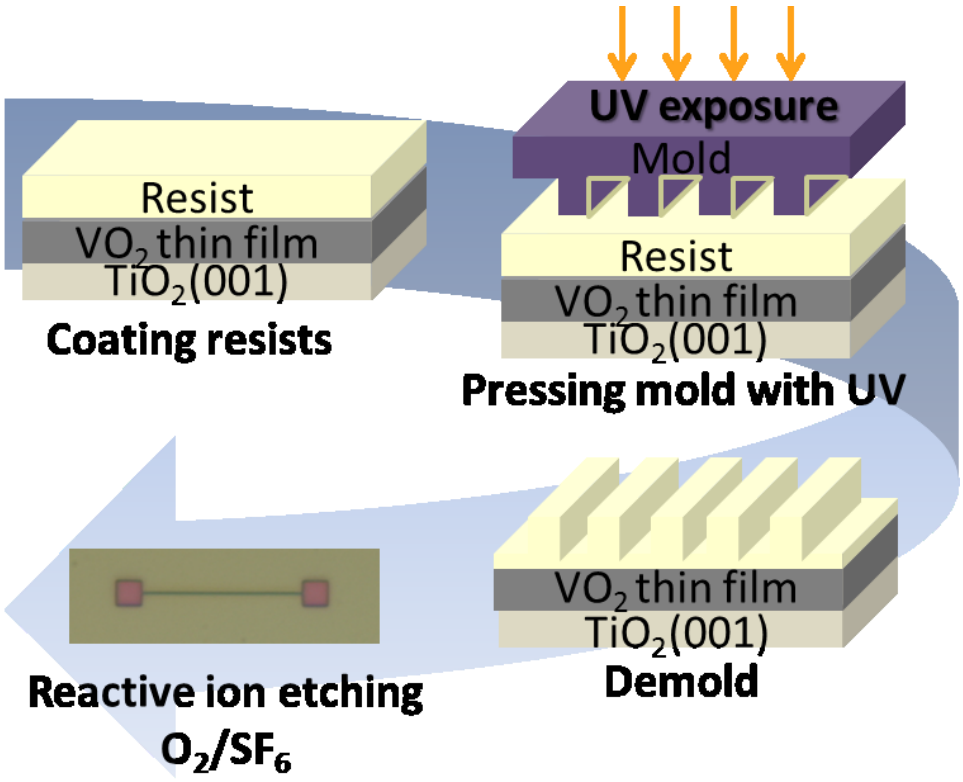

Figure 2.4 Schematic of UV-NIL process.

In my study, the UV-NIL has been employed. A feature is to reduce surface contact contamination or defect without applying high external pressure [16]. UV-NIL process includes two steps as shown in Figure 2.2. The first step is imprint. UV-curable resist is spin-coated onto the substrate, and then a mold pattern with nanostructures is pressed into the resist cast with UV. Followed by demold process, the nanostructures pattern is moved on the substrate. It is noted that during the imprint step, the resist is heated to a temperature above its glass transition temperature. The second step is the pattern transfer using reactive ion etching (RIE) approach. Firstly, the oxygen RIE process is done with a power of 50 W, a pressure of 4 Pa, and oxygen gas with a flow of

70sccm for 150 seconds to remove the residue resist in the compressed regions. Then SF_6 gas is utilized for VO_2 etching (60 W, 1 Pa, 10sccm, 10 sec). We examined the nanowire structure and width using a scanning electron microscope (SEM), which is reported in section 5.2.

2.1.5 Pattern methods

1. Shadow mask method:

Generally, a high resolution pattern is critical for FETs. Pattern methods have developed with the enhanced requirements for devices precision. In my research, two kinds of FET pattern method were used: shadow mask and photolithography. In thin films case, a primitive shadow mask method was employed, which can effectively avoid sample damage resulting from any organic resist. FET electrode patterns were fabricated on the surface of channel oxides ($KTaO_3$ (001) single crystal or VO_2 (001)) through 10 μm thick stainless steel stencil masks. As it was directly put on the sample surface, to preclude any contaminants the mask, the shadow mask was washed by Isopropyl Alcohol (IPA) in ultrasonic wave, and kept a few intervals to sample surface. It is noted that the interval between shadow mask and sample surface cannot be too large, otherwise it would yield a blunt edge even though extended as large as several microns [18].

2. Photolithography:

The facile stencil mask approach is restricted in hundreds of microns because of the strict mask alignment technique and low resolution of pattern itself, thereby, photolithography method substitutes the stencil mask to fabricate nanowire FET pattern. The photolithography is good precision process of transferring patterns of geometric shapes as a photomask to a light-sensitive photoresist covering on the sample surface [19]. According to the different requirements, the photomask can be adjusted each time due to its organization from computerized design, and the resolution limit is approaching to 10 nm. In the present work, we used positive photoresist AZ5206E to satisfy the requirement of nanowire device for high sensitivity, and high resolution. This method is suitable for large-scale and large-lot production.

2.2 Electrical measurement methods

To perform electrical measurement for different samples, two measurement systems were set up in this research. The device behavior of $KTaO_3$-based FETs was investigated by prober measurement system at room temperature in air ambient. While, for VO_2 film and nanowire active channel, an apparatus included a Peltier-based temperature stage was exploited.

2.2.1 Prober measurement system

Figure 2.5 shows the schematic view of prober measurement system. The prepared device was put on the prober stage held in air at room temperature. The three terminals of a FET were contacted by probers, which connected to Keithley 2614B source-meter unit.

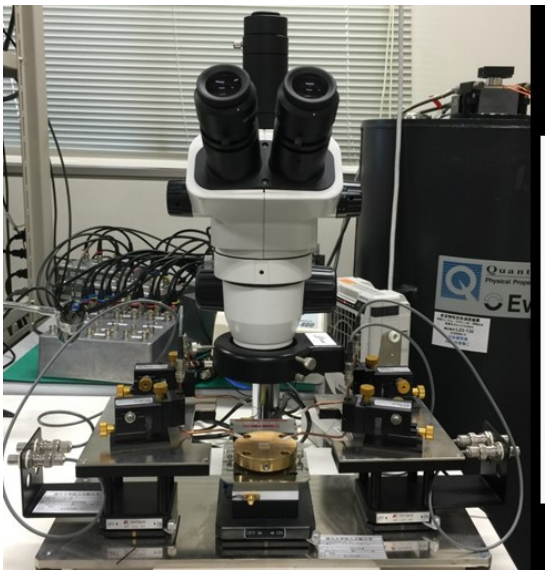

Figure 2.5 Prober apparatus for film-based FET measurement

2.2.2 Peltier-based temperature stage

An apparatus set up for researching the electrical transport characteristics of VO_2 film and nanowire channel depicted in Figure 2.6, which included a Peltier-based stage (T95, Linkam) to control temperature, a source-meter (2635A, Keithley) to measure source/drain voltage V_D, Keithley 236 source-measure unit to monitor gate voltage V_G. Temperature dependent and gate bias dependent electrical properties can be investigated simultaneously. Nitrogen gas is supplied to prevent VO_2 surface from humidity.

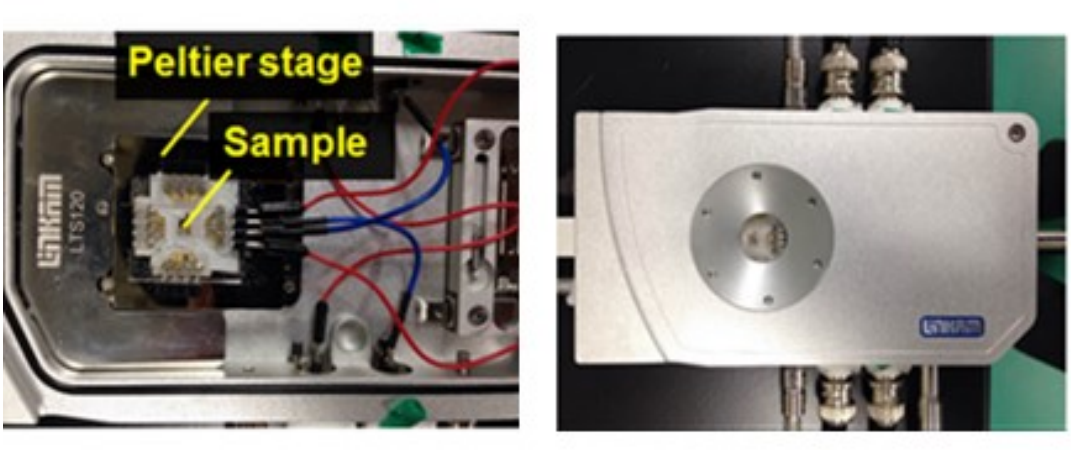

Figure 2.6 A view of Peltier stage.

2.2.3 Capacitance measurement

All the capacitance of gate insulators were performed by the prober measurement system assembled with Agilent E4980A precision LCR meter. Agilent E4980A precision LCR meter supplies two types of capacitance measurement circuit

modes: parallel equivalent circuit mode and serial equivalent circuit mode, described in Figure 2.7. For the case of small capacitance, it owns high impedance, which would cause the impact of parallel resistance Rp to be far larger than that of the serial resistance Rs, thus Rs can be neglected. Contrarily, in the case of large capacitance, the low impedance would influence the serial resistance Rs larger than that of parallel capacitance Rp, thus Rp can be neglected. In my research, parallel mode was employed.

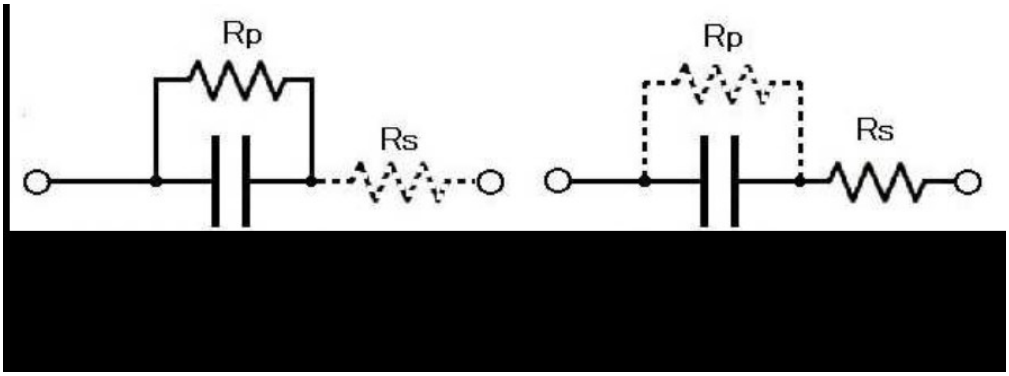

Figure 2.7 Capacitance measurement circuit modes.

A gate insulator was fabricated on a MgO (001) substrate, which was deposited Pt/Ti as ohmic contact. And finally Au film was evaporated for top electrode to constitute metal-insulator-metal (MIM) structure as a parallel capacitance to characterize gate dielectrics. When t is much smaller than the plate dimensions, the value of the capacitance can be approximated as: $C = \frac{\varepsilon_0 \varepsilon_r}{t} A$, where ε_0 is the permittivity of the vacuum (8.85×10^{-12} F/m), ε_r is the relative dielectric constant of the gate dielectrics, A is the area of the electrodes, and t is the thickness of the dielectrics.

According to the formula, the value of ε_r for each dielectric can be calculated through measured C and known parameters. The relative dielectric constants for parylene-C and Y: Ta_2O_5 in this research were estimated 3.25 and 21.5 through the measured capacitance values at 1 kHz as Figure 2.8.

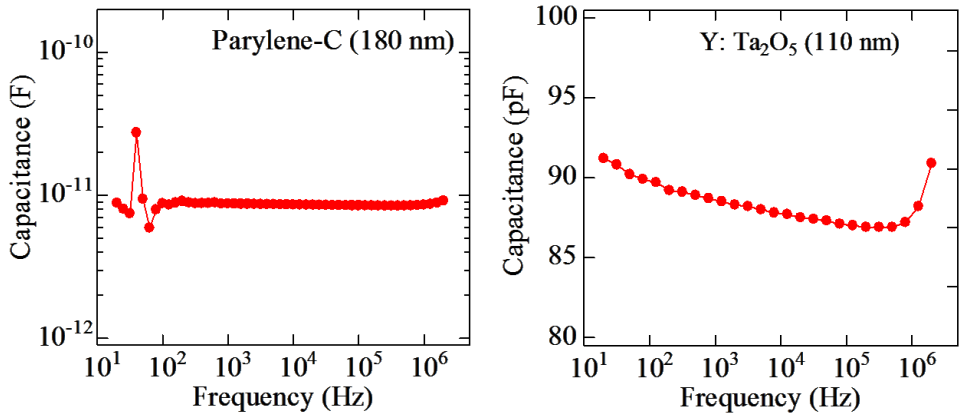

Figure 2.8 Capacitance measurement results for parylene-C and Y:Ta_2O_5 dielectric.

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CHAPTER 3

Synthesis and characterization of hybrid gate insulator

3.1 Introduction

Electrostatic control of charge carrier density using a field-effect transistor (FET) structure is an attractive method for the exploration of novel electronic phases in transition-metal oxides. Recent experiments using electrochemical electric-double-layer transistors that employ an ionic liquid as the gate dielectric have demonstrated field-induced insulator-metal transition [1-3], nonmagnetic-ferromagnetic transition [4], and superconducting transition [5] in oxides whose properties crucially depends on the carrier density. With a perspective towards electronic devices, there have been increasing attempts to replace the ionic liquid with a solid gate dielectric and realize those functional phenomena in all-solid structures [6]. For the gate dielectric, a large electrical capacitance and a low density of charge trapping at the interface with the oxide channel are essential to efficiently accumulate charge carriers on the surface of an oxide. In perovskite-type oxides, for example, high-*k* oxides [7] and ferroelectric oxides [8] hetero-epitaxial grown on the oxide channel have been widely used. As the variety of channel materials expands, however, there is a growing demand for the gate dielectric material that can be formed onto more kinds of materials instead of being restricted by hetero-epitaxial growth conditions.

One potential candidate is an organic polymer dielectric, parylene-C, which can be deposited on various materials at room temperature by a chemical vapor transport technique. $SrTiO_3$ FETs fabricated with parylene-C were reported to perform better FET characteristics especially at low temperatures than those fabricated with oxide-based gate dielectrics [9]. The reduced activity of lattice defects due to the suppression of oxygen vacancy formation and charge trapping at the gate/channel interface is regarded as the origin of the enhanced FET characteristics. Nevertheless, it is known that due to the low relative dielectric constant (~3.15), the utilizing of parylene-C would severely restrict the induced carrier density in the channel (~10^{12} cm^{-2}). Therefore, a strategy to integrate the merits of high-*k* oxide and the universal nature of organic polymer deposition is on demand. Recently, A. B. Eyvazov *et al.* demonstrated that the over-layer deposition of a high-*k* oxide onto parylene-C results in an enhancement of the carrier density up to ~10^{13} cm^{-2} for $SrTiO_3$ FETs [10]. A feature of this approach is potentially to be utilized for any materials, and to be hence expected to broaden the application range of oxide-based FETs. In this part, I attempted to evaluate the characteristics through revealing the connection mode of hybrid gate structure.

3.2 Fabrication of hybrid gate insulator

3.2.1 Parylene-C

Parylene is a generic name for a variety of poly (p-xylylene) polymers and its derivatives, including parylene-C, parylene-D, parylene-N, and so on. Figure 3.1 shows the chemical structures of the major members in the parylene variants. The parylene-N is a linear and highly crystalline polymer. The parylene-C has one chlorine molecule substituted on the aromatic ring. The parylene-D has two chlorine groups per repeat unit. Among them, parylene-C with higher hydrophobic is the most popular choice as an encapsulation moisture barrier for biomedical devices and variety anticorrosion applications, because it can inhibit adsorption of both water vapor and oxygen present in ambient atmosphere [11]. Moreover, parylene-C is conformal, insoluble in common solvents such as acetone, isopropyl alcohol [12]. Furthermore, growth method in gas phase polymerization makes parylene-C absolutely uniform and conformal on all surfaces to provide a pinhole free, which is satisfied with the critical requirement for electronic devices [13]. In this research, the select reason for parylene-C is that it possesses the highest relative dielectric constant, dielectric constant in variant with frequency and higher hydrophobic. Meanwhile, thin parylene-C was reported also to have superior higher thermal stability, dielectric strength, and electrical insulation

characteristics as gate insulator, resulting in the best FET performance [14-16].

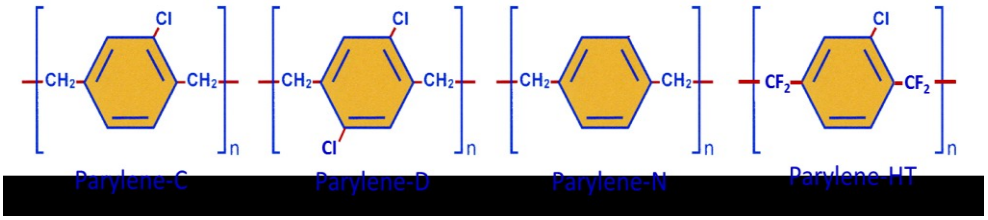

Figure 3.1 Chemical structures of major members in the parylene family.

However, parylene-C cannot provide sufficient carrier density for correlated oxides, due to its low relative dielectric constant (ε_r=3.25). High-k material Ta_2O_5 was hence synthesized as overlay to be responsible for the enhancement of carrier density.

3.2.2 Connection mode for hybrid gate insulator

We first characterized Ta_2O_5/parylene-C gate insulators by means of capacitance measurements, with the setup shown in the inset of Figure 3.2. The hybrid gate insulator was fabricated as follows: A parylene-C dielectric layer was deposited by CVD on a Pt/Ti/MgO(001) substrate held at room temperature, and then a Y: Ta_2O_5 amorphous layer was grown by rf-sputtering. Finally, a 20-nm-thick Au film was evaporated for a top electrode.

We varied the thicknesses of Ta_2O_5 and parylene layers, t_T and t_P, and measured the capacitance C to derive the effective relative dielectric constant (ε_{eff}) of the hybrid gate insulator. Figure 3.2 displayed ε_{eff} calculated from the measured C_s using the following relation: $C_s = \frac{\varepsilon_0 \varepsilon_{eff}}{t_T + t_P}$, where t_T and t_P the thicknesses of Y: Ta_2O_5 and

parylene-C layers, respectively. ε_{eff} monotonically increased with decreasing the ratio of t_P against the total thickness $t_T + t_P$, and became very close to the relative dielectric constant of Y: Ta_2O_5 (~21.5) as $t_P/(t_T + t_P)$ approached to zero. The dashed line in the figure represented the result that calculated according to the series capacitor model through two measured relative dielectric constants of parylene-C and Y: Ta_2O_5 monolayer. And it showed an excellent agreement with the experimentally obtained ε_{eff}. These results indicated that the present hybrid system matches quantitatively with the series connection description as reported in organic material devices [17-18], and the thickness control of the two component dielectric layers was the key to enhance capacitance of the hybrid gate insulator.

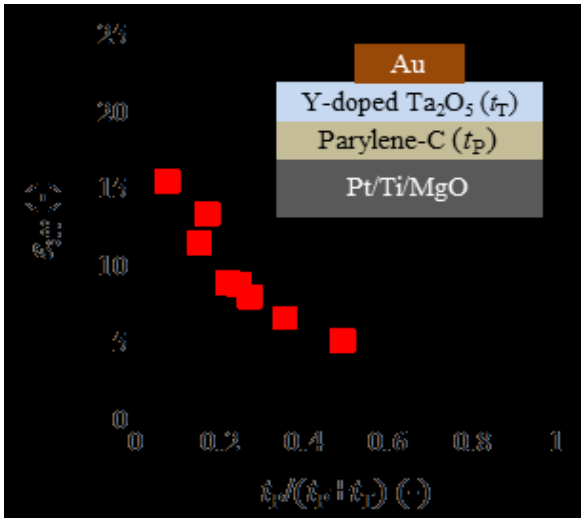

Figure 3.2 Variation of effective relative dielectric constant versus the ratio of $t_{Y:\ Ta2O5}$ to the total thickness $t_{Y:\ Ta2O5}$+ $t_{parylene}$. Inset is the cross-sectional architecture of hybrid capacitance fabricated on single crystalline MgO(001) substrate.

3.3 Evaluation of hybrid structure employing band semiconductor $KTaO_3$

3.3.1 Device preparation

In order to illustrate the characteristics of as-prepared hybrid gate insulator, potassium tantalum oxide $KTaO_3$ with typical cubic perovskite structure has been chosen as a prime candidate for active channel layer. $KTaO_3$ is an *n*-type semiconductor with a band gap of 3.8 eV and, due to the broad conduction band mainly composed of spatially extended 5*d* orbitals, shows a relatively high mobility as a transition-metal oxide [19-20]. At first, a dimension of 5 × 5 × 0.5 mm^3 single-crystalline $KTaO_3$ (001) substrate (as purchased from Shinko-Sha Co.) was annealed at 700°C in oxygen ambient for one hour to obtain an atomically flat surface [21-22]. Surface treatment was well known to be critical to reduce the diffusion and charge trap, and make an atomic layer-by-layer growth of transition metal oxides possible [23-24]. Subsequently, a 20-nm-thick Al film was deposited onto a $KTaO_3$ substrate to serve as source and drain electrodes by stencil mask patterning, and following the hybrid capacitor was formed onto the channel to dope charge carriers. Figure 3.3 a and b displayed the schematic device structure and top-view photograph of $KTaO_3$-based FET, and the cross-sectional scanning electron microscope (SEM) image of a Y: Ta_2O_5/parylene-C/$KTaO_3$ structure,

respectively. The channel size of the device was 200 μm × 400 μm. Electrical measurements were carried out at room temperature in air utilizing the prober measurement equipment.

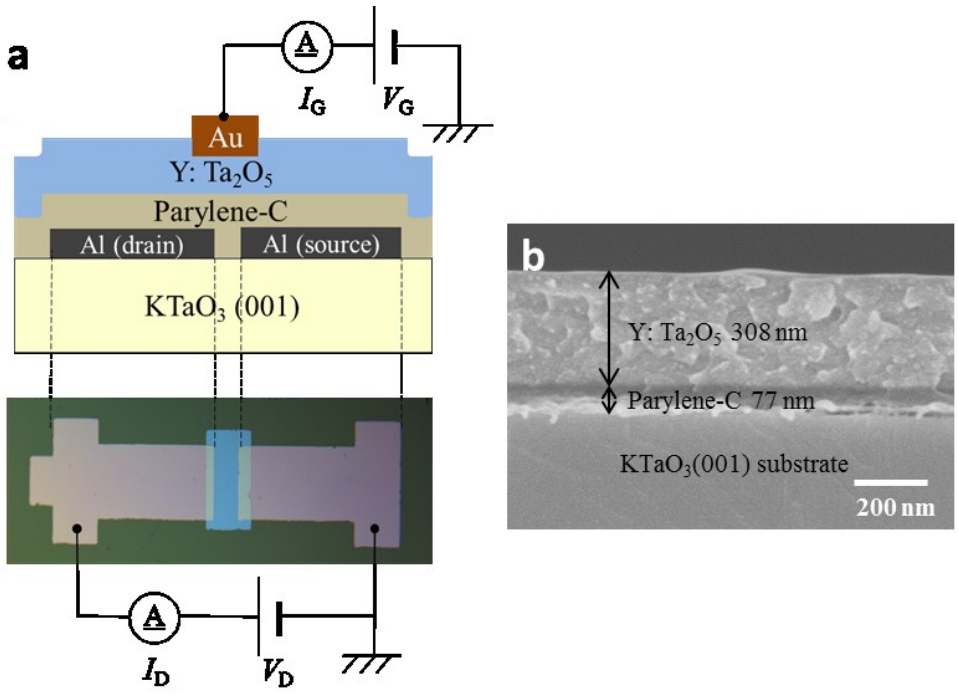

Figure 3.3 (a) Schematic device structure and top-view photograph of a $KTaO_3$ based-FET with hybrid gate insulator; **(b)** Cross-sectional scanning electron microscope (SEM) image of hybrid gate dielectric/$KTaO_3$ FET.

3.3.2 FETs performance at room temperature

The electrical measurement illustrated the superior performance of hybrid gate FETs compared to the Ta_2O_5 monolayer and parylene-C monolayer insulator counterpart. Figure 3.4 a depicted the gate leakage currents (I_G) versus sheet carrier density (n_{sheet}), which was estimated *via* $\frac{C_S V_G}{e}$, for the hybrid and Y: Ta_2O_5 monolayer gate insulators.

Here V_G is the operating gate voltage, e is the elemental charge. We selected n_{sheet} as the variable because it was more convenient for comparing the performance of FETs with different capacitances and the operating voltages. The gate leakage current for the devices with parylene-inserted hybrid gate insulator and parylene-C monolayer was a few orders of magnitude lower than that of Y: Ta_2O_5 monolayer one under same n_{sheet}. Such a beneficial decrease is attributed to the protective function of parylene-C towards the channel surface and suppression of the damage of the over-layer Y: Ta_2O_5 during sputtering. Meanwhile, the insertion of polymeric parylene-C was identified to have impacted on the improvements of device performance. In Figure 3.4 b, the measured drain-source current (I_D) was also plotted as a function of n_{sheet} with a drain-source voltage (V_D) of 1 V. I_D increased dramatically as the addition of n_{sheet}, indicating *n*-type channel characteristics. In contrast to the case of Y: Ta_2O_5 monolayer device, I_D at zero gate voltage was below 0.02 nA for the 70-nm-thick parylene-C-inserted hybrid device. It suggested that the introduction of the organic layer reduced the magnitude of off-state leakage current by nearly one order. In other words, the inserted parylene-C layer sufficiently suppressed the channel oxides defects and reduced the interface trap state densities.

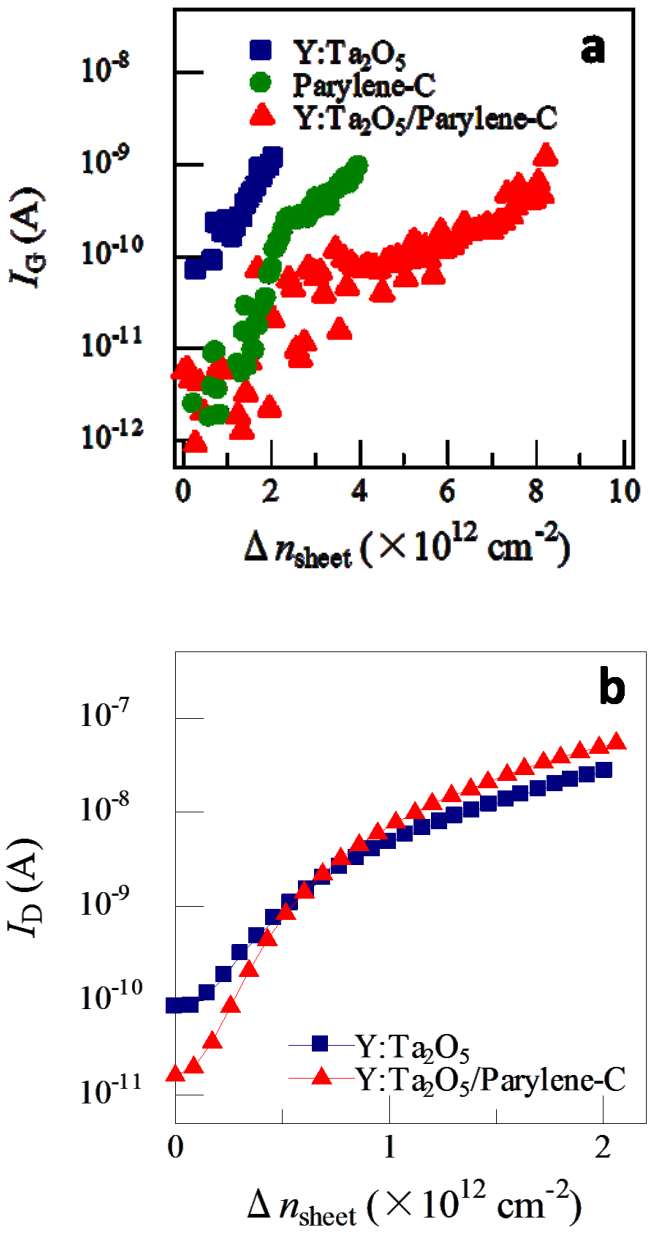

Figure 3.4 (a) Gate leakage current I_G versus sheet carrier density n_{sheet} for Y: Ta_2O_5 (210 nm)/Parylene-C (70 nm) hybrid gate dielectric (red triangles), parylene-C (350 nm) monolayer gate dielectric (green circles), and Y: Ta_2O_5 (315 nm) monolayer gate insulator (blue square); **(b)** Drain-source current I_D plotted against sheet carrier density n_{sheet} for hybrid gate insulator with 70-nm-thick parylene-C insertion (red triangles) and the monolayer Y: Ta_2O_5 one (blue square) with the similar total thickness of 300 nm.

Quantitatively, the on/off ratio for hybrid gate $KTaO_3$ FETs has been enhanced to be 4.5 $\times 10^3$ at $n_{sheet}= 2 \times 10^{12}$ cm $^{-2}$ as long as the device entered the saturation state, compared with 3.13×10^2 at same value of n_{sheet} for Y: Ta_2O_5 monolayer-gated device. Meanwhile, the maximum on/off ratio of the hybrid insulator-gated FET even exceeded 10^5. Simultaneously, we stress that there exists a lower limit of parylene-C thickness, which is in the vicinity of 10 nm. The physical mechanism is that the pinholes in ultra-thin parylene-C may cause damage to the channel surface during the Y: Ta_2O_5 sputtering process. Hence, the off-state leakage current would arise steeply for ultra-thin parylene-C devices to degrade the device performance.

Figure 3.5 a-e summarized the output characteristics, I_D versus V_D of $KTaO_3$ FETs with diverse gate insulator component ratios under varied operating gate voltage (V_G). In Figure 3.5 e, for the FET with Y: Ta_2O_5 monolayer gate dielectrics, I_D showed linear performance at low positive V_D, while a clear saturation is observed at high V_D. On the other hand, for the parylene-C monolayer case (shown in Fig. 3.5 a), the required operating voltage was about 78 V to reach an on-state I_D of 200 nA ($V_D = 5$ V), owing to the low relative dielectric constant of parylene-C. Moreover, the operating gate voltage of the $KTaO_3$ FETs with 70-nm-thick parylene-C (Fig. 3.5 b) as the inserted hybrid gate insulator was approximately 20 V at the same on-state I_D, which is larger than the

previously reported result (4 V on $Al_2O_3/KTaO_3$ [25]). We further decreased the thickness of the parylene-C to 40 nm and 10 nm while fixing the overall dielectric thickness, as depicted in Figure 3.5 c and d. Consequently, the operating voltage required to trigger a drain-source current of 200 nA was reduced to 14 V and 9 V, respectively. The operating voltage of the 10-nm-thick parylene-C FET was similarly as low as that of the Ta_2O_5 monolayer one (Fig. 3.5 e). In addition, for the three devices with different thicknesses of hybrid gate dielectrics, the operating voltages in the linear region (V_D = 1 V, I_D = 50 nA) are approximately 9 V (Fig. 3.5 d), 14 V (Fig. 3.5 c), and 20 V (Fig. 3.5 b), respectively. Since ΔI_D was considered to be similar for the three FETs in the linear regime, ΔI_D was proportional to the induced carrier concentration Δn, which is equal to the product of the capacitance and operating voltage. Thereby, the operating voltages results were found to be consistent with the trend of the capacitance for the three FETs, which are validated to be 54 nF/cm^2, 36 nF/cm^2, and 28 nF/cm^2, respectively. These results suggested that the presence of the hybrid gate insulator was fully in accordance with the series model for the device, and thus made it possible to reduce the operating gate voltage by decreasing the parylene-C thickness.

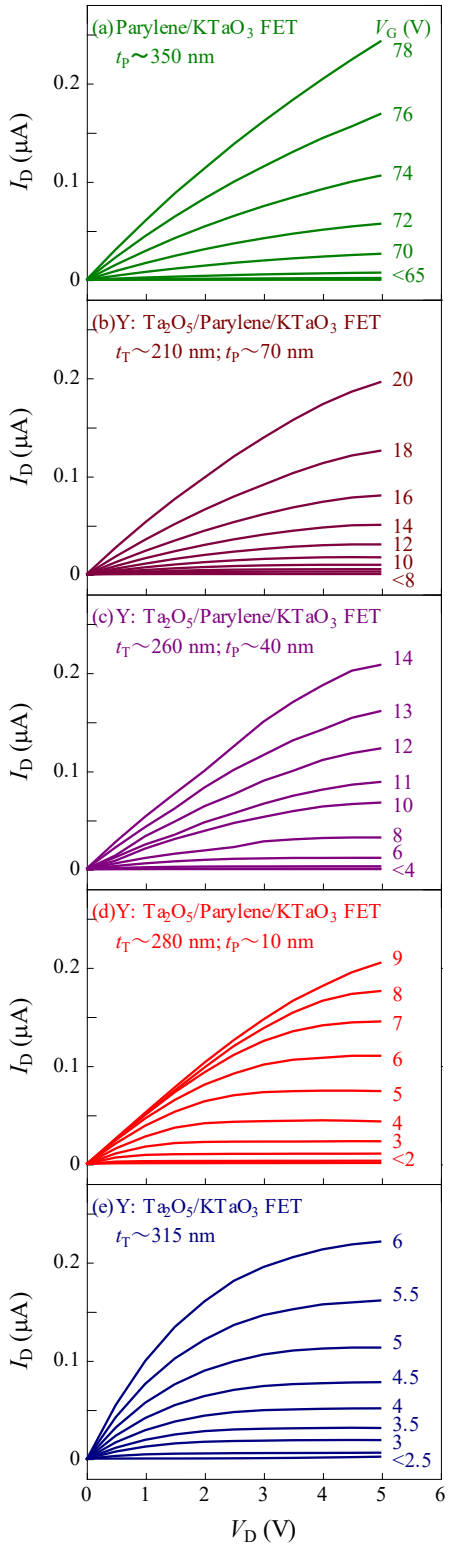

Figure 3.5 (a-e) Output characteristics for $KTaO_3$ based-FETs with various component gate insulators.

3.3.3 Conclusion

In summary, we have fabricated the hybrid gate insulator consisted of inorganic high-*k* material Ta_2O_5 and organic polymer parylene-C, and illustrated high capability and connection mode of the hybrid gate insulator by application in transition metal oxide $KTaO_3$. According to the comparison of hybrid gate insulator-gated device with Ta_2O_5 monolayer insulator one, the dominant contributing factor of organic polymer parylene-C was investigated and parylene-C was indicated to suppress the channel surface damage effectively. Simultaneously, we have demonstrated the feasibility of lowing operating voltage *via* controlling the thickness of parylene-C in hybrid gate dielectrics FETs. The demonstrated step is critical towards practical applications, since the fabricated hybrid gate dielectrics structure can be integrated with various channel oxides and to facilitate the understanding of physical properties at low temperature for strongly correlated oxides.

3.4 References

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CHAPTER 4

Electrostatic carrier doping in VO_2 thin film channels

4.1 Introduction

As mentioned in chapter 2, study on electrostatic carrier doping utilizing a field-effect transistor structure (FET) has developed a new branch to probe underlying physics in condensed matter physics in the last decade. A unique feature of this approach is to supply a continuous carrier doping without introducing any disorders and impurities. Much effort has been attempted and obtained nontrivial phenomenon in strongly correlated materials, from the initial stage $Ba_xLa_{5-x}Cu_5O_{5\,(3-y)}$ [1], $LaMnO_3$ [2] to recent $SrRuO_3$ [3], MoS_2 [4], and so on. Vanadium dioxide (VO_2) as a prospective candidate, which possesses a dramatic resistance change from the insulating monoclinic phase to the metallic rutile phase at T_{MI}=340 K, has attracted considerable attention. Its original mechanism of metal-insulator transition (MIT) has still under intense debate [5-8]. Pure electrostatic doping approach hence would provide an avenue to clarify the physics of VO_2 without inducing any impurity originating from chemical reaction to structure variation. However, so far few reports have focused on VO_2-based FETs stemmed mainly from the gate dielectrics for FETs. For instance, the conventional gate schemes, like SiO_2 [9], Al_2O_3 [10], and HfO_2 [11], were susceptible to atomic mixture at interface or the defects of channel surface induced in the conventional fabrication process. Meanwhile, recent researches of MIT induced in VO_2 by electric double layer

transistor (EDLT) have been demonstrated to tailor giant sheet carrier density approach to 10^{14} cm^{-2} [12-14], while open question about the existence of chemical reaction still remains. Therefore, it is necessary to employ a robust dielectric for gate layer, in order to not only lower the interface trap density, but also trigger huge sheet carrier density. In this chapter, I attempted to trigger carrier transfer modulation in VO_2 thin films by hybrid gate dielectric-gated FETs, excluding the impacts of joule-heating effect and chemical reaction.

4.2 Characterization of VO_2 thin films

4.2.1 Substrate treatment

In this research, high quality VO_2 thin films were epitaxial deposited on rutile TiO_2 (001) single crystal substrates by pulsed laser deposition method (ArF excimer laser, λ=193 nm). The substrate temperature was kept around 450°C in an oxygen flow of 1 Pa. The reason for choosing TiO_2 (001) substrate is that the MIT temperature of VO_2 films grown on TiO_2 (001) substrate was reported close to RT, and the abruptness of MIT was higher than that deposited on other substrates, i.e. Al_2O_3 (0001) [15], *n*-type doped Si (001) [16]. Although a tensile stress along *a*-axis of VO_2 films was yielded due to the lattice mismatch (0.86%) with TiO_2 (001), as summarized in Table 4.1, the value of lattice mismatch was further smaller than that with sapphire substrate (4.49%) [17]. X-ray diffraction revealed high quality and *c*-axis crystallographic orientation of VO_2 thin film [18], as shown in Figure 4.1. Inset showed a cross-sectional high-resolution transmission electron microscopy (HR-TEM) image of VO_2/TiO_2 hetero-interface.

Table 4.1. Lattice parameters of rutile VO_2 and TiO_2 are presented.

Crystal structure / Lattice parameters	a axis (nm)	b axis (nm)	c axis (nm)
Rutile TiO_2	0.4593	0.4593	0.2959
Rutile VO_2	0.4554	0.4554	0.2856
Lattice mismatch (%)	0.856	0.856	3.606

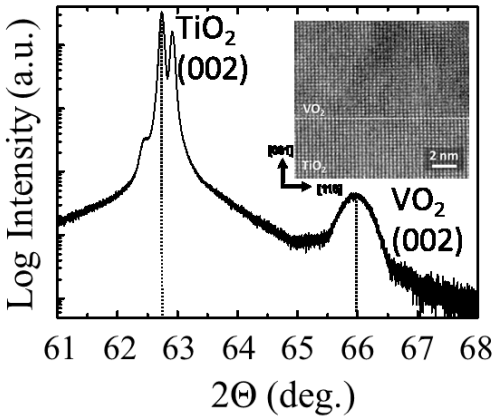

Figure 4.1 X-ray diffraction pattern for an epitaxial VO_2 thin film deposited on TiO_2 (001) single crystal substrates.

The surface treatment of single crystal TiO_2 (001) substrate was performed by rapid thermal annealing (RTA) at 700°C for 1 hour in oxygen ambient to obtain the atomically flat steps and terrace surface. The atomic force microscopy (AFM) images of TiO_2 (001) surface after different temperature thermal treatments were depicted in Figure 4.2. And Figure 4.3 exhibited the temperature dependent resistance for prepared VO_2 film samples with different TiO_2 surface treatment temperatures. The results further indicated the optimum annealing temperature was 700°C.

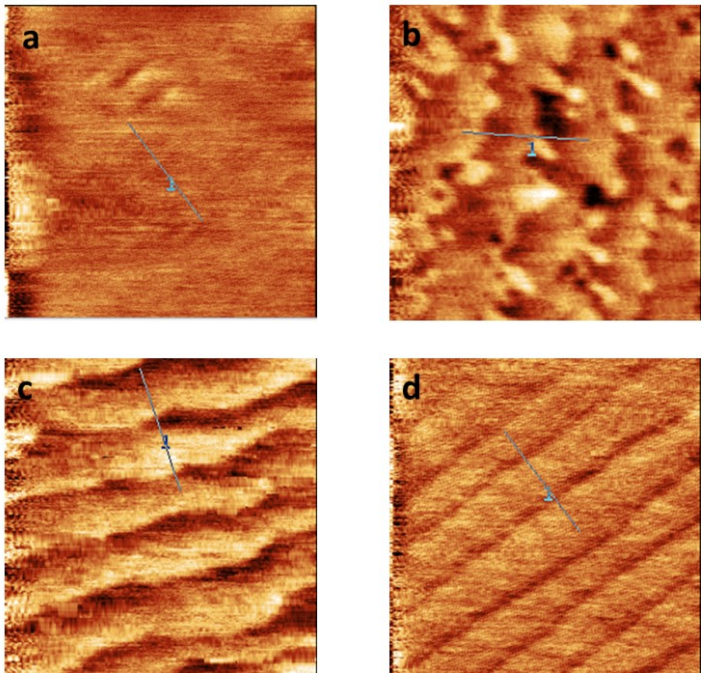

Figure 4.2 AFM images (1×1 μm^2) of the surface morphology for thermal treated TiO_2 (001) substrate under different temperatures. **(a)** as-polished; **(b)** 700°C; **(c)** 800°C; **(d)** 900°C. And 700°C was demonstrated as the optimum temperature to form step and terrace structure and eliminate the surface contamination.

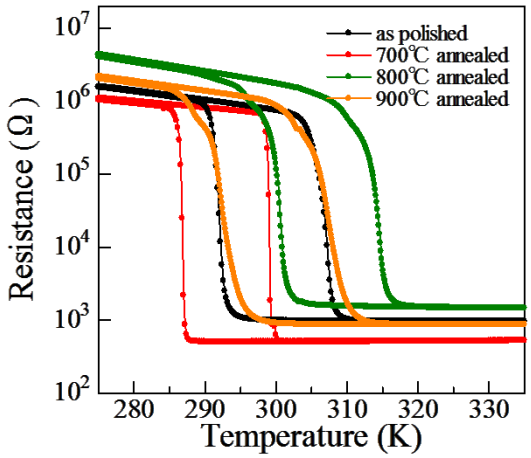

Figure 4.3 Temperature dependent resistance for VO_2 thin films deposited on TiO_2 (001) substrate thermal treated by different annealing temperatures.

4.2.2 Effect of film thickness on metal-insulator transition

Primarily, the effect of film thickness on temperature dependence of resistance (R-T) was investigated. Figure 4.4 described R-T curve for inconsistent thickness varied from 5 nm to 20 nm of VO_2 films deposited on TiO_2 substrates annealed at 700°C. To our knowledge, VO_2 films over 20 nm thick would contain cracks, as reported in Ref. 19. The sample with 5-nm-thick showed sluggish MIT; contrarily the most abrupt MIT occurs in the 20-nm-thick one, which was considered that the electrical properties were influenced by the crystallinity [20]. This result suggested 20-nm-thick VO_2 film in present research owns the best crystallinity; hence such a thickness of film with 20 nm was fabricated in the following experiments.

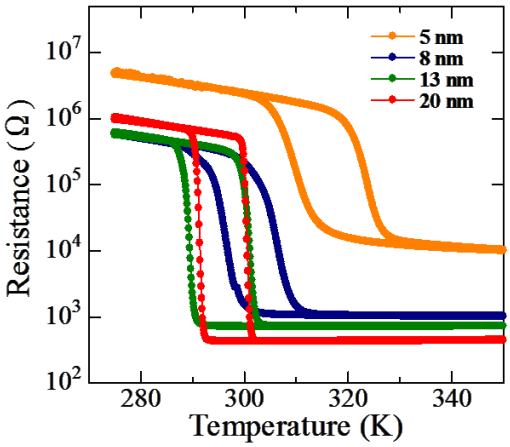

Figure 4.4 Temperature dependence of resistance for different thick VO_2 thin films deposited on TiO_2 (001) substrate under the same surface treatment.

4.3 Electrical transport properties of VO_2-based FETs

A FET has been fabricated with VO_2 as active channel layer. Pt (20 nm)/Cr (5 nm) was deposited on prepared epitaxial VO_2 thin film using stencil mask by e-beam deposition as source/drain contacts. Parylene-C and Ta_2O_5 doped with Y_2O_3 10 at% were grown by chemical vapor deposition and rf-sputtering method in succession. A 20-nm-thick Au was evaporated to serve as the gate electrode, on which Pt wires were placed using Au paste. Figure 4.5 a and b displayed cross-sectional scanning electron microscope (SEM) image and schematic structure of VO_2 film-based FET, respectively. The channel size was 200 μm in length and 400 μm in width, respectively. All electrical experiments were performed under dark condition and nitrogen atmosphere using Peltier-controlled stage to eliminate the effects of photo conductivity and humidity [21].

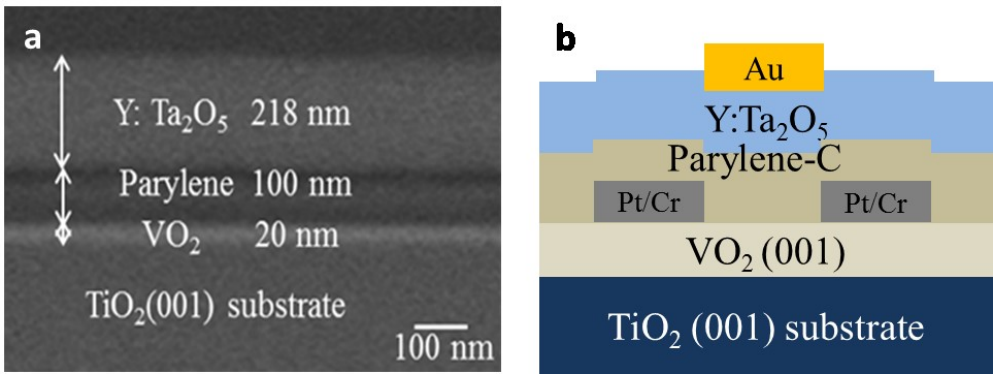

Figure 4.5 (a) Cross-sectional scanning electron microscope (SEM) image of hybrid-gated device; **(b)** Cross-section schematic of VO_2 film device structure with hybrid gate insulator.

4.3.1 Reversible and prompt resistance modulation

We firstly investigated the resistance behavior to a varying square-shaped gate bias V_G near metal-insulator transition temperature T_{MI}. As depicted in Figure 4.6 a-e, the device exhibited excellent reproducibility of rapid resistance responses to the gate bias from 300 K to 320 K at source-drain voltage V_D=0.1 V. In the insulating regime, there was an abrupt decrease in resistance under positive gate voltage. The resistance variation degree was increased with adding positive gate voltage. We note that the gate dielectric has never broken until 30 V, as evidenced through low ratio of the gate current I_G to the source-drain current I_D. Contrasting to the slow hysteretic response in EDLT (The change in conductance was no obvious change at scan rates equal to or faster than 3.3 mV/sec) [22], the abrupt resistance modulation was instantly switched following within 50-millisecond-interval corresponding to 600 V/sec at various temperatures. These results enable us to conclude this modulation attribute to pure electrostatic effect.

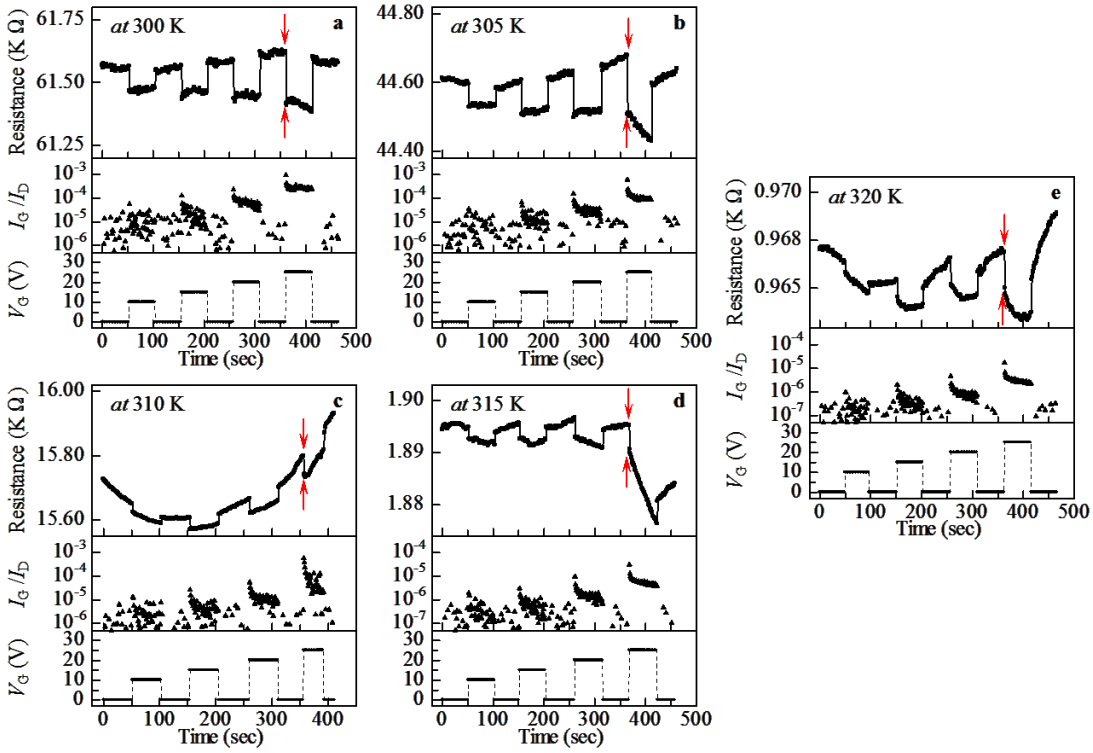

Figure 4.6 (a-e) Temperature-dependent resistance modulation based on gate bias near transition temperature T_{MI} at 300K, 305K, 310K, 315K and 320K.

To accurately investigate the relationship between $\Delta R/R_{off}$ and temperature, change rates in resistance $\Delta R/R_{off} = (R_{on} - R_{off})/R_{off} \times 100\%$ calculated from two borderline points of switching-on and switching-off indicated by arrows were summarized in Figure 4.7 according to above results, as a function of temperature at varied gate voltage V_G. The resistance modulation efficiency was found to be increased with the rise of temperature at first, and reached the maximum near certain temperature. Eventually, with entering the metallic state the variation degenerated even almost disappeared. The maximum resistance change was considered to appear near phase

transition temperature T_{MI} (310.8 K), which can be identified by the minima of temperature derivative of resistance logarithm d(lnR)/dT as shown in the insert of Figure 4.7.

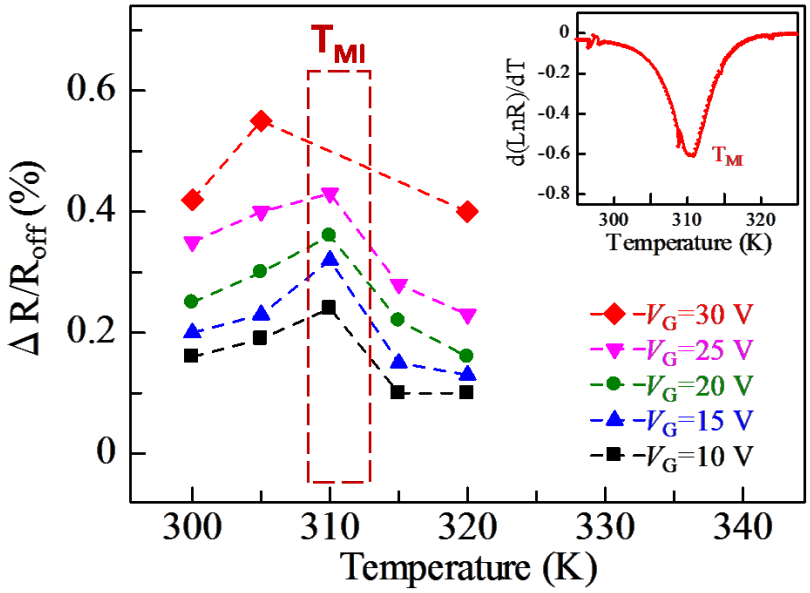

Figure 4.7 Change ratios in resistance against temperature at varied gate voltage V_G, which illustrated the maximum $\Delta R/R_{off}$ appears in the vicinity of T_{MI}. Black squares, blue triangles, green circles, pink inverted triangles, and red diamonds were recorded the gate voltage ranging from 10 V to 30 V with 10V interval. Inset gave the transition temperature T_{MI} identified by the minima of temperature derivative of resistance logarithm.

4.3.2 Low consumption & high modulation in hybrid-gated device

As a frame of reference, we also fabricated only parylene-C monolayer gate dielectric onto VO_2 channel layer with the similar thickness (～350 nm) to hybrid one.

Likewise rapid switching performance was also achieved, and the maximum of $\Delta R/R_{off}$ was about 0.15%. Figure 4.8 depicted the comparison of $\Delta R/R_{off}$ to operating gate voltages V_G for hybrid gate dielectric/VO_2 FET and parylene-C monolayer one. Contrasting to monolayer device, hybrid gate device showed approximately 7 folds higher resistance modulation ratio (0.55% for hybrid FET; while 0.08% for monolayer one) under the same operating gate voltage (V_G=30 V) at 305 K. The tendency is also an important evidence of electrostatic field-induced carrier transport model. That is to say, the resistance modulation efficiency would rise with increasing sheet carrier density *via* enhancing capacitance of hybrid gate insulator that we measured, and the MIT would yield when the crucial carrier density is broken through finally. The resistance modulation efficiency was well corresponded to the transconductance g_m, which shown in the following equation: $g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L} C_s \mu_{FE} V_D$. Here, W and L are the width and length of the channel, μ_{FE} is the field-effect mobility, C_s is the capacitance per unit area represented as $C_s = \frac{\varepsilon_0 \varepsilon_r}{t}$, where ε_r is the relative dielectric constant. It was hence considered that less carrier transport modulation triggered by parylene-C gate insulator than that by hybrid one (ε_r~8.19) as mainly attributed to low relative dielectric constant of parylene-C (ε_r~3.25). It was noted that the actual relative dielectric constants for both dielectrics were extracted from the capacitance per unit area C_s indicated in Figure 4.8,

which was measured through Au/gate-insulator/Pt/Ti/MgO (001) capacitance structure. Additionally, from the point of view of applications, hybrid gate insulator demonstrated a route to fabricating fast switch with low gate bias.

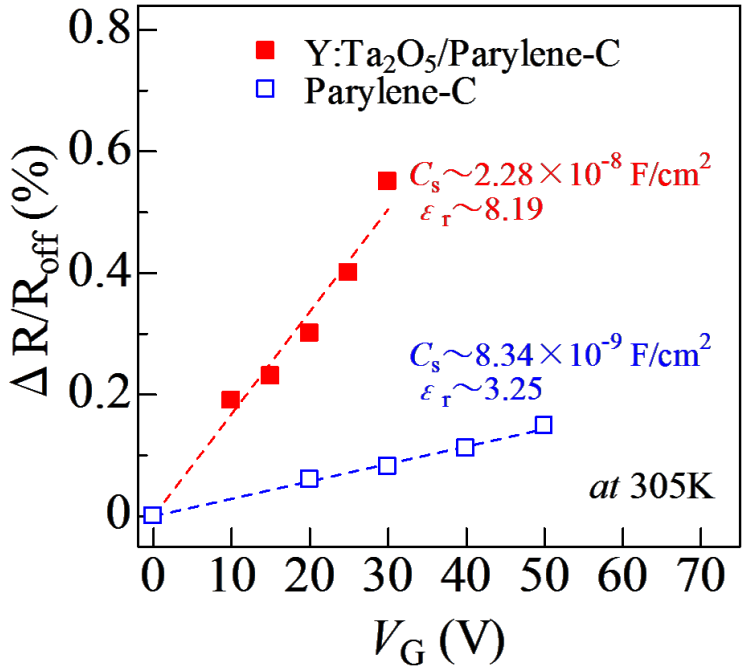

Figure 4.8 Comparison of the resistance modulation ratio to applied gate voltages in VO_2-based FETs with hybrid gate dielectrics and parylene-C monolayer one.

On the theoretical side, sheet carrier density n_{sheet}, which defined by the formula: $n_{sheet} = \frac{C_s V_G}{e}$, has been considered to be a crucial parameter for MIT in correlated metal oxides, where e is the unit of electric charge. Figure 4.9 displayed $\Delta R/R_{off}$ as a function of induced sheet carrier density n_{sheet} for VO_2 FETs with four different dielectrics [10] [23]. Among these studies on reversible and rapid resistance modulation for VO_2-based devices, our result of hybrid gate insulator (depicted in red

solid square) was distinct from the others at room temperature, as the highest resistance percentage with n_{sheet} (~4 × 10^{12} cm^{-2}). It is noteworthy that, for the case of SiO_2 one plotted in a green solid square, despite n_{sheet} exceeded 10^{13} cm^{-2}, $\Delta R/R_{off}$ (~0.3%) was below the value of hybrid one. It was estimated that hybrid gate insulator caused a substantial modulation of carrier density by field effect.

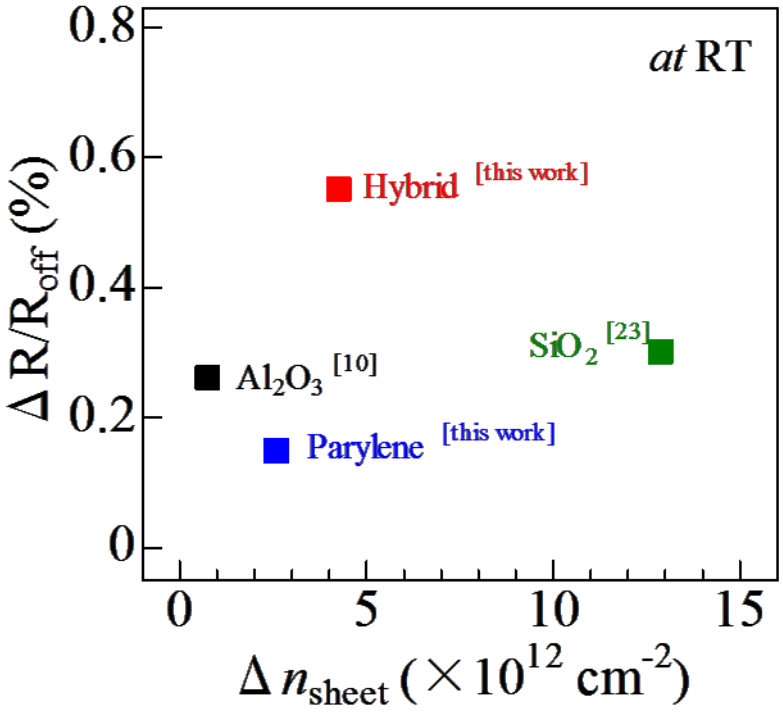

Figure 4.9 A plot of studies on VO_2-based FETs with various gate dielectrics so far, using the parameters of resistance modulation ratio and sheet carrier density. The red and blue solid square represented hybrid gate FET and parylene monolayer-gated FET in this work; the black one depicted as Al_2O_3 back-gated FET from Ref. 10; the green square showed the value for SiO_2-gated FET [23].

4.3.4 Hole-electron asymmetric tuning by electric field

Taking advantage of systematic modulation using parylene-C monolayer and hybrid gated-FETs, furthermore, we demonstrated the pronounced shifts of T_{MI} by gate bias for both devices, as shown in Figure 4.10. Correspondingly, under $\Delta n_{sheet}=1 \times 10^{12}$ cm^{-2}, the average reduction in T_{MI} was approximately ~1.4 K in both gate insulators. T_{MI} was illustrated to be extremely sensitive to positive gate bias as shown on the right panel, which was corresponded to electron doping. Contrarily, the left regime related to hole doping, causes only a slight decline of T_{MI}. Such a significant hole-electron asymmetry associated with the suppression of T_{MI} was also found in cation substitute VO_2 bulk system. Low valent elements substitution for V^{4+}, i.e., Mg^{2+} [24], Al^{3+} [25], Fe^{3+} [26], corresponding to hole doping, reduces T_{MI} tardily; while the pentavalent or hexavalent dopants, i.e., W^{6+} [27], Mo^{6+} [28], Nb^{5+} [29], related to electron doping, introduce abrupt decrease of T_{MI}. In bulk substitution system, it is difficult to separate chemical pressure effect and carrier doping effect. Asymmetric modulation observed in a FET will be an important insight to evaluate carrier doping effect in Mott FET device. Further study would be focused on the origin of this asymmetric system in future.

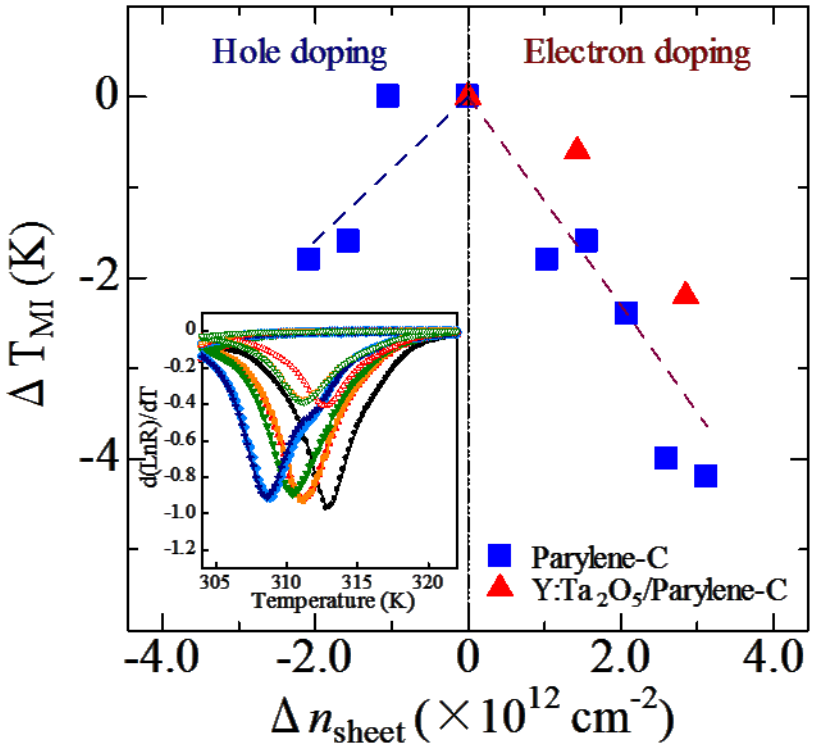

Figure 4.10 An asymmetric hole/electron carrier modulation in VO_2 FETs with hybrid and parylene-C monolayer dielectric. The inset depicts the obvious transition temperature shifts of VO_2 against the gate bias. Open and closed symbols represent negative and positive gate bias, respectively. Black solid dots display the values at V_G=0 V; red triangles, yellow squares, green inverted triangles, blue diamonds, navy crosses were plotted under an applied gate bias stress of ±20 V, ±30 V, ±40V, 50 V and 60 V, respectively.

4.4 Conclusion

In conclusion, reversible and fast resistance switching was achieved *via* effective electrostatic tuning in VO_2-based FETs with hybrid gate insulator, which was considered to effectively reduce interface defects and promote sheet carrier density. The maximum resistance modulation in the insulating regime was verified to appear near T_{MI}. A pronounced shift of phase transition temperature induced by gate bias was demonstrated, and another fascinating behavior on an unequal drop in T_{MI} by hole-electron modulation was observed. Such an asymmetric carrier modulation related to the suppression of T_{MI} triggered by field was found to coincide with that by chemical doping. The results in this part provide a possibility for clarifying the origin of metal-insulator transition in VO_2 through electrostatic field-induced transport modulation. Simultaneously, our findings pave a way for application of oxide thin films-based switch devices with RT control.

4.5 References

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CHAPTER 5

Enhancement of correlated electron mobility by electrostatic carrier modulation in VO_2 nanowire channels

5.1 Introduction

As one of the most representative transition metal oxides with correlated electrons, vanadium dioxide VO_2 has been much attracted attention because of its intriguing properties, for instance, showing obvious resistivity change approximately five orders of magnitude with metal-insulator transition accompanied with a structural transition from low temperature insulating monoclinic phase to high temperature metallic rutile phase, distinct optical property contrast between insulating and metallic phases, and so on [1-3]. Particularly, due to its MIT near to room temperature, its application for implementing electrical switching, such as so-called Mott FETs, has been an attractive issue from last decade [4-6]. Nevertheless, in the few reports on VO_2 thin films-based FETs with a solid gate insulator so far, the resistivity modulation has been quite low value (<0.6%) (~5% in slow switching ones) [7-10]. Many efforts have been attempted to enhance the resistance modulation, which have been mainly tried by inducing giant carrier density due to higher electric field by taking advantage of a high gate dielectric. However, to date, only ionic liquids [11-12] could trigger as high as 10^{14} cm^{-2} sheet carrier density, whereas a slow and irreversible resistance modulation has been reported indicating the presence of chemical reaction in electric double layer-transistors (EDLTs). As a new approach, nanostructure channels, instead of thin

film channels, would be promising because the sensitivity of MIT is intensively responsive to the size that are comparable scale with electronic phase domains, appearing in a drastic resistance jump due to electronic avalanche effects [13-14].

In this chapter, we report enhancement of on/off ratio in VO_2 nanowire-based FETs [15-18], prepared by a ultra-violet nanoimprint photolithography (UV-NIL) technique combined with photolithography method. In contrast to thin film channels, nanowire channels have a superior sensitivity in transport modulation, approximately ten folds higher resistance change than that in thin film channels. As a gate material, high-*k* inorganics Ta_2O_5/organic polymer parylene-C hybrid gate insulator has been adapted to reduce interface defects and keep a high dielectric constant [19-20]. Moreover, we demonstrate the enhanced resistance modulation is owing to logarithmically increased mobility for nanowire-based devices, which was interpreted qualitatively on the basis of strongly correlated electron picture [21].

5.2 Synthesis and properties of nanowires

Various synthetic methods for VO_2 nanowires have been reported, including vapor-liquid solid (VLS) [22-23], chemical vapor deposition (CVD) [24], and solution approach [25]. However, the obstacle for using the nanowires synthesized by these approaches to devices application is the random dispersion and embedding into substrate. Much complex steps related to strip and assemble individual nanowire from the origin substrate have to be carried out. Nanoimprint photolithography (NIL) simplifies the fabrication process and regularly arranges the samples on the substrate with high production. As described in chapter 2, high quality VO_2 nanowires (~ 200 on one chip) with the width of 100-300 nm were synthesized over large area by NIL followed by fabrication of epitaxial VO_2 thin films, which were grown on TiO_2 (001) single crystal substrates by pulsed laser deposition (PLD) using ArF excimer laser at 450°C under an oxygen pressure of 1.0 Pa. Herein, the oxygen reactive ion etching (RIE) was performed with a power of 50 W, a pressure of 4 Pa, a flow of 70 sccm for 150 sec to remove the residue resist in the compressed regions. Subsequently, SF_6 gas was utilized for VO_2 etching (60 W, 1.0 Pa, 10 sccm, and 10 sec). Scanning electron microscope (SEM) was used to confirm the morphology nanowires with high precision, as described in Figure 5.1.

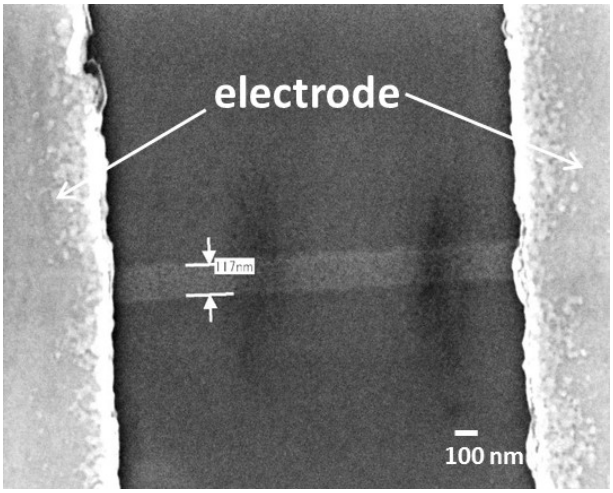

Figure 5.1 A typical morphology of VO_2 nanowire with 120-nm-width.

Temperature dependent resistance measurement was performed to investigate the MIT behavior of the nanowires, as plotted in Figure 5.2. An abrupt MIT without multistep was achieved in all nanowires of different widths, which suggests a high sensitivity of MIT respected to small local variations in temperature for the nanowires.

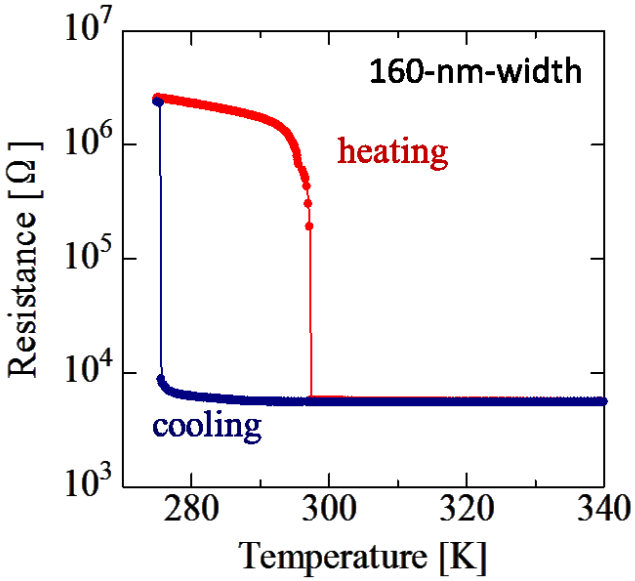

Figure 5.2 R (T) curve for 160-nm-width VO_2 nanowire.

5.3 Enhancement of transport modulation in VO_2 nanowire-based FETs

In this part, we fabricated two types of FET devices, film channel and nanowire channel ones. The film-based FETs were synthesized according to procedures last chapter mentioned. A FET electrodes pattern was directly fabricated onto epitaxial grown VO_2 (001) channel surface through 10 μm thick stainless steel stencil masks. However, this facile approach by stencil mask is restricted in hundreds of microns because of the strict mask alignment technique. For nanowire-based devices, conventional photolithography method substitutes the stencil mask to form the standard three-terminal electrodes pattern. Pt (20 nm)/Cr (5 nm) was sputtered spaced by 2 μm as source-drain contacts; hybrid gate insulator consisted of high-*k* oxide Ta_2O_5 and organic polymer material parylene-C was fabricated subsequently. A 50-nm-thick Au film was deposited by e-beam evaporation as gate electrode. All electrical measurements were performed by an apparatus set up with source-measure unit (2635A, 236, Keithley), within which the attachment Peltier-based stage is responsible to temperature control. Nitrogen gas was supplied to prevent VO_2 surface from humidity [26-27].

5.3.1 High remarkable resistance change in nanowire channels

The as-fabricated FET exhibited a sharp drop in resistance and the hysteresis during heating and cooling process, plotted in Figure 5.3 a, relative to somewhat gradual change for film-based devices in Figure 5.3 b. The main parameters of this device were listed as follows: the width of VO_2 nanowire was 100 nm; the thickness of parylene-C was 80 nm; and the overlay Y: Ta_2O_5 was of 250-nm-thick.

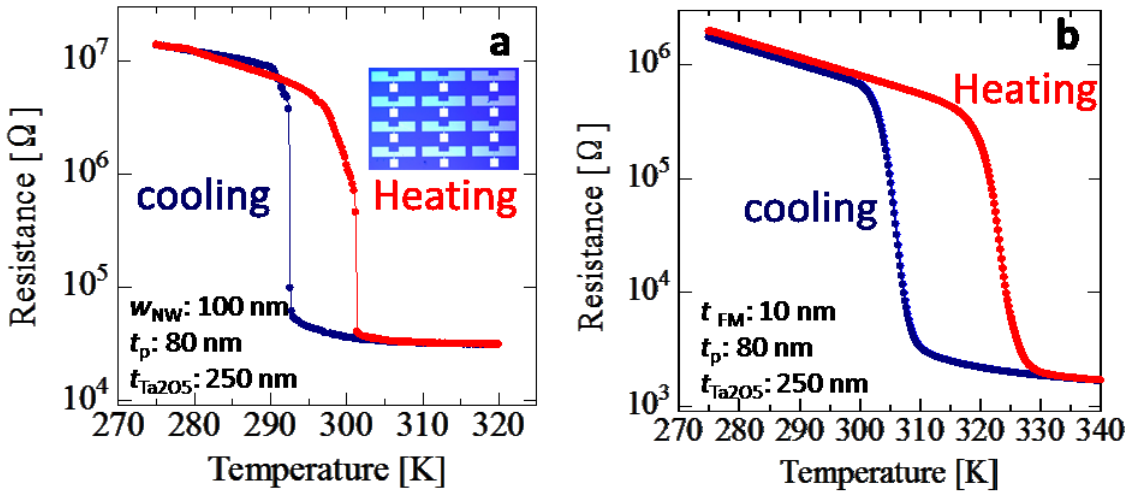

Figure 5.3 (a) and **(b)** Temperature dependent resistance change for 100-nm-width VO_2 nanowire and thin film channel, respectively. Inset of Figure 5.3 (a) Optical image of VO_2 nanowire devices.

To investigate the switching dynamics, the resistance was measured by applying a variety of gate bias (0~±30 V with the internal of 5 V) as a function of time near metal-insulator transition temperature T_{MI}. Since the resistance of VO_2 nanowire

was very sensitive to temperature, a small source-drain voltage V_D=1 V was employed, to hinder possible Joule heating induced by current flowing through nanowire. Each resistance response cycle was observed to follow the trend of gate bias variation, including two processes: a prompt change for initial application of gate bias; a drastic recovery for elimination of operating gate bias. Moreover, the resistance showed an abrupt drop by positive gate voltage; in vise versa, there was a sharp rise in resistance as negative gate bias applied. That is, consistent with previous film-based devices, reversible and prompt resistance response to gate bias was achieved in VO_2 nanowire channel from 280 K to 295 K. On the other hand, the resistance almost unchanged with the variation of gate bias in metallic state (T=300 K). All the data were depicted in Figure 5.4 a-e. It was noted that the leakage current through gate insulator was so small that it can be negligible, and the devices has unbroken until 30 V operating gate bias. For the purpose of comparison to film-based devices, we also fabricated VO_2 film-based FET with the similar thickness of gate insulator. Figure 5.5 a-f exhibit gate bias dependent resistance modulations for thin film-based device. Notably, difference between nanowire and thin film-based devices is in magnitude of resistance modulation by gate bias.

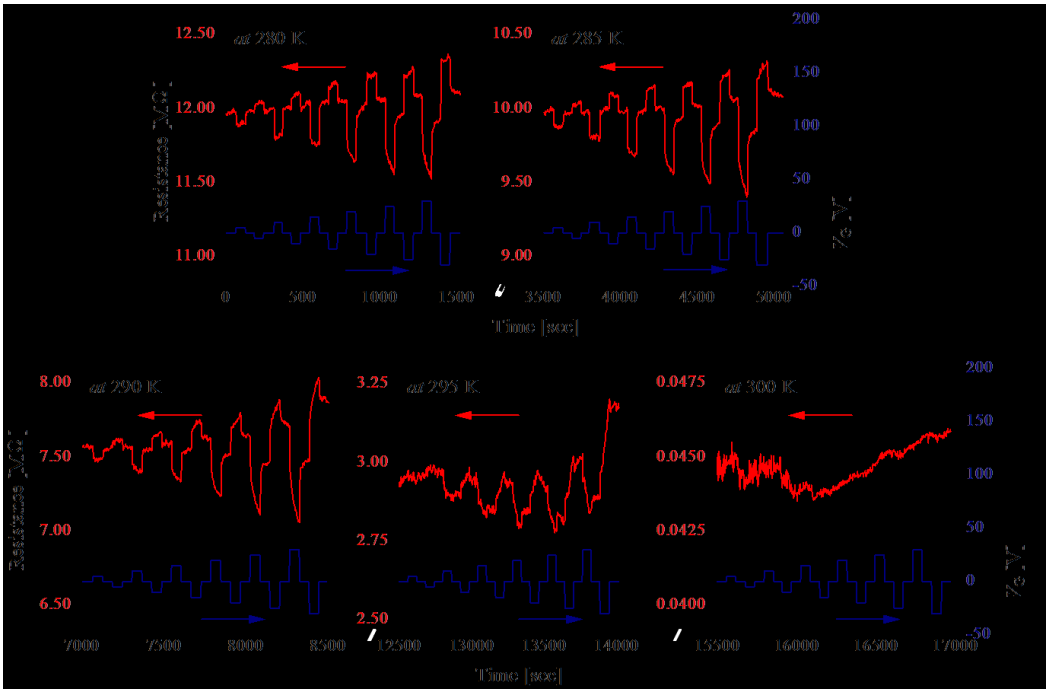

Figure 5.4 (a-e) Response of resistance to gate biases from 280K to 300K for VO_2 nanowire device.

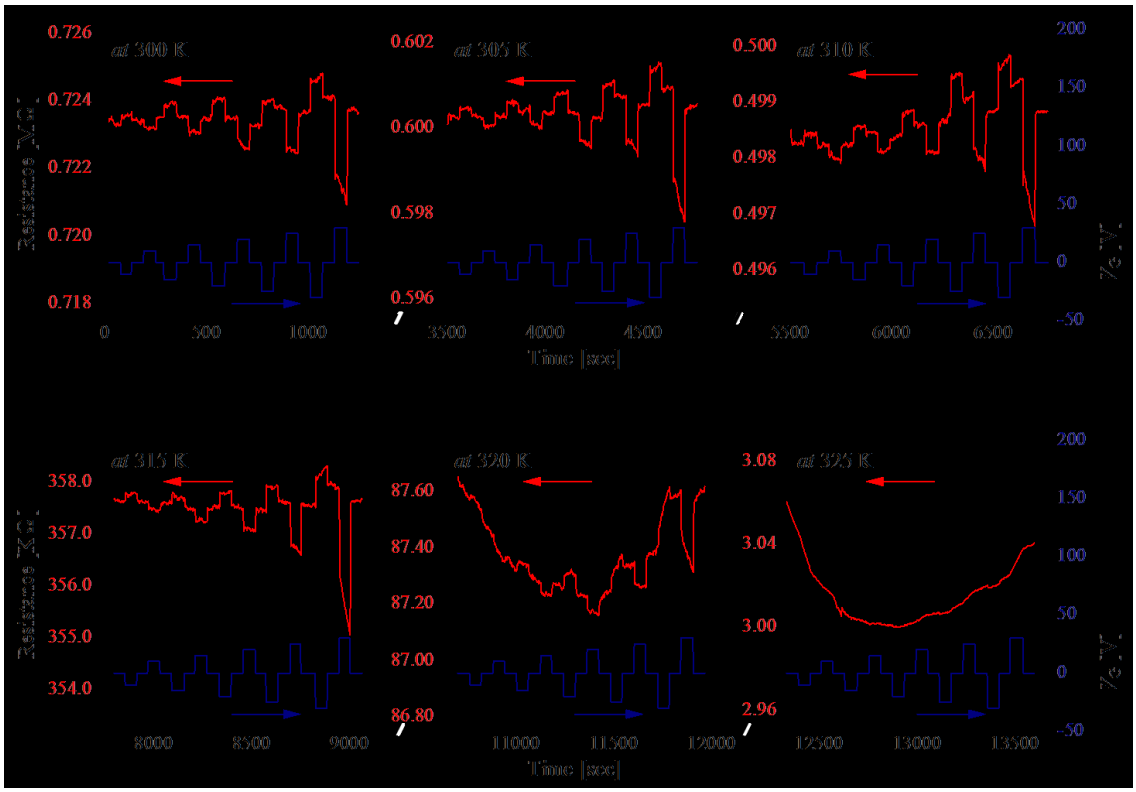

Figure 5.5 (a-f) Gate dependent resistance modulations in VO_2 thin film channel.

5.3.2 The observation of the maximum resistance modulation near phase transition temperature

Regarding the resistance response to the gate bias, the efficiency of resistance modulation is defined as the formula: $\frac{\Delta R}{R_{off}} = \frac{R_{on}-R_{off}}{\mathrm{R}_{off}} \times 100\%$. In nanowire-based FET, the value of resistance change ratio gradually increased from 280 K to 295 K, which is close to the phase transition temperature at each given gate bias, and suddenly became almost zero at 300 K in metallic state as shown in Figure 5.6. Therefore, the maximum of resistance modulation efficiency is close to 8.58% for V_G=±30 V, in vicinity of phase transition temperature at 295 K. The result for film-based devices described in Figure 5.7 has the same tendency. However, the ratio was less than 0.61%. Furthermore, with increasing the gate bias, the resistance modulation efficiency increased linearly in insulating state.

Figure 5.8 illustrated the absolute value of resistance modulation efficiencies as a function of gate bias for both devices near phase transition temperature. The resistance modulation ratio in nanowire channel indicated more sensitive against increasing V_G than that in film ones, and the ratio in resistance modulation in nanowire-based FETs was over 10 times as high, compared with that in the film-based ones.

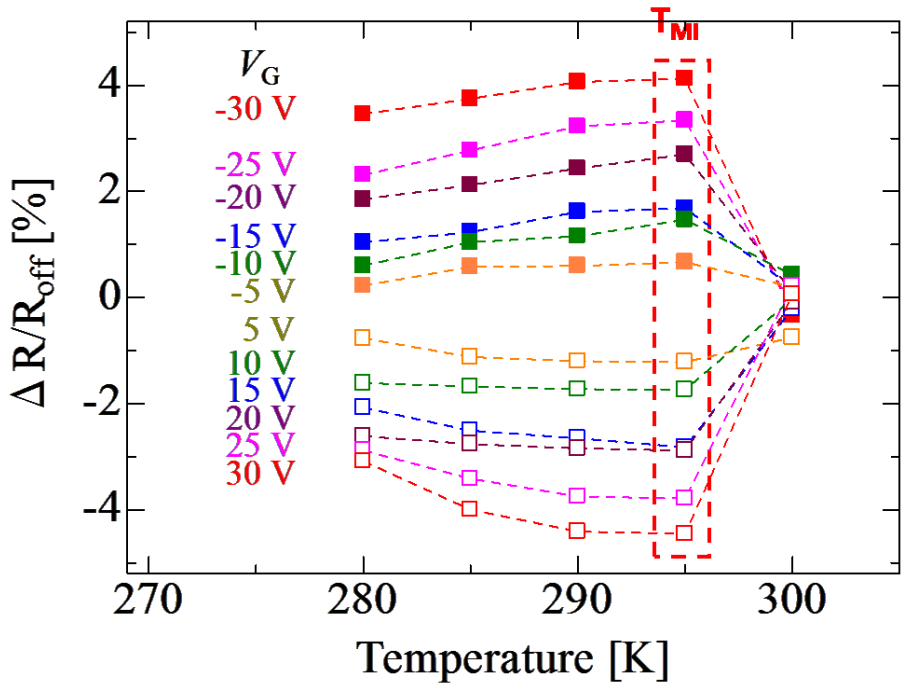

Figure 5.6 Resistance variation efficiency as a function of temperatures at gate bias applied in VO_2 nanowire channel.

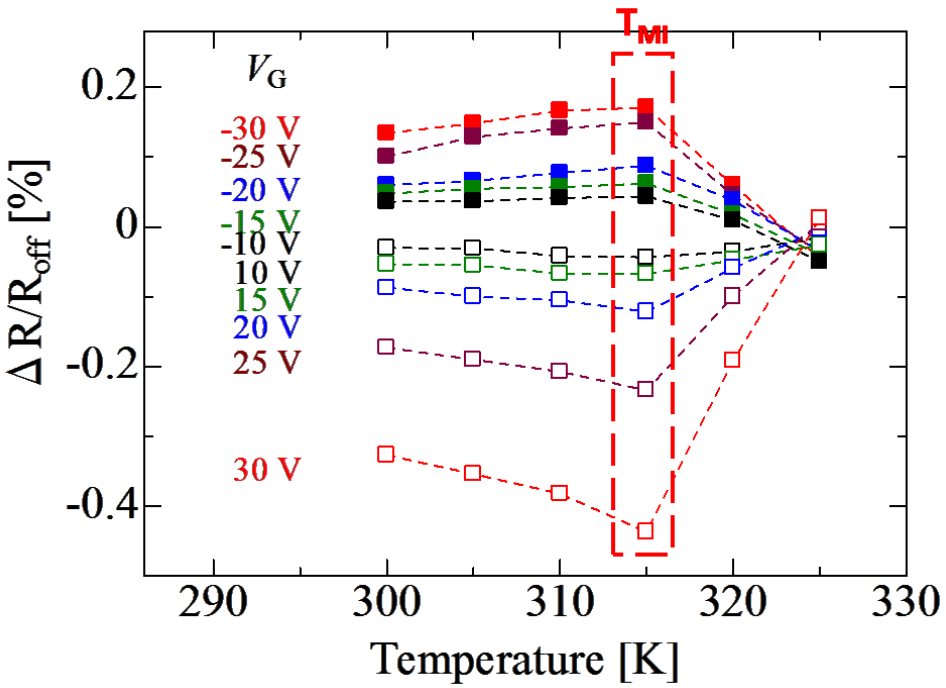

Figure 5.7 Resistance modulation ratios against temperatures for VO_2 thin film-based device.

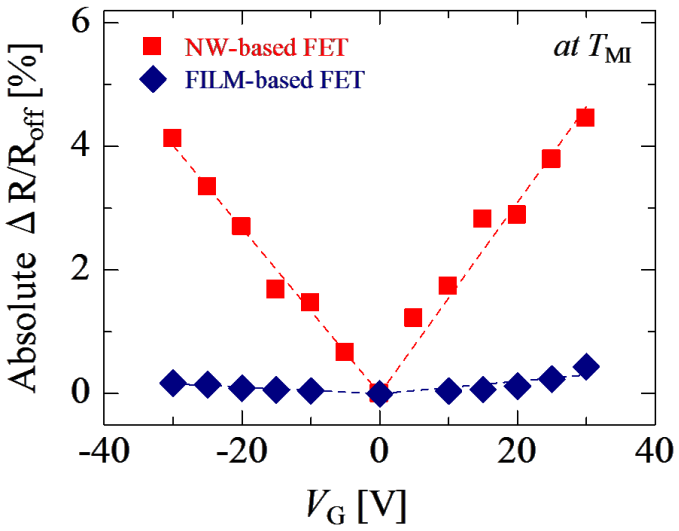

Figure 5.8 Comparison of absolute resistance modulation ratio between nanowire and thin film based-FETs.

5.3.3 Analysis of the origin for enhancement of resistance variation

To clarify the origin of the enhanced resistance modulation in the nanowire-based FETs, we analyzed the electric field distribution for thin film and nanowire channel using simulation based on a Finite Element Method (FEM) Amaze (Advanced Science Laboratory, Inc.), as described in Figure 5.9, resulting the difference. The electric field was uniformly distributed on the surface of thin film channel. On the contrary, the field distribution on nanowire channel exhibited arc shape, and the prevailing field was converged on the edge parts. The electric field value for the edge parts of nanowire channel was enhanced by 1.5 folds towards that of thin film case (in Fig. 5.9 b). However, this estimation cannot explain the experimental result of 10 folds

higher ratio in resistance modulation nanowire-based FETs. Thereby it was suggested that the dominant factor for enhanced resistance modulation is not the number of carrier accumulation due to the electric field distribution.

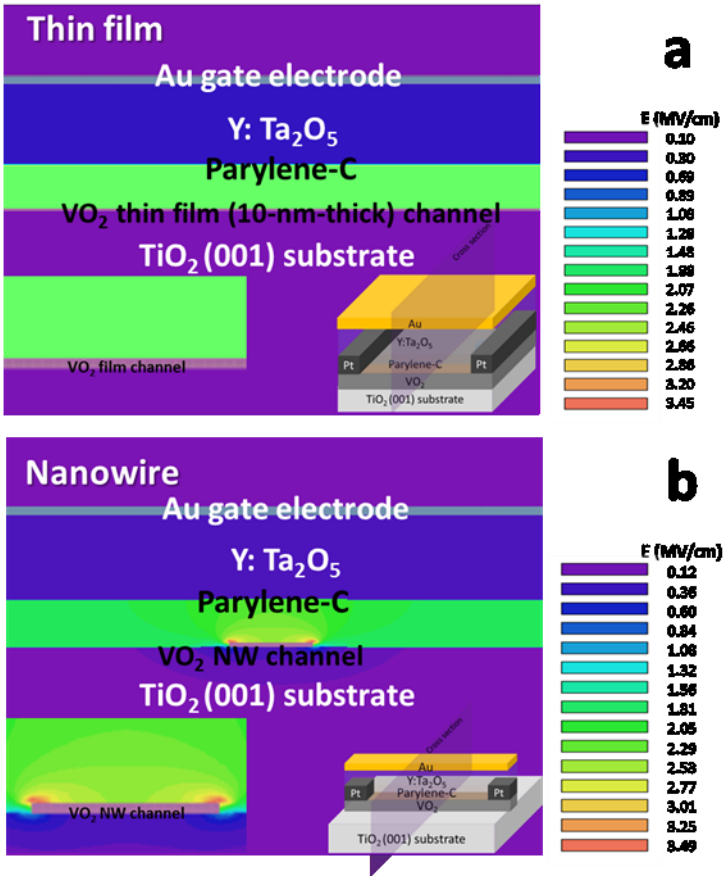

Figure 5.9 (a) and **(b)** describe the electric field strength distribution in nanowire and thin film channels, respectively.

Generally, the resistance modulation efficiency was well corresponded to the trans-conductance g_m defined as Eq. (1)

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_{D=const.}} = C_s \frac{W}{L} V_D \mu_0, \quad (1)$$

where C_s is the capacitance of gate insulator per unit area, W and L are the width and

length of the channel, μ_0 is the Hall mobility. It is noted that here V_D is further less than V_G. Thereby, to give the reasonable explanation of the enhancement in resistance modulation for nanowire channel, we evaluated the field effect mobility μ_{FE} according to Eq. (2) and summarized in Figure 5.10.

$$\mu_{FE} = \frac{1}{C_s}\frac{L}{WV_D}\frac{\partial I_D}{\partial V_G}, \quad (2)$$

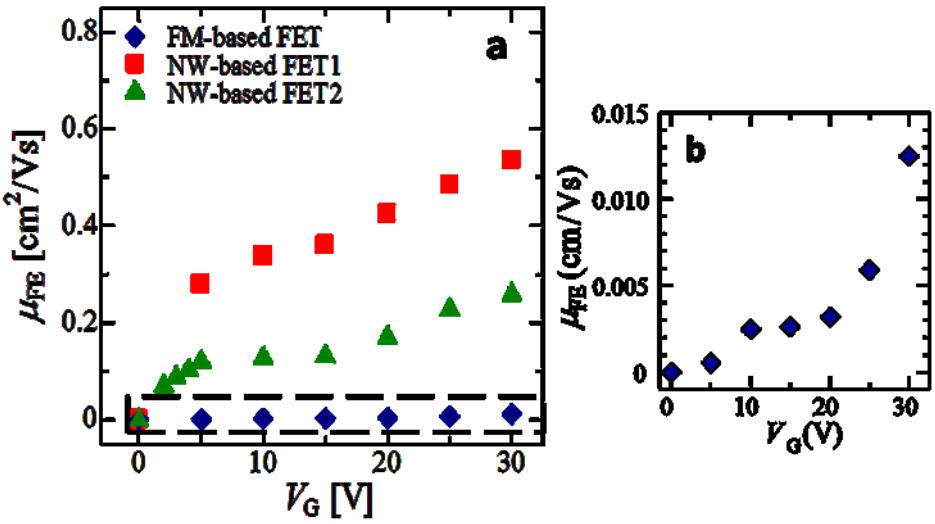

Figure 5.10 (a) A plot of field effect mobility against gate bias for nanowire and film based-FET devices; **(b)** Amplification image for films' case, which remained constant with the addition of gate bias approach to the Hall mobility value as insulating state.

A slight raise of mobility against gate bias was acquired in film-based devices, approximately retaining the constant value close to the Hall effect measurement result in the insulating state (~0.0024 cm^2/Vs), as showed in Figure 5.11. The relative low mobility was considered to induce quite low values in resistance modulation similar to the report in Ref. 28. In contrast to the thin film channels, the nanowire-based FET

displayed a drastic increase of mobility with addition of gate bias, and reached approximately 0.5 cm^2/Vs at V_G=30 V, approaching to the Hall effect measurement value reported as metallic state in rutile phase (~0.4 cm^2/Vs). These results indicate that mobility enhancement is important factor for the origin of the enhanced resistance modulation for nanowire channel.

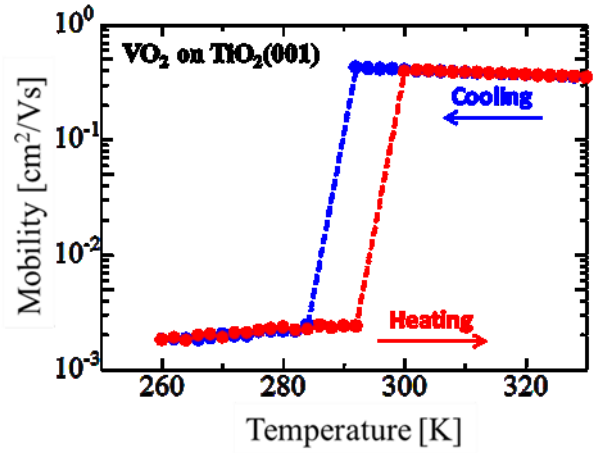

Figure 5.11 Hall electron mobility measured as a function of temperature. The electron mobility increased almost 2 orders of magnitude from insulating state to metallic state. It was noted that electron is confirmed as the major carrier consistent with the recent report [29].

Usually, the electric field-effect would only induce carrier concentration modulation for conventional semiconductors; it would yet tailor not only the carrier density but also change the mobility for correlated oxides. To confirm the above statement, we attempted to deduce the relationship between the mobility and induced carrier concentration. According to Brinkman-Rice (BR) picture [21, 30] based on the

Gutzwiller variational theory [31], the effective mass of a quasiparticle m^* was expressed by the following Eq. (3)

$$\frac{m^*}{m} = \frac{1}{1-\left(\frac{U_{eff}}{U_C}\right)^2}, \tag{3}$$

where U_{eff} is the effective energy, U_C is the critical on-site Coulomb interaction. Further replacing the parameters with $U_{eff} = \frac{\langle e \rangle^2}{r} = \frac{\rho^2 e^2}{r}$, $U_C = \frac{e^2}{r}$, according to the extended BR picture [32]. Eq. (3) would be transferred to Eq. (4)

$$\frac{m^*}{m} = \frac{1}{1-\rho^4} \tag{4}$$

It was noted that the measured charge $\langle e \rangle$ is represented as ρe, indicating the average charge acting at the system, that is, an effective charge per site. Hence, the band filling factor ρ directly impacts on the effective mass in Eq. (4). The effective mobility μ^* can be derived by $m^* = \frac{e\langle \tau \rangle}{\mu^*}$. Assuming $\langle \tau \rangle$ is a constant against carrier modulation, Eq. (4) is described as follow:

$$\frac{\mu^*}{\mu_0} = \frac{m}{m^*} = 1 - \rho^4 = 1 - \left(\frac{n_0 - \Delta n}{n_0}\right)^4 \tag{5}$$

Where n_0 is the initial carrier density without V_G and Δn is the density of accumulation carrier by applying V_G. Thus the band filling can be represented as $(n_0 - \Delta n)/\, n_0$. Thereby, we can draw the ρ vs μ^* curves of Eq. (5) as μ_0 is a fitting parameter in the inset of Figure 5.12 indicating ρ vs μ^*. Although the stronger field in the edge parts (1.5 folds stronger) of nanowire-based devices produces small change in carrier density Δn,

the effective mobility would yield biquadratic enhancement. Therefore, the enhanced mobility in the edge parts of nanowire-based FETs is a main trigger for 10 folds enhancement of resistive switching ratio compared with that in thin film-based FETs. The experimental Hall and electric field mobility were plotted in the inset, approximately following the calculated dot curve in the BR picture. In correlated materials, modulation of mobility due to small change of carrier density would be a crucial parameter contributing to the large resistance modulation.

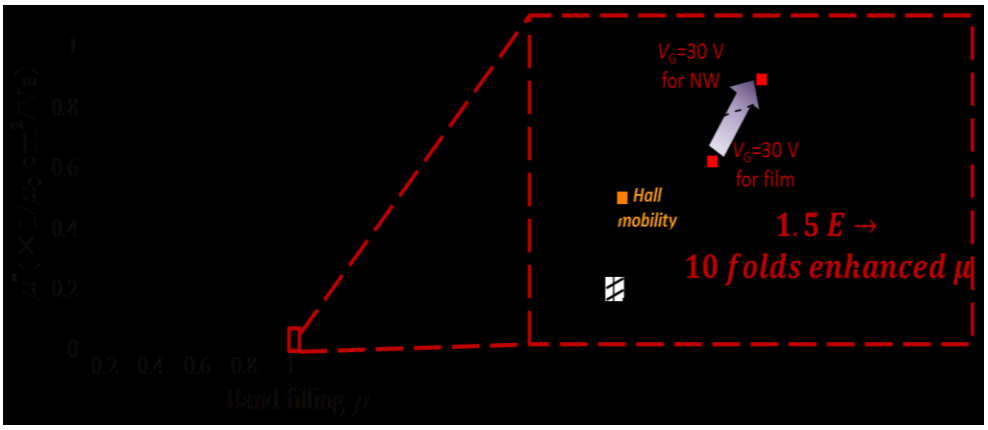

Figure 5.12 The correlation of the effective mobility and band filling. Focused regime showed the effective mobility versus the band filling. The experimental results were plotted as red squares, orange square exhibited the hall mobility of insulating state, and the dash line gave the curve fitting according to Brinkman-Rice picture.

5.4 Conclusion

In summary, a superior sensitivity in resistance modulation was realized through decreasing channel scale down to nanometer scale size (100 nm) in VO_2 nanowire-based FETs devices synthesized by a nanoimprint lithography technique, with hybrid gate insulator for the first time. Moreover, I found the maximum resistance modulation efficiency in the vicinity of transition temperature. On the basis of electric field distribution simulation and Brinkman-Rice picture representing mobility enhancement by small band filling variation, I newly proposed that the enhancement in resistance modulation for nanowire channel was primary due to the logarithmic like-increment of mobility on the edge parts of nanowire-based devices, and found this proposed model will explain experimental results. These results open an insight into probe the underlying properties for strongly correlated oxides, and provide possibility for exploiting nano-devices for high performance next generation electronics.

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CHAPTER 6

Summary and prospect

In this thesis, I investigated the electrical transport modulation in correlated oxide VO_2 employing hybrid gate insulator composed of inorganic high-*k* material Ta_2O_5 and organic polymer material parylene-C.

Chapter 3 has devoted to fabricate the hybrid gate insulator, and achieved relative high effective dielectric constant *via* the verification of series connection mode. According to the practical application into band semiconductor $KTaO_3$, the as-fabricated hybrid gate insulator was illustrated to provide excellent hetero-interface due to protection of parylene-C and giant carrier density for sufficient electrostatic modulation owing to contribution of high-*k* oxide Ta_2O_5 layer. In addition, such a hybrid gate insulator was suggested to supply the low operating gate voltage through the thickness adjustment of two layers.

Following, I have tailored the transport properties in VO_2 thin film channel taking advantage of this hybrid gate insulator in chapter 4. A reversible and prompt resistance variation was switched by gate bias, which indicated the transport properties were attributed to pure electrostatic effect excluding oxygen migration, chemical reaction or joule heating. Moreover, the maximum resistance modulation was observed in the vicinity of transition temperature approximately 0.6%, which was five-fold higher than that of parylene-C monolayer-gated FETs. It was well explained by the promoted

sheet carrier density induced by electric field.

In chapter 5, I have further enhanced the sensitivity in resistance through decreasing the channel scale to nanometer in VO_2 active channel. In addition, I have realized the enhancement of maximum resistance variation (8.58%) near transition temperature, which was over ten-fold larger than films' case. On the basis of electric field distribution simulation and BR picture, we firstly proposed that the enhancement of mobility was the predominant factor for the enhanced in resistance modulation in strongly correlated system.

Through systematical investigations on electrical transport properties of correlated oxide VO_2 thin films and nanowires, I have constantly enhanced the resistance modulation, and achieved the highest value in the all-solid-gated FETs so far as plotted in Figure 6.1. Moreover, I have demonstrated the significance of a solid-gate-insulator to induce electrostatic transport modulation for strongly correlated system and supplying possibility for exploiting low-dimensional devices for next generation electronics.

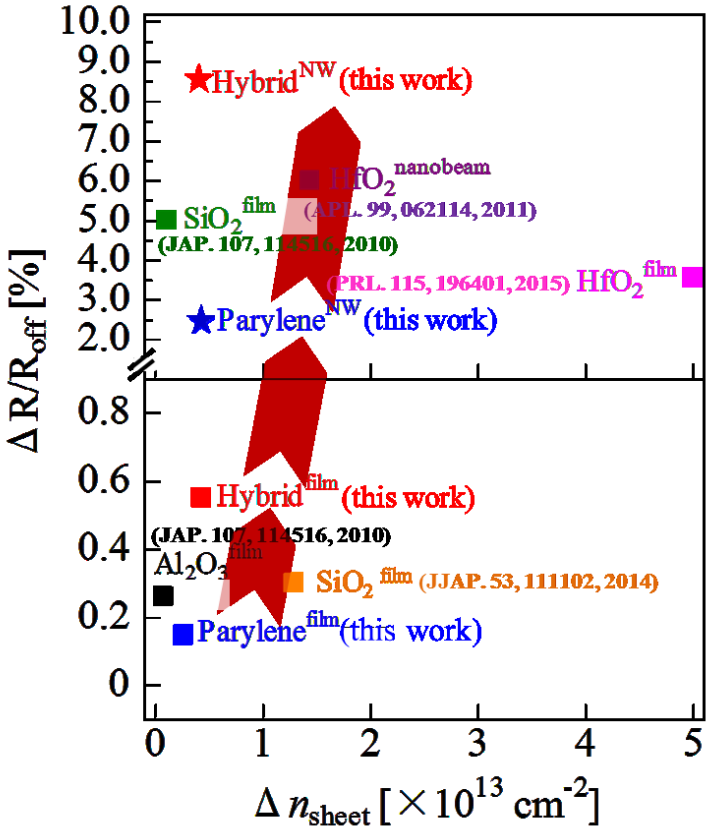

Figure 6.1 A list of studies on VO_2-based FETs with various gate dielectrics so far, using the parameters of resistance modulation ratio and sheet carrier density. The pink arrow indicated the enhanced progress in resistance variation in this Ph.D. research.

For now, our illustration of the characteristics related to nanoscale VO_2 definitely provides an avenue for probing underlying nature, further research in this regime is expected to give an explicit answer for the controversy between Peierls and Mott-Hubbard MIT. As mentioned above, the future directions of this theme can be separated to two: One is to further induce carrier density up to critical value to realize MIT behavior through the thickness control of hybrid gate insulator; The other one is to

scale down the size of nanowire to domain size, taking advantage of which would drastically raise the resistance modulation beyond the limitation of the Moore's Law in size and conventional semiconductor theory. My achievement in this thesis would be the important foundation towards these prospective to clarify the nature of correlated system and broaden the practical application in electronic devices.

List of Publications

[1] Scientific Journal

[1-1] "Impact of parylene-C thickness on performance of $KTaO_3$ field-effect transistors with high-*k* oxide/parylene-C hybrid gate dielectric"

T. Wei, K. Fujiwara, T. Kanki, and H. Tanaka

J. Appl. Phys. **119** (2016) 034502.

[1-2] "Electric field-induced transport modulation in VO_2 FETs with high-*k* oxide/ organic parylene-C hybrid gate dielectric"

T. Wei, T. Kanki, K. Fujiwara, M. Chikanari and H. Tanaka

Appl. Phys. Lett. **108** (2016) 053503.

[1-3] "Enhancement of electrical transport modulation in high-*k* Ta_2O_5/organic polymer parylene-C hybrid gate dielectric coated VO_2 nanowire field-effect transistor"

T. Wei, T. Kanki, M. Chikanari, T. Uemura, T. Sekitani and H. Tanaka

In preparation.

[1-4] "Electrostatic carrier modulation-mediated enhancement of correlated electron mobility in single crystalline VO_2 nanowires"

M. Chikanari, T. Kanki, **T. Wei**, and H. Tanaka

In preparation.

[2] International Conference

[2-1] "Electrostatic carrier doping to transition-metal oxides via organic parylene-C insulator"

T. Wei, K. Fujiwara, and H. Tanaka

The 18th Sanken Nanotechnology Symposium, Osaka, Japan (Dec. 2014) (Poster)

[2-2] "Electric field-induced resistance switching in VO_2 channels using hybrid gate dielectric of High-*k* Ta_2O_5/Organic Parylene-C"

T. Wei, T. Kanki, K. Fujiwara, and H. Tanaka

The 19th Sanken Nanotechnology Symposium, Osaka, Japan (Dec. 2015) (Poster)

[2-3] "Electric Field-induced Resistance Switching in VO_2 Channels using Hybrid Gate Dielectric of High-*k* Ta_2O_5/Organic material Parylene-C"

T. Wei, T. Kanki, K. Fujiwara, M. Chikanari and H. Tanaka

The March Meeting 2016 of the American Physical Society (APS), Baltimore, Maryland, USA (Mar. 2016) (Oral)

[3] Domestic Conference

[3-1] "High-*k* oxide/organic polymer hybrid gate structure for oxide field-effect transistors"

T. Wei, K. Fujiwara, and H. Tanaka

The 75th JSAP Autumn Meeting, Hokaido University, Japan (Sep. 2014) (Poster)

[3-2] "Electrostatic carrier doping to transition-metal oxides via organic parylene-C insulator"

T. Wei, K. Fujiwara, and H. Tanaka

第 2 回アライアンス若手研究交流会　大阪大学　(Nov. 2014) (Poster)

[3-3] "Electrostatic carrier doping to $KTaO_3$ using organic parylene-C/high-*k* oxide hybrid gate insulator"

T. Wei, K. Fujiwara, and H. Tanaka

The 62nd JSAP Spring Meeting, Tokai University, Japan (Mar. 2015) (Oral)

[3-4] “Electric-field induced carrier modulation in VO_2 FETs with organic parylene-C/high-*k* oxide hybrid gate dielectric”

T. Wei, T. Kanki, K. Fujiwara, and H. Tanaka

The 76th JSAP Autumn Meeting, Nagoya Congress Center, Japan (Sep. 2015) (Oral)

[3-5] “Resistance switching in VO_2 field-effect transistors with high-*k* Ta_2O_5/organic parylene-C hybrid gate dielectric”

T. Wei, T. Kanki, K. Fujiwara, and H. Tanaka

CEMS Topical Meeting on Oxide Interfaces 2015, Riken, Japan (Nov. 2015) (Poster)

[4] Related papers as appendix

[4-1] “Growth and Extension of One-Step Sol-Gel Derived Molybdenum Trioxide Nanorods via Controlling Citric Acid Decomposition Rate”

S. Cong, T. Sugahara, **T. Wei**, J. Jiu, Y. Hirose, S. Nagao, and K. Suganuma

Cryst. Growth Des. **15** (2015) 4536

[4-2] “Diverse Adsorption/Desorption Abilities Originating from the Nanostructural Morphology of VOC Gas Sensing Devices Based on Molybdenum Trioxide Nanorod Arrays”

S. Cong, T. Sugahara, **T Wei,** J. Jiu, Y. Hirose, S. Nagao, and K. Suganuma

Adv. Mater, Interfaces. **4** (2016) 1600252

Acknowledgements

I have spent a splendid time at Osaka University in these four years. Here I would like to express my appreciation to those who contributed to this dissertation.

First and above all, my heartfelt thanks to my advisor, Professor Hidekazu Tanaka of Institute of Scientific and Industrial Research, Osaka University. Under his guidance, I have continuously enriched my knowledge from a layman. His enthusiasm and cautious attitude in research affect me deeply.

Second, I am indebted to Associate Professor Teruo Kanki for his valuable supervision and guidance in experiments. He is one of the nicest associate professors I have ever met. And his wisdom always leads me to the right direction when I encounter problems.

Special thanks to Dr. Kohei Fujiwara of Institute for Materials Research, Tohoku University, for experiment training, advices in research theme and discussion at the first two years. Although he was strict with me at first, his intelligence and ability convince me. From him, I have mastered experiment methods, correct way of thinking, and more than physics.

I would like to acknowledge Dr. Azusa Hattori for her help not only in research but also in my daily life.

I want to express my appreciation to the secretary Ms. Tomoko Okumoto for contributing immensely in innumerable small things during my study at Tanaka lab.

I am also grateful to Ms. Michiko Sakuma, and the other members in Tanaka lab. Forgive me for not enumerate their names here. I'm extraordinarily fortunate to study and work with them. They have supported me, encouraged me and rejuvenated me because most of them are 10 years younger than me. It is also because of them, I can deeply understand Japanese culture.

I want to express the sincere thanks to my family. My parents had achieved relative good education in China, so they focused on my interests much more than others since I was a child. Motivated by them, I had a great interest in science, and was very firm to pursue an advanced degree even if I was over 30 years old and have a son. I appreciate their education and continuous support to me, including the help for taking care of my son all these years. Last but the most important, I thank my husband, who is also a Ph.D student in Osaka University. Although he has always been much busier than me, he helps me to afford homework without any complaint. Simultaneously, his inspiration in various ways brings me positive energy and makes me persist to complete PhD course.

This dissertation is dedicated to my son and new baby who will be born soon!