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論文内容の要旨

This thesis discusses reliability-aware coarse-grained reconfigurable architectures. Bridging the gap between Application Specific Integrated Circuits (ASICs) and microprocessors, reconfigurable devices gained a remarkable popularity in the last couple of decades. Just as many times as computer software can be updated, hardware now can be updated as well. These revolutionary devices introduced a new class of flexibility in hardware design and implementation. The reconfigurable device domain is divided into fine-grained reconfigurable devices, such as Field Programmable Gate Arrays (FPGAs), and coarse-grained reconfigurable devices.

Unlike FPGAs, conventional coarse-grained architectures lack reliability consideration in their designs, and they are not capable of reliability-demanding computing. With the aggressive process technology scaling, many reliability issues are becoming more pronounced. They are mostly dominated by process variation expressed as randomness in device properties, environmental variations such as voltage and temperature fluctuation, negative bias temperature instability (NBTI) and soft errors. For this purpose, reliability consideration in the design process of coarse-grained reconfigurable devices should be taken into account.

On the other hand, FPGAs have been dominating the reconfigurable computing device domain due to their flexibility, universal capabilities, and their standard HDL/C programming model. Despite that coarse-grained architectures are much more superior in there processing power, dramatic reduction in configuration memories yielding in smaller silicon area, less power consumption, and less placement and routing efforts, they are not successful in gaining popularity. This is traced back to the weakness of the programming model and to the fact that they require some special constraint of programming to optimally utilize their hardware. Briefly stated, there is a strong need for coarse-grained architectures to standardize their programming models, and establish compatibility with existing tools, such as high level synthesis tools.

Addressing these issues in coarse-grained architectures, this thesis proposes a coarse-grained dynamically reconfigurable architecture with an embedded mechanism enabling flexible reliability. The reliability level for each basic element is individually selected, and the overall achieved reliability is tuned to match the designer requirements and reduce the excessive area and power overhead. The reliability issues addressed in this architecture are NBTI and soft errors. Application specific acceptable soft error rates are accomplished by mitigating soft errors with partial spatial redundancy. NBTI is mitigated through regularly swapping active elements with relaxing ones. In order to effectively decide which part of the application requires a higher reliability consideration, a model needs to be established to correlate a specific mapping of the application with the mean time to failure (MTTF) and the failure in time (FIT) rate. Upon deciding the acceptable FIT rate, a corresponding application mapping can be generated by trading area with FIT rate. For this purpose, radiation tests on a test chip fabricated in a 65 nm process were carried out, and the experiment results show that the MTTF and the FIT rate are well characterized with the number of sensitive bits, which is a variable estimated solely through simulation. A model was extracted, and the minimum resources necessary to achieve the required FIT rate are identified using this model.

Next, this thesis addresses reliability threats that are composed of process, voltage and temperature variations (PVT). Such variations cause timing failures in the circuit. In the reconfigurable devices domain, guard-bands are still utilized to accommodate the process, power supply voltage, and temperature variations. This thesis investigates mitigation techniques for PVT variation-induced timing errors. Such techniques include path-replica circuits, circuit-replicas, and time-shifted redundant circuits. Experiments were performed using a fabricated chip, and the results of each technique are compared and analysed. For an approximately similar false positive error probability for the path-replica and circuit-replica, the false negative error probability of circuit-replica is approximately two orders of magnitude less than that of the path-replica circuits. When attaining a false negative of zero, the probability of error detection and re-execution is higher in path-replica circuits than in time-shifted circuits by one order of magnitude or more.

Finally, addressing the compatibility issue with compilation tools in coarse-grained reconfigurable devices, a mixed-grained reconfigurable architecture with flexible reliability is investigated for gaining compatibility with high level synthesis tools. This architecture is composed of a mixture of fine-grained processing elements with coarse-grained ones. This architecture strongly exploits multi-step processing through dynamic reconfiguration. The fine-grained fabric is used to implement state machines, conditional statements, and control signals, while the coarse-grained fabric is in charge of the intensive data processing, and data storage. This architecture allows the ease of implementing state machines and utilizing dynamic reconfiguration required for high level synthesis tools.

As a conclusion, this thesis addresses very important issues in the coarse-grained reconfigurable device domain. This thesis takes a comprehensive approach towards enhancing and promoting coarse-grained reconfigurable architectures by devising several architectures, by introducing and evaluating techniques and mechanisms for various reliability issues in coarse-grained architectures concerning soft errors, NBTI and PVT variations, and by demonstrating architectural designs to increase the compatibility of coarse-grained reconfigurable architectures with high level synthesis tools.

論文審査の結果の要旨

本論文は、信頼性を考慮した粗粒度再構成可能アーキテクチャに関する研究の成果をまとめたものであり、以下の主要な結果を得ている。

1. 柔軟な信頼性をもつ粗粒度再構成可能アーキテクチャの実装

これまでに提案されてきた粗粒度再構成可能アーキテクチャは、性能のみが追求され、高信頼アプリケーションの実装に適さなかった。本論文では、ソフトエラーと経年劣化に対して、柔軟な信頼性が実現できる粗粒度再構成可能アーキテクチャを提案した。基本構成要素毎に信頼性モードを設定できるアーキテクチャであり、同一アプリケーションに対しても連続的な信頼性と面積のトレードオフが提示できる。提案アーキテクチャを65nmプロセスで試作し、アルファ線源を用いて照射実験を行った。測定結果より、平均故障間隔がセンシティブビット数で特性付けられることを示し、必要十分な信頼性を持つマッピングの実現を可能とした。

2. レプリカ回路と時間冗長性を利用したタイミングエラー検出精度の評価

プロセス、電源電圧、温度ばらつきによって生じるタイミングエラー検出手法を調査した。設計マージン、動作マージンを削減することを目的とし、パスレプリカ、回路レプリカ、時間多重回路の有効性を、試作チップを用いて実験的に評価した。同程度の偽陽性確率を実現したパスレプリカと回路レプリカを比較し、回路レプリカの偽陰性確率が2桁程度小さいことを示した。動的な電源ノイズに対してゼロ偽陰性確率を達成する場合、時間多重回路はパスレプリカ回路と比較して一桁小さい再実行確率となることを確認した。

3. 複数粒度再構成可能信頼性可変アーキテクチャの提案

高位合成技術が利用可能な信頼性可変再構成可能アーキテクチャを考案した。提案アーキテクチャは細粒度構成要素と粗粒度構成要素の両方から構成され、複数サイクル処理を容易に実装できるよう、毎サイクル切り替え可能な命令レジスタをALUに実装した。データパスは粗粒度構成要素を、状態遷移機械は細粒度構成要素を用いて実装する。提案アーキテクチャを65nmプロセスで試作し、画像アプリケーションによる基本動作を確認した。

以上のように、信頼性を考慮した粗粒度再構成可能アーキテクチャに関する研究は、高信頼アプリケーションを高性能な粗粒度再構成可能アーキテクチャ上で実現できる点で非常に有用である。これにより、VLSIシステムの信頼性向上に貢献するものと期待できる。従って、博士（情報科学）の学位論文として価値のあるものと認める。