Doctoral Dissertation

Germanium-Tin-Based Optoelectronic Integration Utilizing Nucleation-Controlled Liquid-Phase Crystallization

Hiroshi Oka

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Department of Material and Life Science
Graduate School of Engineering
Osaka University

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Chapter 1 Introduction

1.1 Background

1.1.1 Development of Advanced Information Society

In recent years, due to the expansion of internet and spread of personal information technology (IT) devices such as computers, smartphones and tablet-type portable terminals, the amount of information distribution is now significantly increasing. It has been predicted that the internet traffic throughout the world reaches 121000 Gbps (=121 Tbps) by 2025, which is about 190 times larger than that in 2005 (Fig. 1-1(a)) [1]. With the rapid growth of information society, the power consumption of IT devices is considerably increasing. As shown in Fig. 1-1(b), the IT power consumption in Japan increased year by year and it reaches 2500 billion kWh at 2025, [1] which is 20% of the domestic electric generation amount in Japan. Under such background, sustainable development and multi-functionality is required for IT device to deal with the advanced information society.

1.1.2 Improvement of Semiconductor Device Performance

1.1.2.1 Scaling Limit of Silicon (Si)-based Integrated Circuit

Up to this day, the growing of advanced information society is accomplished by the development of Silicon (Si)-based large-scale integrated circuit (LSI). LSI is an electronic circuit formed on semiconductor microchip that is composed of

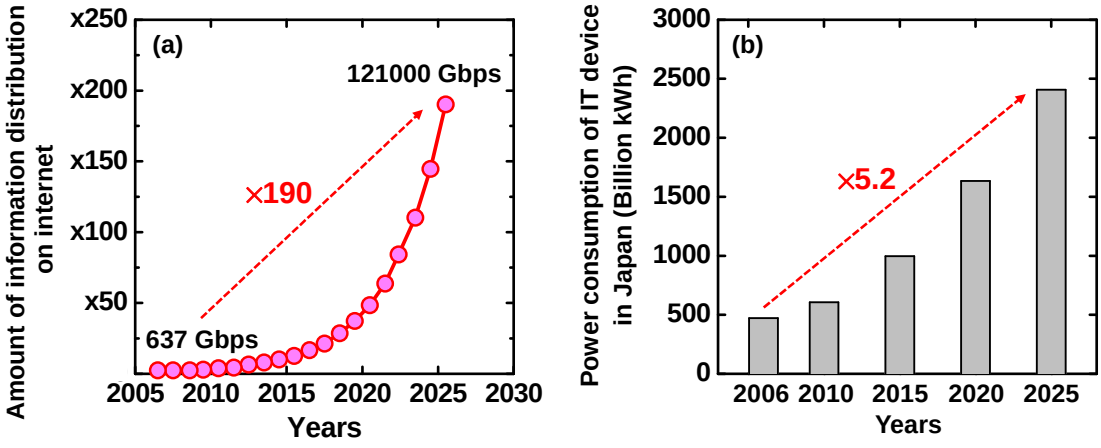


Fig. 1-1 (a) Amount of information distribution on worldwide internet as function of years. (b) Transition of power consumption of IT devices in Japan. [1]

transistors. The metal-oxide-semiconductor field-effect transistor (MOSFET) is a popular type of transistor and a key component of LSI, which is now most widely used. [2]

The basic characteristics of MOSFET is switching and amplifying the electrical signals. The MOSFET is fabricated on a single-crystalline semiconductor substrate and consisted of gate electrode, gate insulator and source/drain (S/D) region with four electrical terminals as shown in Fig. 1-2. The S/D region is heavily-doped and has opposite conduction type to substrate (when substrate is p-type, S/D region should be n^+-type). The gate stack has a metal-oxide-semiconductor (MOS) structure, which act as a capacitor. Since the electrical charges under the gate stack can be controlled by applying the gate voltage, the current flowing from source to drain region can be controlled and electrically switches on- and off-states of the device. The equation of drive current of MOSFET is also shown in Fig. 1-2. The drive current depends on the gate voltage, and it is proportional to gate width (W), carrier mobility (μ_{eff}) and capacitance of gate oxide (C_{ox}), while inverse proportional to gate length (L). Here, the carrier mobility is the average drift velocity of hole and electron which is specific to semiconductor material (in the case of Si, mobility of hole and electrons are 1600 and 430 cm^2/Vs, respectively). Therefore, scaling of the dimension of device size (gate length) is effective to increase the drive current of MOSFET and improve the performance of LSI. In the past few decades, Si-MOSFET has been aggressively scaled down and significantly increased number of transistor on a microchip. This scaling of MOSFET has been achieved with the rule generally known as Dennard scaling [3]. In the Dennard scaling, in order to keep the electric field in transistor constant, the dimension of device size

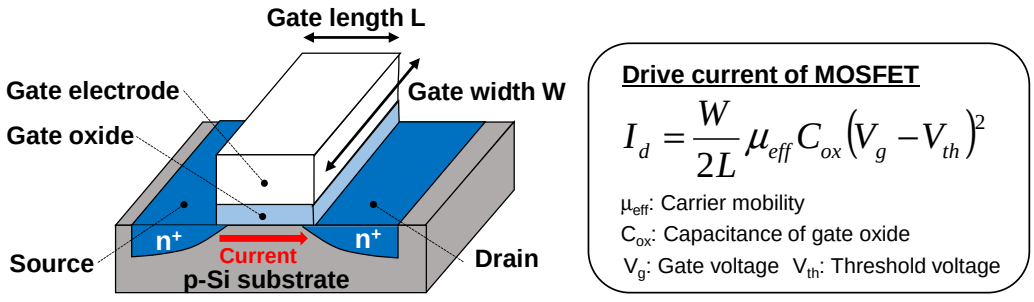
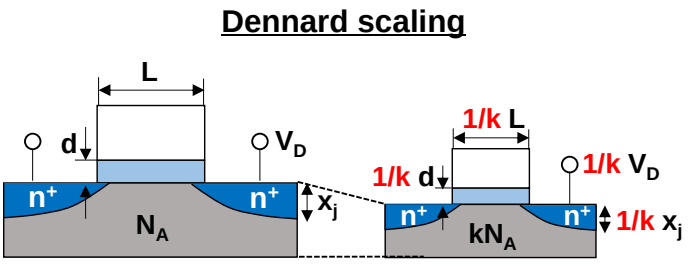


Fig. 1-2 Schematic illustration of structure and equation of drive current of MOSFET.



Device parameters	Scaling factor
Gate length	1/k
Gate width	1/k
Gate oxide thickness	1/k
Delay time	1/k
Power consumption	$1/k^2$
Electric field	1

Fig. 1-3 Dennard scaling of MOSFET.

and other parameter such as a gate oxide thickness reduced by 1/k, which leads to decrease in delay time and power consumption of MOSFET by 1/k and $1/k^2$, respectively (Fig. 1-3). This is an attractive approach to improve the performance of LSI. As shown in Fig. 1-4, the minimum feature size of transistor is about 10000 nm (= 10 μm) at 1970, the size scaled down exponentially year by year.

However, when the minimum feature size reached 100 nm or less around 2010, it have become difficult to improve the transistor performance with conventional scaling due to the physical limitations such as gate leakage current and the short channel effects [4]. The representative short channel effects are limitation imposed on carrier drift characteristics and the threshold voltage shift in the aggressively scaled channel. In order to deal with these problems and keeping up the performance improvement, several approaches have been explored and introduced into the scaled MOSFET, which is generally called "technology boosters". For example, high-permittivity (high-*k*) gate insulator

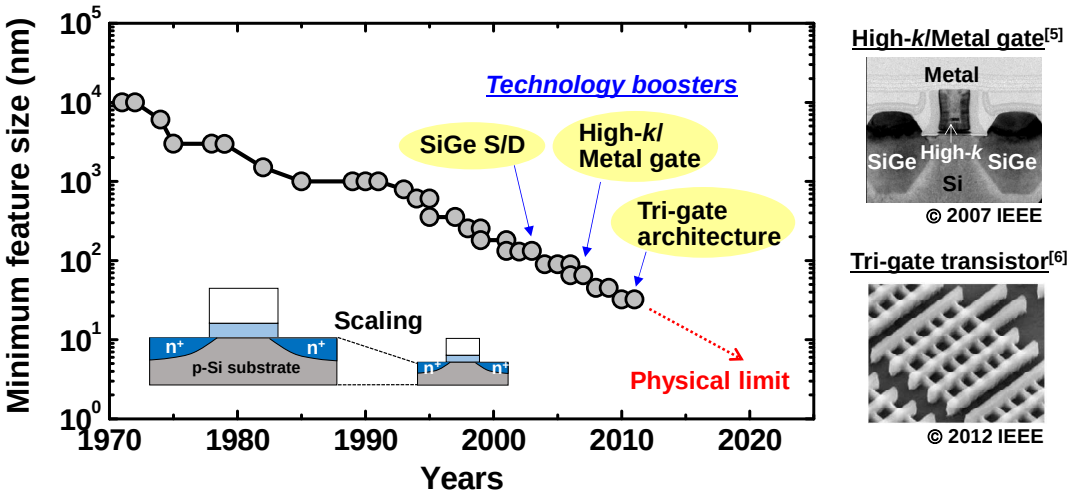


Fig. 1-4 Scaling of Si-MOSFET (minimum feature size as function of years).

was adopted instead of silicon dioxide (SiO_2), which can reduce the equivalent oxide thickness (EOT) and suppress the gate leakage current [5]. Also, the architecture of transistor have been also changed from the conventional planar transistor to non-planar tri-gate transistor to provide a better drivability and electrostatic control to the channel [6]. By combining above innovative technology, the performance of sub-90-nm node transistor have been enhanced until now. However, although the great effort has been paid to keeping up the scaling of MOSFET, the minimum feature size is now reaching sub-10 nm and it has become difficult to improve the performance of Si-based MOSFET.

Furthermore, in addition to the scaling limit of Si-MOSFET, the interconnect delay becomes severe performance limiting factor of the LSI. In the current LSI, a copper wire has been used to transfer electrical signals which connects device to device (Fig. 1-5) [7]. In general, the processing speed of LSI is determined by transistor gate delay (switching time) and interconnect delay. With the dimension of transistor decreased and the number of transistor integrated on a chip increased, the resistance-capacitance (RC) delay of the copper interconnections has become a severe bottleneck for data processing. As shown in Fig. 1-6, while the gate delay decreased with decreasing the line width (gate length), the interconnect delay increased with decreasing the line width and crossover happened at a line width of around 0.2 μm, and it shows rapid increase [8]. This results in degradation of processing speed and increase in power consumption.

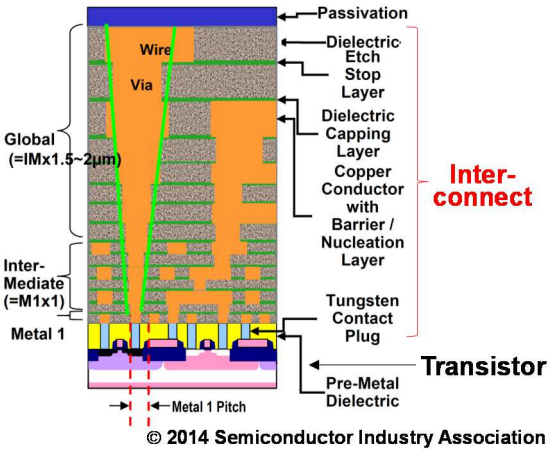


Fig. 1-5 Cross-section illustration of LSI [7].

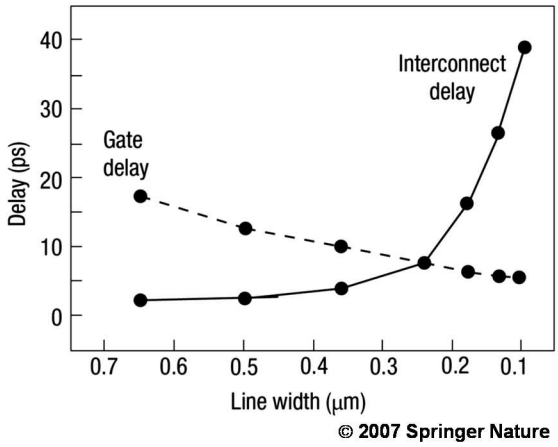


Fig. 1-6 Trends in gate delay and interconnect delay as function of line width. [8]

Therefore, in order to continue the development of advanced information society, alternative technological solutions that break the limitation of conventional Si-LSI are now strongly required.

1.1.2.2 High-Mobility Channel

As mentioned in the above session, the conventional Si-based LSI is now facing with the physical limitation in performance improvement for both device and interconnection side, and the technological breakthrough is strongly desired.

One of the promising approach is the introduction of high-mobility channel material instead of Si. As shown in Fig. 1-2, the drive current of MOSFET is proportional to carrier mobility. Thus, it has become possible to improve the device performance which does not rely only on the scaling. Table 1-1 summarizes carrier mobility for typical group-IV and III-V semiconductor materials. In order to construct a digital logic circuit, both p- and n-channel MOSFET (i.e. complementary MOSFET, CMOS) is required so that the semiconductor material which has high hole and electron mobility is desired. The III-V semiconductors such as Indium-gallium-arsenide (InGaAs) and Indium-arsenide (InAs) show a very high electron mobility. On the other hand, there is no advantage in hole mobility compared to Si. Also, in order to introduce a high-mobility channel material into advanced logic circuit seamlessly, compatibility to a mature Si-CMOS technology is required. However, III-V elements behave as impurity for group-IV semiconductor (p- or n-type dopants), which is a severe obstacle to implement III-V channel using conventional Si technology.

Germanium (Ge) is a group-IV semiconductor as in the case of Si, thus it has an advantage in process integrity with Si-CMOS technology and there are no

Table 1-1 Carrier mobility for typical group-IV and III-V semiconductors.

Semiconductor	Group	Bandgap (eV)		Mobility (cm^2/Vs)	
		Direct	Indirect	Electron	Hole
Silicon (Si)	IV	3.4	1.1	1600	430
Germanium (Ge)	IV	0.80	0.66	3900	1900
Gallium arsenide (GaAs)	III-V	1.4	1.7	9200	400
Indium arsenide (InAs)	III-V	0.36	1.1	40000	500

concern about cross contamination. Although the electron mobility is lower than that of typical III-V semiconductors, Ge has both high electron and hole mobility compared to Si, which makes it attractive material for post-Si channel material.

1.1.2.3 Si Photonics

Another approach to improve the performance of LSI is an electronic and photonic integration on a microchip based on group-IV semiconductors, which is generally called Si photonics. In this session, current status and technological outlook of Si photonics were described.

As mentioned in session 1.1.2.1, with the size of transistor decreased and number of transistor per chip increased, the interconnect delay becomes bottleneck for data transfer in the LSI due to the RC delay of copper interconnect. Thus, alternative technological solution for the massive data transfer is strongly desired in the post-scaling era. One of the most attractive approach to overcome this issue is the implementation of optical interconnect instead of conventional electrical interconnect, in which the high-density and high-speed data transmission is possible. In the long distance data transmission, the optical interconnect have been already introduced and widely used until now. Figure 1-7 shows the trend in the information-carrying capacity of a single line (metal wire or optical fiber) as a function of year [8]. The displacement of electric interconnection to optical fiber was carried out around 1990, and the information capacity was significantly increased more than three order of magnitude

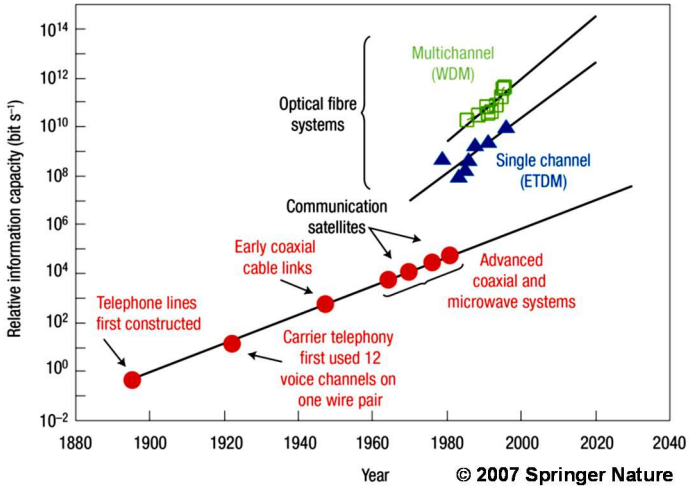


Fig. 1-7 Trend in the information-carrying capacity of a single line (metal wire or optical fiber) as function of year and technology [8].

compared to conventional metal wire, which clearly indicates the advantage of optical data transmission. Therefore, realization of optical interconnection at the level of electronic microchip would be an ideal approach to break the physical limitation of processing bandwidth in the current LSI.

So far, photonic devices such as light emitting diode (LED) or photodetector have been developed based on III-V semiconductors such as InP or GaAs, which have a direct bandgap structure and offer highly efficient light emission/detection (Fig. 1-8). Since Si has an indirect bandgap, phonon assistance is required for carrier recombination and thus luminescence efficiency is fundamentally poor. In order to enable the optical interconnect on an electronic microchip, an integration of photonic devices on a Si-platform is required. Although heterogeneous integration of III-V-based photonic devices on Si substrate using a wafer bonding or epitaxy would be one of solutions [9], there are several disadvantages in the cost, large-volume manufacturing and process integrity to conventional Si-CMOS technology. Thus, integration of group-IV-based optical devices on Si-platform would be an ideal approach to enable the optical interconnect.

Among the group-IV material, Ge has an indirect bandgap structure, but the energy difference between Γ and L valleys in conduction band is only 0.14 eV ($E_{g\ Direct}$: 0.80 eV, $E_{g\ Indirect}$: 0.66 eV), which is much smaller than the energy difference of Si (2.3 eV). Since the wavelength corresponding to the direct bandgap of Ge (E = 0.80 eV, λ = 1550 nm) is within the telecom optical wavelength range currently used, it has been regarded as promising group-IV material to enable optical interconnection on the Si-platform. In order to improve

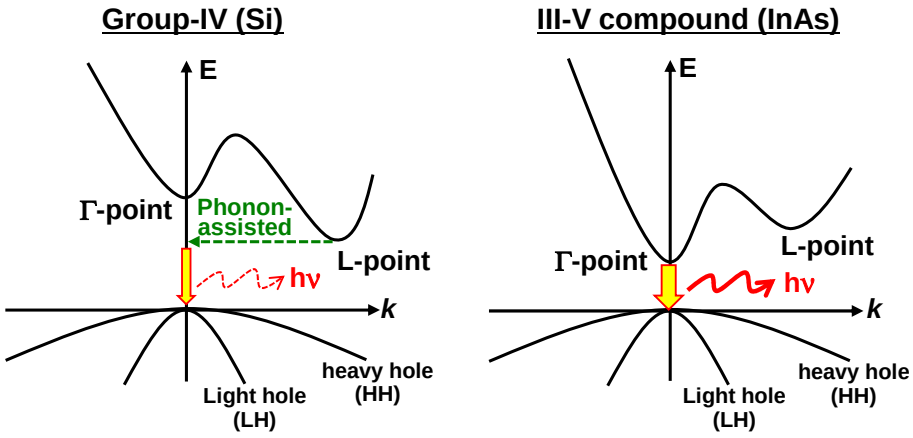


Fig. 1-8 Band structure of group-IV (Si) and III-V semiconductors (InAs).

the light emission/detection efficiency of Ge to compete with the III-V semiconductors, several approaches have been explored to modulate the band structure, such as inducing tensile strain or n-type doping [10,11]. From the theoretical calculation, by applying the tensile strain to Ge, the direct bandgap decreased faster with respect to indirect bandgap. Therefore, the energy difference between Γ- and L-valley reduced and thus enhancing light emission/detection efficiency (Fig. 1-9(b)). It is predicted that Ge exhibits the indirect-to-direct bandgap transition by applying biaxial tensile strain for about 1.5% [10]. Also, the increase in electron population at L-valley by n-type doping promotes the electron injection into Γ-valley and also improves the light emission efficiency of Ge (Fig. 1-9(c)).

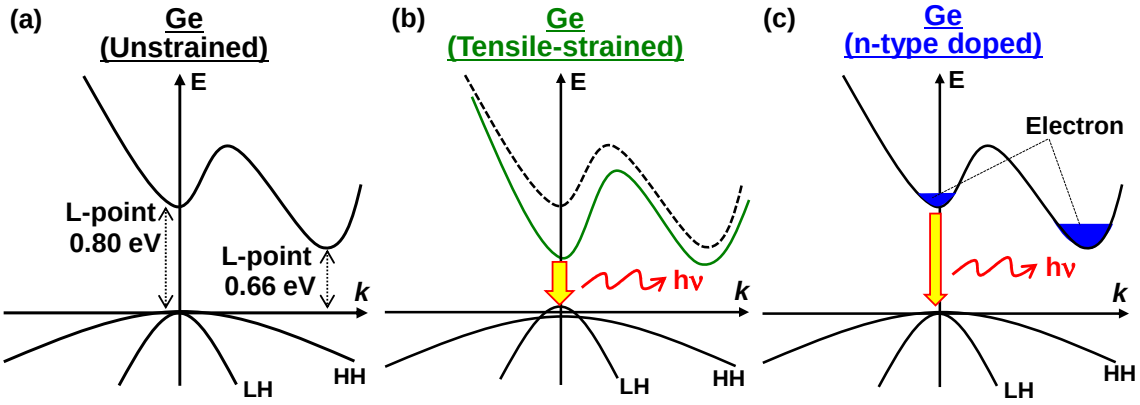


Fig. 1-9 Band structure of (a) unstrained Ge, (b) tensile-strained Ge, and (c) n-type doped Ge.

As described in this session, Ge is a promising group-IV material in the post scaling era for its high carrier mobility and unique band structure, and the Ge-based technology is expected to break the physical limitation of Si-based LSI.

1.2 Germanium-Tin (GeSn) Alloy

As mentioned in the previous session, introduction of high-mobility channel material and implementation of Si photonics are attractive post-scaling technology, and Ge is regarded as a most promising post-Si material. So far, great efforts have been paid to modulate band structure of Ge and to exhibit enhanced electronic and photonic properties by strain engineering. However, it is quite difficult to form direct bandgap Ge since biaxial tensile strain as high as 1.5% is

required for indirect-to-direct transition [10].

Recently, group-IV mixed crystal, germanium-tin (GeSn) alloy, has gained a significant interest due to its improved electronic and photonic properties with respect to Ge thanks to its tunable band structure. In this session, the band structure, optoelectronic properties and application fields of GeSn alloy were described in detail.

1.2.1 Band Structure

Recently, GeSn alloy has attracted a significant interest for both electronic and photonic applications due to its tunable band structure. Sn is a group-IV semi-metal element, which has a nearly zero bandgap [12]. An incorporation of Sn into Ge modulates the band structure and reduces the energy of Γ- and L-valleys in conduction band as illustrated in Fig. 1-10. Although Ge has an indirect band structure, GeSn alloy shows indirect-to-direct bandgap transition by incorporating certain amount of Sn because the Γ conduction valley decreases faster than the L valley. Recent theoretical calculations predicted incorporating

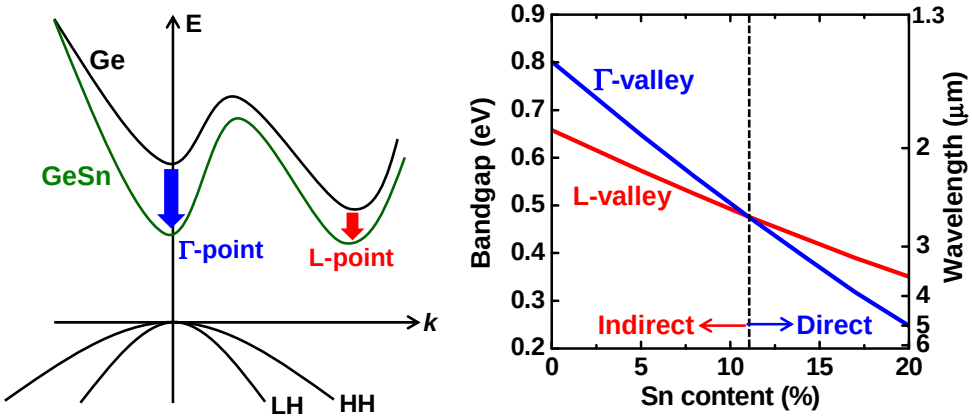


Fig. 1-10 Electronic band structures of GeSn alloy [13].

around 6-10% of Sn is required for indirect-to-direct bandgap transition (Fig. 1-10) [13,14]. Due to this bandgap modulation by GeSn alloy, significantly improved electronic and photonic properties have been expected as described in following session.

1.2.2 Theoretical Calculations of Electronic and Optical properties

Due to the tunable band structure of GeSn alloy, it has become possible to

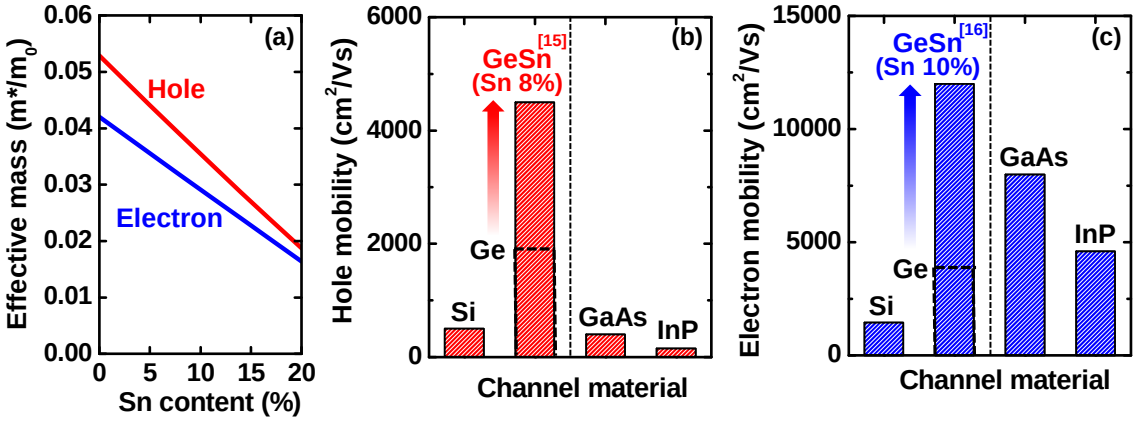


Fig. 1-11 Theoretical calculations of (a) carrier effective mass [13], (b) hole mobility [15] and (c) electron mobility [16] in GeSn alloy.

realize group-IV-based high-performance electronic and photonic devices. Theoretical calculations predict that the both hole and electron effective mass in GeSn reduce with increasing Sn content (Fig. 1-11(a)) [13]. Since carrier mobility is inverse proportional to effective mass, enhancement in both hole and electron mobility are expected. Figure 1-11(b) and 11(c) show theoretical calculation of hole and electron mobility in GeSn alloy in comparison with group-IV and III-V semiconductors, respectively [15,16]. The predicted hole mobility of GeSn is much higher than that of Si (1600 cm^2/Vs) or Ge (3900 cm^2/Vs), and it also outperform the electron mobility of III-V semiconductors. Therefore, GeSn alloy is only semiconductor material having high hole and electron mobility. Also, since GeSn alloy is a group-IV mixed material, it can be easily introduced into conventional Si technology.

In addition to the improved electronic property, GeSn alloy is also attractive for Si photonics. With increasing Sn content, the energy difference between Γ and L valleys in conduction band decreases as shown in Fig. 1-10. Thus, improved light emission/detection efficiency is expected. Also, as a result of bandgap shrinkage of GeSn alloy, a corresponding cut-off wavelength extends to longer which reaches beyond 2 μm (Fig. 1-12) [17]. Figure 1-13 shows the wavelength range and its photonic applications together with corresponding semiconductor materials. As mentioned before, Ge has a direct bandgap of 0.80 eV and corresponding cut-off wavelength is 1550 nm, which is matched to conventional optical data transmission (C-band). In the wavelength range beyond

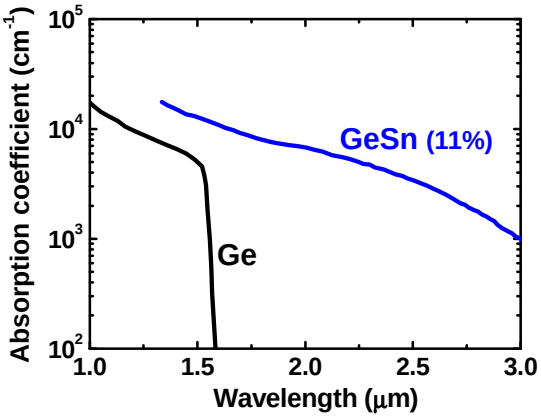


Fig. 1-12 Absorption coefficient of Ge and GeSn [17].

1550 nm and around 2000 nm, there are many emerging applications including extended optical transmission bands, near-infrared (NIR) imaging [18] and biochemical sensing [19]. Since bandgap of GeSn alloy matches to these wavelength range, it has become possible to fabricate GeSn-based photonic components that enables not only massive and high-speed data transmission with an optical interconnect but also NIR imaging and sensing on a semiconductor microchip.

As described in this session, in addition to the superior electronic property such as high hole and electron mobility compared to other group-IV and III-V semiconductors, GeSn alloy has a great potential for NIR photonic applications. Therefore, monolithic integration of GeSn-based electronic and photonic devices is a promising post-scaling technology to break the physical limitation of Si-LSI.

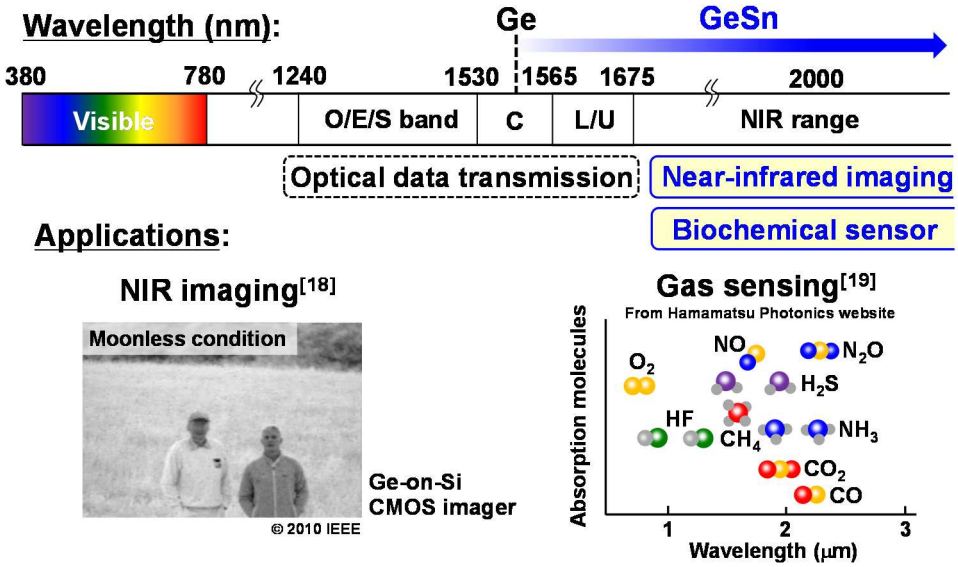


Fig. 1-13 Bandgap of GeSn alloy and its photonic application fields.

1.3 Issues in Crystal Growth of GeSn Alloy

As described in the previous session, GeSn alloy has an excellent electronic and photonic properties and is familiar to conventional Si-CMOS process. Thus, it is considered to be one of the most attractive group-IV material for breakthrough the scaling limit of Si-LSI. It offers advanced electronic and photonic integrated circuit that would be applicable to not only optical data transfer but also imaging, environmental or medical fields.

However, it is quite difficult to obtain high-quality GeSn crystal due to the lack of suitable crystallization method, which is a severe obstacle to fabricate GeSn-based optoelectronic devices. In this session, technological outlook and key challenges of crystallizing GeSn alloy are described.

1.3.1 Epitaxial Growth on Si Substrate

In the case of crystal growth of GeSn alloy, a low equilibrium solid solubility limit of Sn in Ge as low as 1% [20] and a large lattice mismatch between Sn and Ge or Si [21] are severe obstacles (Fig. 1-14). To deal with these issues and provide a single-crystalline GeSn layer with high Sn content, non-equilibrium low-temperature epitaxial growth technique has been widely used in recent years. “Epitaxy” means a growth of single-crystalline thin-film on top of the crystal face of another single-crystalline substrate. Thanks to the compatibility of group-IV GeSn alloy to Si process, GeSn layer can be grown on a Si substrate. A method such as molecular beam epitaxy (MBE) or chemical vapor deposition (CVD) are commonly used for epitaxial growth of GeSn layer.

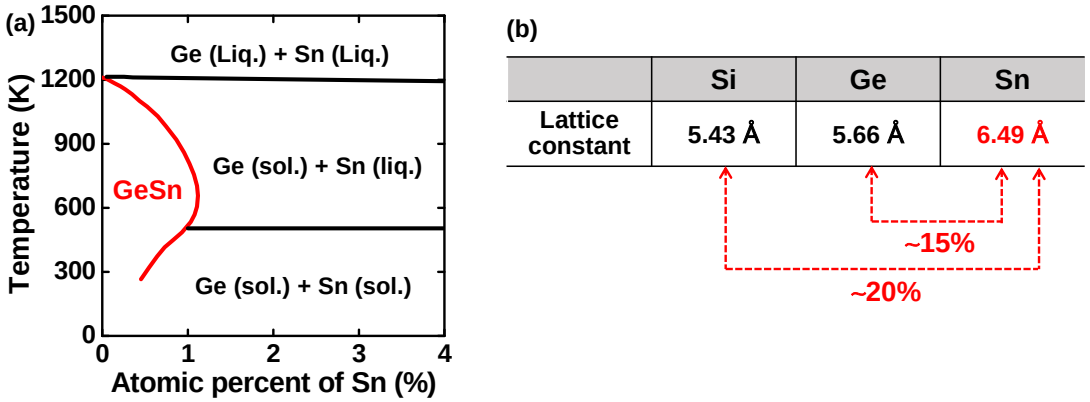


Fig. 1-14 (a) equilibrium solid solubility of Sn in Ge [20]. (b) Lattice constant of Si, Ge and Sn [21].

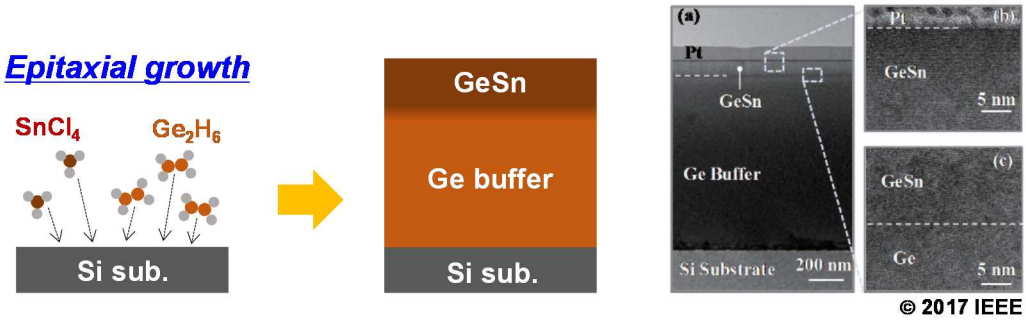


Fig. 1-15 Schematic illustration of single-crystalline GeSn layer grown on Si substrate by CVD system [22].

Figure 1-15 show the schematic illustration of single-crystalline GeSn layer grown by CVD system [22]. Precursors such as Ge_2H_6 and $SnCl_4$ were commonly used. By using these techniques, single-crystalline GeSn layer with a Sn content up to 12.5% has been grown via thick Ge buffer layer [23].

However, due to the large difference in lattice constant between GeSn and Si, dislocations are induced in epitaxially-grown GeSn layer, which deteriorate crystalline quality (Fig. 1-16) [24]. Although thick Ge buffer with a thickness of a few hundred nm to a 1 μm can mitigates dislocations, it is not suitable for fabricating electronic and photonic devices in stacked structure or in-plane integration. Moreover, unfavorable compressive strain was inevitably induced in epitaxially-grown GeSn layer, which lifts up the both Γ- and L-valleys in conduction band and offset the effect of Sn alloying.

Despite the drawback of epitaxial growth methods, great effort has been paid in recent years and direct bandgap GeSn lasers have been successfully

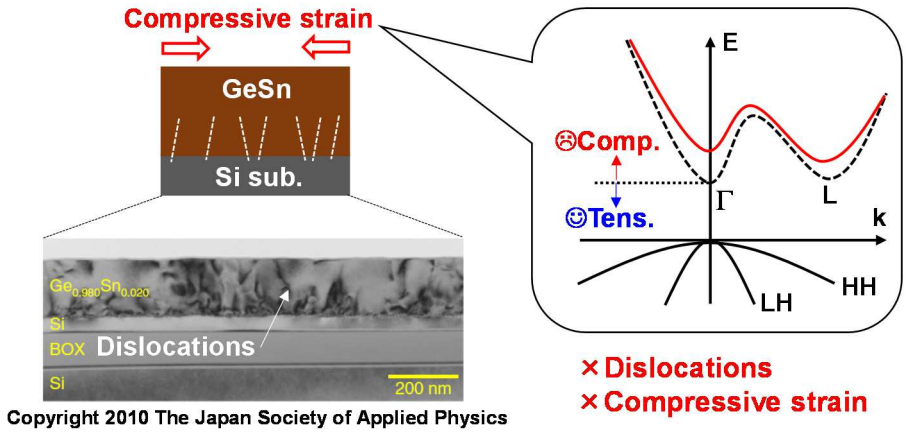


Fig. 1-16 Issues in epitaxially-grown GeSn layer. Dislocations and compressive strain are inevitably induced due to lattice mismatch.

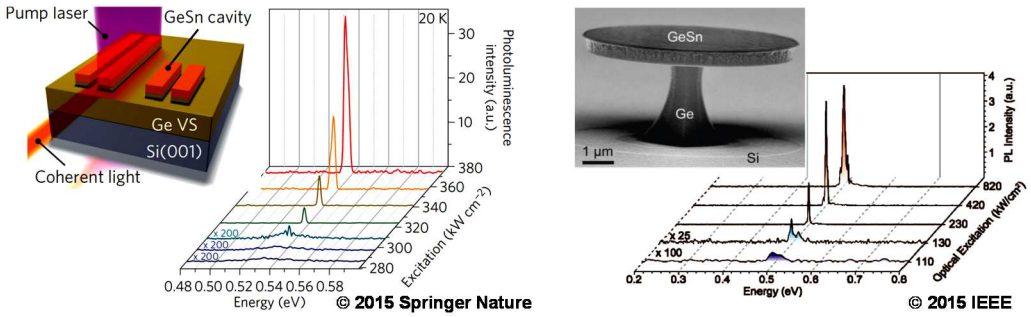


Fig. 1-17 Direct bandgap GeSn lasers fabricated on epitaxially-grown GeSn layer on Si substrate.

demonstrated using epitaxially-grown GeSn layer on Si substrate (Fig. 1-17) [25,26]. However, operating temperature of GeSn lasers were quite low and threshold voltage is still very high, which is originating from poor crystalline quality of compressive-strained single-crystalline GeSn layer. Thus, further improvement of crystalline quality is essential to realize high-performance GeSn-based optoelectronic devices.

1.3.2 Non-Epitaxial Growth on Insulating Layer

Recently, "non-epitaxial" methods such as solid-phase crystallization [27,28] or metal-induced crystallization [29] have been developed for crystallizing GeSn alloy on insulating layers, in which an amorphous GeSn (a-GeSn) layer deposited on insulators are annealed to induce crystallization at a temperature usually below the melting point of GeSn. Figure 1-18 shows crystal orientation map of GeSn layer on quartz substrate after solid-phase

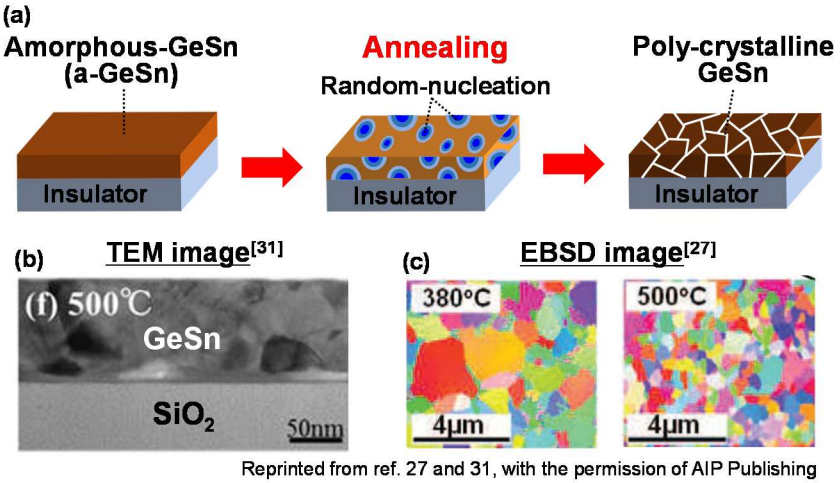


Fig. 1-18 (a) Schematic illustration, (b) TEM [31] and (c) EBSD [27] images of solid-phase grown GeSn layer on insulator.

crystallization evaluated by electron back-scatter diffraction (EBSD) spectrometry. Various colors were observed in the EBSD image, indicating a poly-crystalline GeSn layer was formed by this method. This poly-crystallization is caused by random nucleation during the annealing process. Since crystalline quality of poly-crystalline layer is much poor than that of single-crystalline one, they exhibit significantly degraded electronic and photonic properties. For example, both hole and electron mobility in poly-crystalline GeSn layer are less than 100 cm^2/Vs [30-33], which is much lower than that of single-crystalline Ge and even single-crystalline Si.

1.3.3 Lateral Liquid-Phase Epitaxy (LLPE)

In the case of Ge, a high-quality tensile-strained single-crystalline Ge wire can be grown on an insulator by utilizing the lateral liquid-phase epitaxy (LLPE) [34-38], which is one of the most useful methods for fabricating Ge-on-insulator structure. With this method, an amorphous Ge wire, which is surrounded by SiO_2 layer but partly connected to a Si substrate, is annealed above the melting point of Ge to induce lateral liquid-phase growth from the Si-seed region (Fig. 1-19). Due to the dislocation confinement at the seed region, a defect-free single-crystalline Ge wire can be obtained. In this method, tensile strain can be induced in Ge layer due to the difference in the thermal-expansion coefficients between Ge and the Si (Fig. 1-20) [39]. Here, thermally-induced strain is determined by thermal-expansion coefficients of materials and maximum crystallization temperature. In the case of LLPE, since epitaxial growth starts at

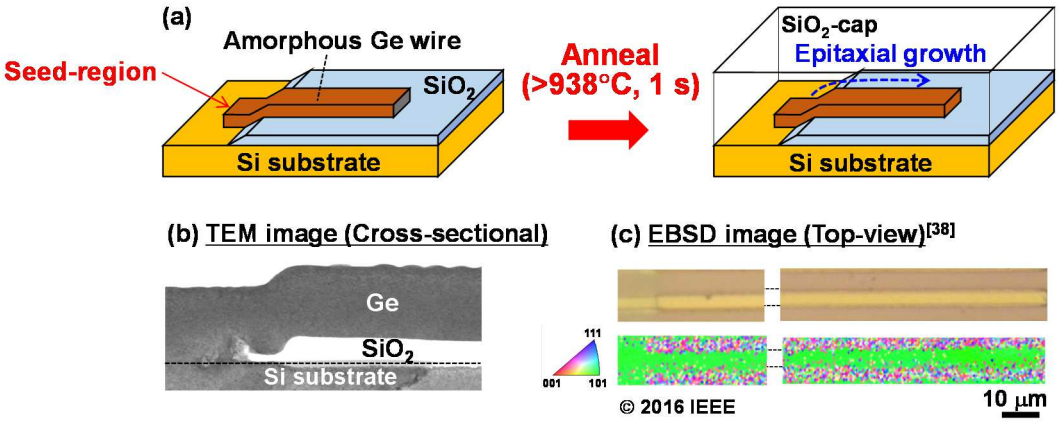


Fig. 1-19 (a) Schematic illustration, (b) TEM and (c) EBSD images of LLPE-grown GeSn wire [38].

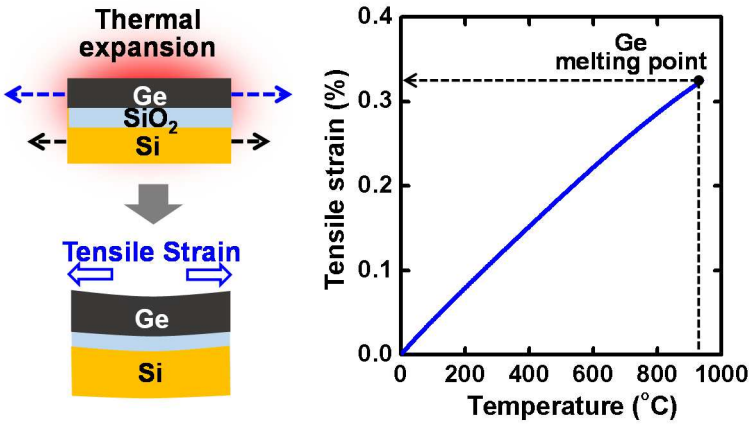


Fig. 1-20 Thermally-induced strain in LLPE-grown Ge layer. Strain is determined by difference in thermal expansion coefficient between Ge and substrate, and crystallization temperature [39].

the melting point of Ge, tensile strain as high as 0.4% can be induced [37].

Previously, several groups have examined the LLPE-growth of GeSn alloy and obtained a tensile-strained single-crystalline GeSn wires [40-43]. Based on the liquid-phase-grown GeSn wire, a significantly enhanced photoluminescence was observed with respect to bulk Ge substrate [43], which is originating from the direct bandgap shrinkage and clearly indicates an excellent crystalline quality of single-crystalline GeSn wire formed by the LLPE.

However, with this method, crystal-seeds such as a Si substrate is required to induce the LLPE growth, which severely limits the process window and has difficulty in monolithic integration. Moreover, there is a diffusion of Si atoms into GeSn wire from seed region [43], which lifts up the energy of Γ-valley as in the case of inducing compressive strain.

Therefore, it has become necessary to find an alternative way to fabricate high-quality single-crystalline GeSn layer that would be applicable to electronic and photonic integrated circuit.

1.4 Aim of This Study and Contents of Thesis

As described in this chapter, GeSn alloy has attracted a great interest due to its enhanced electronic and photonic properties, and the monolithic integration of GeSn-based optoelectronic devices is regarded as most promising post-scaling technology that offers not only high-speed and massive data transmission, but

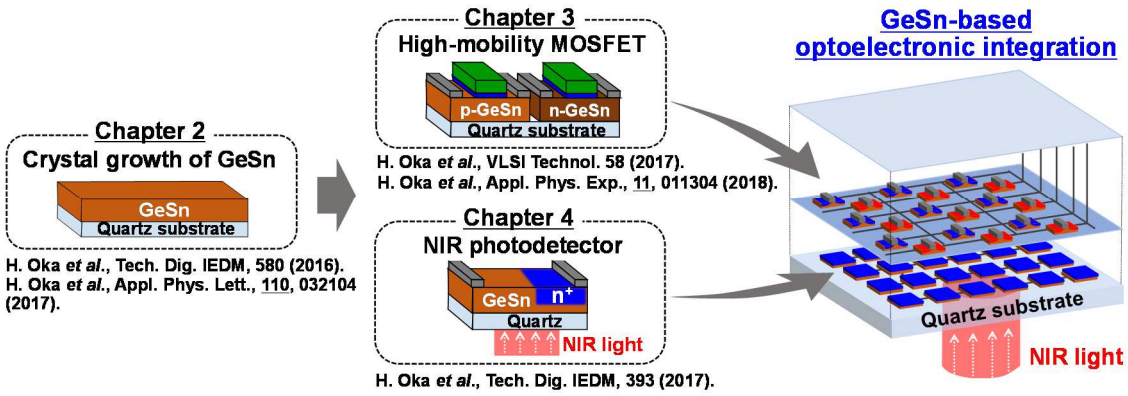


Fig. 1-21 Contents of this thesis. The aim of this study is to demonstrate GeSn-based optoelectronic integrated circuit.

also emerging NIR imaging/sensing microchip. However, due to the lack of suitable formation method of high-quality GeSn crystals, there are still difficulties in fabricating GeSn-based electronic and photonic devices, and a potential of GeSn alloy for advanced optoelectronic applications are not fully demonstrated.

The aim of this work is to provide an advanced GeSn-based optoelectronic platform that would break the physical limitation of conventional Si-based LSI and to offer emerging multi-functional devices such as NIR imaging/sensing semiconductor microchip. For this purpose, we proposed a novel crystal growth method of GeSn alloy, and fabricated high-performance GeSn devices including high-mobility CMOS and NIR photodetector. By integrating fabricated GeSn-based electronic and photonic devices, we demonstrated world's first fully-integrated group-IV-based NIR imager chip. Contents of this thesis is summarized in Fig. 1-22.

Chapter 2 focuses on crystal growth of GeSn alloy on transparent substrate. Since LLPE method requires crystal seed such as a Si substrate and thus not applicable to monolithic integration, we proposed a novel liquid-phase crystallization by controlling the nucleation during the crystallization. A crystalline quality, Sn content, and strain in fabricated GeSn layer on quartz substrate were studied in detail. Both p- and n-type single-crystalline GeSn wires

were successfully grown on a quartz substrate, which would be an ideal platform for GeSn-based electronic and photonic integration.

In order to investigate the potential of liquid-phase grown GeSn wires as a post-Si high-mobility channel material, p- and n-channel thin-film transistors (TFT) were fabricated in chapter 3. A mobility behavior in GeSn alloy is studied in detail, and revealed the mobility limiting factor in GeSn-based transistor. Based on findings, high-performance GeSn p- and n-channel TFTs were successfully demonstrated. This is the first report of GeSn-based CMOS fabricated on transparent substrate.

In Chapter 4, we examined the fabrication of GeSn-based photodiode array on a quartz substrate and evaluated the optical properties of GeSn alloy in the NIR wavelength range. Since GeSn alloy is expected to exhibit high light emittion/detection efficiency, it becomes possible to fabricate fully-integrated group-IV-based imager chip with low-cost and large-volume manufacturing using conventional Si-CMOS process, that would outperforms imaging device based on III-V semiconductors. For this purpose, we further developed the liquid-phase crystallization technique by utilizing laser scanning annealing, which can provide a single-crystalline GeSn array structure on quartz substrate with high-integrity with low thermal budget. The NIR optical response of GeSn photodiode array on a quartz substrate was studied in detail.

Finally, Chapter 5 provides general conclusions for GeSn-based electronic and photonic devices on a quartz substrate fabricated by liquid-phase crystallization.

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Chapter 2

Single-Crystalline GeSn Growth on Quartz Substrate by Nucleation-Controlled Liquid-Phase Crystallization

2.1 Introduction

As described in the previous chapter, formation of a high-quality single-crystalline GeSn layer is required for advanced optoelectronic integration in the post-scaling era. In this chapter, a novel crystallization technique for fabricating a tensile-strained single-crystalline GeSn layer on transparent substrate have been presented. By using this technique, both p- and n-type single-crystalline GeSn wires were successfully formed on a quartz substrate without using any crystal seed or catalyst, which enables the monolithic integration of high-mobility CMOS and highly-efficient photonic devices on a transparent substrate. The crystalline quality, Sn content and strain of fabricated single-crystalline GeSn wire were also characterized in detail in this chapter.

2.2 Nucleation-Controlled Liquid-Phase Crystallization

2.2.1 Concept of This Technique

In order to provide a single-crystalline GeSn layer on a transparent substrate, we developed a novel crystallization technique based on the LLPE. In the conventional LLPE of GeSn wire, Si-seed was utilized to induce the lateral liquid-phase growth, which severely limits the process window and has disadvantage in the process integrity. Thus, we proposed an alternative method to induce the lateral liquid-phase growth without using any crystal-seed or catalyst. Figure 2-1 shows the basic concept of our proposed crystallization technique. The key is local melting of amorphous GeSn wire to control the nucleation and crystal growth in the liquid-phase GeSn. In the case of complete melting of amorphous GeSn wire, spontaneous-nucleation in the liquid-phase GeSn results in poly-crystallization. However, as for the local melting, it is expected that the solidification initiated at the single-nucleus formed at the solid/liquid interface, and lateral crystallization quickly propagated along the wire. If the lateral growth

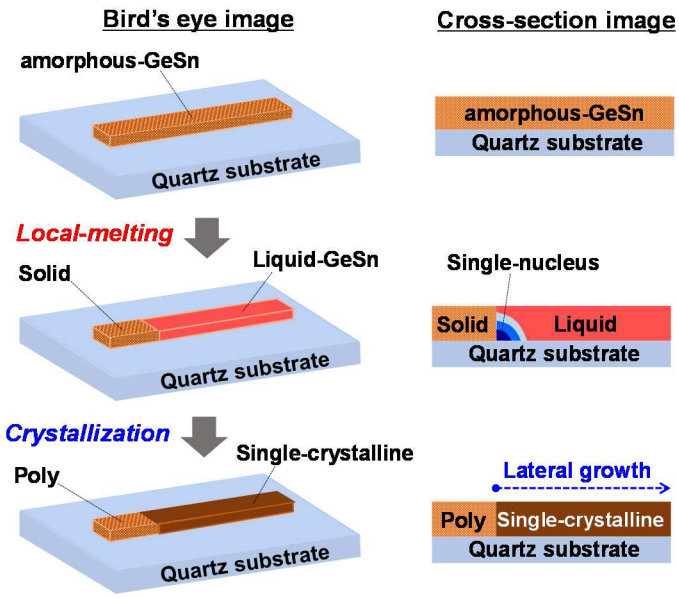

Fig. 2-1 Schematic illustrations of nucleation-controlled liquid-phase crystallization of GeSn wire on quartz substrate. Local-melting is key to control nucleation in liquid-GeSn.

speed is enough high to prevent the spontaneous nucleation in the growth front, single-crystallization GeSn wire can be obtained on a designated area on transparent substrate without using crystal seed. This nucleation-controlled liquid-phase crystallization technique is quite simple and integration-friendly, which would be a suitable approach for fabricating a high-quality GeSn-on-insulator structure.

2.2.2 Fabrication Process

Figure 2-2 shows the fabrication process of single-crystalline GeSn wire on a quartz substrate by using the local melting process. We used a commercially available quartz substrate as a starting substrate. A 100-nm-thick amorphous GeSn layer was deposited using a molecular beam deposition system at room temperature (R.T), and patterned into narrow stripes (for example, W/L = 3/300 μm) by CF_4-based reactive ion etching. The Sn content inside the amorphous GeSn layer was estimated to be around 2% through XPS measurement. It should be noted that Sn segregation at the surface of an as-deposited GeSn layer was observed due to the low solid solubility of Sn in Ge. After depositing a thick SiO_2 capping layer (~1 μm) by RF-sputtering to prevent agglomeration of the GeSn

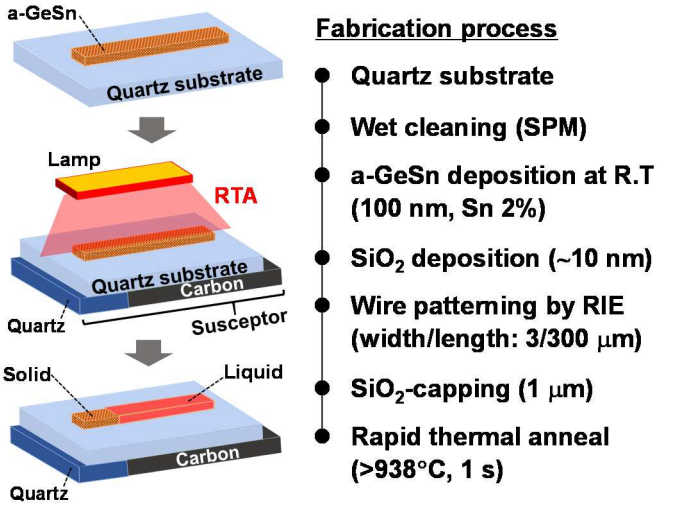

Fig. 2-2 Fabrication process of single-crystalline GeSn wire on quartz substrate by local-melting process.

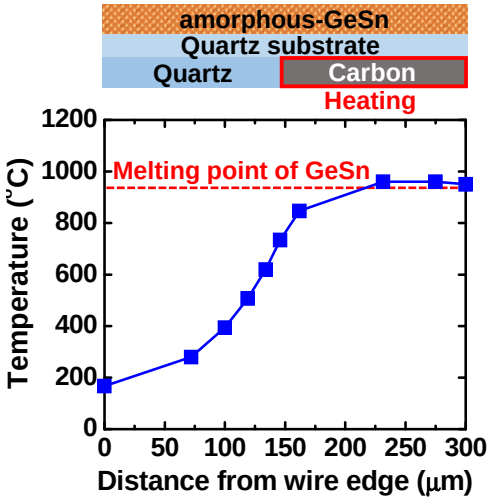

Fig. 2-3 Simulation study of temperature gradient along the GeSn wire under the local heating condition.

alloy, rapid thermal annealing (RTA) was performed in nitrogen (N_2) ambient above the melting point of GeSn (~938°C) for 1 s. In the RTA process, in order to melt a GeSn wire locally, sample was placed on a susceptor consisting of carbon and quartz. Since a quartz is transparent to the infrared (IR) light used in this lamp annealing equipment (λ = 1.2 μm), only the carbon part can be heated to above the melting point of GeSn. Figure 2-3 shows simulation study of temperature gradient along the 300-μm-long GeSn wire on a quartz substrate under local heating condition, in which carbon susceptor acts as a heat source that is placed under the half area of sample. From the simulation result, it was found the temperature gradient was formed along the GeSn wire, which would be a driving force for lateral crystal growth.

2.3 Physical Characterization

2.3.1 Crystalline Quality and Sn Content

First we investigated the crystalline quality of fabricated GeSn wire on a quartz substrate by using nucleation-controlled liquid-phase crystallization. Figure 2-4 shows the optical and electron back-scatter diffraction (EBSD) images of the 300-μm-long GeSn stripes after RTA. As shown in the EBSD image of the completely-melted GeSn stripes (Fig. 2-4(a)), the various colors were observed

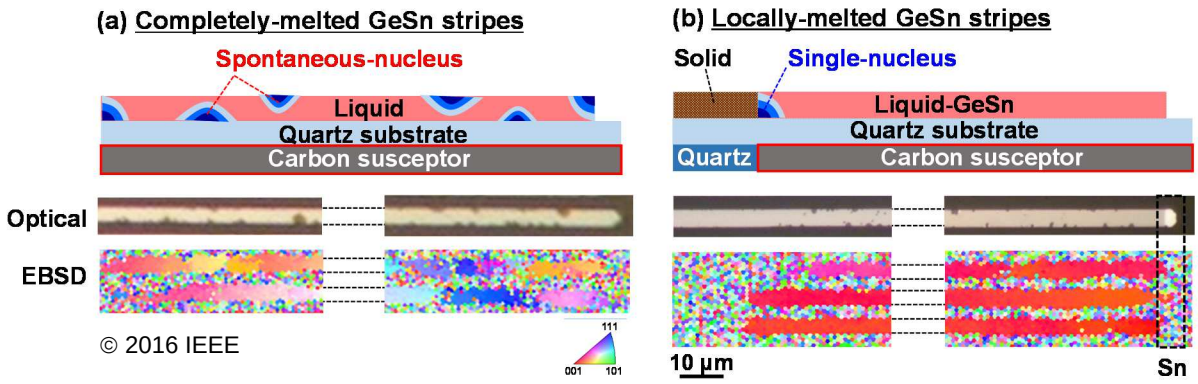

Fig. 2-4 Optical and EBSD images of GeSn stripe on quartz substrate formed by (a) complete- and (b) local-melting process [1].

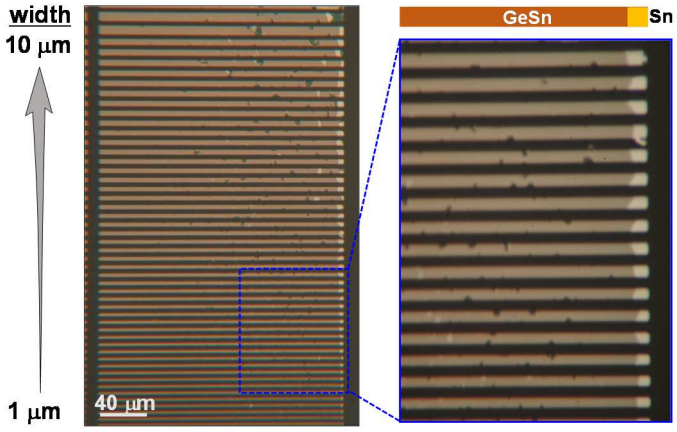

Fig. 2-5 Optical image of GeSn stripe on quartz substrate after local-melting with various width ranging from 1-10 μm.

in each wire, which is corresponding to various crystal orientatio ns and indicating poly-crystallization. This result indicates that it is difficult to suppress the preferential random nucleation within the complete melting process. However, for the locally-melted sample, most of the GeSn stripes appeared in the same color in the EBSD image from the middle to the end of the wire for over 250-μm-long (Fig. 2-4(b)), which means that lateral liquid-phase crystallization was initiated from a single-nucleus formed near the solid/liquid interface. We have succeeded in fabricating a single-crystalline GeSn wire with a length up to 2 mm by this method (data not shown). Also, we confirmed that almost all of single-crystalline wires were (100)-oriented in the direction normal to the surface. This preferential orientation of GeSn wires would be determined by an interface energy between liquid GeSn and quartz. It should be noted that the bright

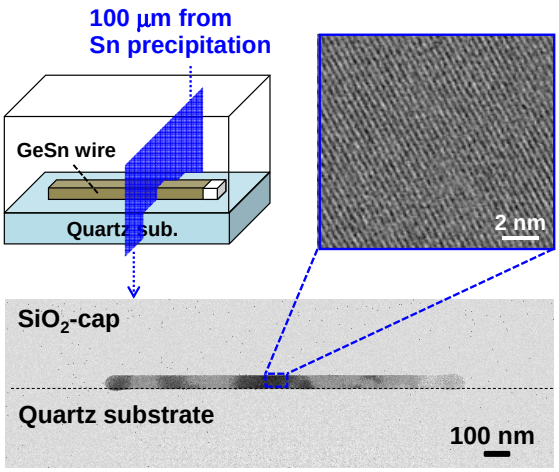

Fig. 2-6 Cross-sectional TEM images of single-crystalline GeSn wire formed on quartz substrate [1].

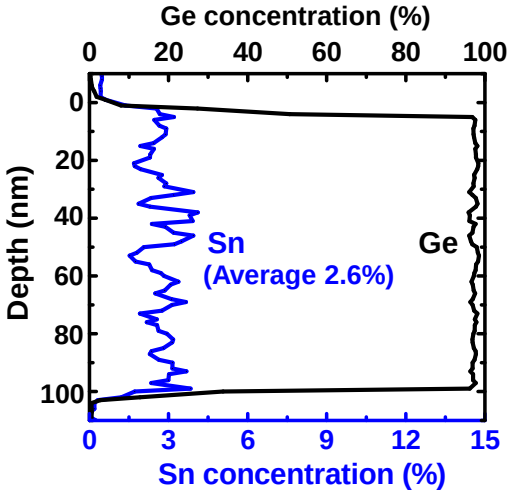

Fig. 2-7 Depth profiles of Sn and Ge composition in GeSn layer by EDX. Average Sn composition (Sn/Ge+Sn) is determined to be 2.6% [1].

contrast region in the optical image of the single-crystalline GeSn stripes is the Sn precipitation that is swept out during lateral growth due to the low solid solubility of Sn in Ge. Also, we have examined the local melting process for wide GeSn wires (width: 1-10 μm) to investigate the feasivility of our proposed crystallization technique. As shown in Fig. 2-5, Sn precipitation, the sign for accomplishment of lateral growth, was observed for all of GeSn wires, indicating simultaneously obtained single-crystalline wires with the widths of 1-10 μm. This clearly indicates the advantage of our crystallization technique in terms of device fabrication.

Figures 2-6 show the cross-sectional transmission electron microscope (TEM) images of a single-crystalline GeSn wire measured 100 μm from the Sn precipitation. It was found that a dislocation-free single-crystalline GeSn layer was grown on a quartz substrate.

Then we investigated the Sn content in the single-crystalline GeSn wire by energy dispersive X-ray spectrometry (EDX). From the EDX depth profiles of Ge and Sn shown in Fig. 2-7, over 2% of Sn uniformly distributed in the depth. The average Sn content along the depth direction was estimated to be 2.6%, which exceeds the solid solubility limit of Sn in Ge. It should be noted that the Sn content in the single-crystalline GeSn layer was higher than the initial Sn

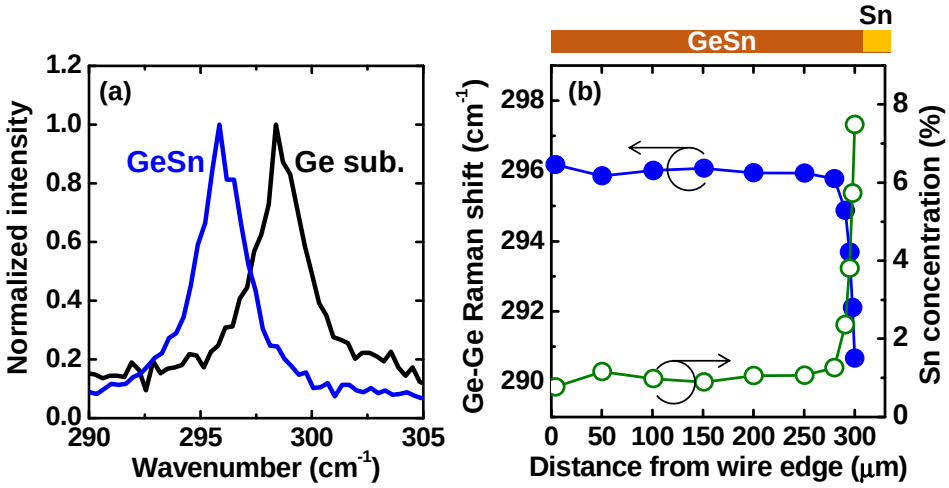

Fig. 2-8 (a) Raman spectra obtained from single-crystalline GeSn wire and control bulk Ge substrate, (b) Position dependence of Raman shift and extracted Sn content.

content inside the amorphous GeSn layer (~2%). This can be explained by the diffusion of Sn, which was segregated at the surface of the as-deposited GeSn layer, during the melting growth process.

We have also confirmed Sn content along the lateral growth direction through micro-probe Raman spectroscopy. Since the excitation beam size is enough small (~1 μm) compared to the GeSn wire (~3 μm), position-dependent Raman spectra can be obtained. Figure 2-8(a) shows the normalized Raman spectra from Ge-Ge vibration mode for single-crystalline GeSn wire on quartz substrate measured 100 μm from Sn precipitation and control bulk Ge substrate. The Raman peak of GeSn wire is shifted to a lower wave number compared to that of bulk Ge substrate, which is originating from the incorporation of Sn and inducing tensile strain. According to the experimental study, the correlation between Raman shift and Sn content/strain is expressed by the following equation [2].

$$\Delta\omega = -(82\pm 4)\chi - (563\pm 34)\varepsilon$$

($\Delta\omega$: Raman shift, χ: Sn content, ε: Strain,)

By assuming the strain is uniformly induced along the wire, we can evaluate the Sn distribution along the wire from Raman shift. Figure 2-8(b) shows the position dependence of Raman shift (blue line) and extracted Sn content by using the above equation (green line) for 300-μm-long GeSn wire. It was found that the Sn content in GeSn wire is almost constant for the most part of wire (0-295 μm),

which would be suitable for electronic and photonic device fabrication. It should be noted that the Sn content rapidly increased near the growth end (295-300 μm) and reaches as high as 8%, which is due to the Sn segregation during the lateral growth.

2.3.2 Determination of Strain by Synchrotron X-ray Diffraction

We also evaluated the strain in the GeSn stripes crystallized on a quartz substrate. For an accurate measurement of strain in the narrow GeSn stripes (W = 3 μm), we employed synchrotron micro X-ray diffraction (μ-XRD) with a beam size of 700×200 nm^2 and an acceleration energy of 12 keV (Fig. 2-9) [3].

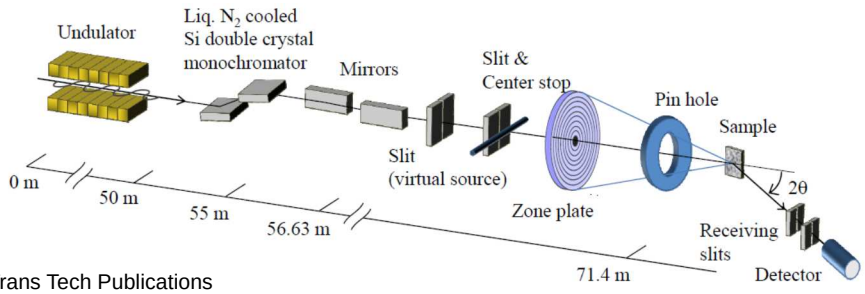

Fig. 2-9 Experimental setup of synchrotron μ-XRD used in this study [3].

The obtained diffraction peak of (004) planes for a single-crystalline GeSn wire on a quartz substrate and a control bulk Ge substrate were shown in Fig. 2-10(a). The diffraction peak from GeSn wire was observed at a higher 2θ angle compared to that from bulk Ge substrate, indicating a decrease in lattice constant perpendicular to the planes. From the diffraction peak position of the GeSn wire and the Sn content evaluated by EDX, in-plane strain was estimated using Vegard's law for GeSn alloy [4,5]. Figure 2-10(b) shows the strain evaluated from the μ-XRD results as a function of distance from the Sn precipitation. It was found that over 0.5% of tensile strain was induced in the GeSn wire crystallized on the quartz substrate. This tensile strain is in good agreement with the value calculated from the differences in the thermal expansion coefficient between GeSn and quartz (dashed line in Fig. 2-10(b)). From these results, we confirmed that a highly tensile-strained single-crystalline GeSn layer with a Sn content exceeding solid solubility was grown on a quartz substrate.

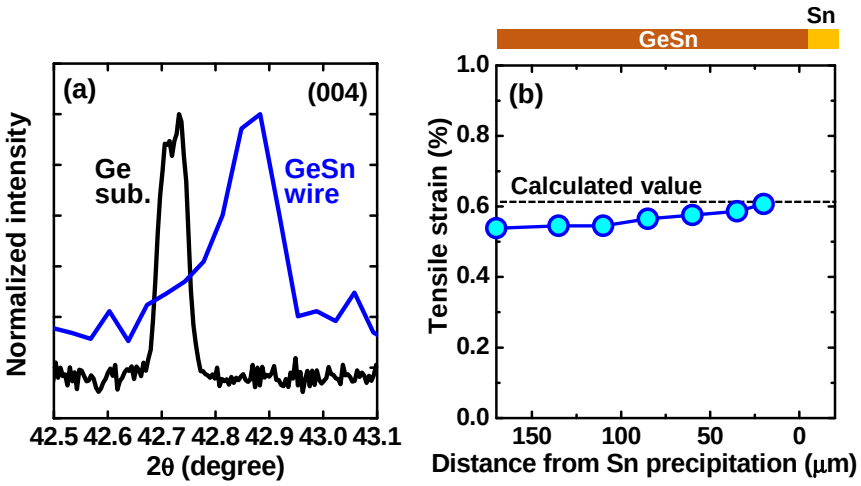

Fig. 2-10 (a) (004) μ-XRD diffraction patterns of single-crystalline GeSn wire and bulk Ge substrate. (b) Strain distribution evaluated from μ-XRD and EDX results as function of distance from Sn precipitation [1].

2.4 Optical Characterization

Then we investigated the luminescence property of the fabricated single-crystalline GeSn wire on a quartz substrate by micro-photoluminescence (μ-PL) measurement. The 20-mW excited laser with a wavelength of 647 nm was focused on the sample surface through neutral density (ND) filter with a diameter of about 1 μm. Light emission was detected from a wavelength of 1.1 to 2.2 μm using a cooled, wavelength-extended InGaAs 1024 pixel linear photodiode array (Table 2-1, Princeton Instruments: PyLon-IR-2.2) optically coupled to a spectrograph system. In this experiment, all PL spectra were acquired at room temperature.

Figure 2-11 shows the PL spectra obtained from single-crystalline GeSn wire on a quartz substrate with different measurement position (middle and near the edge of the wire) and control bulk Ge substrate. The PL spectra from middle

Table 2-1 Specifications of photodetector used in μ-PL system.

Model	PyLon-IR 1023
Image sensor	Linear InGaAs photodiode array
Format	25 μm (W) x 250 μm (H)
Spectral range	1.0 - 2.2 μm
Operation temp.	-100°C
Quantum efficiency at 2 μm	70%

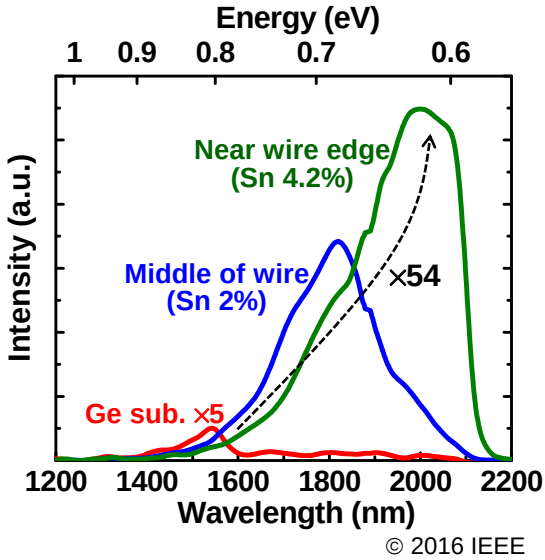

Fig. 2-11 PL spectra for middle and near edge of single-crystalline GeSn wire on quartz substrate and cotrol bulk Ge substrate [1].

part of GeSn wire shows direct bandgap emission at the peak wavelength of around 1800 nm, which is red-shifted with respect to that from bulk Ge substrate (0.80 eV, 1550 nm) for about 0.1 eV. This bandgap shrinkage is caused by the alloying Sn and inducing biaxial tensile strain. Also, an enhanced direct bandgap emission was observed (×34 bulk Ge), indicating an excellent crystalline quality of the fabricated single-crystalline GeSn wire. As for the near edge of GeSn wire, a significantly enhanced luminescence (×54 bulk Ge) with a peak wavelength of about 2 μm was observed, which is originating from the increase in Sn content due to the Sn segregation. From the theoretical calculation, the indirect-to-direct bandgap transition energy of tensile-strained GeSn alloy is predicted to be around 0.69 eV. Thus, it is expected that near the edge of GeSn wire has a direct bandgap electronic structure.

2.5 Evaluation of Conduction Type and Carrier Concentration

2.5.1 Hall Effect Measurement

As described in the previous session, we have succeeded in fabricating a high-quality tensile-strained single-crystalline GeSn wire on a quartz substrate. In order to reveal the electrical property, we have investigated the conduction type and carrier concentration of fabricated single-crystalline GeSn wire.

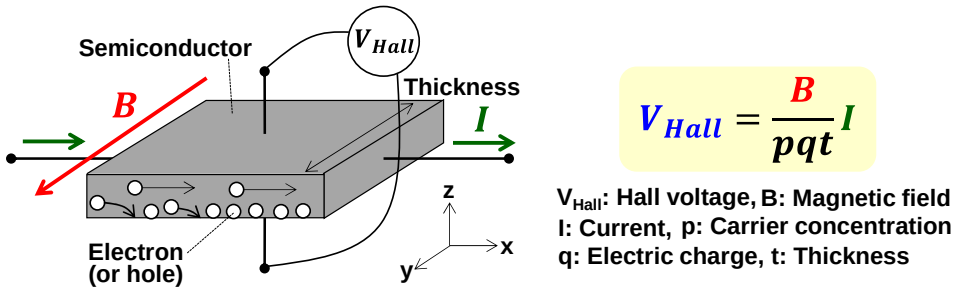

Fig. 2-12 Basic physical principle of Hall effect measurement.

One of the most popular and useful method for characterizing a conduction type is the Hall effect measurement. In this method, when the current flows in the semiconductor along a direction perpendicular to an applied magnetic field, electron (or hole) that is flowing across the semiconductor is influenced by Lorentz force, and moved toward a direction perpendicular to both current flow and magnetic field (z direction). This movement of electron to the z direction forms a positive charge on the opposite side, and thus forming an internal electric field along z direction, which is measured as Hall effect voltage and we can estimate the conduction type and carrier concentration from the equation shown in Fig. 2-12. In this method, current-voltage characteristic is measured by probing metal contact on four side on a semiconductor substrate as illustrated in Fig. 2-12.

However, the fabricated single-crystalline GeSn is a narrow stripe with a wire width of 3 μm, and thus it has been difficult to evaluate electrical properties by Hall effect measurement.

2.5.2 Fabrication of Hall-Bar Shaped GeSn Wire

In order to enable the Hall effect measurement and evaluate the exact carrier concentration of fabricated single-crystalline GeSn wire, we examined the liquid-phase growth of branched single-crystalline GeSn wire as shown in Fig. 2-13. Since four probes can be contacted crossover the sample, Hall voltage can be measured with this Hall-bar shaped GeSn wire. Figure 2-13(b) shows the optical image of Hall-bar shaped GeSn wire (T_{GeSn}: 200 nm) after local melting process. The Sn precipitation was clearly observed at the edge of each branch (bright contrast region), suggesting that the single-crystallization was successfully propagated. This would be beneficial not only for Hall effect

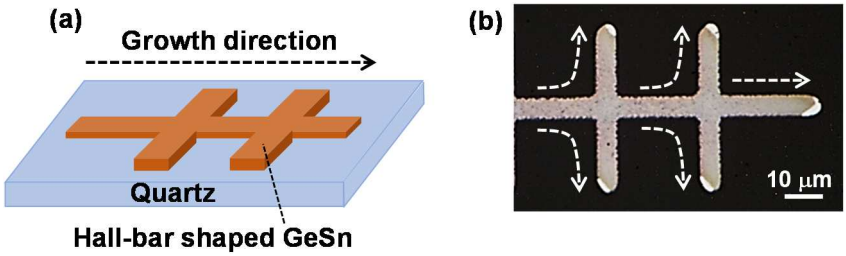

Fig. 2-13 (a) Schematic illustration of Hall-bar shaped GeSn wire on quartz substrate. (b) Optical image of Hall-bar shaped GeSn after liquid-phase growth.

measurement, but also GeSn-based optoelectronic device fabrication that requires flexibility in device structure.

Figure 2-14 shows the Hall current-voltage characteristics of fabricated liquid-phase grown GeSn wire. In this experiment, magnetic field was set to be 0.1 T by using neodymium magnet. From positive slope of the plot, the conduction type of liquid-phase grown undoped GeSn wire was found to be p-type. This p-type conduction is typical feature of undoped GeSn layer and that is explained by the point defect in Ge or GeSn, which act as acceptor-like state. By using the equation shown in Fig. 2-12, the carrier concentration of undoped GeSn wire was estimated to be around 3×10^{16} cm^{-3}, which is much smaller than that of poly-crystalline GeSn layer ($>10^{18}$ cm^{-3}) [6] or epitaxially-grown single-crystalline GeSn layer (10^{17}-10^{18} cm^{-3}) on Si substrate [7]. This indicates the excellent crystalline quality of the fabricated liquid-phase grown GeSn wire on a quartz substrate, which would be an attractive platform for GeSn-based optoelectronic integration on a transparent substrate.

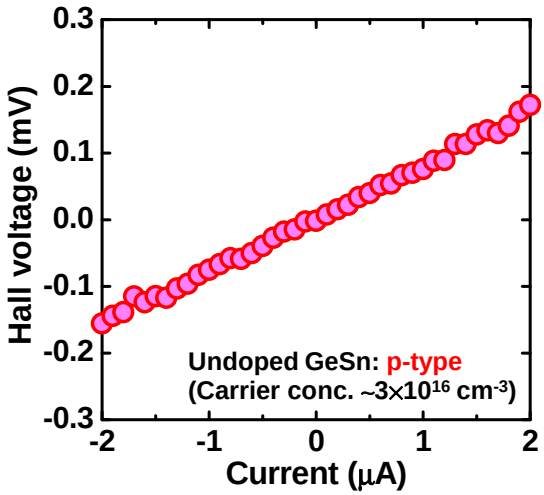

Fig. 2-14 Hall plot of fabricated liquid-phase grown undoped GeSn wire.

2.6 N-type Doping into Liquid-Phase Grown Ge and GeSn Wires

2.6.1 Issues in n-type GeSn Formation

In the previous session, we have succeeded in fabricating a single-crystalline GeSn wire on a quartz substrate by nucleation-controlled liquid-phase crystallization. The Hall effect measurement revealed that the undoped GeSn wire is p-type due to the acceptor-like point defects as in the case of Ge. Also, carrier concentration was evaluated to be around 3×10^{16} cm^{-3}, indicating an excellent crystalline quality of the fabricated single-crystalline GeSn wire.

Considering the monolithic integration of CMOS and light emission/detection devices, not only p-type but also n-type GeSn layer is indispensable. In general, n-type doping of Ge is still difficult due to the high diffusivity and low solid solubility of n-type dopants in Ge [8]. In addition, in the case of GeSn, a low thermal budget is required for dopant activation annealing due to its poor thermal stability, which makes it much more challenging to form a high-quality n-type GeSn layer [9]. Previously, a unique n-type doping technique using the LLPE has been reported, in which the P ions were implanted into amorphous Ge wire followed by RTA to induce the LLPE and dopant activation simultaneously [10]. An advantage of this method is to avoid implantation damage and does not require additional activation annealing, which seems to be an attractive approach for fabricating a high-quality n-type single-crystalline GeSn wire. In recent years, the LLPE-growth of P^+-implanted GeSn wire was also reported from our group and the enhanced direct bandgap PL emission was demonstrated [1,11]. However, the doping concentration and profile in liquid-phase grown Ge and GeSn wire is still unclear and the electrical properties have not been investigated in spite of its importance.

In this session, in order to provide a further insight into this n-type doping technique, we systematically investigated the diffusion and activation behaviors of n-type dopant during the liquid-phase crystallization process. In our work, Sb was selected as an n-type dopant since a high activation rate is expected during the melting and recrystallization process of Sb-doped Ge. [12] The physical,

optical and electrical properties of Sb-doped single-crystalline Ge and GeSn wires were studied in detail.

2.6.2 LLPE-Growth of Sb-Doped Ge on Silicon Substrate

2.6.2.1 Fabrication Process

Fabrication process of Sb-doped LLPE-Ge wire is illustrated in Fig. 2-15. After wet cleaning the silicon-on-insulator wafer with 50-nm-thick Si layer and 150-nm-thick buried oxide, the Si layer was patterned by tetramethyl ammonium hydroxide (TMAH) solution to define the seed region. Then, a 100-nm-thick amorphous Ge layer was deposited by molecular beam deposition system at room temperature. For the n-type doping, Sb was simultaneously evaporated during Ge deposition. From the secondary ion mass spectrometry (SIMS) measurement, the Sb concentration in the amorphous Ge layer was estimated to be around 5×10^{19} cm^{-3}. After patterning the Sb-doped amorphous Ge layer into narrow stripes (W/L = 2/100 μm), a thick SiO_2-capping layer (~1 μm) was deposited to prevent agglomeration of liquid-phase Ge. Then, RTA was performed in nitrogen ambient over 938°C for 1 sec to induce the LLPE-growth from the seed region.

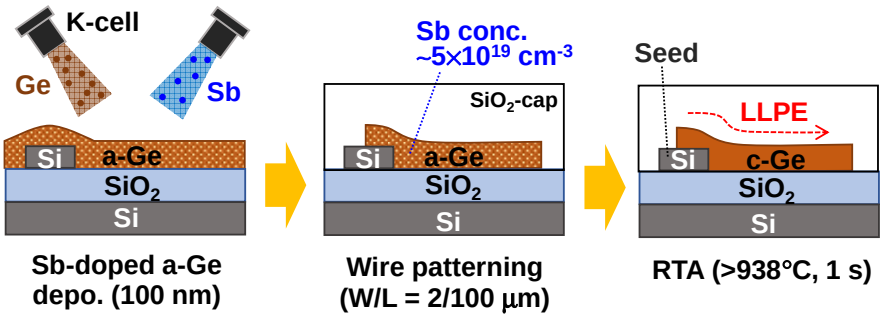

Fig. 2-15 Schematic illustrations of LLPE-growth of Sb-doped Ge wire.

2.6.2.2 Evaluation of Sb Distribution

Figure 2-16(a) shows the typical optical microscope and EBSD images of the Sb-doped Ge wire after RTA. As shown in the EBSD image, the Sb-doped Ge wire exhibited a single-crystalline (001) orientation, which is identical to the Si-seed. This indicates that the LLPE-growth proceeded from the seed region and that the Sb incorporation hardly affected the lateral crystal growth of Ge.

Then we investigated the doping profile of Sb in LLPE-grown Ge wire. For an accurate measurement of Sb concentration in the narrow Ge wire (W = 2 μm), micro-SIMS (μ-SIMS) measurement with a detection area size of 10×10 μm^2 was employed. Figure 2-16(b) shows the Sb depth profiles in LLPE-Ge measured at different position along the wire. Although the Sb concentration in the middle part of wire was under the detection limit (<10^{18} cm^{-3}), high concentration of Sb exceeding the solid solubility (>10^{19} cm^{-3}) was detected at the edge of wire. These results indicate that the Sb atoms were swept out toward the growth direction during the LLPE, resulting in a formation of highly Sb-doped region near the growth end. This would be due to the low segregation coefficient of Sb in Ge, and coincides well with the calculated profile based on Scheil's equation [13]. We also confirmed Sb precipitation at the end of wire (dark contrast region in Fig. 2-16(a)). Similar dopant segregation phenomena was reported for LLPE growth of P-doped Ge [10].

In order to provide a further insight into the activation behavior of Sb during the liquid-phase crystallization process, μ-PL measurement was performed. In the case of Ge, it is known that the electron population at Γ-valley increases by n-type doping, leading to enhancement of direct bandgap emission. Since the

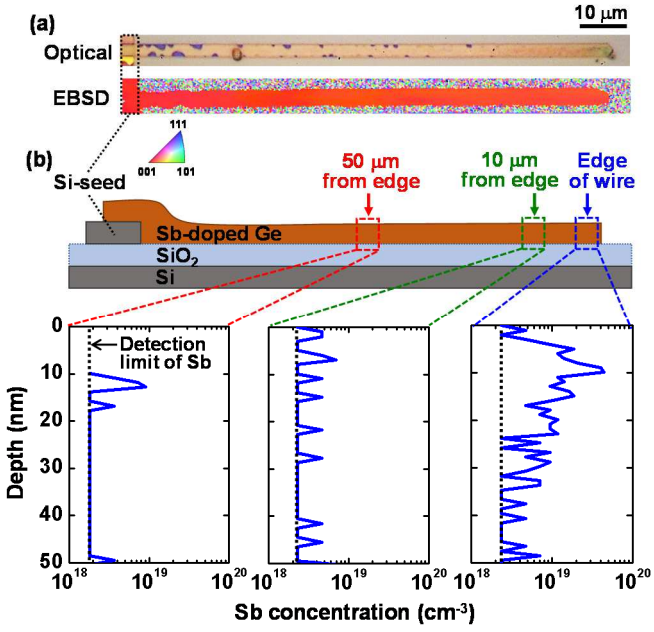

Fig. 2-16 (a) Optical and EBSD images of Sb-doped Ge wire after RTA. (b) μ-SIMS depth profiles of Sb concentration in LLPE-Ge wire measured at different position along the wire (Ref. 16, Copyright 2018 The Japan Society of Applied Physics).

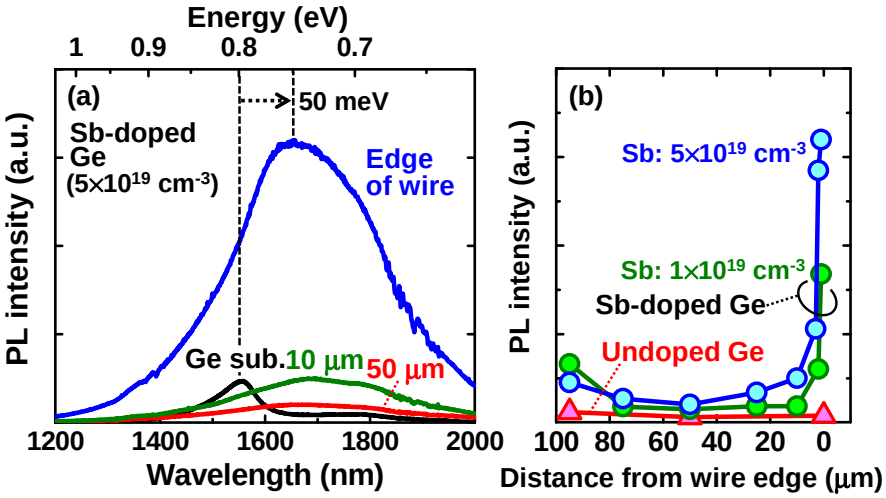

Fig. 2-17 (a) PL spectra of Sb-doped LLPE-Ge wire on SiO_2/Si substrate measured at different position and control bulk Ge substrate. (b) Position-dependence of peak PL intensity for Sb-doped and undoped LLPE-Ge wires (Ref. 16, Copyright 2018 The Japan Society of Applied Physics).

emission intensity increased with increasing electrically active donor concentration [14], we can estimate the active Sb distribution. The excited laser with a wavelength of 647 nm was focused on the sample surface with a diameter of about 1 μm, enabling the evaluation of position-dependent PL spectra along the narrow Ge wire (W = 2 μm).

Figure 2-17(a) shows the PL spectra obtained from Sb-doped Ge wire with different measurement position along the wire and control bulk Ge substrate. The Sb-doped Ge wire exhibits direct bandgap emission at the peak wavelength of 1660 nm, which is red-shifted with respect to that from bulk Ge substrate (0.80 eV, 1550 nm) for about 50 meV. This bandgap shrinkage is caused by the biaxial tensile strain of about 0.3%, which is originating from the large difference in thermal expansion coefficient between Ge and Si [15]. The tensile strain of about 0.3% was also estimated from Raman measurement (data not shown). Also, a significant increase in the PL intensity was observed at the edge of Sb-doped Ge wire (×7 Ge substrate), indicating the formation of heavily n-type doped region, and this is consistent with the Sb distribution evaluated by μ-SIMS measurement (Fig. 2-16(b)). The position-dependence of peak PL intensity for the Sb-doped and undoped LLPE-Ge wires are shown in Fig. 2-17(b). In contrast to the undoped Ge wire, the Sb-doped Ge wire shows remarkable increase in the PL

intensity near the edge of wire due to high Sb concentration. However, at the most part of Sb-doped Ge wire (20-100 μm far from edge of wire), the PL intensity is comparable to that of undoped Ge wire and nearly constant along the wire. This indicates that the electrically active doping concentration in Sb-doped LLPE-Ge wire was low and almost uniform along the wire except for near the growth end. We have also confirmed that the PL intensity near the growth end was strongly affected by the initial Sb concentration, while negligible change was observed at the most part of wire (Fig. 2-17(b), 1×10^{19} cm^{-3}).

2.6.3 Liquid-Phase Growth of Sb-Doped GeSn on Quartz Substrate

2.6.3.1 Fabrication Process

We next examined the nucleation-controlled liquid-phase growth of Sb-doped GeSn wire on a quartz substrate to obtain a high-quality single-crystalline n-type GeSn wire. In order to induce the lateral liquid-phase crystallization without using crystal-seed, the local melting process was employed (Fig. 2-18). The detail of this crystallization process is described in session 1.2. After wet cleaning a quartz substrate, a 80-nm-thick Sb-doped amorphous GeSn layer was deposited and patterned into narrow stripes (W/L = 2-5/300 μm). The Sn and Sb concentrations in the amorphous GeSn wire were estimated to be 2.5% and 5×10^{19} cm^{-3}, respectively. Then, a thick SiO_2-capping layer was deposited and RTA was performed for the local melting of amorphous GeSn wire to induce the liquid-phase growth.

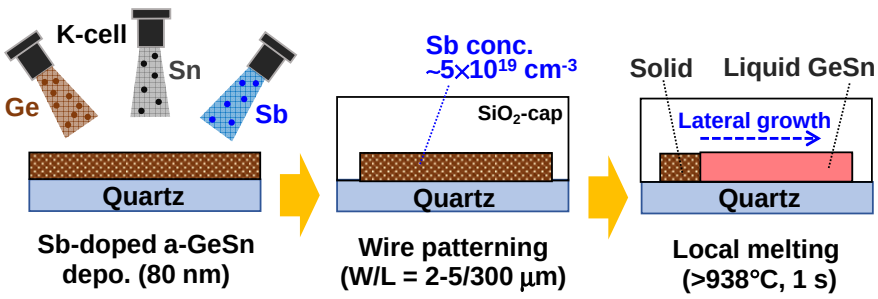

Fig. 2-18 Schematic illustrations of nucleation-controlled liquid-phase growth of Sb-doped GeSn wire on quartz substrate.

2.6.3.2 Crystalline Quality

Figure 2-19(a) shows the typical optical and EBSD images of Sb-doped GeSn wire on a quartz substrate after RTA. The bright contrast region in the optical image (edge of wire) corresponds to a Sn segregation, which is the sign for accomplishment of lateral crystal growth. The identical color in EBSD image observed from the middle to end of wire for over 250-μm-long indicates a single-crystallization propagated along the wire from a single-nucleus formed at the solid/liquid interface, which acts as a self-organized seed. It should be noted that the Sb-doped GeSn wires almost exhibited (001) orientation. This would be originating from the interface energy minimization between GeSn and SiO_2, which is in good agreement with the result of liquid-phase grown undoped GeSn wire.

The crystalline quality of fabricated Sb-doped single-crystalline GeSn wire was evaluated by the micro-probe Raman measurement (beam spot size: ~1 μm). Since a quartz has low thermal conductivity, we carefully optimized the excitation conditions in order to avoid thermal effect during the measurement. As shown in the inset in Fig. 2-19(b), the Raman peak originating from Ge-Ge vibration mode obtained from Sb-doped GeSn wire is shifted toward lower wave number compared to that from bulk Ge substrate, which is due to the Sn incorporation and biaxial tensile strain. By combining the EDX result with Raman measurement, the Sn content and biaxial tensile strain was estimated to

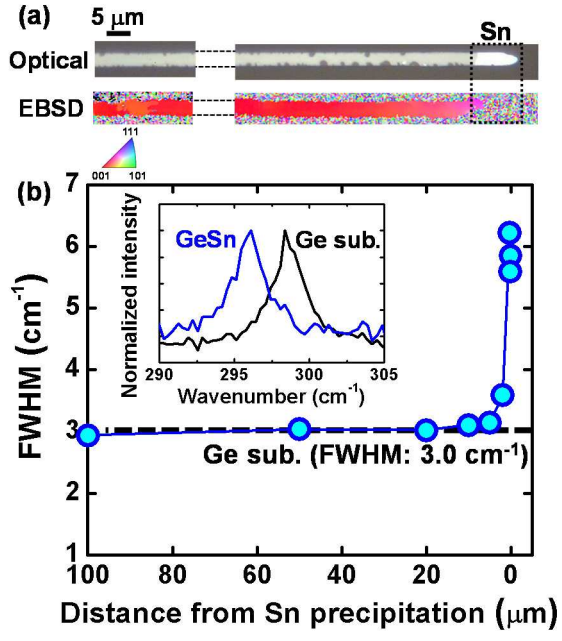

Fig. 2-19 (a) Optical and EBSD images of Sb-doped GeSn wire after RTA. (b) Position-dependence of extracted FWHM from Raman peak of Sb-doped GeSn wire. Inset shows Raman peak obtained from Sb-doped GeSn wire and control bulk Ge substrate (Ref. 16, Copyright 2018 The Japan Society of Applied Physics).

be around 2% and 0.3%, respectively. The position dependence of full-width at half maximum (FWHM) extracted from Raman peak was plotted in Fig. 2-19(b). It was found that the FWHM obtained from Sb-doped GeSn wire is comparable to that from bulk Ge substrate and nearly constant along the wire, indicating an excellent crystalline quality of the Sb-doped single-crystalline GeSn wire grown on a quartz substrate. It should be noted that the drastic increase in the FWHM near the Sn precipitation is attributed to the increase in Sn content, which degraded the crystalline quality due to the large lattice mismatch between Ge and Sn.

2.6.3.3 Photoluminescence-Based Study

The activation behavior of Sb in the liquid-phase grown GeSn wire was also evaluated by the μ-PL measurement (Figs. 2-20(a) and 2-20(b)). Since the Sn content rapidly increased at the growth end (Fig. 2-19(b)), the PL measurement was performed at the position enough far from Sn precipitation (>1 μm), where the Sn content is almost uniform (Sn ~2%). Similar to the Sb-doped Ge wire, a significant increase in the PL intensity was observed near the edge of Sb-doped GeSn wire, while the nearly constant intensity was observed at the most part of wire. This indicates that the single-crystalline GeSn wire is also uniformly-doped

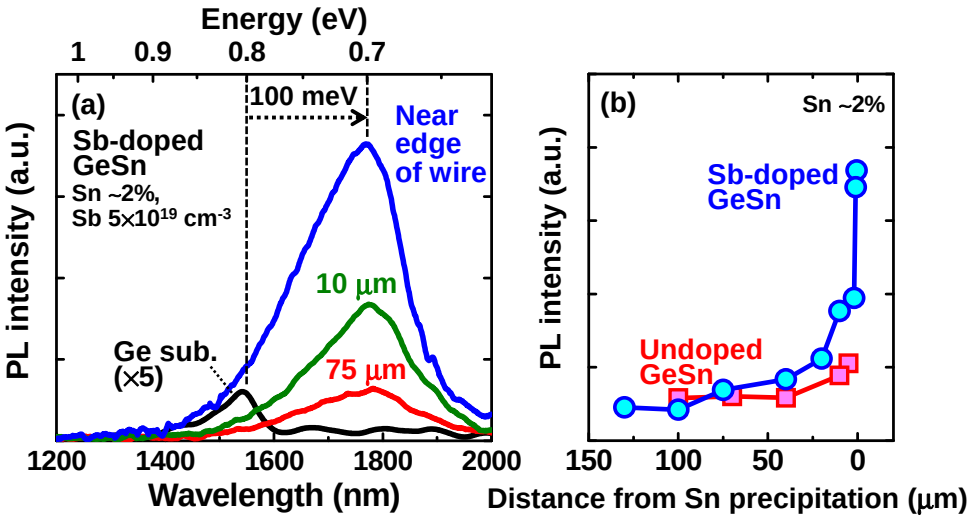

Fig. 2-20 (a) PL spectra of Sb-doped liquid-phase grown GeSn wire on quartz substrate measured at different position along the wire and control bulk Ge substrate. (b) Position-dependence of peak PL intensity for Sb-doped and undoped liquid-phase grown GeSn wires (Sn ~2%) (Ref. 16, Copyright 2018 The Japan Society of Applied Physics).

along the wire. The direct bandgap emission from Sb-doped GeSn wire is red-shifted compared to that from bulk Ge substrate for about 100 meV, which is due to the biaxial tensile strain and Sn incorporation. It should be noted that the PL enhancement factor at the growth end compared to the bulk Ge substrate is much higher than that of Sb-doped Ge wire (×30 Ge substrate). According to the theoretical calculation [17], the indirect-to-direct bandgap transition energy of GeSn alloy is around 0.69 eV when biaxial tensile strain is induced. Thus, the fabricated Sb-doped GeSn alloy would have an indirect bandgap structure, but the reduced energy difference between Γ- and L-valleys due to Sn alloying would attributed to the enhancement of luminescent efficiency.

2.6.3.4 Hall Effect Measurement

Then we investigated the conduction type and carrier concentration of Sb-doped GeSn wire formed on a quartz substrate. For the Hall effect measurement, Hall-bar shaped Sb-doped GeSn wire was fabricated by the liquid-phase crystallization. The detail of fabrication procedure is described in session 2.5.2. In this study, the middle part of Sb-doped GeSn wire, where Sb was uniformly doped, was used for Hall effect measurement. From the Hall voltage-current characteristic of Sb-doped GeSn wire as shown in Fig. 2-21, the Sb-doped GeSn wire was found to be n-type, and the carrier concentration was estimated to be around 4×10^{16} cm^{-3}. It should be noted that the carrier

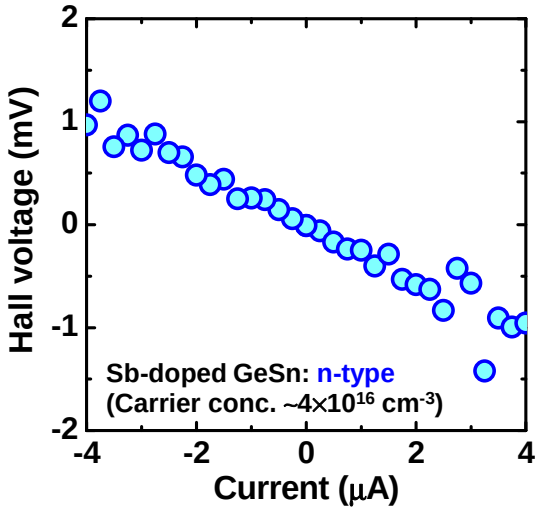

Fig. 2-21 Hall current-voltage characteristc of fabricated liquid-phase grown Sb-doped GeSn wire.

concentration in Sb-doped GeSn wire is quite low with respect to that of epitaxially-grown n-type GeSn layer reported so far. This would be attributed to an excellent crystalline quality (reduced acceptor-like point defects) of the liquid-phase grown GeSn layer and Sb segregation during lateral growth.

From these results, we have succeeded in fabricating uniformly and lightly n-type doped high-quality single-crystalline GeSn wire by Sb incorporation, which would be an ideal platform for GeSn-based photonic and electronic devices.

2.7 Summary

In this chapter, we proposed a novel method of fabricating a high-quality single-crystalline GeSn wire on a quartz substrate. By controlling a nucleation by local melting process, lateral liquid-phase crystallization propagates along the GeSn wire without using any crystal-seed or catalyst, and obtained a defect-free single-crystalline GeSn wire. Due to the large difference in thermal expansion coefficient between GeSn and quartz, tensile strain as high as 0.6% was induced in the liquid-phase grown GeSn, which promotes the bandgap modulation of GeSn and is beneficial for optoelectronic applications. From the Hall effect measurement, the conduction type of undoped GeSn was found to be p-type, and carrier concentration was estimated to be around 3×10^{16} cm^{-3}, indicating an excellent crystalline quality of liquid-phase grown GeSn. We have also examined the liquid-phase growth of Sb-doped GeSn wire on a quartz substrate for fabricating an n-type single-crystalline GeSn wire. It was found that the Sb incorporation hardly affect the liquid-phase growth of GeSn, and the Sb-doped GeSn wire has an excellent crystalline quality comparable to that of bulk Ge substrate. PL-based study revealed that Sb atoms were uniformly doped in the most part of liquid-phase grown GeSn wire due to the Sb segregation. The Hall effect measurement revealed that the Sb-doped GeSn wire was n-type with a carrier concentration of about 4×10^{16} cm^{-3}. The presented work in this chapter, single-crystalline undoped p-GeSn and Sb-doped n-GeSn wires, will offer an ideal platform for GeSn-based optoelectronic integration.

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Chapter 3

High-Mobility P- and N-Channel GeSn Thin-Film Transistors

3.1 Introduction

To enable the advanced monolithically-integrated optoelectronic circuit, high-mobility GeSn thin-film transistor (TFT) is strongly desired. However, there are only a few report on the GeSn-based TFT despite of its importance. In the previous chapter, we proposed a novel method of fabricating a tensile-strained single-crystalline GeSn wires on a quartz substrate. It was found that the both undoped p-type and Sb-doped n-type GeSn wires have an excellent crystalline quality that is comparable to a bulk Ge substrate, which would be an ideal platform for electronic device fabrication.

The aim of this chapter is to realize high-mobility p- and n-channel transistors based on the liquid-phase grown GeSn wires. The electrical properties of both undoped p-type and Sb-doped n-type GeSn wires were studied in detail and mobility behaviors were discussed.

3.2 Accumulation-Mode GeSn P-Channel Thin-Film Transistor

3.2.1 Fabrication process

First we investigated the electrical properties of undoped p-type GeSn wire on a quartz substrate. Figure 3-1 shows the device structure and fabrication process of top-gate undoped GeSn TFT. An 80-nm-thick undoped amorphous GeSn layer was deposited on a quartz substrate using a molecular beam deposition system and patterned into narrow stripes (W/L = 3/300 μm). After depositing a thick SiO_2 capping layer (~1 μm), RTA (938°C, 1 s) was performed in N_2 ambient for the local melting of a-GeSn wire. After thinning the SiO_2-capping layer to 230 nm to use as a gate insulator, source/drain (S/D) contact windows were patterned by reactive ion etching (RIE) and buffered hydrofluoric acid (BHF) etching. Then, Al gate (gate length (L_g) of 80 μm) and

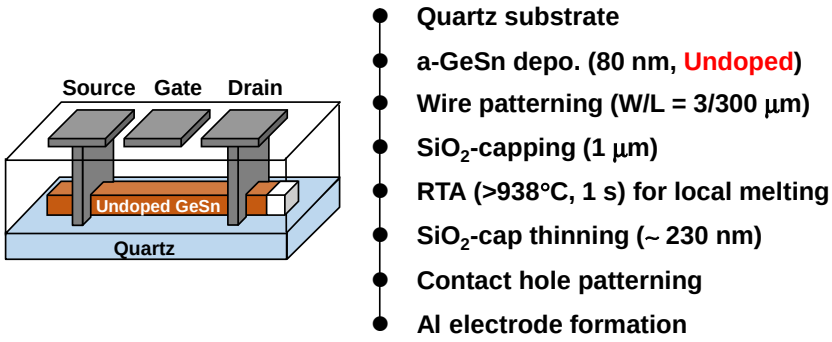

Fig. 3-1 Fabrication process of top-gate undoped GeSn TFT on quartz substrate.

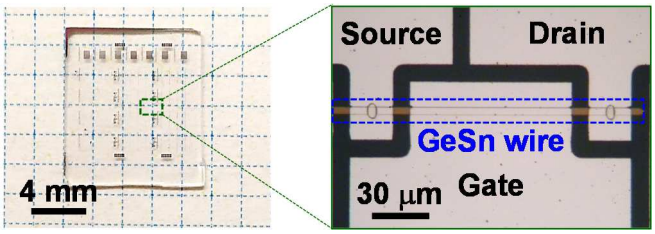

Fig. 3-2 Photograph and optical image of fabricated top-gate undoped GeSn TFT on quartz substrate. Dotted line indicates single-crystalline GeSn wire (channel).

S/D electrodes were formed by vacuum evaporation and wet etching. For a comparison, poly-crystalline undoped GeSn TFT was also fabricated by complete melting process. Figure 3-2 shows the photograph and optical image of fabricated top-gate undoped GeSn TFT.

3.2.2 Transistor Operation and Mobility Characterization

Figures 3-3(a) and 3-3(b) show the drain current-gate voltage (I_d-V_g) and drain current-drain voltage (I_d-V_d) characteristics of the single-crystalline undoped GeSn TFT formed on quartz substrate, respectively. The electrical characteristics of a poly-crystalline GeSn TFT formed by complete melting of the amorphous GeSn wire are also shown in Fig. 3-3(a). Since point defects are known to act as acceptor-like state in the GeSn crystals, the undoped GeSn TFTs were operated in the p-type accumulation-mode, which is consistent with the result obtained from Hall effect measurement (Fig. 2-14). As shown in Fig. 3-3(a), well-behaved p-FET operation with an on/off ratio of over 10^2 was achieved for the single-crystalline GeSn TFT (blue), which is much better than the poly-crystalline TFT (red).

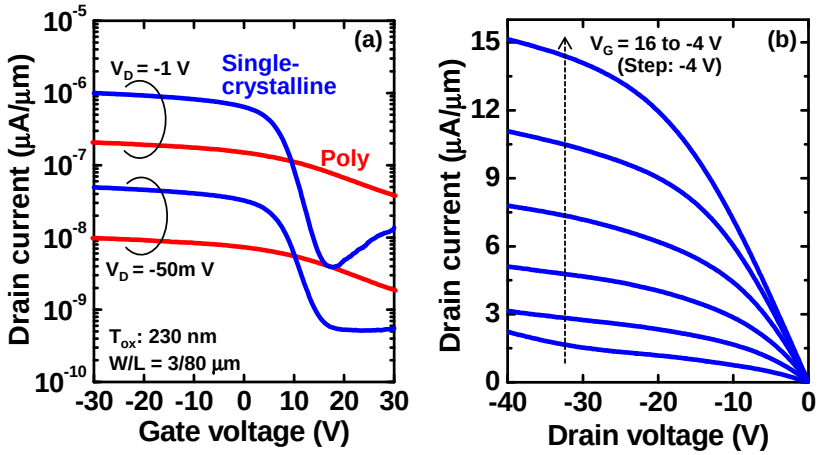

Fig. 3-3 (a) I_d-V_g and (b) I_d-V_d characteristics of single-crystalline undoped GeSn TFT fabricated on quartz substrate. Those of poly-crystalline GeSn TFT are also shown for comparison (Reprinted from ref 12, with the permission of AIP Publishing).

Then we investigated the hole mobility in the single-crystalline undoped GeSn wire. The field-effect mobility (μ_{FE}) is widely used to evaluate the carrier transport property of transistor, which is described as following equation:

$$\mu_{FE} = \frac{g_m L_g}{W C_{ox} V_D}$$

where g_m and C_{ox} denote the transconductance and capacitance of the gate insulator, respectively. As shown in Fig. 3-4(a), the peak field-effect hole mobility of undoped p-channel GeSn TFT was estimated to be 423 cm^2/Vs. This value is much higher than that of poly-crystalline one (μ_{FE}: 26 cm^2/Vs) and

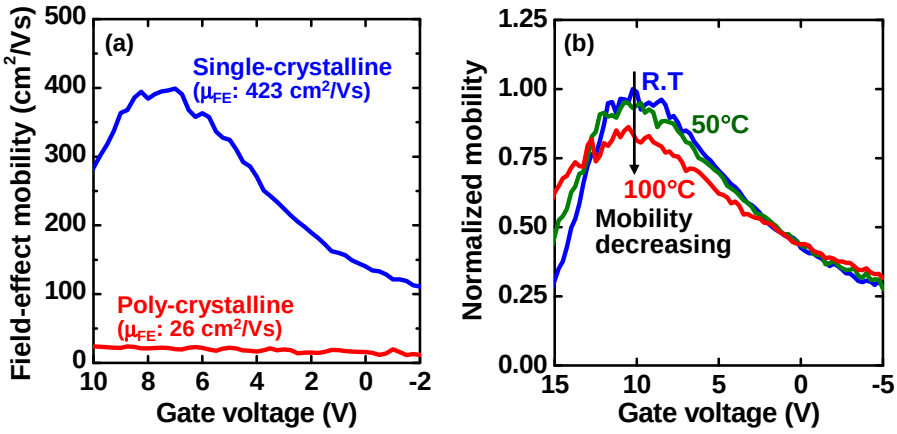

Fig. 3-4 (a) Field-effect hole mobility of undoped single- and poly-crystalline GeSn TFTs. (b) Temperature-dependence of field-effect hole mobility for single-crystalline GeSn TFT.

exceeds the reported values for Ge and GeSn TFTs [1-3]. It should be noted that the obtained hole mobility is comparable to or higher than that of a single-crystalline GeSn MOSFET fabricated on bulk Ge substrate [4-5]. Also, as shown in Fig. 3-4(b), the field-effect hole mobility decreased with increasing measurement temperature (×0.85 in the peak mobility at 100°C compared to the R.T.), suggesting that the mobility was limited by phonon scattering. This indicates excellent crystal quality of the GeSn wire formed with this technique. For further investigation of the effect of Sn incorporation and tensile strain on mobility enhancement, low-field hole mobility (μ_0) was also extracted from the I_d-V_g characteristics on the basis of the following equation, which is so called Y-function method [6].

$$\frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{WC_{ox}\mu_0 V_D}{L}}(V_G - V_{FB})$$

where V_{FB} is the flatband voltage. Figure 3-5 shows the Y-function-gate voltage plot of the undoped p-channel GeSn TFT. From the slop of the Y-function plot, the low-field hole mobility was estimated as high as 1029 cm^2/Vs at a drain voltage of -50 mV, where V_g range used in the calculation was 5 to 2 V.

By using the following equation [7], the hole concentration of the single-crystalline GeSn layer can be roughly estimated.

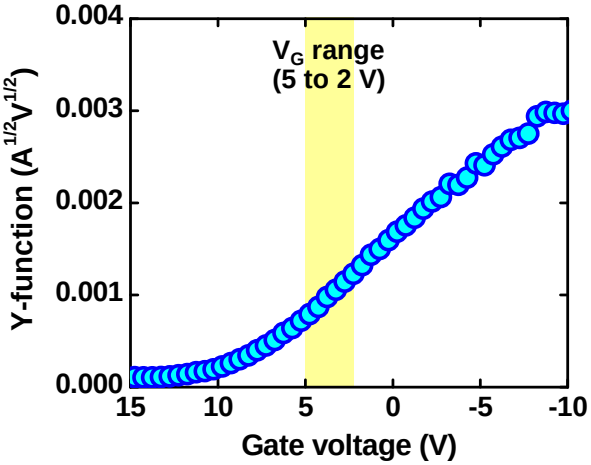

Fig. 3-5 Y-function-gate voltage plot of the undoped p-channel GeSn TFT.

$$p = \frac{1}{q\mu\rho}$$

Where p is the hole concentration, q is the electrical charge, and ρ is the resistivity of the GeSn channel, which was experimentally extracted. The hole concentration was estimated to be 2.5×10^{17} cm^{-3}. By using Irvin's curve for Ge [8], which is well-known as a practical relation between carrier concentration and resistivity, the bulk hole mobility of Ge at a given hole concentration can be theoretically calculated using the above equation (Fig. 3-6). The corresponding hole mobility of bulk Ge with a hole concentration of 2.5×10^{17} cm^{-3} was estimated to be 873 cm^2/Vs, which means 18% mobility enhancement for single-crystalline GeSn (μ_0: 1029 cm^2/Vs) with respect to bulk Ge. Since the channel Sn content in the single-crystalline GeSn MOSFET (2.6%) is not enough for 18% enhancement in hole mobility [9], the improved hole mobility is also attributed to the biaxial tensile strain by increasing the light hole population [10]. These results clearly demonstrate the advantage of our proposed crystallization technique to integrate high-mobility GeSn transistors on quatz substrates together with high-efficiency GeSn optical devices.

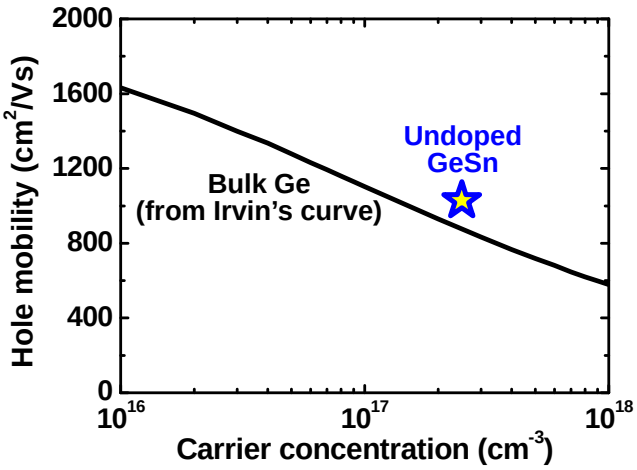

Fig. 3-6 Benchmark of low-field hole mobility for undoped GeSn TFT with in comparison with that of bulk Ge calculated using Irvin's curve.

3.2.3 Thickness Dependence of Mobility

We have also investigated the thickness dependence on carrier mobility in the p-channel GeSn TFT (Fig. 3-7(a)). In this study, amorphous GeSn wires with

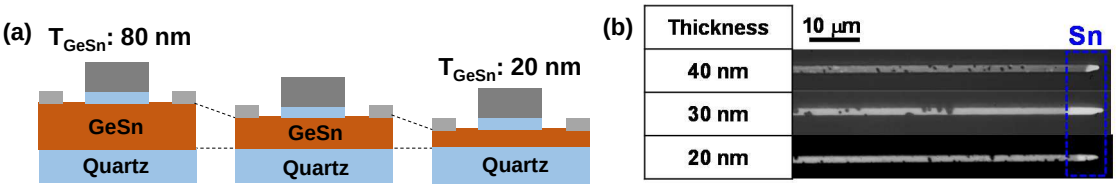

Fig. 3-7 (a) Schematic illustration of p-channel GeSn TFTs with various thicknesses. (b) Optical images of GeSn wire after nucleation-controlled liquid-phase growth with GeSn thicknesses down to 20 nm.

various thicknesses (20 to 80 nm) were locally melted to induce the lateral liquid-phase growth. We have confirmed that the single-crystallization successfully proceeded even in the ultra-thin 20-nm-thick GeSn wire (Fig. 3-7(b)). The GeSn p-channel TFTs with various thicknesses were fabricated with same procedure described in session 3.2.1. For a comparison, Ge p-channel TFT was also fabricated on a commercially-available Ge-on-insulator (GeOI) substrate.

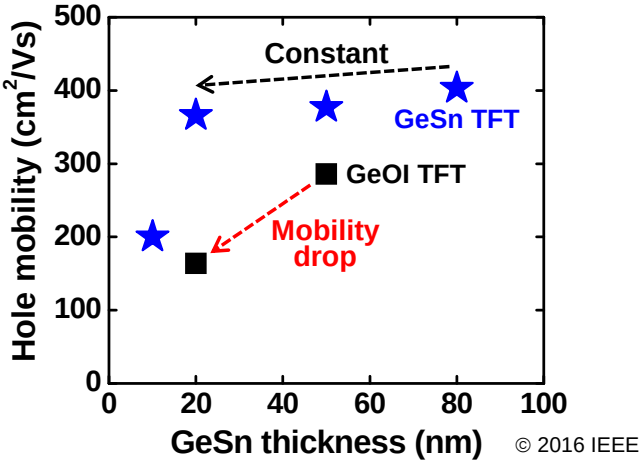

Fig. 3-8 Thickness dependence of field-effect hole mobility in GeSn and control GeOI TFTs [22].

Figure 3-8 shows GeSn (or Ge) thickness dependence on the field-effect hole mobility. In contrast to the GeOI TFTs, hole mobility of GeSn p-FETs hardly degraded with reducing GeSn layer thickness down to 20 nm, suggesting excellent crystalline quality near quartz substrate and superior interface property compared to the commercially-available GeOI substrate formed by wafer bonding. This clearly indicates the advantage of fabricated GeSn TFT that would be applicable to aggressively scaled MOSFET, which has immunity to short channel effect.

In this session, well-behaved accumulation-mode p-FET operation was successfully demonstrated for a fabricated single-crystalline undoped GeSn TFT on a quartz substrate. Also, a record-high field-effect hole mobility of 423 cm^2/Vs was obtained, indicating excellent crystal quality and mobility enhancement due to Sn incorporation and tensile strain. These results clearly reveal the potential of liquid-phase grown GeSn wire, which would be applicable to monolithically-integrated optoelectronic circuit.

3.3 Accumulation-Mode GeSn N-Channel Thin-Film Transistor

3.3.1 Fabrication process

In the previous session, we have demonstrated a record-high hole mobility GeSn p-channel TFT based on the undoped GeSn wire on a quartz substrate. To realize a high-performance GeSn CMOS circuit, fabrication of high-mobility GeSn n-channel TFT is also quite important. As described in chapter 2, we have fabricated a Sb-doped single-crystalline GeSn wire with an excellent crystalline quality. Also, the PL-based study revealed that the Sb was uniformly doped in the most middle part of liquid-phase grown GeSn wire, which would be useful for transistor fabrication. In this study, we fabricated an Sb-doped GeSn TFT and investigated the electrical properties in detail.

Figure 3-9 shows the fabrication process of Sb-doped GeSn TFT. An 80-nm-thick Sb-doped amorphous GeSn layer was deposited on a quartz substrate using a molecular beam deposition system, where Ge, Sn and Sb were co-evaporated. The Sb concentration in a-GeSn layer was around 5×10^{19} cm^{-3}. After patterned the Sb-doped a-GeSn layer into narrow stripes (W/L = 2/300 μm), thick SiO_2 capping layer was deposited and RTA (938°C, 1 s) was performed in N_2 ambient for the local melting of Sb-doped a-GeSn wire. After thinning the SiO_2-capping layer to 200 nm to use as a gate insulator, Al gate and S/D electrodes were formed. In this study, the middle part of Sb-doped GeSn wire, where the active doping level was almost uniform (Fig. 2-20), was used as a channel.

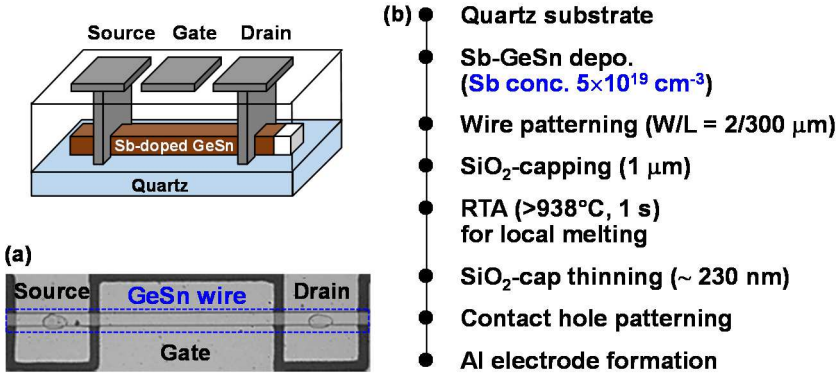

Fig. 3-9 (a) Optical image and (b) fabrication process of Sb-doped GeSn TFT on quartz substrate.

3.3.2 Transistor Operation and Mobility Characterization

The I_d-V_g and I_d-V_d characteristics of the fabricated Sb-doped GeSn TFT are shown in Figs. 3-10(a) and 3-10(b), respectively. A well-behaved accumulation-mode n-channel operation was obtained, and again confirmed a successful n-type doping by Sb incorporation.

The extracted field-effect electron mobility was 84 cm^2/Vs, which is much lower than the expected electron mobility in tensile-strained GeSn alloy [11]. Also, as shown in Fig. 3-11, the electron mobility increases with increasing measurement temperature. In the case of undoped p-channel TFT, the hole mobility decreased with increasing measurement temperature, (Fig. 3-4(b)) suggesting that the mobility was limited by phonon scattering [12]. Although the Sb-doped GeSn wire has an excellent crystalline quality comparable to that of

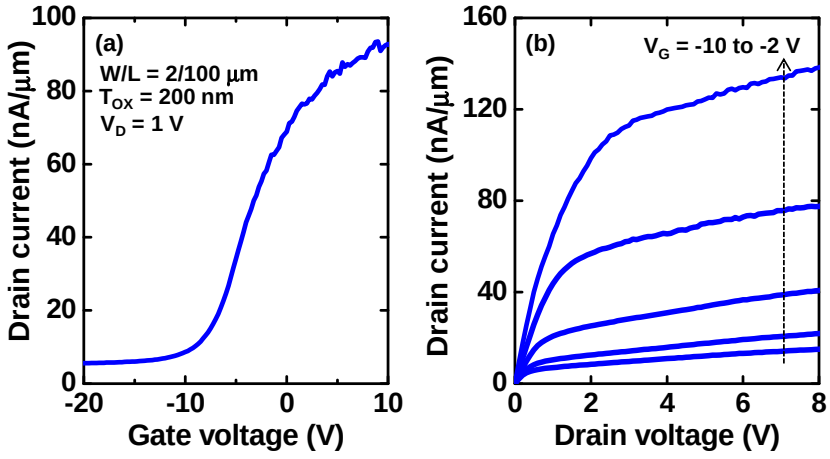

Fig. 3-10 (a) I_d-V_g and (b) I_d-V_d characteristics of single-crystalline Sb-doped GeSn TFT fabricated on quartz substrate (Ref. 23, Copyright 2018 The Japan Society of Applied Physics).

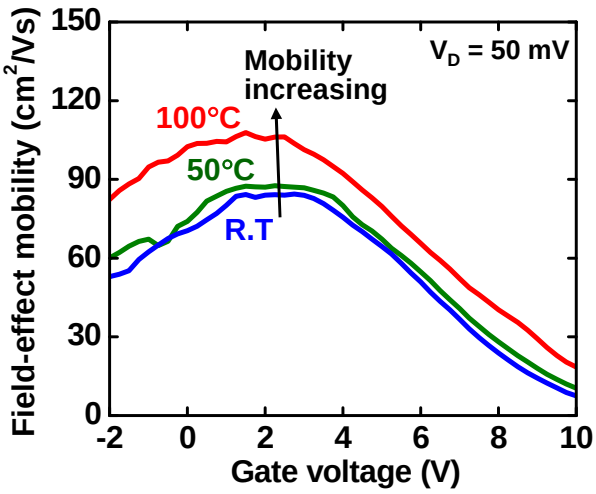

Fig. 3-11 Temperature-dependence of field-effect hole mobility for single-crystalline Sb-doped GeSn TFT.

undoped GeSn wire (Fig. 2-19), the temperature dependence of mobility is entirely different. It is generally known that the presence of large amount of interface states would attribute to mobility enhancement with increasing measurement temperature due to thermally generated carriers, but there is negligible threshold shift in the peak electron mobility, which means the the effect of interface states is less likely. From these results, it is strongly suggested that the high parasitic resistance in Sb-doped GeSn TFT severely limits the electron mobility.

It is well known that the high S/D contact resistance is formed at the metal/n-type Ge interface due to the Fermi level pinning (FLP) effect, in which the Fermi level of various metals is pinned near the valence band edge, leading to a high Schottky barrier height of about 0.60 eV for electron, while Schottky barrier height for hole is quite low (Fig. 3-12) [13,14]. Similar FLP effect for metal/GeSn contacts was also reported [15]. Thus, the limited electron mobility would be attributed to the FLP effect at the metal/n-GeSn interface. (Fig. 3-13) When a GeSn layer is heavily n-type doped, the Schottky barrier depletion width becomes narrower and thus reducing the contact resistance. However, the fabricated Sb-doped GeSn wire is lightly doped n-type with a carrier concentration of about 4×10^{16} cm^{-3} (Fig. 2-21), which leads to a high Schottky barrier height at metal/n-GeSn interface.

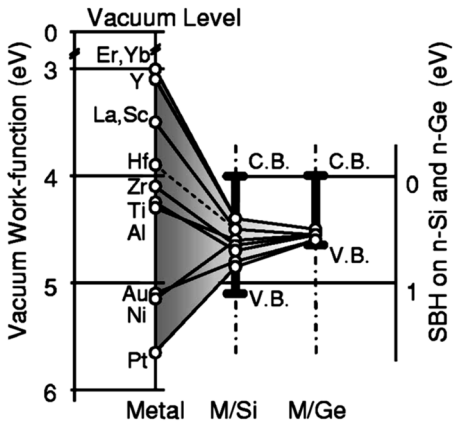

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Fig. 3-12 Fermi level of metal/Si and metal/Ge contacts with various metals. In case of Ge, Fermi level is pinned near valence band edge [13].

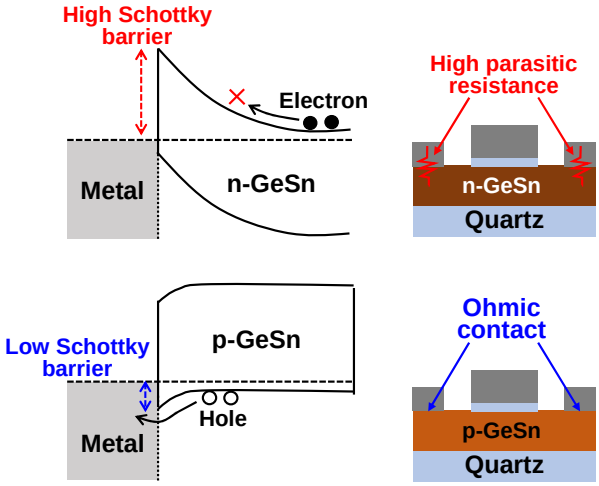

Fig. 3-13 Schematic illustrations of Fermi level pinning at metal/Ge contacts.

Although the lightly n-type doped GeSn wire is beneficial for various optoelectronic applications, the electron mobility was quite low in an accumulation-mode transistor due to FLP effect and not suitable for GeSn-based CMOS circuit. Therefore, further improvement in electron mobility is required.

3.4 High-Mobility Enhancement-Mode N-Channel Thin-Film Transistor Based on Single-Crystalline GeSn n^+/p Junction

3.4.1 Concept of This Work

By using the nucleation-controlled liquid-phase crystallization technique, we fabricated a high-quality single-crystalline undoped p-type and Sb-doped n-type GeSn wires on a quartz substrate and demonstrated accumulation-mode p- and n-channel TFTs. However, the device performance of Sb-doped GeSn n-channel TFT was severely limited by high contact resistance at the metal/n-GeSn interface due to FLP effect. One of the most effective method to reduce the contact resistance is a heavy n-type doping, in which the Schottky barrier depletion width becomes narrower as shown in Fig. 3-14. Therefore, in this study, we have examined P^+ implantation into liquid-phase-grown undoped GeSn wire to form high-quality n^+/p junction (Fig. 3-15). We systematically

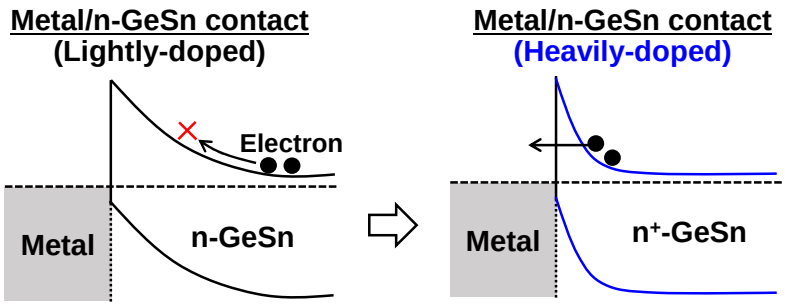

Fig. 3-14 Band diagrams of metal/n-GeSn contacts with lightly- and heavily-doped GeSn layer.

investigated the activation behavior of P ions in GeSn layer and evaluated the electrical characteristics of GeSn n^+/p junction. Also, enhancement-mode n-channel TFT was demonstrated based on GeSn n^+/p junction and mobility behavior was studied in detail.

3.4.2 Single-Crystalline GeSn n^+/p Junction

3.4.2.1 Fabrication Process

Figure 3-16 shows the fabrication procedure of n^+/p junction in a single-crystalline GeSn on a quartz substrate. A 230-nm-thick undoped amorphous GeSn layer was deposited on a quartz substrate by molecular beam deposition system and patterned into narrow stripes (W/L = 3/300 μm, Sn 2%). Then, a thick SiO_2-capping layer (1 μm) was sputter deposited and RTA (>938°C, 1 s) was performed for the local annealing of amorphous GeSn wire to induce the nucleation-controlled liquid-phase growth. After thinning the SiO_2 layer down to 50 nm, P ions were implanted (2×10^{15} cm^{-2}, 40 keV) through a photo resist mask.

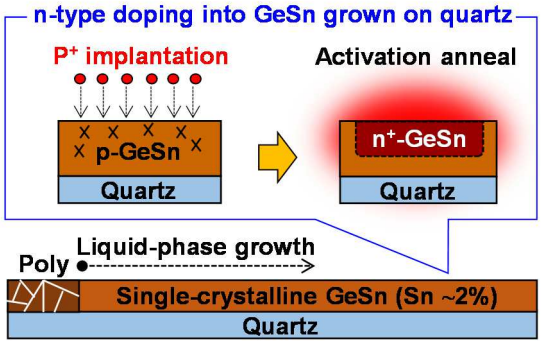

Fig. 3-15 Single-crystalline GeSn n^+/p junction by combination of nucleation-controlled liquid-phase growth and ion-implantation.

A simple ion-trajectory simulation [16] indicated that the peak of implanted P^+ profile located near GeSn surface (Fig. 3-17). Then, oxide mask was dry etched and a 100-nm-thick field oxide was sputter deposited. Dopant activation annealing at various temperatures (400-600°C) was performed in N_2 ambient for 5 min. For the electrical characterization, Al contact was formed on both undoped and P^+-implanted side in the GeSn wire.

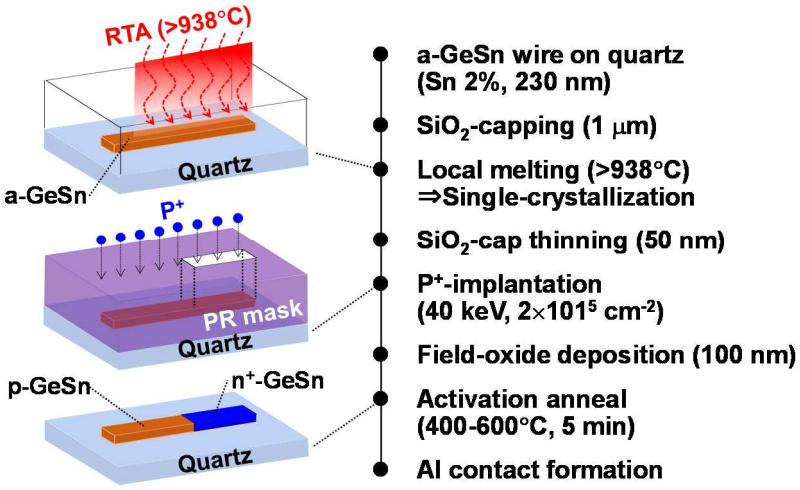

Fig. 3-16 Fabrication process of single-crystalline GeSn n^+/p junction on quartz substrate.

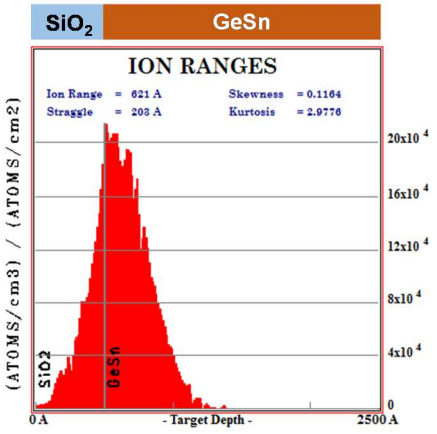

Fig. 3-17 Ion-trajectory simulation (TRIM) of P^+ profile in GeSn layer with acceleration energy of 40 keV.

3.4.2.2 Activation Behavior of P^+ in GeSn

In order to optimize the activation annealing temperature, we first investigated the crystallinity of P^+-implanted GeSn wire. Figure 3-18 shows the Raman spectra obtained from P^+-implanted GeSn wires with different activation

annealing temperature. The Raman peak of GeSn wire is shifted to a lower wave number compared to the bulk Ge substrate, which is originating from a Sn incorporation and tensile strain. This result is consistent with our previous study (Fig. 2-8). The increased peak intensity was observed for the P^+-implanted GeSn wire with higher activation annealing temperature, suggesting the recovery of implantation damage. It should be noted that the Raman shift remains constant to activation annealing temperature, which indicates the negligible Sn segregation or out-diffusion during activation annealing. Thus, we can conclude that the P^+-implanted GeSn wire is thermally robust up to 600°C, which would be enough high temperature for device fabrication and operation.

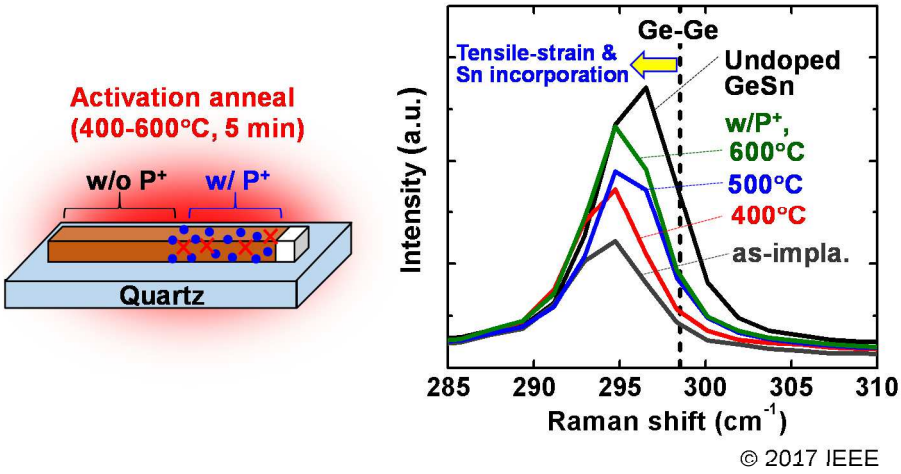

Fig. 3-18 Raman spectra from P^+-implanted GeSn wires with activation annealing at various temperatures [24].

The activation behavior of P^+ in the GeSn wire was evaluated by the μ-PL measurement. As mentioned in session 2.6.2.2, since PL intensity increased with increasing electrically active donor concentration, we can evaluate the temperature dependence of active P^+ concentration in GeSn. As shown in Fig. 3-19, significant enhancement of PL intensity was observed for the sample annealed above 500°C, which is due to increase in electron population at Γ-valley by n-type doping. Thus, it is suggested that the heavily n-type doped GeSn was formed by activation annealing at 500 and 600°C. It should be noted that the slight decreased PL intensity was observed for the sample annealed at 600°C, which can be explained by the diffusion of P^+ [17]. Figure 3-20 summarizes the peak PL intensity as a function of annealing temperature. For a

comparison, P^+-implanted Ge wire was also fabricated on a commercially available GeOI substrate. In contrast to the enhanced luminescence of P^+-implanted GeSn wire, P^+-implanted Ge wire exhibited the degraded PL intensity which is lower than undoped one. This result suggest that the implantation-damage in Ge wire hardly recovered, and the Sn incorporation promotes the recovery of crystallinity from implantation damage. However, the physical mechanism is unclear and further studies are needed.

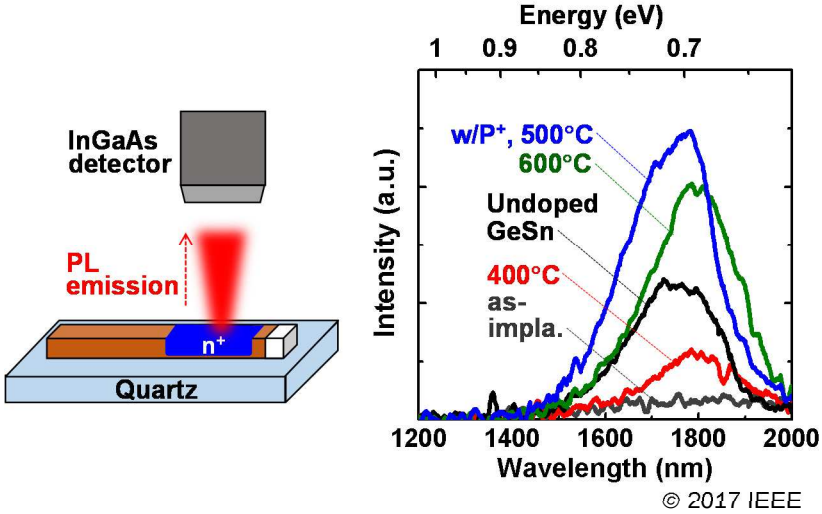

Fig. 3-19 Raman spectra from P^+-implanted GeSn wires with activation annealing at various temperatures [24].

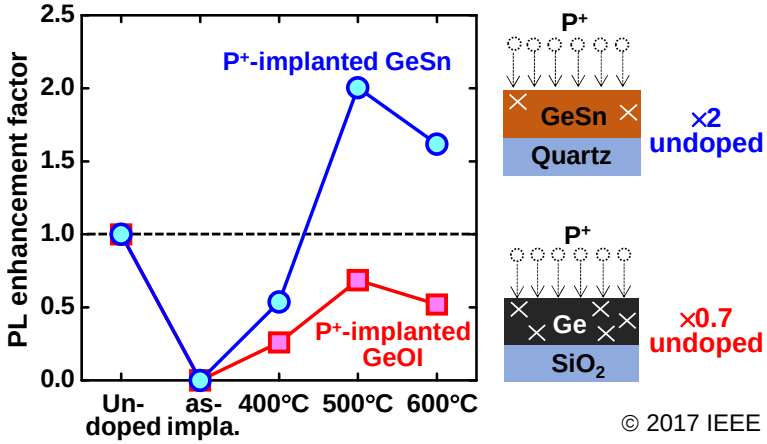

Fig. 3-20 Enhancement of PL peak intensity for P^+-implanted GeSn and GeOI wires as a function of annealing temperature [24].

Figure 3-21 shows the position dependence of PL intensity for P^+-implanted GeSn wire. It was found that the enhanced luminescence was observed only in the implanted region (×2 undoped) and it exhibits rapid increase at the

undoped/implanted interface, suggesting that the abrupt n^+/p junction was formed along the wire (Fig. 3-21).

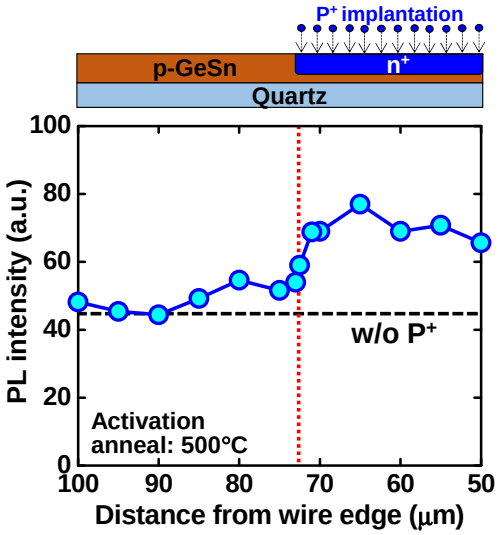

Fig. 3-21 Position dependence of PL intensity for P^+-implanted GeSn wire [24].

3.4.2.3 Current-Voltage Characteristics

Figure 3-22 shows the optical image and I-V characteristics of GeSn n^+/p diodes fabricated on a quartz substrate with activation annealing at various temperatures. For a comparison, I-V characteristic of undoped GeSn wire is also shown. Due to the FLP effect at metal/GeSn interface, Schottky barrier height for hole is quite low (<0.1 eV) and thus Ohmic feature was observed for undoped GeSn wire. On the other hand, well-behaved rectifying characteristics with an

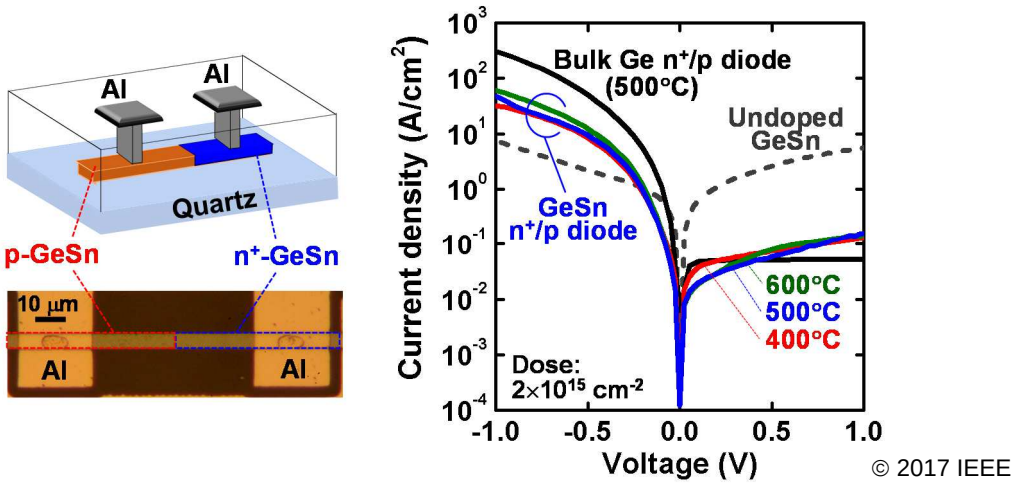

Fig. 3-22 I-V characteristics of n^+/p diodes fabricated in GeSn wires on quartz substrate with activation annealing at various temperatures [24].

on/off ratio of 10^3 were obtained for the GeSn n^+/p diodes, suggesting P ions were highly activated in GeSn layer and that is consistent with photoluminescence results. Also, a dark current is comparable to n^+/p diode formed on bulk Ge substrate, which would be due to an excellent crystalline quality of the liquid-phase grown GeSn wire.

3.4.3 Transistor Operation and Mobility Characterization

As described in the previous session, we have succeeded in fabricating a high-quality n^+/p junction by P^+ implantation into liquid-phase grown GeSn wire. Based on the GeSn n^+/p junction, we next fabricated an enhancement-mode n-channel TFT. Although high electron Schottky barrier height is formed at the metal/n-GeSn interface, heavily n-type doping reduces Schottky barrier depletion width and thus reducing contact resistance. Therefore, mobility enhancement is expected in enhancement-mode n-channel TFT compared to accumulation-mode one.

Figure 3-23 shows the fabrication procedure and optical image of enhancement-mode GeSn n-channel TFT. After forming a single-crystalline GeSn wire (Sn ~2%) on a quartz substrate, P ions were implanted into the S/D region. After performing an activation annealing at 500 or 600°C, Al gate and S/D contact were formed. Figure 3-24 shows the I_d-V_g and I_d-V_d characteristics of the fabricated enhancement-mode GeSn n-channel TFT. Successful n-channel transistor operation was observed, and the on-current of enhancement-mode TFT was found to be much higher than that of accumulation-mode one (Fig. 3-24).

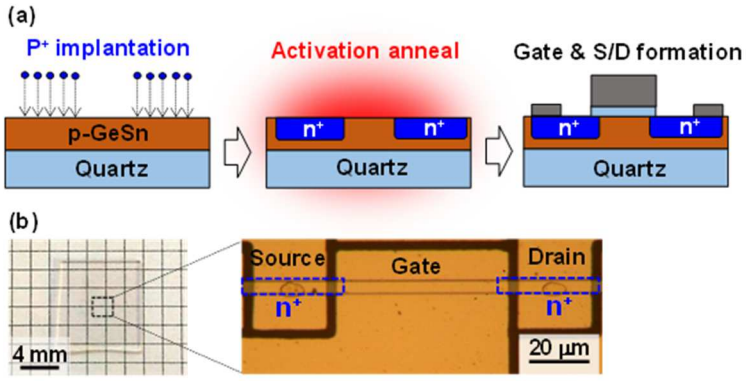

Fig. 3-23 (a) Fabrication procedure and (b) optical image of enhancement-mode GeSn n-channel TFT

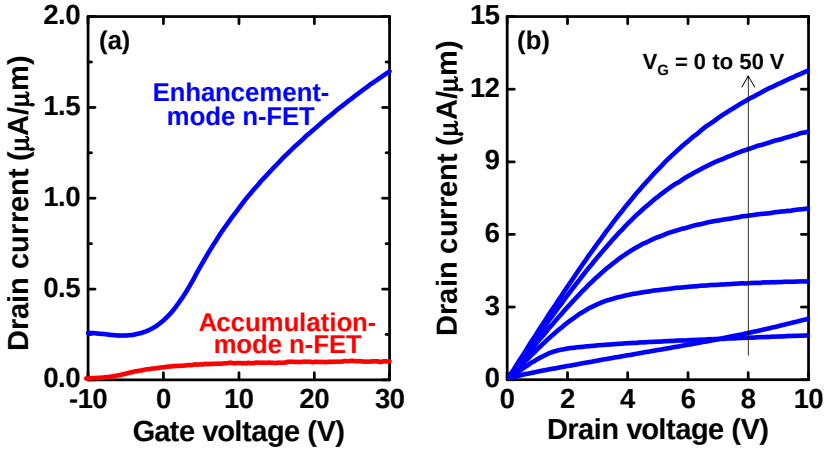

Fig. 3-24 (a) I_d-V_g and (b) I_d-V_d characteristics of single-crystalline GeSn n-channel TFT fabricated on quartz substrate.

The extracted field-effect electron mobility of enhancement-mode GeSn TFT is shown in Fig. 3-25(a). The improved electron mobility over 220 cm^2/Vs was obtained, which is much higher than that of accumulation-mode TFT (Fig. 3-11). Temperature-dependent mobility behavior was also studied. In contrast to an accumulation-mode GeSn TFT, the electron mobility in enhancement-mode TFT decreased with increasing measurement temperature (Fig. 3-25(b)), which indicates the mobility was limited by the phonon scattering as in the case of undoped GeSn TFT. This is a clear evidence of reduced contact resistance by heavy n-type doping, in which Schottky barrier depletion width at metal/n-GeSn contacts becomes narrower. Figure 3-26 shows the benchmark of electron

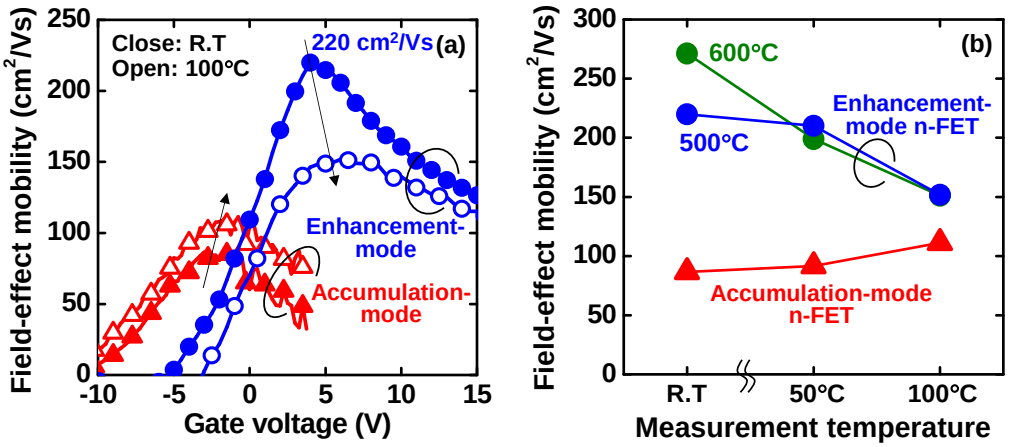

Fig. 3-25 (a) Temperature dependence of field-effect electron mobility for enhancement-mode and accumulation-mode GeSn n-channel TFTs. (b) Field-effect electron mobility as function of measurement temperature.

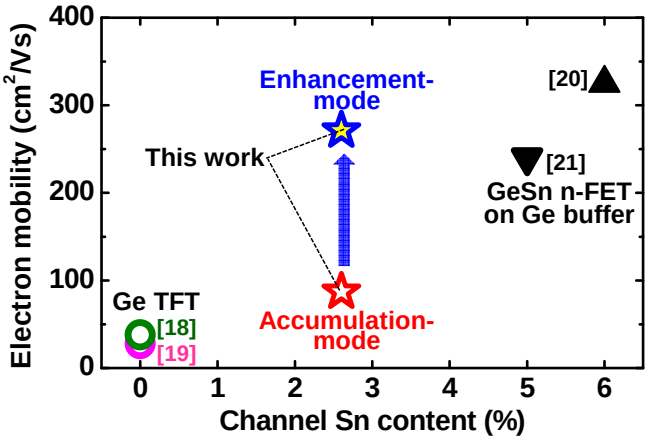

Fig. 3-26 Benchmark of electron mobility with previously reported Ge-based n-channel TFTs.

mobility with previously reported Ge-based n-channel transistors. In this work, record-high electron mobility of 271 cm^2/Vs was achieved for the enhancement-mode GeSn n-channel TFT (600°C activation anneal), which is much higher than Ge n-channel TFT and comparable to that of GeSn n-MOSFET fabricated on a bulk substrate. This result again indicates the excellent crystalline quality of the liquid-phase grown GeSn wire, and we have succeeded in demonstrating a potential of GeSn alloy as a high-mobility CMOS channel material.

3.5 Summary

In this chapter, we demonstrated both p- and n-channel GeSn TFTs based on undoped p-type and Sb-doped n-type liquid-phase grown GeSn wires, respectively. A record-high hole mobility of 423 cm^2/Vs was obtained for the undoped p-FET, which indicate the excellent crystalline quality of liquid-phase grown GeSn wire. On the other hand, it was found that the electron mobility in Sb-doped n-FET is severely limited by high parasitic resistance at S/D region due to the FLP effect. In order to improve the n-channel transistor performance, we examined heavy n-type doping by P^+ implantation. An well rectifying behavior with on/off ratio of 10^3 was obtained, and the PL-based study revealed the abrupt n^+/p junction was successfully formed. Based on single-crystalline GeSn n^+/p junction on a quartz substrate, we fabricated an enhancement-mode n-channel TFT. A record-high electron mobility of 271 cm^2/Vs was obtained, and the temperature-dependence of mobility revealed that the mobility was limited by

phonon scattering, which clearly indicates the reduced contact resistance by heavy n-type doping.

From these result, we have succeeded in fabricating a high-mobility GeSn p- and n-channel TFTs for the first time based on liquid-phase grown GeSn wires. The presented CMOS technology will facilitate the monolithic integration of optoelectronic devices on various insulating substrates.

References – Chapter 3 –

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Chapter 4

Fabrication of Back-Illuminated GeSn Photodiode Array for Monolithically-Integrated Near-Infrared (NIR) Imager Chip

4.1 Introduction

As mentioned in chapter 1, GeSn alloy is also promising for photonic applications especially imaging/sensing in the NIR wavelength range (1.5-5 μm) due to its tunable bandgap. So far, NIR photonic devices such as laser or photodetector have been developed based on direct bandgap III-V compound semiconductors, which have high sensitivity to the NIR wavelength range (Fig. 4-1). However, there are several issues in III-V-based electronic and photonic integrated device such as a NIR imager chip. Figure 4-2 illustrates device structure of conventional NIR imager chip (left figure). Light receiving component (photodiode array) is fabricated on III-V semiconductors such as an InGaAs, while Si-LSI is commonly used for signal processing component (read-out circuit) that is fabricated on Si substrate by mature CMOS technology. In order to integrate III-V photodiodes on Si-based read-out circuit, wafer bonding or heteroepitaxy have been utilized. However, an incorporation of III-V material to Si-process leads to increase in process complexity, and it is generally

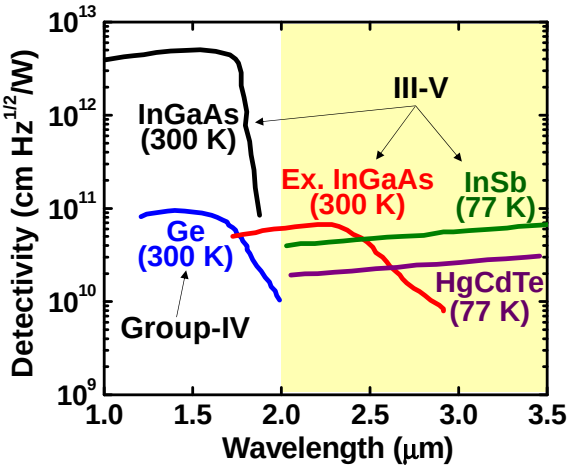

Fig. 4-1 Detectivity of group-IV and III-V compound semiconductors in NIR wavelength range [1].

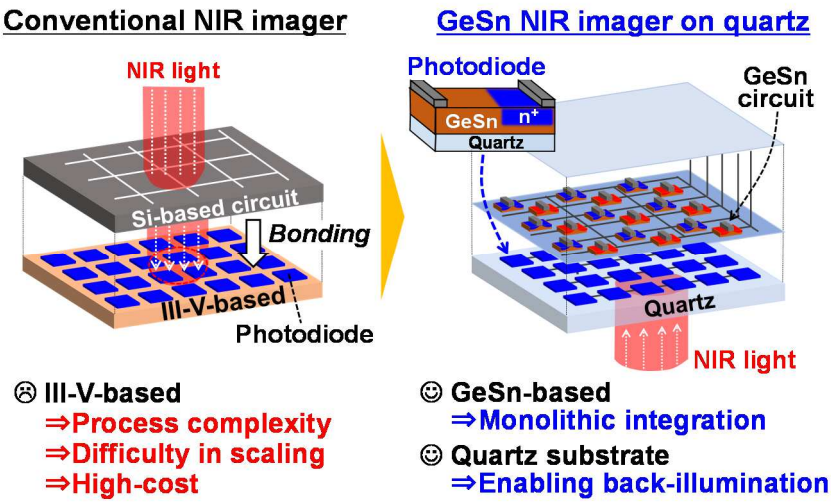

Fig. 4-1 Schematic illustrations of conventional NIR imager chip and our proposed monolithically-integrated GeSn-based NIR imager chip on quartz substrate.

high-cost. Also, there is a concern about cross contamination since group-III and group-V elements behave as p- and n-type dopants, respectively. Therefore, realization of fully-integrated group-IV-based optoelectronic circuit is strongly desired for not only optical interconnection on Si-LSI but also various photonic applications in the NIR wavelength range.

In this work, by using the liquid-phase crystallization technique, a high-quality tensile-strained single-crystalline GeSn wire was successfully grown on a quartz substrate (Chapter 2). Based on the liquid-phase grown GeSn wires, we report the first demonstration of p- and n-channel GeSn TFTs and achieved record-high hole and electron mobility that outperforms previously reported Ge-based TFTs. These results clearly indicate the potential of tensile-strained GeSn alloy as a high-mobility CMOS channel material (Chapter 3). Thus, integration of GeSn-based NIR photonic devices and CMOS circuit opens a way for advanced group-IV-based optoelectronic circuit. Also, since a quartz has high transparency to the NIR light, single-crystalline GeSn layer on a quartz substrate would be an ideal platform for NIR photodetection or light emission. Therefore, in this chapter, we examined the fabrication of highly-efficient GeSn photodetector based on the liquid-phase grown GeSn layer on quartz substrate to demonstrate fully-integrated GeSn-based NIR imager chip.

For this purpose, we proposed a novel liquid-phase crystallization technique based on laser annealing to form a single-crystalline GeSn array on quartz

substrate for enabling NIR image sensor. By performing P ion implantation, GeSn photodiode array was successfully fabricated and the electrical properties were studied in detail. Also, NIR photoresponse of GeSn n^+/p photodiode under both front- and back-side illumination was evaluated.

4.2 Laser-Induced Liquid-Phase Crystallization

4.2.1 Concept of This Technique

In order to fabricate an image sensor, two-dimensional focal plane array is required for photodetection. However, the lateral liquid-phase growth of GeSn wire by local melting based on RTA requires non-melting region and cannot be used for crystallization of GeSn array, since completely melted GeSn array becomes poly-crystalline while that in non-melted region remains amorphous as illustrated in Fig. 4-3 (left figure). Thus, alternative method for crystallizing GeSn array is required for enabling NIR image sensor on a quartz substrate.

Figure 4-4 shows the captured images of *in-situ* optical microscope movie recording the lateral liquid-phase crystallization of GeSn wire on quartz substrate just after turning off the RTA lamps. Since the lateral growth is expected to propagate very fast within a nanosecond, long working distance optical microscope (WD: 100 mm) equipped with digital high-speed camera (2000 fps, 1280×1024 dots) was used for the observation. As shown in Fig. 4-4(b), bright contrast region in GeSn wire moves toward the edge of wire, suggesting the successful direct observation of lateral growth. To the best of our knowledge, this is the first report of direct observation of liquid-phase crystallization of GeSn

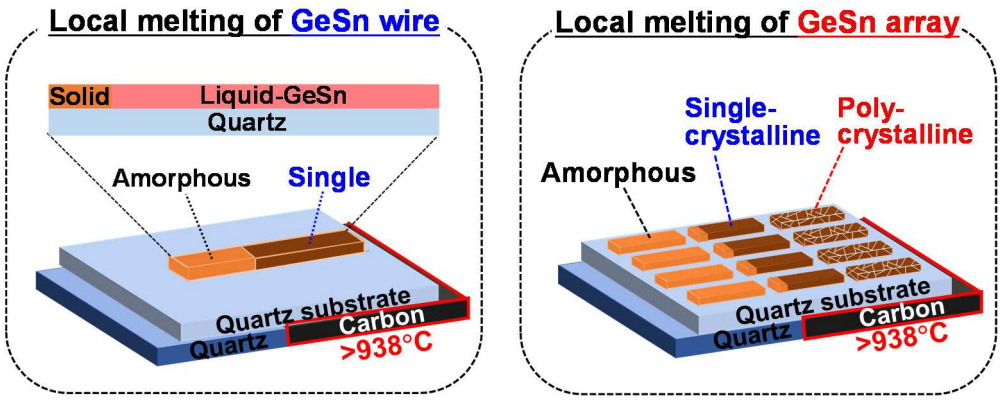

Fig. 4-3 Schematic illustrations of RTA-based local melting for GeSn wire and array on quartz substrate. Single-crystalline GeSn array cannot be formed with this method.

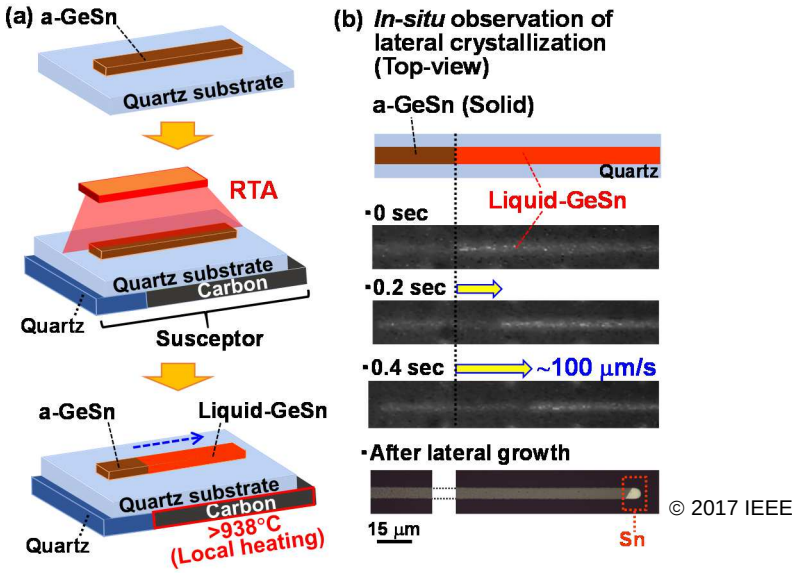

Fig. 4-4 (a) Schematic illustration and (b) in-situ observation of lateral liquid-phase growth of GeSn wire on quartz substrate [2].

alloy. It was found that the crystallization was initiated at the solid/liquid interface and laterally propagated along the wire with a growth speed of about 100 μm/s. This indicates the temperature gradient along the wire is the key for single-crystallization. Since the local melting with temperature gradient would be performed by laser scanning annealing, we have examined the laser-induced liquid-phase crystallization by scanning laser beam along the GeSn wires to form large-area GeSn array (Fig. 4-5).

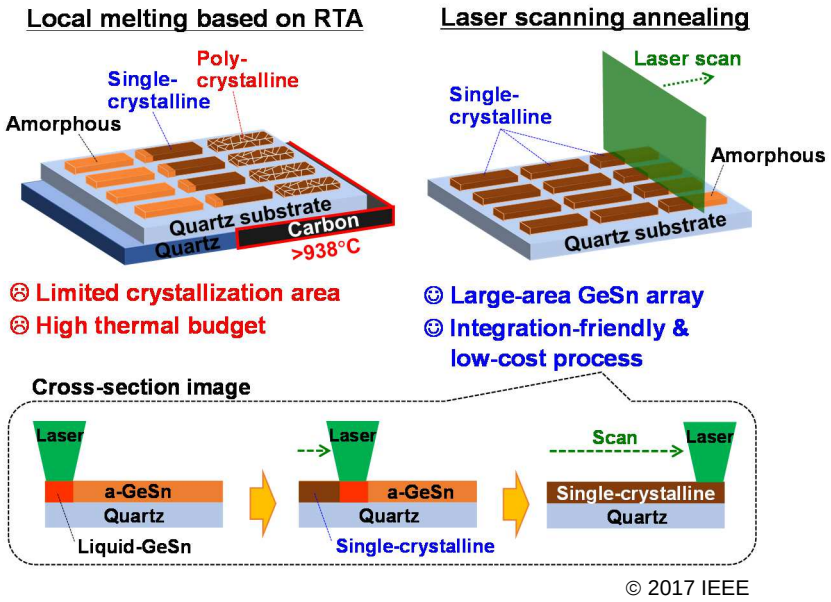

Fig. 4-5 Schematic illustrations of proposed laser-induced liquid-phase crystallization technique [2].

4.2.2 Fabrication Process

Figure 4-6 shows the fabrication process of single-crystalline GeSn array on a quartz substrate by laser-induced liquid-phase crystallization. A 250-nm-thick amorphous GeSn layer was deposited using a molecular beam deposition system and patterned into array (W/L = 5/30 μm with a spacing of about 5 μm) by CF_4-based reactive ion etching. The Sn content inside the amorphous GeSn layer was controlled to be around 2.5%. Then, after depositing a thick SiO_2 capping layer (1 μm) to prevent the agglomeration of GeSn, one-scan laser annealing with a continuous laser (λ: 532 nm, laser power: 9 W) developed at Hiroshima university was performed to induce the liquid-phase crystallization. The detail of experimental setup for laser annealing is described elsewhere [3,4]. The laser with an area of 1.1 mm × 50 μm was scanned along the amorphous GeSn array at the speed of 100 μm/s, which is the same speed to lateral liquid-phase growth based on RTA (Fig. 4-4).

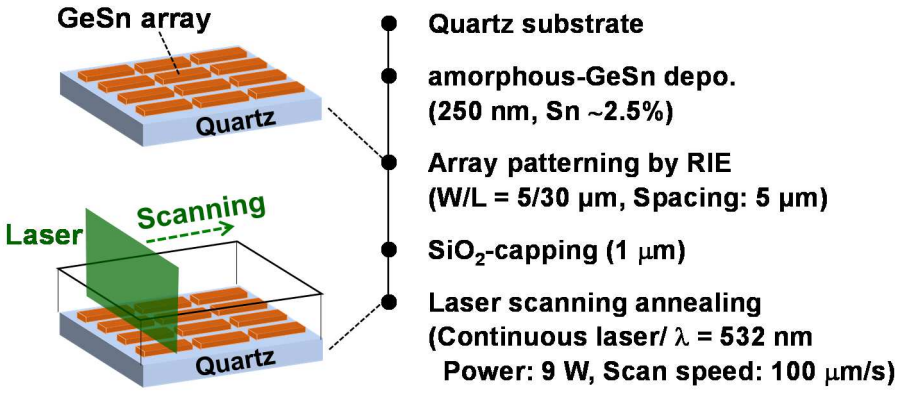

Fig. 4-6 Fabrication process of single-crystalline GeSn array on quartz substrate by laser scanning annealing.

4.2.3 Crystalline Quality and Sn content

Figure 4-7(a) shows the optical image of GeSn array after laser scanning annealing. The Sn precipitation (bright contrast region), sign of single-crystallization, was clearly observed in the entire GeSn array similar to the RTA case. Also, as shown in the EBSD image of GeSn array (Fig. 4-7(b)), highly (001)-oriented single-crystalline GeSn array was successfully grown on a quartz substrate, indicating the lateral growth can be induced by laser scanning annealing. The preferential (001) orientation would be determined by the

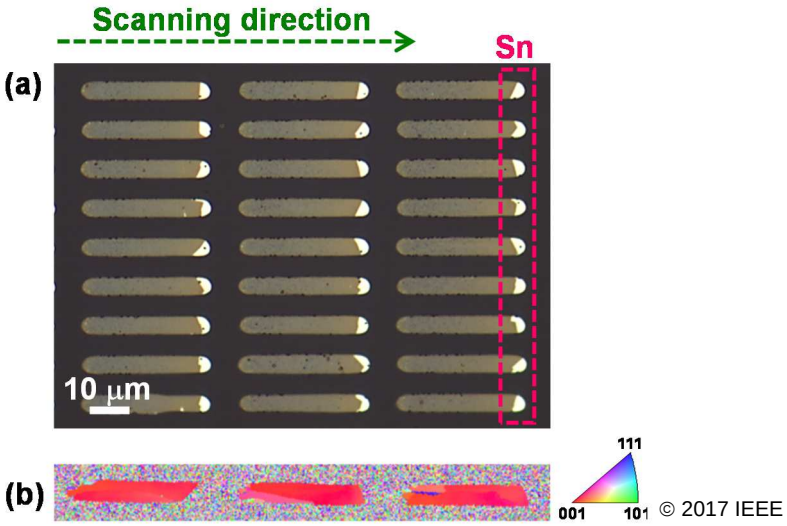

Fig. 4-7 (a) Optical and (b) EBSD images of GeSn array after laser scanning annealing [2].

interface energy between GeSn and quartz, and consistent with our previous result (Fig. 2-4).

Then we investigated the crystallinity of single-crystalline GeSn wire formed by laser scanning annealing through μ-Raman measurement. Figure 4-8 shows the Raman spectra obtained from single-crystalline GeSn wire formed by laser scanning anneal and RTA. The Raman peak of Ge-Ge vibration mode for GeSn wire formed by both methods shifted toward lower wave number with respect to bulk Ge wafer for same extent, which indicates the identical Sn content (~2%) and strain (~0.6%). Also, from the comparable full-width at half

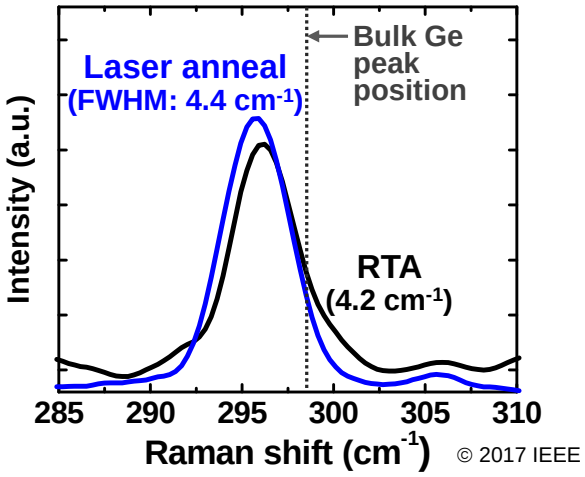

Fig. 4-8 Raman spectra obtained from single-crystalline GeSn wires formed by RTA (local melting) and laser scanning annealing [2].

maximum (FWHM) of Raman peak to that formed by RTA, it was found that the single-crystalline GeSn wire formed by laser scanning anneal has an excellent crystalline quality.

4.2.4 Laser Scanning Speed Dependence

We have also investigated the laser scanning speed dependence on the crystallinity and Sn content. Figure 4-9 shows the optical images of GeSn wire after laser anneal with different scanning speed (laser power: 9 W). The Sn precipitation was observed for all samples, indicating successful single-crystallization. Figure 4-10(a) shows the Raman spectra of GeSn wire with different laser scanning speed. The extracted FWHM from each Raman peak was summarized in Fig. 4-10(b). The FWHM slightly decreased with slow down the scanning speed, suggesting the better crystalline quality. As for the Sn content, it was found that the Raman shift remains constant with respect to laser scanning

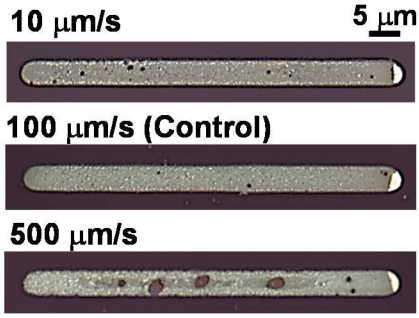

Fig. 4-9 optical images of GeSn wire after laser annealing with different scanning speed. Laser power was set to 9 W for all sample.

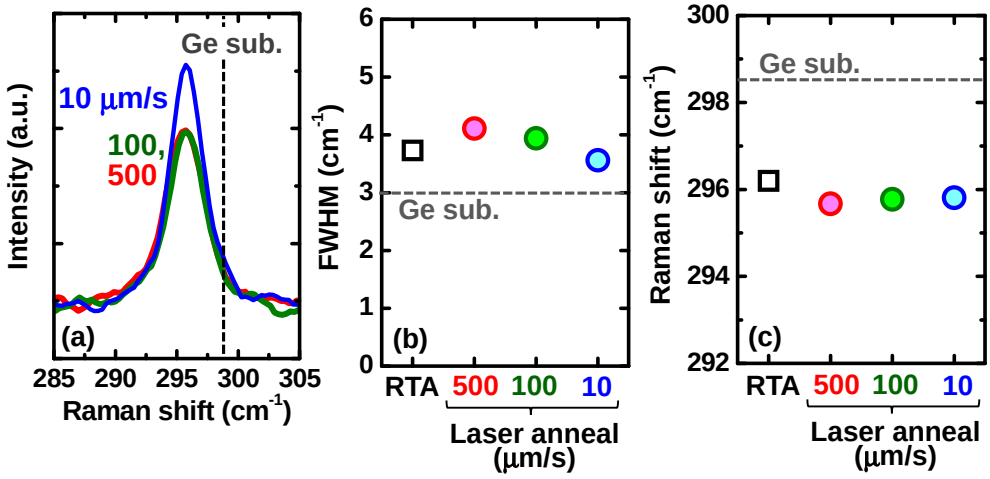

Fig. 4-10 (a) Raman spectra, (b) FWHM and (c) Raman shift obtained from GeSn wire formed by laser anneal with different scanning speed.

speed (Fig. 4-10(c)). This result indicate the Sn content was hardly changed by the scanning speed, and it is expected that the Sn content in liquid-phase grown GeSn is largely determined by segregation coefficient of Sn in Ge. However, further investigation is needed to control the Sn content.

4.2.5 Photoluminescence Study

In order to investigate the detection wavelength range of single-crystalline GeSn array, μ-PL measurement was performed. Figure 4-11 shows room temperature PL spectra for single-crystalline GeSn wires formed by laser scanning annealing. The red-shifted PL peak at a wavelength of around 1.75 μm with respect to the direct bandgap of Ge (1.55 μm) was observed, indicating a bandgap shrinkage due to Sn incorporation and tensile strain. Also, significantly enhanced PL intensity was observed compared to bulk Ge substrate. This would be due to the improved light emission efficiency by direct bandgap shrinkage. Also, by increasing the Sn content up to 5%, the peak wavelength reaches beyond 2 μm. This result indicates the detection wavelength range of GeSn photodiode can be designed by controlling the Sn content. In the following experiment, GeSn array with the Sn content of 2% was used.

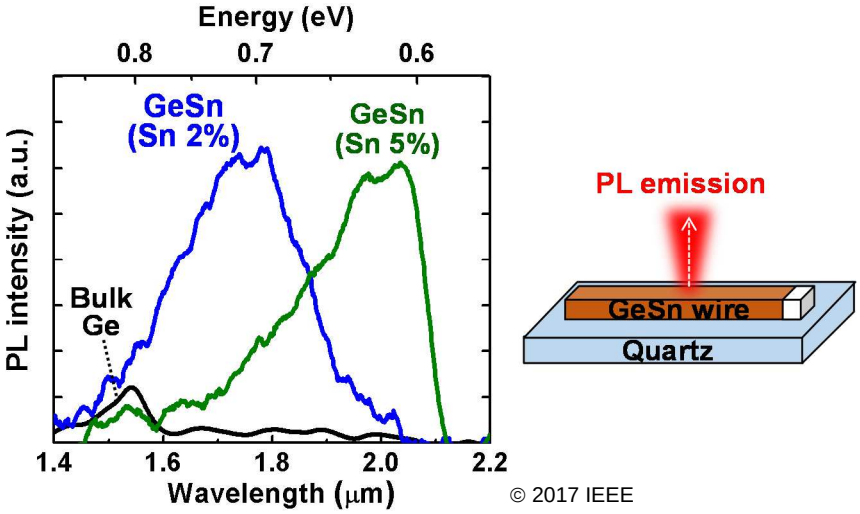

Fig. 4-11 PL spectra obtained from GeSn wire formed by laser scanning anneal with Sn content of 2% and 5% [2].

4.3 Single-Crystalline GeSn n^+/p Photodiode Array

By using the laser-induced liquid-phase crystallization, we have succeeded in fabricating single-crystalline GeSn array on a quartz substrate. Also, the PL

study revealed that the fabricated GeSn alloy has reduced bandgap with respect to Ge and thus extending cut-off wavelength is expected. Therefore, we then moved to GeSn NIR photodetector fabrication in combination with laser-induced liquid-phase crystallization with P^+-implantation.

4.3.1 Fabrication Process

Figure 4-12 shows the fabrication process of single-crystalline GeSn n^+/p photodiode array. A 250-nm-thick amorphous GeSn layer was deposited on a quartz substrate and patterned into array (W/L = 5/30 μm with a spacing of about 5 μm). Then, after depositing a thick SiO_2 capping layer (1 μm), one-scan laser annealing with a scanning speed of 100 μm/s was performed to induce the liquid-phase crystallization. After thinning the SiO_2-capping layer down to 50 nm, P^+ was implanted at a dose of 2×10^{15} cm^{-2} and an acceleration energy of 40 keV through a photoresist mask. P^+ implantation was performed at one side of each array, and the doping profile was well optimized by ion-trajectory simulation (shown in Fig. 3-17). After wet etching the SiO_2 implantation through mask, a 100-nm-thick field oxide was deposited and dopant activation anneal was performed at 500°C for 5 min to form n^+/p junction. Finally, Al contacts to p- and n^+-regions were formed.

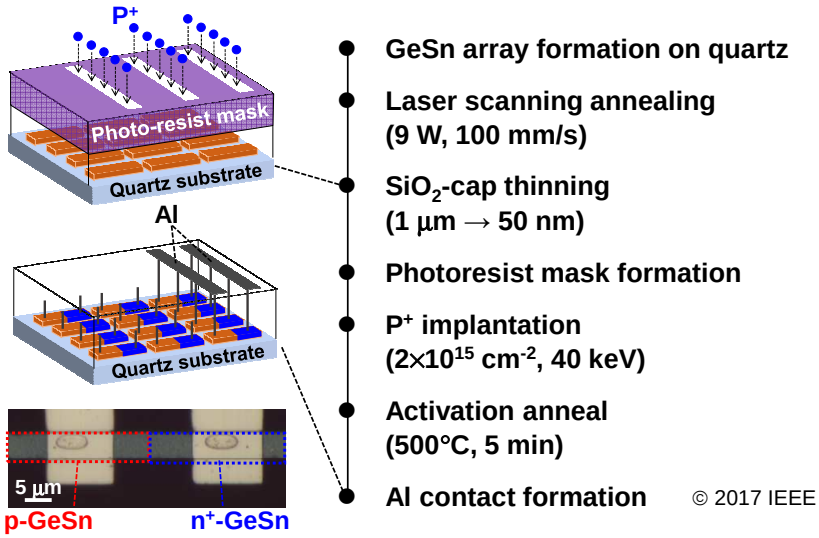

Fig. 4-12 Fabrication process of single-crystalline GeSn n^+/p diode array on quartz substrate [2].

4.3.2 Electrical Characterization

Figure 4-13(a) shows the temperature-dependent I-V characteristics of the fabricated single-crystalline GeSn n^+/p diode on a quartz substrate. For a comparison, that of poly-crystalline GeSn n^+/p diode formed by complete melting based on RTA was also shown in Fig. 4-12(b). In contrast to the poly-crystalline GeSn n^+/p diode, well-behaved rectifying characteristics with a low dark current of 10^{-1} A/cm^2 and an on/off ratio of 10^3 was obtained for the single-crystalline GeSn n^+/p diode formed by laser scanning annealing at R.T (290 K). This is sufficiently low dark current for practical application. Furthermore, the dark current was significantly reduced with decreasing measurement temperature and a low dark current of 10^{-3} A/cm^2 with an I_{on}/I_{off} ratio of over 10^5 was achieved at 120 K, which is a record-high performance and clearly indicates the potential of liquid-phase grown GeSn for NIR photodetector.

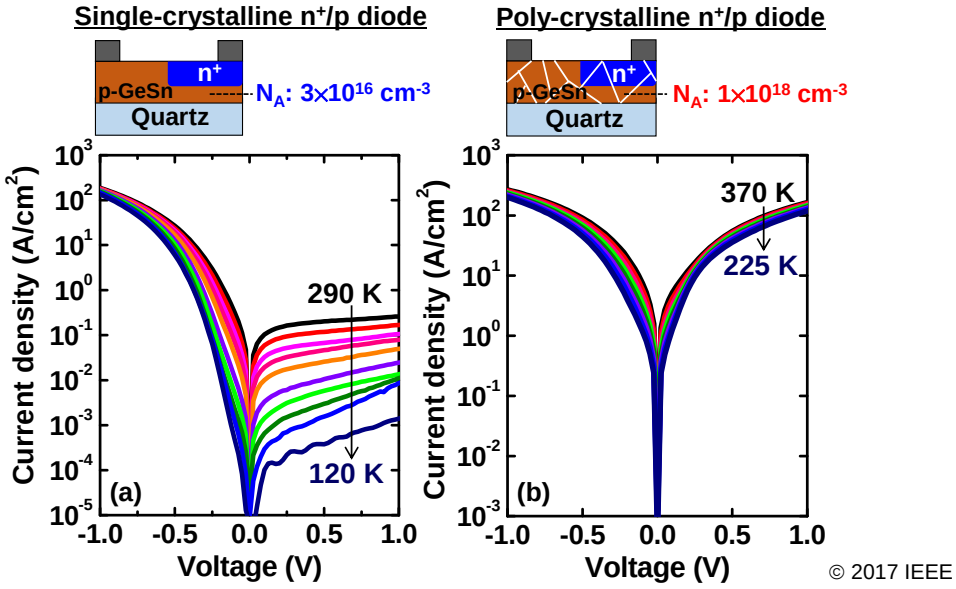

Fig. 4-13 Temperature dependence of I-V characteristics for (a) single- and (b) poly-crystalline GeSn n^+/p diodes on quartz substrate [2].

In order to provide a further insight into the diode characteristics such as leakage current, we investigated Arrhenius plot for GeSn n^+/p diode (Fig. 4-14). Since dark current is modeled by following equation, we can evaluate the activation energy from the plot [5].

$$I_{Dark} = BT^{\frac{3}{2}} e^{-\frac{E_A}{kT}} \left(e^{\frac{qV_a}{2kT}} - 1\right)$$

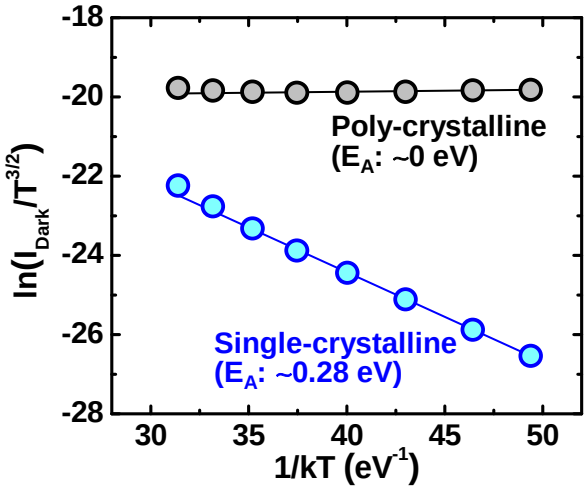

Fig. 4-14 Arrhenius plot of single- and poly-crystalline GeSn n^+/p diodes. Activation energy was extracted from slope of Arrhenius plot [2].

Here, B is a constant, T is the temperature, E_a is the activation energy, and V is the applied voltage. In the both single- and poly-crystalline GeSn n^+/p diodes, linear correlation between dark current and temperature was observed. For single-crystalline n^+/p diode, an activation energy is estimated to be 0.28 eV, which is about half of the bandgap of GeSn. On the other hand, that of poly-crystalline one is ~0 eV, indicating the leakage current was generated from shallow defect level or metallic conduction pass. From these results, we again confirm the excellent crystalline quality of the single-crystalline GeSn wire formed by laser-induced liquid-phase crystallization.

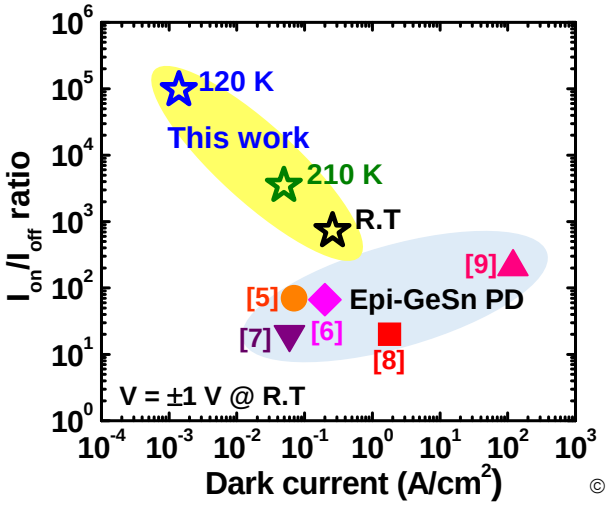

Fig. 4-15 Benchmark of I_{on}/I_{off} ratio as a function of dark current for single-crystalline GeSn n^+/p diode in comparison with previously reported eputaxially grown GeSn-based diodes on Si substrate [2].

Fig. 4-15 shows the benchmark of I_{on}/I_{off} ratio as a function of dark current in comparison with the previously reported GeSn-based p-i-n photodiodes. We have succeeded in obtaining a record-high I_{on}/I_{off} ratio together with a very low dark current, which is a great advantage in NIR photodetection.

4.4 Evaluation of NIR Optical Response of GeSn n^+/p Photodiode

As described in previous session, we have succeeded in fabricating a high-quality single-crystalline GeSn array on a quartz substrate by laser-induced liquid-phase crystallization. By combining P ion implantation, high-performance GeSn n^+/p diode with a record-low dark current and high I_{on}/I_{off} ratio was demonstrated. In this session, we evaluated the NIR optical response of fabricated GeSn n^+/p photodiode, and examined the first demonstration of back-illuminated GeSn-based image sensor on a quartz substrate.

4.4.1 Front-Side Illuminated Photodetection

For the evaluation of optical response of each GeSn diode array with narrow wire width (W/L = 5/30 μm), we developed a focused NIR laser irradiation system equipped with visible and NIR (1550 nm and 2000 nm) light source as shown in Fig. 4-16. The incident laser was optically coupled to the objective lense (10×, 20×, 50×), and the photocurrent was analyzed by semiconductor

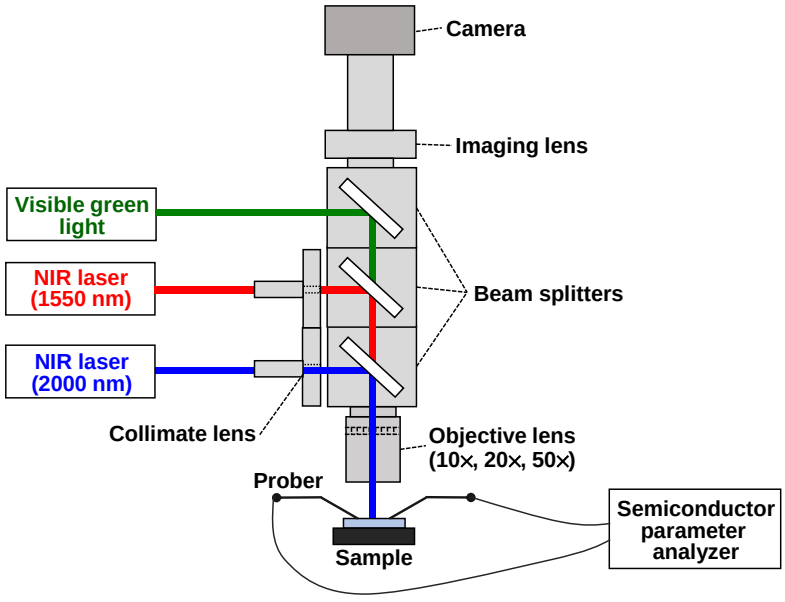

Fig. 4-16 Experimental setup for photoresponse measurement.

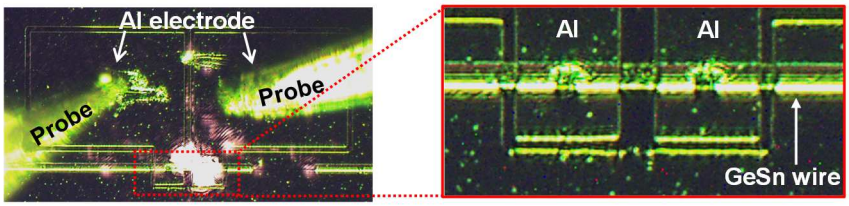

Fig. 4-17 Captured image of GeSn photodiode during optical response measurement under visible laser irradiation.

parameter analyzer. The captured image of GeSn diode during visible laser irradiation is shown in Fig. 4-17.

The photocurrent of single-crystalline GeSn n^+/p photodiode under NIR illumination is shown in Fig. 4-18(a). The light was illuminated normal to the n^+/p diode array from front-side. The optical response to NIR illumination was clearly observed. For the image sensor application, performance variation in the photodiode array is a critical issue. Thus, we also evaluated the variation in diode characteristics in the fabricated GeSn photodiode array (N = 9). As shown in Fig. 4-18(b), it was found that the variation in the both dark current and photocurrent are within one order of magnitude. This performance variation would be acceptable but further improvement is required for the practical image sensor application, which can be achieved by optimizing laser annealing conditions.

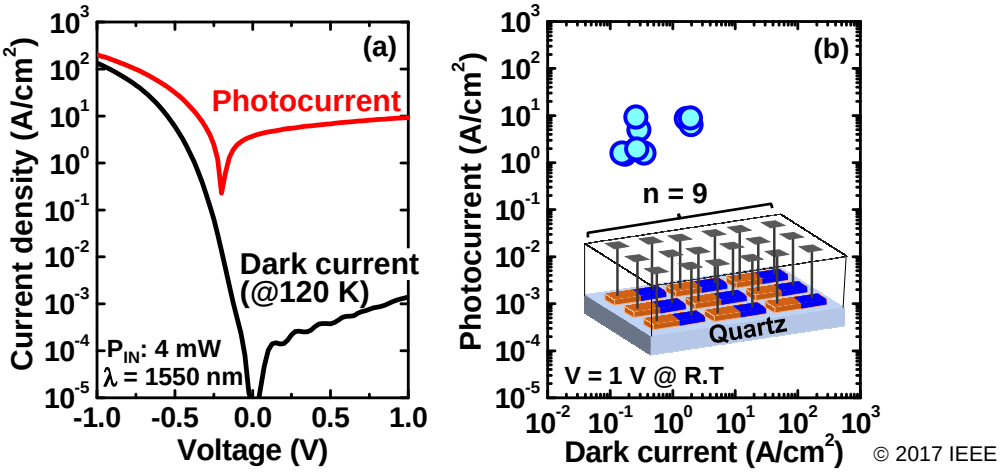

Fig. 4-18 (a) optical response of front-side illuminated GeSn n^+/p photodiode (λ = 1550 nm). (b) Performance variation of GeSn n^+/p photodiodes (n=9) [2].

4.4.2 Back-Side Illuminated Photodetection

As mentioned before, since a quartz has a high transparency to NIR light

(over 90%), highly-efficient back-side illuminated NIR photodetection would be achieved by GeSn photodiode array fabricated on a quartz substrate. In this session, we evaluated the NIR optical response of GeSn n^+/p photodiode on a quartz substrate under back-side illumination.

For the back-illuminated experiment, the sample was turned upside down and bonded to the stage for the photocurrent measurement. The photocurrent under back-side illumination with a wavelength of 1550 nm was shown in Fig. 4-19. It was found that the photocurrent under back-side illumination is one order of magnitude higher than that under front-side illumination, and the photocurrent reached almost comparable to the forward current. There are several possible reasons for this increasing photocurrent. First, under the front-side illumination, a part of laser was blocked by Al electrodes and effective input laser power would be reduced compared to the back-side illumination. Second, in the case of back-side illumination, some stray light is induced depending on the sample structure such as reflection or scattering of the input laser at Al electrodes, which would attributed to generating the photocurrent. Also, as shown in Fig. 4-20, the photocurrent depends on the input laser power, which is a clear evidence of normal operation of photodiodes.

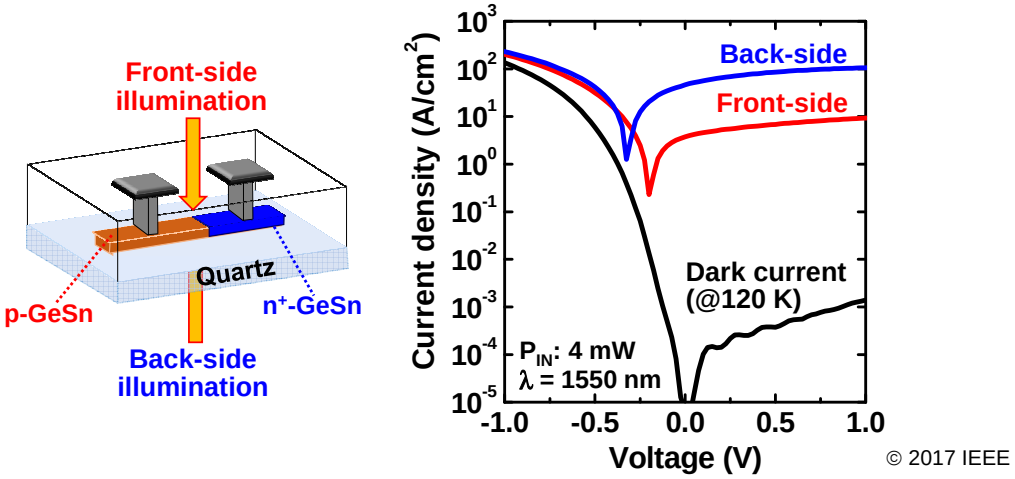

Fig. 4-19 optical response of back-illuminated GeSn n^+/p photodiode (λ = 1550 nm). Enhanced photocurrent was observed [2].

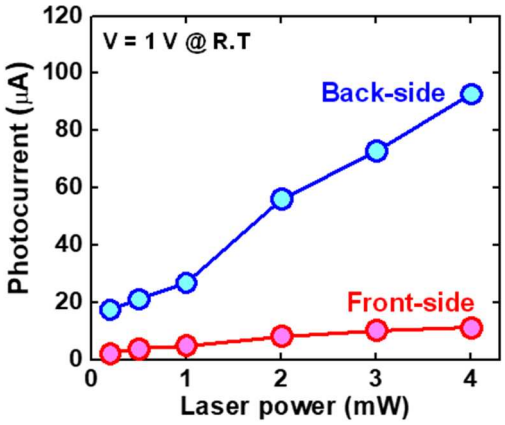

Fig. 4-20 Input laser power dependence on photocurrent of GeSn n^+/p diode under front- and back-side illumination.

4.4.3 Extraction of Optical Responsivity

Then we evaluated the performance of fabricated GeSn photodiode by extracting the optical responsivity, which is an input to output gain and expressed by following simple equation:

$$R = I/P$$

Here, R is the responsivity, I is the generated photocurrent, and P is the input laser power. From the laser power dependent I-V characteristics (Fig. 4-21(a)), optical responsivity at 1550 nm was extracted as shown in Fig. 4-21(b). A high responsivity of 1.3 A/W was obtained.

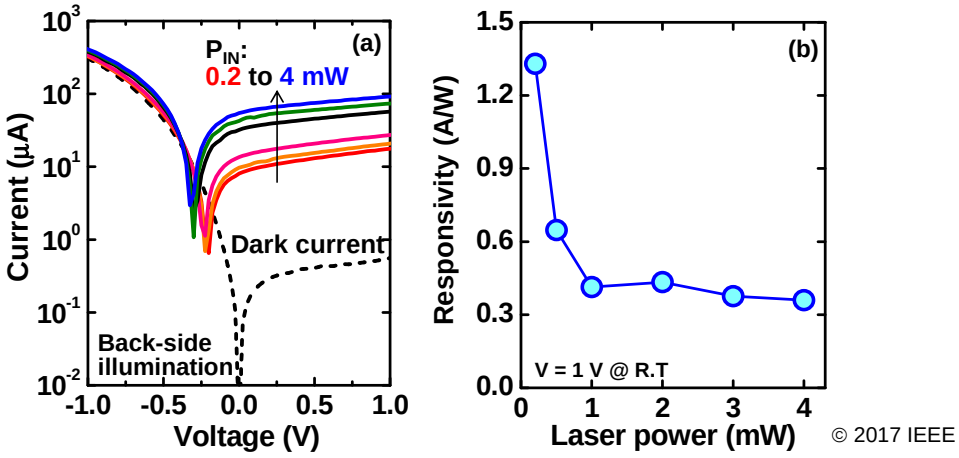

Fig. 4-21 (a) Input laser power dependent I-V characteristics and (b) extracted responsivity of GeSn n^+/p photodiode measured under back-side illumination of 1550-nm-wavelength laser [2].

From the following equation, quantum efficiency (incident photon to converted photogenerated carrier ratio) was also calculated and found to be around 100%.

$$QE = R \times 1240/\lambda$$

Although there is a possibility of slight overestimation of the input laser power due to reflected or scattered stray light at the Al electrodes, these results clearly indicated the advantage of fabricated tensile-straiend GeSn photodiode.

Figure 4-22 shows the benchmark of responsivity at the wavelength of 1550 nm in comparison with the previously reported GeSn-based photodiodes fabricated on Si substrate. In this work, a record-high responsivity of 1.3 A/W was achieved, which would be due to the enhanced absorption efficiency and an excellent crystalline quality compared to the epitaxially-grown GeSn layers.

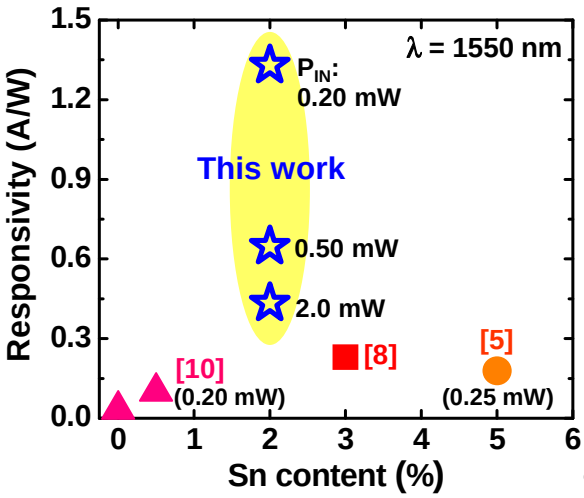

Fig. 4-22 Benchmark of responsivity at a wavelength of 1550 nm for GeSn-based n^+/p photodiodes [2].

4.4.4 Optical Response in 2 μm Wavelength Range

We further investigated the optical response in the 2 μm wavelength range. In order to investigate the effect of Sn alloying and tensile strain on cut-off wavelength, Ge control n+/p diode was also fabricated on a commercially available unstrained GeOI wafer. Figure 4-23(a) shows the time-dependent photocurrent under periodic 2000-nm-wavelength laser illumination for GeSn n^+/p diode together with control bulk Ge n^+/p diode. Significantly enhanced photocurrent and clear optical response were observed for GeSn diode. Also, as shown in Fig. 4-23(b), the photocurrent for GeSn diode linearly increases with

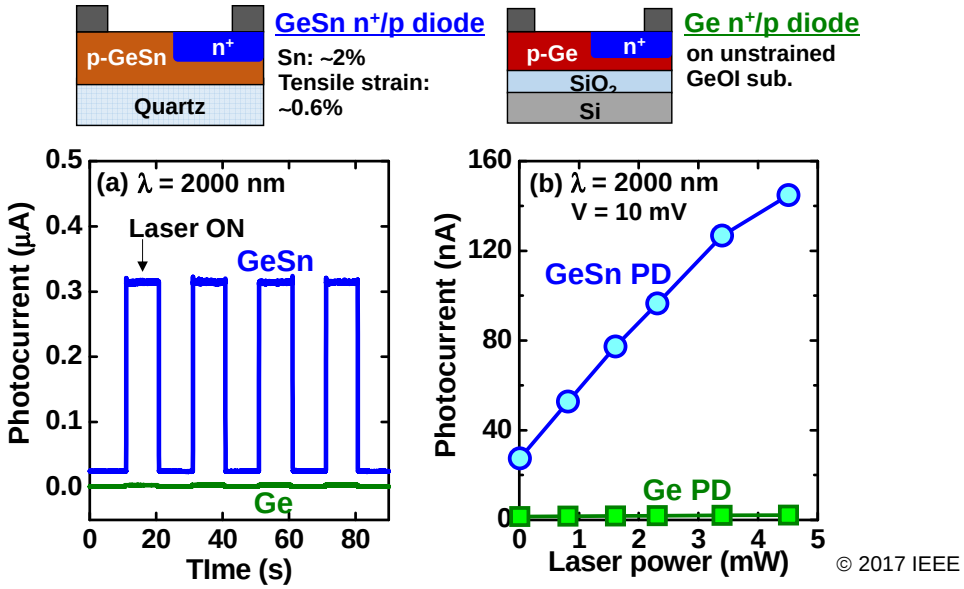

Fig. 4-23 (a) Time-dependent optical response under periodic 2000-nm-laser irradiation. (b) Laser power dependence on photocurrent for GeSn and Ge n+/p photodiode [2].

increasing the input laser power, despite a negligible response for the Ge diode. These results clearly indicate the cut-off wavelength of GeSn diode is extended to beyond 2 μm owing to Sn alloying and tensile strain. Further enhancement in photoresponse would be achieved by increasing the Sn content up to 5% (Fig. 4-11).

This is the first demonstration of single-crystalline GeSn photodiode array integrated on a transparent substrate which covers a wavelength beyond 2 μm, and the laser-induced liquid-phase crystallization will enable back-side illuminated NIR image sensor on a quartz substrate.

4.5 Summary

In order to enable fully-integrated GeSn-based NIR imager chip, a novel liquid-phase crystallization method was developed. By utilizing the laser scanning annealing, a large-area single-crystalline GeSn array was successfully formed on a quartz substrate with high-integrity and low thermal budget. GeSn-based n^+/p photodiode array was also fabricated by performing P^+ implantation and NIR optical response were studied in detail. Thanks to the high transparency of quartz substrate to NIR light, GeSn photodiode on quartz substrate can be operated under back-side NIR illumination, and it exhibited a

record-high responsivity owing to a very low dark current.

As described in chapter 3 and chapter 4, we have succeeded in fabricating a high-mobility CMOS and high-performance NIR photodiode integrated on a quartz substrate based on a liquid-phase grown GeSn layer. This technology provides an ideal platform for group-IV-based monolithically-integrated NIR imager chip.

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Chapter 5 Conclusions

The aim of this study is to provide an advanced monolithically-integrated group-IV-based optoelectronic platform that is expected as a promising post-scaling technology. For this purpose, we developed a novel crystal growth method of GeSn layer on insulators based on liquid-phase crystallization, and demonstrated GeSn-based high-mobility CMOS and photonic devices integrated on a quartz substrate. The main achievements of this study are summarized below:

Due to the lack of suitable crystal growth method of GeSn layer, fabrication of high-quality GeSn layer is strongly desired for the monolithic optoelectronic integration. In the chapter 1, we proposed a novel method of forming a high-quality single-crystalline GeSn wire on a quartz substrate based on the lateral liquid-phase crystallization. By controlling a nucleation by local melting process, lateral growth propagated along the GeSn wire without using any crystal template such as Si substrate, and a defect-free single-crystalline GeSn wire was successfully grown on a quartz substrate. Due to the large difference in thermal expansion coefficient between GeSn and quartz, tensile strain as high as 0.6% was induced in the liquid-phase grown GeSn, which promotes the bandgap modulation of GeSn and is great advantage for optoelectronic applications. Since the undoped GeSn wire is p-type due to the acceptor-like point defects in GeSn, n-type GeSn layer was fabricated by liquid-phase growth of Sb-doped GeSn wire. It was found that the Sb incorporation hardly affect the liquid-phase growth of GeSn, and the Sb-doped GeSn wire has an excellent crystalline quality comparable to the p-type GeSn layer. From the Hall effect measurement, carrier concentration for both p- and n-type single-crystalline GeSn wires were found to be lower than 10^{17} cm^{-3}, indicating an excellent crystalline quality and having a great advantage in electronic and photonic device fabrication.. The presented work in this chapter, single-crystalline undoped p-GeSn and Sb-doped n-GeSn wires, will provide an ideal platform for GeSn-based optoelectronic integration.

In the chapter 2, we demonstrated both p- and n-channel GeSn thin-film transistors based on undoped p-type and Sb-doped n-type liquid-phase grown GeSn wires, respectively. A successful p- and n-channel transistor operation was

obtained for fabricated accumulation-mode TFT. Although a record-high hole mobility of 423 cm^2/Vs was achieved for the undoped p-FET, it was found that the electron mobility in Sb-doped n-FET is severely limited by high parasitic resistance at S/D region due to the FLP effect. To improve the n-channel transistor performance, we examined heavy n-type doping by P ion implantation. An inversion-mode GeSn n-channel TFT with an n^+/p junction was fabricated, and a well rectifying behavior with on/off ratio of 10^3 and a record-high electron mobility of 271 cm^2/Vs was obtained, which clearly indicates the reduced contact resistance by heavy n-type doping. This is the first demonstration of GeSn-based p- and n-channel TFTs fabricated on a transparent substrate that outperforms previously reported Ge or Si-based TFT.

Finally, in order to enable GeSn-based optoelectronic integrated device, high-performance GeSn photodiode was demonstrated. In this chapter, we further developed the liquid-phase crystallization method to provide single-crystalline GeSn array for NIR imager chip. By utilizing the laser scanning annealing, a large-area single-crystalline GeSn array was successfully formed on a quartz substrate with high-integrity and low thermal budget. By performing P ion implantation, single-crystalline GeSn n^+/p photodiode array was fabricated on a quartz substrate. From the optical characterization, liquid-phase grown GeSn array has extending cut-off wavelength beyond 2 μm, and thanks to the high transparency of quartz substrate to NIR light, significantly enhanced optical response was observed under back-side NIR illumination. The extracted optical responsivity at 1550 nm was 1.3 A/W, which is record high responsivity reported so far. The present GeSn-based photodiode is quite integration friendly and three-dimensional stackable, and thus enabling NIR imager chip integrated with high-mobility GeSn CMOS circuit.

In summary, we developed an advanced single-crystalline GeSn platform based on the novel nucleation-controlled liquid-phase crystallization. High-quality p- and n-type single-crystalline GeSn layers were formed on quartz substrate, and GeSn p- and n-channel TFTs with record-high mobility was demonstrated for the first time. Moreover, by utilizing laser scanning annealing, large-area single-crystalline GeSn array was grown on a quartz substrate, and

GeSn photodiode that is competing with direct bandgap III-V-based devices are demonstrated. The fabricated GeSn-based CMOS and photonic device can be easily integrated on a single-chip, which is a promising optoelectronic platform. The present GeSn-based technology opens a way for fully-integrated group-IV-based optoelectronic integration in the post-scaling era.

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Hiroshi Oka

Publication List and Awards

Journal Publications Related to This Thesis Work

[1] **H. Oka**, T. Amamoto, M. Koyama, Y. Imai, S. Kimura, T. Hosoi, T. Shimura, and H. Watanabe, "Fabrication of tensile-strained single-crystalline GeSn on transparent substrate by nucleation-controlled liquid-phase crystallization", Appl. Phys. Lett., vol.110, pp. 032104-1~5 (2017).

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[1] **H. Oka**, Y. Minoura, T. Hosoi, T. Shimura, and H. Watanabe, "Understanding and engineering of NiGe/Ge junction formed by phosphorous ion implantation after germanidation", Appl. Phys. Lett., vol.105, pp.062107-1~4 (2014).

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