論 文 内 容 の 要 旨

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論文題名	An MTTF-aware Design and Post-Silicon Validation Methodology for Adaptive Voltage Scaling (適応的電圧制御に向けたMTTF考慮設計と製造後テスト手法)

論文内容の要旨

Aggressive device miniaturization due to VLSI technology scaling has been improving the average device performance. Circuits, meanwhile, have become sensitive to static manufacturing variability and dynamic environmental fluctuation. These static and dynamic variations directly lead to circuit reliability degradation. To overcome variability mentioned above, a traditional worst-case (WC) design gives design and operational margins to ensure correct circuit operation in design time and in field, respectively. However, as the performance variation becomes significant, such margins tend to be too painful for designers. Therefore, the conventional WC design with guard-banding is becoming less efficient.

The most effective tuning knob for post-silicon performance compensation is supply voltage control, and then adaptive voltage scaling (AVS) is intensively studied. AVS is expected to minimize process, voltage, temperature, and aging (PVTA) margin of each chip and allocate only a small margin taking into account the entire lifetime. The conventional PVTA margins, which are determined by the worst chip across all the variation sources, are excessive in most of the chips, and they can be exploited as the source of power reduction.

To put the AVS circuit into practical use, a designer needs (1) design methodology, (2) performance evaluation in design time, and (3) post-silicon validation methodology. In the AVS circuit, the sensors, which estimate the timing slack of the main logic and detect/predict the timing errors, are embedded, and the supply voltage is adjusted referring to the sensor output. Note that timing errors can occur even with this AVS due to, for example, insufficient sensor insertion. Therefore, to design the reliable AVS, the design parameters such as sensor type and insertion place should be determined carefully, and then the circuit performance needs to be validated in terms of power and lifetime. After the design parameters are fixed and the circuit performance is estimated, the design needs to be validated. Note that even in the well-designed AVS circuit, some fast-transient delay fluctuation such as supply noise may induce timing errors. Hence, in the post-silicon validation, each chip needs to be verified in terms of whether the AVS can appropriately work in field under various operation conditions. In the post-silicon validation, once an unexpected system behavior is observed, the circuit operation is analyzed. In this analysis, the most challenging tasks is error localization since the time interval between the error occurrence and the detection of such an abnormal behavior is quite long. Due to such a long error detection latency, it is difficult to know when and where the timing error occurred. Consequently, to facilitate the error localization, the post-silicon validation methodology which can quickly detect the timing error is essential. Here, as a performance evaluation framework, a stochastic error rate estimation method, which quickly estimates a mean time to failure (MTTF) and average power dissipation, was proposed. However, neither the design methodology which enhances the AVS performance under an MTTF constraint nor the post-silicon validation method which facilitates the timing error localization in AVS operation are not fully studied yet.

This thesis studies the design and post-silicon validation of AVS and proposes a design and post-silicon validation methodology for the AVS circuit. The proposed design methodology consists of three steps: (1) select the type of sensor, (2) optimize the main logic under AVS, and (3) insert sensors into the optimized main logic. In the first step of the sensor selection, this thesis discusses supply voltage reductions achieved by AVS circuits with different sensors, i.e., timing error predictive FF and critical path replica. In this work, we give the MTTF as a design constraint and compare the trade-offs of clock period and average supply voltage between AVS circuits with these two sensors.

In the second step of the main logic design, this thesis introduces the MTTF as a design constraint and optimizes the design with an activation-aware slack assignment (ASA). The MTTF constraint helps explore a set of necessary operating conditions, such as clock period and supply voltage, and reduces the operation margin from the WC design while keeping the target MTTF. This margin reduction directly leads to the supply voltage reduction. ASA, meanwhile, gives timing slacks to non-intrinsic active critical paths by ECO, where non-intrinsic critical paths are timing paths whose slacks were originally large but are reduced by downsizing and replacement to high-Vth cells for power savings. Thus, ASA reduces the number of active critical paths whose delays are very close to those of the intrinsic critical paths, i.e., timing paths whose slacks cannot be reduced by re-synthesis, replacement to low-Vth cells, and sizing. In this case, we can expect that circuits with ASA have fewer paths where timing errors are likely to occur, which can reduce the number of monitoring paths with AVS and thus can contribute to facilitating the following sensor insertion. Also, the reduction of active critical paths helps to extend the MTTF and thus reduce the supply voltage. Therefore, ASA can further improve performance from the simple MTTF-aware operation of conventionally designed main logic.

In the third step of the sensor insertion, this thesis aims at maximizing the MTTF to reduce the power dissipation, which is based on a hypothesis that a circuit with the longer MTTF has a larger room for power saving. To maximize the MTTF, the supply voltage should be adjusted frequently and thus timing critical paths should be monitored frequently. Based on this consideration, this thesis proposes a novel insertion method that maximumly decreases the sum of gate-wise timing failure probabilities. Note that the timing failure probability of a flip-flop (FF) is the joint probability of activation and timing violation probabilities of the FF, and the gate-wise failure probability is calculated from timing failure probabilities of endpoint FFs. By exploiting the information on the paths with the higher timing failure probability, the proposed sensor insertion makes AVS efficiently monitor the timing-critical and highly-active FFs.
Moreover, by maximizing the sum of gate-wise failure probabilities, the proposed sensor insertion can cover the larger set of instances that can contribute to causing timing errors.

With the proposed design methodology consisting of these three steps, 38.0% power reduction is achieved while satisfying the target MTTF. This work also experimentally confirmed that simultaneous optimization of sensors and main logic synergistically enhances the performance and reliability of AVS. For example, the proposed sensor selection and insertion methodology achieved the target MTTF whereas straightforward slack-oriented sensor insertion did not satisfy the target MTTF at all. Moreover, the proposed main logic optimization is highly compatible with the sensor optimization and further improves the AVS performance, e.g, the proposed ASA further saves power by 10.6% from the AVS circuit without main logic optimization.
As for the post-silicon validation methodology, this thesis devises the error detection mechanisms for short latency (EDM-L) and evaluates the performance of EDM-L for timing error localization with a noise-aware logic simulator and 65-nm test chips assuming the following two EDM-L usage scenarios:
(1) localizing a timing error that occurred in the original program and
(2) localizing as many potential timing errors as possible. Simulation results show that the EDM-L cannot locate supply noise induced timing errors in the original program in the first scenario, but it detected 86% of non-masked errors in the second scenario, which mean the EDM-L performance of detecting supply noise induced timing errors affecting execution results is high.
Hardware measurement results show that the EDM-L detects 25% of original timing errors and 56% of non-masked errors. These measurement results were not consistent with the simulation results. We found that this inconsistency came from (1) the design of the power distribution network, and (2) the definition of FMAX used for evaluation. By updating the simulation setup, the EDM-L performance evaluated by the simulation was consistent with that by the chip measurement. The devised EDM-L helps to localize the supply noise induced timing errors in post-silicon validation and thus contributes to improving reliability of the AVS circuit.

The design and post-silicon validation methodology established in this thesis helps to construct the reliable AVS, which overcomes the PVTA variation and thus dramatically improves the performance of VLSI circuit. The proposed design methodology enables designers to provide the MTTF aware design flow which is essential for the reliable VLSI design. The post-silicon validation methodology provided by this thesis helps to localize the timing error with short latency. This quick error localization substantially reduces the debugging costs in the post-silicon validation and therefore mitigates the design time-to-market, which is the one of the most serious constraints in the VLSI design.

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論文審査の結果の要旨及び担当者

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論文審査の結果の要旨

本論文は、適応的電圧制御（adaptive voltage scaling; AVS）の設計手法と製造後テスト手法に関する研究の成果をまとめたものであり、以下の主要な結果を得ている。

1. AVS の MTTF 考慮設計手法の提案

AVS は、各チップが動作時に自身の速度余裕を見積もり、電源電圧を自律的に調整する設計技術である。AVS を搭載した回路は、理想的には、最小の電圧マージンを保って動作するため、目標の寿命を満足しつつ消費電力を最小化できると期待される。AVS の実装として、被制御回路にセンサを搭載し、センサの出力に基づき電源電圧を制御する手法が有望視されている。この実装を用いるためには、センサとその挿入個所の選定手法および被制御対象回路の最適化手法が不可欠である。本論文では、AVS の実用化を目指して、平均故障発生時間（mean time to failure; MTTF）を制約条件とする設計手法を提案した。提案設計は、1）MTTF 制約下の電源電圧削減効果に基づくセンサの選定、2）活性化率考慮スラック割当（activation-aware slack assignment; ASA）による被制御回路の最適化、3）故障率を考慮したセンサ挿入、から構成される。提案設計全体の効果を評価したところ、年単位の MTTF の制約下において、38.0% の省電力効果を達成した。また、ASA により、省電力効果が10.6%高まることを確認した。

2. AVS 回路の製造後テスト容易化に向けた EDM-L の提案と電源ノイズ起因遅延故障への有効性評価

AVS では、動作時に急峻な電源ノイズが発生すると、電源電圧調整が間に合わず遅延故障を起こす可能性がある。AVS 回路の信頼性を高めるためには、製造後に様々な環境で動作検証（製造後テスト）を行い、故障が発生した場合にはデバッグする必要がある。従来の製造後テストでは、故障発生後、その検出までに長い時間を要し、デバッグが困難であるという課題があった。本論文では、製造後テストで実行するテストパターンに対して、故障の高速検出能力を付与する EDM-L（error detection mechanisms for short latency）を提案し、EDM-L の電源ノイズ起因遅延故障への有効性を実機とシミュレーションの両面から評価した。実行結果に影響を与えた電源ノイズ起因遅延故障に対して、EDM-L は実機評価で 86%、シミュレーション評価で 56% が早期検出できることを確認した。

以上のように、AVS の設計手法に関する研究では、センサと被制御回路の一体最適設計により、目標寿命を満足しつつ AVS 回路の性能を相乗的に高めることに成功している。また、製造後テスト手法の研究は、EDM-L が AVS の信頼性向上に不可欠な電源ノイズ起因遅延故障のデバッグ容易化に貢献できる点で有用である。これにより、高性能かつ高信頼な AVS の実現に貢献するものと期待できる。従って、博士（情報科学）の学位論文として価値のあるものと認める。