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論 文 内 容 の 要 旨

氏 名 (廖 望)	
論文題名	Evaluation on Muon and Neutron-induced Single Event Upsets in Planar CMOS SRAMs （プレーナ CMOS SRAMにおけるミュオン及び中性子が起因シングルイベントアップセットの評価）

論文内容の要旨

This thesis discusses muon- and neutron-induced SEUs (Single Event Upsets) in planar CMOS SRAM. SEU is often called as soft errors, which means the upsets in memory components of electronic devices induced by radiation effect. As we are stepping into the Information Society, the electronic devices are becoming more relevant to safety. For example, in the field of the autonomous driving, the level of automation at present is defined as partial driving automation, which means the electronic systems only assist the drivers, e.g. adaptive cruise control. However, in the next level, the systems will take over the control of driving at the daily life. At that level, once a system failure occurs, an accident is more likely to occur.

Random hazard is one of three main sources for such failure in the electronic systems t the level of hardware. Among the random hazard, soft error is the representative one. Due to the high density, narrow margin and no timing or logical masking, SRAM (Static Random Access Memory) is thought to be the main concern of SEUs in semiconductor devices. SEUs are unpredictable, and some of them are even uncorrectable and undetectable depending on the patterns of errors. Therefore, the evaluation on SER (Soft Error Rate) is important for device reliability.

Previous research devoting to the terrestrial SER have developed the evaluation methods of simulation, real-time test and irradiation test. However, to the author’s best knowledge, two issues for terrestrial SER evaluation are highly desirable to solve. The first issue is to quantify the contribution of SRAM to the neutron-induced chip-level SER at the low voltage. The neutron has been thought to be the main source for terrestrial cosmic ray-induced SEEs (Single Event Effects). This SEE does not only influence on SRAM, but also influences on FFs (Flip-Flops) and other combinational logic components in the chip. Compared to the measurement of SEUs in SRAMs, the effect of SET (Single Event Transient) is hard to be observed due to the complexity of its propagation. Therefore, lots of work were devoted to analyze the precise SER of SET in association with clock frequency to calculate the chip-level SER. However, despite the clock frequency, operating voltage also influences the SER in each component. More and more devices will be put to near-threshold computing, but the low voltage operation increases SERs. Therefore, it is highly demanded to evaluate on chip-level SER at the low operating voltage with experimental data, which are the most precise and reliable ones compared to other methods.

The second issue is the characteristics of muon-induced, especially negative muoninduced SEUs. As technology scaling down, the critical charge Qc, which is the threshold to induce SEUs, is becoming lower. According to a prediction work with simulation, once the Qc decreased to 0.34 fC and below in their calculation model, the SER induced by muons will exceed that of neutrons. Consequently, the terrestrial SER will be largely underestimated since the neutrons are mainly considered for terrestrial cosmic rays inducing soft error in current framework of evaluation. However, for the muon-induced SEUs, a lack of experimental knowledge about negative muon-induced SEUs is perceived. The most recent irradiation test using negative muon source was 1987, at which the Qc of the devices is much larger than those of modern devices. Therefore, an experimental work on characterization of muon-induced, especially negative muon-induced soft error, is highly desirable.

For the first issue, this thesis analyzes the chip-level SER for high-performance and embedded processors of 65-nm planar bulk and SOTB (Silicon On Thin Box) devices
at nominal and low operating voltage. As an alternative way to evaluate precise SET in combinational logic, a test chip including a circuit for worst-case evaluation is utilized
for irradiation test of neutron source. SBU (Single Bit Upset) and MCU (Multiple Cells Upset) rates are obtained from the previous work. To make the SER analysis closer to
the practical use, MBU (Multiple Bits Upset) rates with and without ECC are derived from the analysis of MCU patterns. Combing with SEU in FF reported before, the chiplevel SERs are calculated. In all conditions without ECC (Error Correction Code), SBUs and MCUs in SRAM contribute to more than 95 % of chip-level SER at the evaluated 65-nm technology node. With ECC, the FF contributes from 65 % to 95 % to the chiplevel SER, and it has dominance at the chip level. The result shows a high priority for ECC

applied to SRAMs at low and nominal voltage operation and also suggests FF as the second priority.
For the second issue, this thesis characterizes the negative muon-induced SEUs in 65-nm planar bulk SRAMs via irradiation test using monoenergetic muon beams. Highproportion and large-scale muon-induced MCUs are observed during the test. The voltage dependence of muon-induced SEUs suggests a high possibility of existence of PBA (Parasitic Bipolar Action) induced by muon capture process. For a further analysis, particle transport simulation is conducted to obtain the threshold of deposited charge for PBA. The threshold explained direct ionization is not sufficient to induce PBA for both negative and positive muons, while the charge deposited by moun capture is possible to induce PBA.
As a further investigation on muon-induced SEUs, the MCUs, which have possibility to spoil the ECC, are compared between muons and neutrons. Spallation and quasi-monoenergetic neutron sources are utilized for the comparison with monoenergetic muon source. The results show a strong similarity between negative muon- and neutron-induced MCUs, including the voltage dependence and spatial patterns. This suggests the ECC effective to neutron-induced MCUs will also work for muon-induced ones. A further investigation of particle transport simulation shows that the similarity originates from the LET (Linear Energy Transfer) of the ions generated in neutroninduced nuclear reaction and muon capture reaction.
As a more comprehensive analysis by the author and his colleagues, the muoninduced SER in 65-nm is still negligible in the open air. But, it is of interest to know whether the muon-induced SER would exceed neutron-induced one at more advanced technology node. This thesis conducted an irradiation test on 28-nm bulk SRAM at the same muon facility. The results suggests an increase in SER compared to the 65-nm technology. While some works reveal the neutron-induced SER per bit is decreasing in more scaled technology, muon shows a higher potential to be a dominant cause of system failure.

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論文審査の結果の要旨及び担当者

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論文審査の結果の要旨

本論文は、SRAMにおける中性子及びミュオン起因ソフトエラーの評価に関する成果をまとめたものであり、以下の主要な結果を得ている。

1. 実測結果に基づくチップレベルの中性子起因エラーレート評価

SRAMやフリップフロップといった基本記憶素子に対するソフトエラー率の評価は多数行われている一方で、チップレベルエラーレートに対するSRAMやフリップフロップ、組み合わせ回路の寄与度に関する評価は少ない。SRAMで発生したエラーが多数を占めていると言われているが、その定量的な評価は不十分であり、特に低電圧動作時の寄与は不明である。本論文では、照射実験のデータに基づき、65nm bulkデバイス及び65nm SOTBデバイスで設計されたプロセッサのチップレベルソフトエラーレートを評価した。本評価のため、組み合わせ回路に対して中性子照射実験を行って低電圧動作時のエラーレートを取得し、またSRAMの多ビットエラー空間分布を考慮してECC適用時のエラーレートを計算した。本評価により、65nm bulk及びSOTBデバイスにおいて、SRAMで発生したエラーの割合が95%以上であること、ECC適用時にはフリップフロップがチップレベルエラーの主要因になることを明らかにした。

2. ミュオン起因ソフトエラーのエラーレート評価とメカニズム分析

デバイスの微細化に伴い、中性子だけでなく地上宇宙線に含まれる他の粒子もソフトエラーを引き起こす可能性がある。ミュオンは地上宇宙線の60%以上を占める一方で、ビーム施設が極めて少ないためソフトエラーに関する実測が不十分で、特にエラー誘起能力が高い負ミュオンに対する実測評価は行われていない。本論文ではミュオンビームを用いた照射実験で、65-nm SRAMにおける正負ミュオン起因のソフトエラーレートを実測で評価した。実測結果より、定量的に負ミュオンのエラー誘起能力が正ミュオンより少なくとも6倍以上高いことを明らかにした。更に、負ミュオンによる多ビットエラーを観測し、寄生バイポーラ効果によるものであることを確認した。

3. ミュオン、中性子起因のソフトエラーの特徴比較

本論文では負ミュオン起因、中性子起因のソフトエラーの特徴を比較し、次の三つの類似点を明らかにした。エラーレートの電圧依存性、多ビットエラーの規模分布と空間パターン分布である。更に、負ミュオン及び中性子によって生成される二次イオンの電荷付与能力が同程度であることから、上記の類似性が生じていることをシミュレーションで明らかにした。さらに、ミュオンエラー率のデバイス世代依存性を評価した。

以上の成果より、現段階で最重要視されている中性子によるチップレベルを把握するとともに、潜在的な脅威であるミュオンによるソフトエラーの特性を評価し、現在から将来にかけての地上環境におけるソフトエラーに対する理解を深めた。これにより、半導体デバイス設計時の信頼性要求に対する設計最適化に貢献するものと期待できる。従って、博士（情報科学）の学位論文として価値のあるものと認める。