Doctoral Dissertation

Development of highly-efficient slurryless electrochemical mechanical polishing for silicon carbide wafers

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Chapter 1
Background

1.1 Introduction

Manufacturing techniques play a very important role in the progress of human civilization. From Stone Age to Copper Age, to the current Information Age, manufacturing techniques dominate the development level of science and technology of a civilization. In the current Information Age, for instance, electronic devices play a very important role in information processing and transformation. With respect to the development of science and technology, the human research field continues to expand. The trend for electronic devices seems to encompass and accommodate increasingly harsh environments normally characterized by high temperature, high power, high radioactivity, high-frequency, and so on, whereas their demands of power and performance tend to go higher and higher. Such issues pose a major challenge to the widely used electronic devices at the present.

On another perspective, energy shortage and global warming become more and more severe as of late, thereby necessitating the major role of reduction of energy consumption and waste discharge for the continued development of human civilization. Power electronics technology, which controls power energy with high and optimum efficiency, has greatly contributed to energy and resource saving. As a technology, it converts direct current to alternating current, or reversely, alternating current to direct current, or convert the current or voltage from power frequency to the frequency required by devices, or by effectively controlling power by properly controlling voltage. In other words, if power electronics equipment is utilized, electric energy can be used efficiently to directly contribute in suppressing the energy consumption of an accompanying economic activity.

Silicon (Si) semiconductor devices have been used for power devices, the key parts of power electronics equipment. With the evolution of power devices, the high power density of power electronics devices has been achieved, although further progress is becoming difficult due to the physical properties of Si-power devices [1)]. Under such circumstances, there has been much attention placed on semiconductor materials with a dramatic improvement in material properties compared to Si, such as wide bandgap semiconductor material silicon carbide (SiC), gallium nitride (GaN), diamond, etc., which can realize drastic high performance/low loss compared to the Si-power devices [2)].

These materials can be best applied on a smooth and damage-free surface. For instance, surface roughness of Si and SiC surface strongly affects their electronic properties [3,4] and the quality of epitaxial layer [5,6], which subsequently affects the performance of electronic power devices. Therefore, development of manufacturing techniques for these next-generation semiconductor materials also becomes an essential move to realize their application in electronic devices. However, the high hardness, high brittleness, and chemical inertness of these materials make their manufacture difficult, as they normally cannot be finished by conventional mechanical polishing techniques without induction of subsurface damage (SSD). Currently, chemical mechanical polishing (CMP) has been industrially used to finish the surface of SiC and GaN [7,8], but its material removal rate (MRR) is very low and the cost is very expensive [9,10]. For these reasons, it is imperative to develop a novel, highly-efficient, low-cost, and environmentally friendly polishing technique for these materials.

1.2 4H-SiC

1.2.1 Comparison of Si and SiC

Jöns Jakob Berzelius made the first attempt to prepare and characterize Si in pure form in 1983. The element's excellent semiconductor properties make it an ideal material for transistors that amplify electrical signals. Si is also the second most abundant element in the Earth's crust following oxygen, making it extremely affordable and appealing. Silicon has thus become the basis of memory chips, computer processors, transistors, and all other electronics [11,12], which accompanied the mature development of fabrication techniques of Si wafer and electronic devices.

SiC is a kind of carbide accidentally discovered by Acheson in 1891, being obtained in an experiment whose actual goal was to create a diamond-like crystal from carbon and alundum. Acheson firstly believed that these crystals were a compound of carbon and aluminum, thus naming the new compound carborundum, which was later verified as SiC [13]. Nevertheless, the name carborundum has become synonymous with SiC the world over. Not long after such discovery, that is, in 1893, Acheson developed a more efficient electric furnace for smelting SiC commonly known as the Acheson furnace [14]. This original design concept has long been used in the industry in almost all SiC-related fields. In this technique, electrodes that connect to a graphite core are laid within a surrounding mixture of reactant carbon, salt, and sand. The surrounding reactants get heated as electric current passes through the graphite core, leading to the formation of a hollow cylinder of SiC and the expulsion of carbon monoxide gas. SiC has been widely used in jewelry and grinding wheel trades due to its poor crystallinity, small size, but excellent polishing properties at that time.

Forward and reverse bias electroluminescence in SiC crystals was first observed by Round in 1907 [15]. It has been continuously studied since then to become an important electronic material by 1955, after proposal of the Lely method for production of bulk SiC crystals through the process of sublimation [16]. In the Lely method, SiC powder is loaded into an Argon-gas-purged graphite crucible and then heated to approximately 2,500 °C (4,530 °F). The SiC near the outer walls of the crucible sublimes gets deposited on a graphite rod near the center of the crucible, which is at a lower temperature [17]. Several modified versions of the Lely method exist, of which the most common is the SiC getting heated from the bottom end rather than the crucible walls, before being deposited on the lid. Other modifications include varying the temperature, temperature gradient, Argon pressure, and geometry of the system [18]. Currently, SiC substrates are mainly fabricated in diameters of 76 mm (3 inch) and 100 mm (4 inch) using the modified Lely method. Besides, the fabrication of 150-mm (6-inch)-diameter SiC substrates has been reported [19,20] and is expected to lead to a major decrease in the manufacturing cost of SiC power devices.

SiC exhibits prominent polymorphism (also called polytypism), resulting in more than 200 crystalline structures with varying stacking sequences [21,22]. On one hand, two of the most simplified polytypes are 3C (pure cubic stacking) and 2H (pure hexagonal stacking), which correspond to zinc-blende and wurtzite structures, respectively. On the other hand, the most

Table 1.1 Comparison of properties of Si and SiC [25-27]

Semiconductor materials	Si	SiC		
		3C	4H	6H
Bandgap (eV)	1.1	2.2	3.3	2.9
Breakdown electric field (MV/cm)	0.3	3	3.5	3
Thermal conductivity (W/cmK)	1.5	4.9	4.9	4.9
Electron mobility (cm^2/Vs)	1350	800	1000	460
Hole mobility (cm^2/Vs)	450	40	120	95
Saturation velocity ($\times 10^7$ cm/s)	1	2.5	2.7	2
Relative permittivity	11.8	9.7	10	10
BFOM*	1	487	997	289
BHFFOM*	1	59	101	34
Melting point (°C)	1420		2830±40	
Young's modulus (GPa)	190		441-500	

*BFOM (Burger Performance Index: Low Frequency) = $\varepsilon\mu_e E_c^3$, BHFFOM (Burger Performance Index: High Frequency) = $\mu_e E_c^2$. Here, μ_e is the electron mobility (cm^2/Vs), ε is the dielectric constant, E_c is the dielectric breakdown electric field strength (V/cm).

common polytypes are 4H and 6H structures, which exhibit a hexagonal symmetry with *ABCB* and *ABCACB* stack sequences, respectively. Different polytypes exhibit distinct band structures and band gaps [23,24]. Table 1.1 shows the electronic, thermal, and mechanical properties of Si, 3C-SiC, 4H-SiC, and 6H-SiC. Apparently, SiC has better excellent electronic and physical properties than Si. Moreover, although 3C-SiC, 4H-SiC, and 6H-SiC have similar properties, 4H-SiC demonstrates the most excellent electronic and physical properties. The bandgap, breakdown electric field, and thermal conductivity of 4H-SiC are 3, 10, and 3 times greater, respectively, than that of Si, and are particularly useful in withstanding a high-voltage, low-resistance (low-loss), and high-temperature operation. As such, excellent properties for power device applications can be expected. Excluding the excellent properties of SiC, its other similar material properties with Si makes it the most attractive as a research interest among the next-generation semiconductor materials, as many state-of-the-art silicon technologies can be analogized to the applications of SiC.

1.2.2 Application prospect of SiC

The excellent physical properties of SiC give SiC power electronics higher operating voltage, lower voltage drops, higher maximum operation temperatures, and higher thermal conductivities than Si electronics. At present, 1.2-kV SiC MOSFETs (metal-oxide-semiconductor field-effect transistors) with current ratings of 10–20 A and on-state resistances of 80 and 160 mΩ, along with 1.7-kV SiC-JFETs (junction field-effect transistors) with current rating of 48 A, are available on the market. SiC MOSFET chips rated at 10 A and 10 kV have also been investigated by Cree as a part of a 120-A half-bridge module [28]. A very small increase in leakage current is demonstrated even at high temperature owing to the wide bandgap of SiC, wherein a stable high-temperature operation can be realized. Theoretically, the maximum operation temperature of SiC devices is very high (> 700˚C), much higher than that of Si devices. Small-signal MOSFETs in SiC have been shown to be functional at 650˚C; an integrated operational amplifier was also functional at 300˚C based on NMOS (negative-channel metal-oxide-semiconductor) devices [29].

Energy loss can be greatly reduced by using SiC. In SiC transistors, for instance, the thickness of the drift layer, which is a main factor of electric resistance upon manufacture of a switching device, can be reduced to 1/10 of Si as the dielectric breakdown electric field of SiC is approximately 10 times higher than that of Si. On this basis, power loss can be greatly reduced with the resistance value between the drain electrode and the source being greatly reduced. Additionally, owing to the less power loss (the amount of heat generation) and the high-temperature operating characteristics of the power devices, the cooling system, which is

indispensable for the application of the power devices, can be miniaturized and the size and weight of the device can be reduced [30]. Owing to the bipolarity of SiC transistors, there are almost no overshoot current and tail current during switching (ON and OFF), so that the energy loss can be significantly reduced compared with the Si-power module [31,32]. By using SiC, the energy loss of inverters on the train is reduced by 30%, whereas the inverter volume and mass is reduced by 40% [33]. This property also allows SiC transistors to be turned on or off in nanoseconds [34], which is very useful in high-frequency switching applications [35,36] and high-frequency conditions [37,38].

The above discussions suggest the very promising position of SiC inverters in the fields of photovoltaics, hybrid electric vehicles, and high-power applications. The advantageous features of the SiC transistor perfectly match to meeting the two basic requirements of the photovoltaic industry, namely, increase in efficiency and integration of the inverter with the photovoltaic panel [39]. By applying SiC IPM (intelligent power module), Mitsubishi Electric Corporation is able to achieve 4.4 kW power conditioner for solar power generation system with power conversion efficiency of 98.0% [40]. The performance of hybrid electric vehicles can also be greatly improved by the application of SiC inverters [41,42]. For instance, after applying an SiC inverter to a plug-in charger, size and cost were decreased to 1/10 of the present charger [43], which shows a very promising application prospect. For high-power applications, SiC inverters are very especially attractive in grid applications, especially in high-voltage direct current (HVdc) transmission, which can greatly reduce the energy loss compared to high-voltage alternating current transmission due to its stability. If equipped with future 3.3 kV 1.2 kA SiC-JFETs, a 300-MW modular multilevel converter (M2C) for HVdc transmission would potentially have an efficiency of approximately 99.8% [44].

At present, cost is the main difficulty in the spread of SiC applications. The growth techniques of SiC ingot, especially for large-size SiC, is still undergoing development, owing to the extreme difficulty in controlling defects in the crystal growth process [45,46]. Furthermore, the efficiency of manufacturing techniques for mass production of SiC is still unsatisfied with the high hardness and chemical inertness of the material. Both problems increase fabrication cost of SiC electronics than Si electronics, which significantly inhibits the applications of SiC; thus, development of low-cost production techniques for SiC is a necessary goal.

1.3 Motivation of this study

As mentioned in the previous sections, atomically smooth damage-free surface is an essential requirement in the application of SiC wafer, whereas applying mechanical polishing in the current manufacturing process would face challenge to satisfy these demands. Besides, the high

fabrication cost of SiC significantly hinders mass production. Another important problem is the environment and energy consumption of the current manufacturing process. The motivation of this study is the development of a novel polishing technique in order to resolve the problems associated with the current polishing techniques for these difficult-to-machine materials. As such, the study introduces a novel polishing technique named slurryless electrochemical mechanical polishing (ECMP). Slurryless ECMP presents an organic combination of surface modification using anodic oxidation and removal of modified layer using fixed soft abrasives. Specifically, the study aims to develop a highly-efficient, low-cost, and damage-free manufacturing process based on slurryless ECMP for next-generation wide-gap semiconductor materials.

1.4 Thesis organization

This thesis consists of six chapters.

In current chapter (Chapter 1), the background of this study, current issues in the manufacture of SiC wafers, the performance, properties, and applications of SiC, and the aim of this study are described.

In Chapter 2, slurryless ECMP is proposed on the basis of the introduction of existing polishing techniques of SiC. Basic concepts and principles of slurryless ECMP are described and the feasibility analysis of slurryless ECMP is conducted.

In Chapter 3, anodic oxidation mechanism of 4H-SiC (0001) surface is investigated. The influence of anodic oxidation conditions on the oxidation properties of SiC is studied; the reason for the non-uniform oxidation of SiC is investigated and the strategy for obtaining smooth surface using slurryless ECMP is proposed. Besides, possible generation mechanism of surface microstructures on SiC surface by anodic oxidation and HF etching is discussed.

In Chapter 4, a prototype slurryless ECMP machine is developed to realize the polishing of SiC wafers, the structure and polishing properties of this slurryless ECMP machine are introduced. Then, slurryless ECMP is applied to 4H-SiC wafers. The polishing properties of different grinding stones and the performance of two-step ECMP and simultaneous ECMP are investigated. The application results of slurryless ECMP on the sliced SiC wafers are introduced and analyzed. Besides, the polishing motions and polishing process of slurryless ECMP are optimized. A novel manufacturing process for 4H-SiC wafers is established by applying slurryless ECMP.

In Chapter 5, the influence of SSD on the polishing performance of slurryless ECMP is studied. The relationship between MRR and SSD is investigated, and a method to further improve the MRR by introducing thin SSD film in the ECMP process is investigated and studied.

Chapter 6 is a summary of this thesis.

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Chapter 2
Slurryless electrochemical mechanical polishing

2.1 Introduction

As described in Chapter 1, silicon carbide has a very broad application prospect and can significantly alleviate the current energy consumption issues to contribute to the realization of a low carbon society. However, the difficulty and cost in the manufacture of SiC wafers seriously slow the spread of SiC wafers. The most direct processing technique for SiC is removal of the SiC material by applying abrasives that are harder than SiC, i.e., diamond in general, but such technique makes scratches and SSD inevitably form on the SiC surface with the mechanical removal of the material [1,2]. Scratches and SSD deteriorate the surface roughness and electronic performance of SiC wafers. Nonetheless, although the scratch depth and SSD thickness can be reduced through application of small-sized abrasives, they cannot be completely removed. Preventing the induction of SSD during mechanical removal of the surface can be achieved with the increasingly popular chemical processing techniques, which can realize damage-free polishing as no pressure is introduced to the base material during removal. On the contrary, pure chemical etching, with etching being an isotropic process, exhibits poor flattening ability. Thus, a combination of the flattening ability of mechanical polishing and the damage-free characteristics of chemical etching has been seen as a very promising way to achieve a flat damage-free surface.

2.2 Current manufacturing process of SiC wafers

SiC wafers are generally characterized by density of defects, flatness, roughness, bow, warp, total thickness variation, and local thickness variation. Of these, density of defects is mainly determined by the crystal growth process, whereas the other indicators are determined by the subsequent machining process, which requires SiC wafers to be not only flattened but also become smooth and mechanical-damage-free. The most common methods of producing flat and smooth substrates involve a sequential series of material removal steps to gradually achieve a high level of flatness and low roughness. Each polishing step uses smaller and smaller abrasive particles in reducing the surface roughness to a target level. Because the surface and subsurface damage cannot be completely removed by mechanical polishing, chemical polishing techniques are applied to the final finishing of SiC wafers.

A typical manufacturing process of SiC wafers is shown in Figure. 2.1 [3]. SiC ingot grown by the modified Lely method is first processed to the desired diameter by external grinding. The ingot is then sliced to SiC wafers by a multi-wire saw. As slicing of the ingot causes saw marks, surface damage, and SSD to the cut wafers, the wafers are treated with grinding and lapping process to make each face of the substrate parallel and achieve global flatness, while surface and subsurface damage is reduced. To avoid chipping at the circumference of the wafer or cracking during the grinding, edge chamfer should be made prior to the grinding. The wafers are finally brought for finishing by CMP, for complete removal of the surface and subsurface damage toward a certain target surface roughness.

Currently, this manufacturing process is successfully applied to the fabrication of Si wafers. However, SiC being naturally hard and chemically inert, cutting, grinding, and polishing methods for single-crystal SiC resort to applying diamond and metal carbide abrasives for the primary shaping of the substrates. Compared to the standard abrasives that are used to polish silicon substrates, the diamond abrasives required to process SiC are very costly. Additionally, the polishing times of SiC are quite long even with the diamond abrasives—the MRRs for SiC are 5–20 times lower than the corresponding silicon substrate process. Inefficient removal rates and expensive abrasives make the process to polish SiC extremely costly, especially when conventional strategies to produce flat wafers are applied to SiC.

There have been many research dedicated to improving the existing manufacturing process. For example, Kim *et al.* proposed the femtosecond laser induced slicing method, in which the exfoliated surface with root-mean square roughness of 5 μm and cutting-loss thickness smaller than 24 μm were successfully achieved [4]. Additionally, by forming a light-absorbing separation

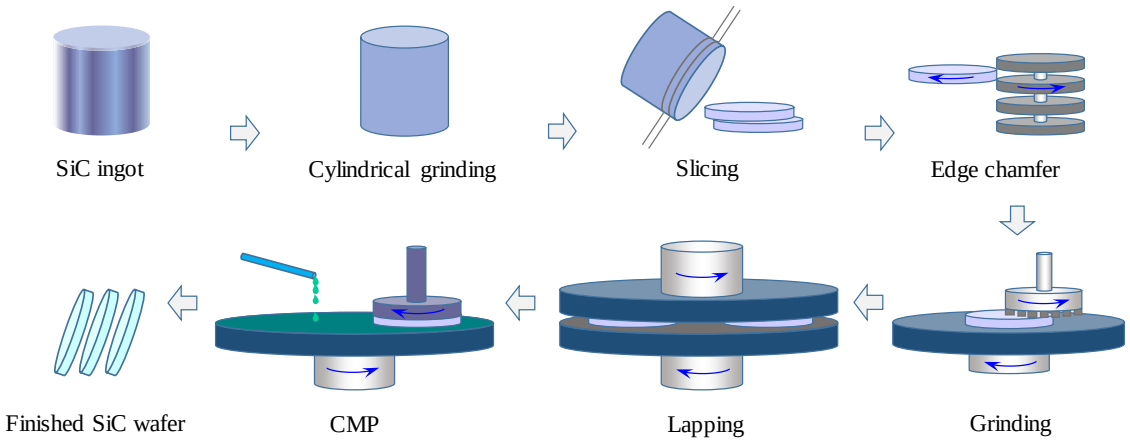

Figure 2.1 Typical manufacturing process of SiC wafers [3].

layer (KABRA layer) in a flat shape to an arbitrary depth using laser, the slice time and cutting-loss thickness of a SiC wafer was significantly decreased [5]. However, there was still no good way to flatten the wafers, so that grinding and lapping seem irreplaceable. By contrast, many polishing techniques based on chemical modification are being developed to obtain high efficiency and smooth surface with high integrity and high crystallinity.

2.3 Current polishing techniques of SiC wafers

Many polishing techniques that combine chemical reaction and mechanical polishing are presently being developed for the finishing of SiC wafers. These include CMP, plasma-assisted polishing (PAP), catalyst-referred etching (CARE), and UV-assisted polishing, among others. The basic strategy is similar: modify the SiC surface by physical or chemical method and remove the modified layer by etching or mechanical polishing. The poor machinability of difficult-to-machine materials can be resolved by surface modification. Optimization of the polishing conditions to obtain perfect surfaces with a relatively low polishing cost and high efficiency has been widely conducted in recent years.

2.3.1 Chemical mechanical polishing

CMP, also referred to as chemical mechanical planarization, was initially used as an enabling technology to fabricate high performance multiple-level metal structures. The first CMP application attempt to semiconductor fabrication was done at IBM [6,7], using the company's expertise to their own silicon wafer fabrication technology. A typical structure of CMP setup is shown in Figure 2.2. The setup can be divided into three parts, namely, machines, polishing pads, and slurries. Figure 2.3 shows the polishing mechanism of specimens. The slurry used in CMP is

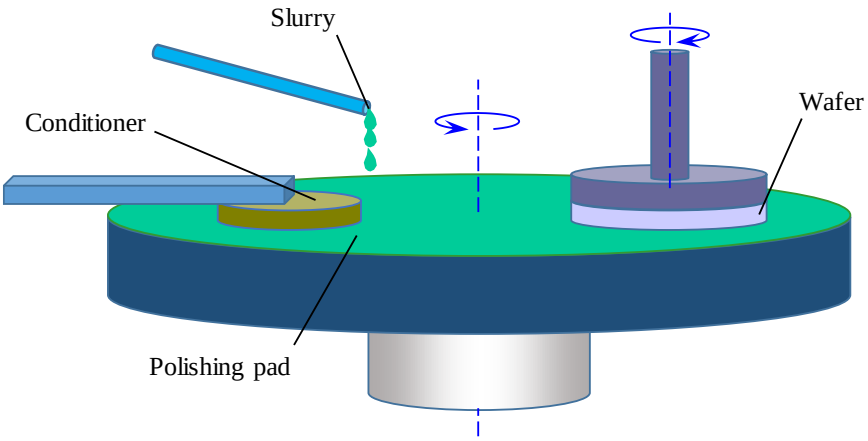

Figure 2.2 Schematic diagram of CMP.

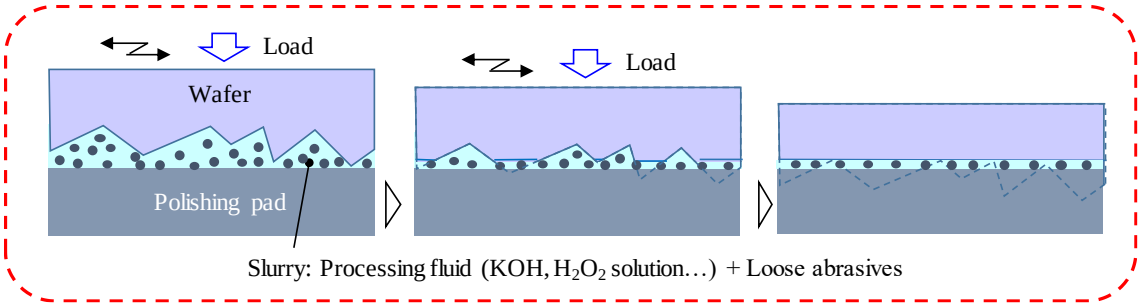

Figure 2.3 Polishing mechanism of CMP.

usually made of alkali, oxidant, and abrasives, although dispersant is generally needed to prevent abrasive particle aggregation. In CMP, the specimen is modified by alkali or oxidant through hydroxylation, hydration or oxidation reactions, and then the modified layer is subsequently removed by abrasives. Because atomically smooth and flat surfaces can be obtained by CMP, such technique widely used in the finishing of optical components and Si wafers. Si wafers in CMP display an MRR higher than 10 μm/h [8,9]; this allows CMP become an industrially applicable finishing technique for Si wafers.

Furthermore, as a mature polishing technique for Si wafers and many other dielectric materials, CMP is naturally used for the polishing of SiC. In the CMP of SiC, an alkaline colloidal silica slurry is widely used. The Vickers hardness of the silica is 7.6 GPa [10], which is smaller than that of SiC (24–28 GPa [11]); therefore, there are no scratches generated as silica cannot remove SiC but only remove the modified layer. There have been reports of achieving SiC surface with *S*q surface roughness of less than 0.2 nm, through CMP application [12], with observed step-terrace structure, although not uniform, on the processed surface. As such, SiC surfaces obtained by CMP can almost satisfy the application of SiC wafer in electronic power devices, but the MRR of CMP is limited by the chemical activity of specimens, as the high chemical inertness of SiC, generally, the MRR of SiC in CMP, is less than 0.5 μm/h [13,14].

The MRR in CMP of SiC wafers can be normally increased by increasing the modification rate of SiC surface through the application of a strong oxidant or catalyst to the slurry. Hydrogen peroxide (H_2O_2) and potassium permanganate ($KMnO_4$) as processing chemical have been successful on this respect [15,16]. Application of abrasives applied in CMP has also attracted research focus. For one, manganese dioxide (MnO_2) and $KMnO_4$ slurry were reported to improve the MRR via the oxygen (O_2) generated during the polishing process [17]. There were also studies on hybrid polishing with submicron diamond and colloidal silica slurry, taking into consideration the very low MRR of colloidal silica slurry [18-20]; the possible mechanism of this hybrid polishing is proposed by Lee *et al.* [21]. Here, the diamond abrasives mechanically remove SiC and induce

stress on the relatively low-stressed surface of SiC. The stressed areas react more readily with slurry chemicals and are easily smoothed with colloidal silica abrasives. Therefore, hybrid polishing can remove the relatively low stress area faster than CMP with colloidal silica slurry. With the addition of diamond abrasives, the MRR of SiC increased from 0.21 to 0.55 μm /h. Adding a 0.1-μm diamond abrasive and sodium hypochlorite oxidizer to the colloidal silica slurry further yielded a relatively high MRR of 0.92 μm/h [22].

Although several optimizations have been done to improve the MRR in CMP of SiC, these were not enough to yield an MRR that satisfies the industrial production requirement of SiC wafers. Besides, the addition of catalyst or application of strong oxidants to the slurry not only increases the processing cost, but also the difficulty in management and post-treatment of the slurry. Furthermore, the non-uniform step-terrace structure obtained in CMP is a big problem in the fabrication of electronic devices, as it affects the following epitaxial growth process [23].

2.3.2 Catalyst-referred etching

Hara *et al.* [24,25] proposed CARE mainly to overcome the anisotropic etching in chemical etching or electrochemical etching of SiC surfaces. The flattening mechanism of SiC surface in CARE is depicted in Figure 2.4. A catalyst plate (generally Pt) is applied to activate the processing fluid (generally hydrofluoric acid: HF) near the surface of the catalyst, and etching of the SiC surface only occurs in the reaction area because SiC cannot be etched by the processing fluid without the catalyst. Therefore, only the raised part on the SiC surface can be removed. An atomically flat SiC surface can be obtained with the etching progress. SiC surface with root-mean square surface roughness of less than 0.1 nm was obtained by applying CARE, but its MRR seriously depended on the orientation of the SiC surface [26,27]. The MRR of on-axis SiC wafer was approximately 1 nm/h, and 60 nm/h for 8°-off SiC wafer.

Efforts have been done to improve the MRR of CARE. By optimization of rotational velocity and processing pressure, an MRR of approximately 0.5 μm/h was obtained for an 8°-off 4H-SiC

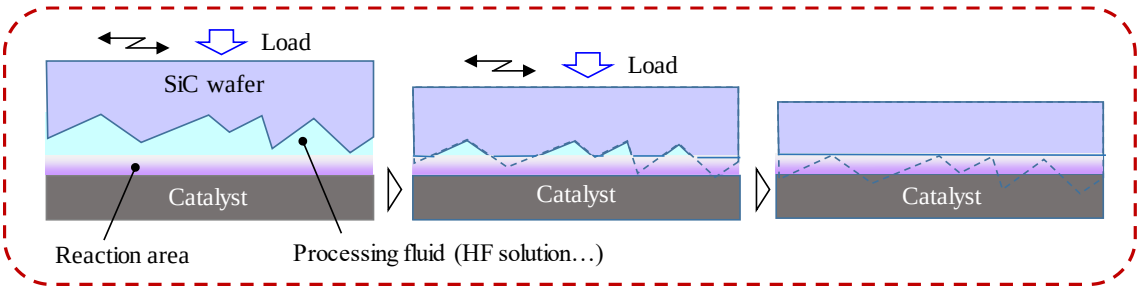

Figure 2.4 Flattening mechanism of SiC surface by CARE.

wafer [28]. UV irradiation was also applied to CARE; by using nitric acid (HNO_3) as processing fluid under UV irradiation, an MRR of 21 nm/h was obtained [29]. Parallel efforts to minimize the cost of implementing CARE have also been carried out. Recently, there were studies conducted to replace the catalyst plate with inexpensive metals [30]. Furthermore, water-CARE has been investigated to make CARE more practically applicable and environment-friendly [31].

2.3.3 Plasma-assisted polishing

Yamamura *et al.* [32] proposed PAP, a technique utilizing the high reactivity of radicals in plasma so as to modify the SiC surface. Figure 2.5 illustrates the polishing mechanism of a SiC surface by PAP. The SiC surface is first irradiated by water vapor plasma or oxygen plasma to modify the surface to a soft oxide layer. The oxide layer is then removed by fixed soft abrasives, such as ceria or silica, that are softer than SiC. Because the soft abrasives can only remove the oxide layer, no scratches and SSD form on the processed surface. In PAP, the hard SiC surface can be softened eight times using the above technique. Through the use of a ceria grinding stone, a damage-free atomically smooth surface with *S*q surface roughness of less than 0.2 nm was obtained [33]. Nonetheless, the MRR of SiC in PAP is generally lower than 1 μm/h [34].

PAP can change the gas composition of the plasma, and thus, is also effective in the finishing of GaN [35], reaction sintered silicon carbide (RS-SiC) [36], and diamond [37]. In the PAP of GaN with carbon tetrafluoride (CF_4) plasma, the hardness of GaN surface was decreased by almost half, surface with *S*q surface roughness of less than 0.1 nm was obtained, and with no pits generated on the sites of dislocation. Due to the non-uniform modification of Si and SiC that construct the RS-SiC material, it was very difficult to decrease the surface roughness of the RS-SiC by PAP, and thus, a surface with *S*q surface roughness of 0.91 nm was obtained. For the PAP of a single-crystal diamond wafer, a polishing rate of 2.1 μm/h and an *S*q surface roughness of 0.13 nm were obtained, but the removal mechanism of diamond in PAP remains unclear.

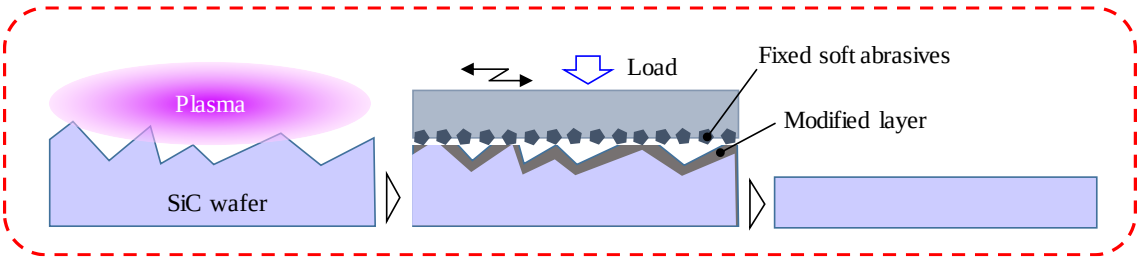

Figure 2.5 Polishing mechanism of PAP.

2.3.4 Mechanochemical polishing

Yasunaga *et al.* [38] proposed mechanochemical polishing (MCP) for polishing of sapphire using steel in a dry ambient. Soft abrasives with high affinity to the specimen are used in MCP. The abrasives react with the specimen around the contact points, which locally have high temperature and high pressure. The reaction products are combined to the abrasives and are removed, resulting in the polishing of the specimen. Yasunaga *et al.* also applied this polishing technique to single-crystal Si and quartz crystal, in which they concluded that a damage-free mirror surface could be achieved with powders, i.e., $BaCO_3$, $CaCO_3$, for Si wafers, and i.e., Fe_3O_4, MgO, for quartz crystals [39].

Kikuchi *et al.* conducted an MCP study of SiC using Cr_2O_3 abrasives [40]. Cr_2O_3 played two roles in this polishing process. First, it acted as a catalyst to promote the reaction between SiC and oxygen from the ambient, leading to the oxidization of SiC. Second, it acted as an abrasive to remove the oxide layer by abrasion. Consequently, a damage-free and scratch-free surface with PV surface roughness of less than 5 nm was obtained, and MRRs of 0.408, 11.3, 5.27, and 4.27 μm/ks for (0001), (000–l), (1–100), and (11–20) oriented samples were obtained.

2.3.5 Ultraviolet-assisted polishing

Watanabe and Touge *et al.* [41] proposed ultraviolet (UV)-assisted polishing, wherein they applied a quartz plate to polish the SiC surface with the assistance of UV irradiation, as demonstrated in Figure 2.6. This polishing technique is considered as an MCP process combined with a UV-induced photochemical reaction. Here, UV light passes through the quartz plate and irradiates the SiC surface, and SiC surface is modified owing to the oxygen radicals that generated from the ambient oxygen molecule by irradiation of UV. Simultaneously, the contaminant on the quartz glass is removed by the UV irradiation, thus, enhancing the contact between the SiC surface and the quartz glass, and further improves the modification of SiC surface as that in MCP. Subsequently, the modified layer is removed by relative sliding of the quartz plate. Smooth surface can be obtained with the progress of modification and polishing. In their latter study, TiO_2 and CeO_2 abrasives were coated on the quartz glass to improve the MRR and surface roughness [42]. Here, with the CeO_2 abrasives an MRR of 0.86 μm/h was obtained in atmospheric ambient; this increased to 1.487 μm/h in O_2 atmosphere in the polishing of a 4°-off 4H-SiC substrate, and yielded a surface with *R*a roughness of less than 0.5 nm [43].

UV-assisted polishing was more effective in the polishing of diamond [44]. In the polishing of single-crystal diamond substrate, surfaces with *R*a surface roughness of 0.2–0.4 nm and MRR of approximately 0.5 μm/h were obtained. In the polishing of polycrystalline diamond substrate, an

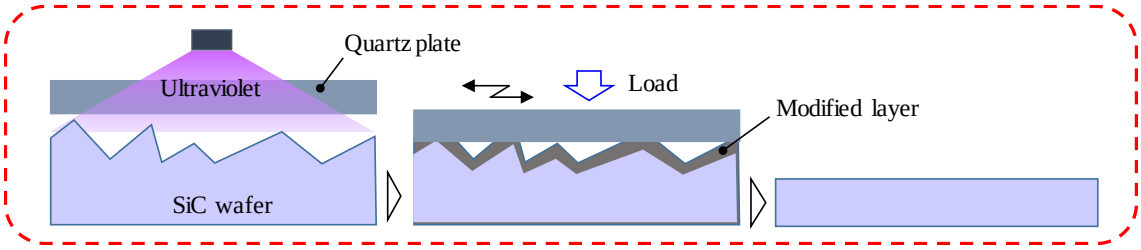

Figure 2.6 UV-assisted polishing.

MRR of 2.0 μm/h was obtained in atmosphere, which increased to 6–7 μm/h in higher oxygen concentration (approximately 82%). The polishing mechanism of diamond is considered as follows: C atoms on the topmost surface of diamond are oxidized by active species, such as hydroxyl radicals (OH radicals) and oxygen radicals, at localized high temperature and finally removed as CO and CO_2.

2.4 Proposal of slurryless electrochemical mechanical polishing

2.4.1 Introduction

Although SiC polishing can be realized with the above-discussed polishing techniques, several problems hinder their application, including high cost, low MRR, and relatively poor surface roughness. Besides, these techniques can only be applied at the final finishing process of SiC wafers, and are not able to simplify the manufacturing process. Therefore, it is essential to develop a highly-efficient, low-cost, and highly-precise polishing technique for SiC. Electrochemical methods are interesting means of increasing the modification rate of the surface. During electrochemical reactions, electron transfer between substances can be enhanced by the applied potential, greatly increasing the reaction rate. Carriers are generated in the bulk SiC as a result of SiC doping, and this allows SiC to have certain electric conductivity. On such basis, there is a positive light that the modification rate of SiC is likely to get improved by the electrochemical method.

2.4.2 Electrochemical properties of SiC [45,46)]

In aqueous solutions in general, the Fermi level of N-type SiC (E_F) is greater than that of redox pair ($E^0_{F(O/R)}$). Therefore, when N-type SiC contacts with an aqueous solution electrolyte, electrons (e) in the N-type SiC transfer to the redox pairs in the electrolyte, redox reactions occur. With the transfer of electrons, there is a positive charge associated with the space charge layer formed below the SiC surface, while anions gather at the side of electrolyte at the interface

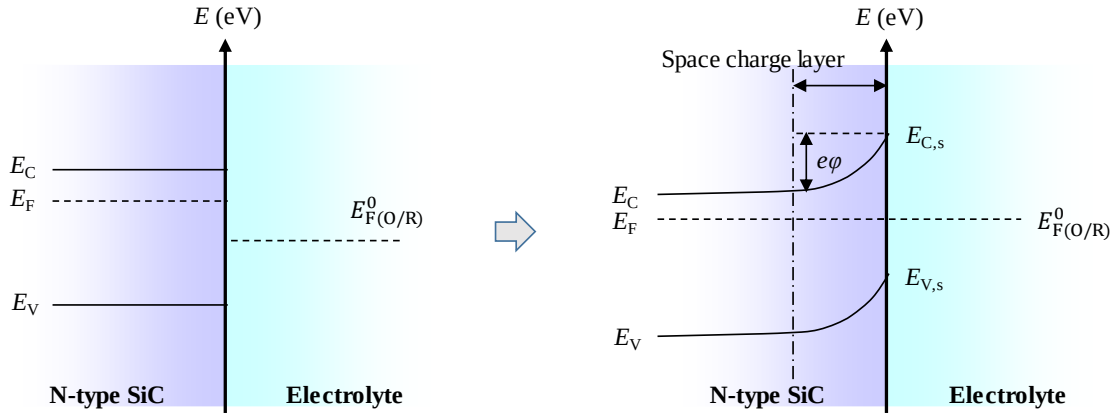

Figure 2.7 Band structure of N-type SiC before and after contacting with electrolyte.

between SiC and electrolyte. Since the majority charge carrier (electrons) of the N-type SiC has been removed from this region, this region is also referred to as a depletion layer, whose thickness varies within 0.01–1 μm. An interface electric field forms, while the transfer of electrons at the interface achieves a dynamic balance. The electric field results in a local positive potential on the space charge layer, and makes the electrons in the space charge layer achieve an additional potential energy ($-e\varphi$). Because the interface electric field is far smaller than that of nucleus, the additional potential energy only results in the upward bending of the conduction and valence bands of SiC. After reaching the balance, E_F is equal to $E^0_{F(O/R)}$, as shown in Figure 2.7. Oxidation and reduction reactions at the interface also reach a dynamic balance. It can be considered that no redox reactions occur at this time.

The potential of the space charge layer can be changed by an applied electric field. Figure 2.8 shows the band structure of an N-type SiC after a positive potential U has been applied. During this time, the potential of bulk SiC increases, along with the band bending in the space charge layer, so that electrons move to the bulk SiC and holes move to the SiC surface, resulting in the gathering of more holes in the space charge layer and the oxidation of SiC surface as below [47]:

$$SiC + 6h^+ + 6OH^- \rightarrow SiO_2 + CO\,(g) + 3H_2O, \quad (2.1)$$

$$SiC + 8h^+ + 8OH^- \rightarrow SiO_2 + CO_2\,(g) + 4\,H_2O. \quad (2.2)$$

H^+ ions generated in these two reactions move to the cathode under the applied electric field, and participate in the reduction reaction:

$$2H^+ + 2e^- \rightarrow H_2\,(g). \quad (2.3)$$

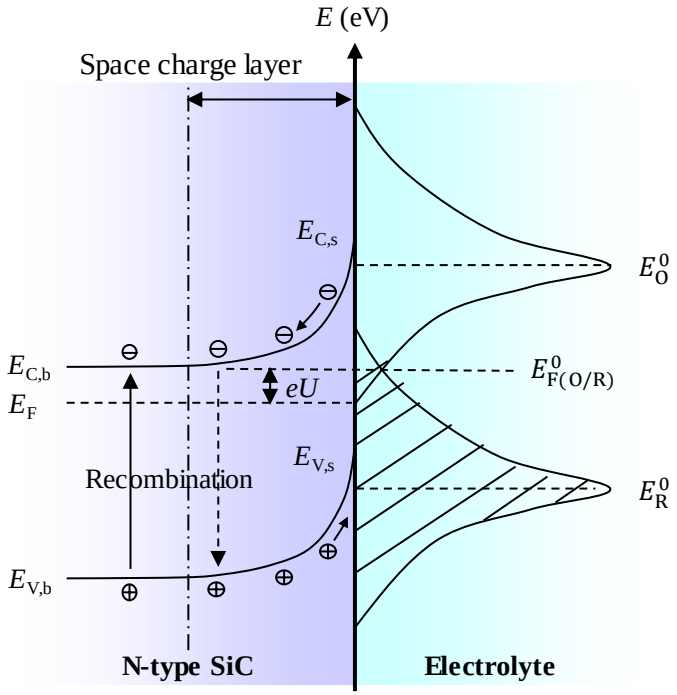

Figure 2.8 Changes in energy band of N-type SiC after applying a positive potential *U* on SiC.

By increasing the potential of the space charge layer through the applied electric field, the oxidation rate can be greatly enhanced. Therefore, controllable and high-rate modification of SiC surface can be realized by anodic oxidation.

2.4.3 Slurry electrochemical mechanical polishing

Electrochemical mechanical polishing using slurry was proposed on the basis of the excellent performance of anodic oxidation [48-50]. Li *et al.* made the first attempt on the application of ECMP to 4H-SiC wafers, using a KNO_3 and H_2O_2 solution as an electrolyte and silica slurry as the polishing medium [48]. Smoothed 4H-SiC (0001) surface with large-area was obtained by both two-step and simultaneous ECMP; however, several etch pits were also generated on the polished surface that significantly increased the surface roughness, onto which additional hydrogen etching was applied to finish the surface to obtain atomic-scale roughness. Deng *et al.* [49] used ceria slurry as both an electrolyte and a polishing medium and obtained a damage-free surface with an *S*q surface roughness of 0.23 nm, although not atomically smooth. Murata *et al.* [50] proposed a polishing-pad-free ECMP using polyurethane-CeO_2 core-shell particles, and obtained a surface with relatively high *R*a surface roughness of 0.52 nm. Studies of ECMP using slurry yielded relatively high MRRs of 3–4 μm/h; nonetheless, the flattening of the SiC surface and the obtained surface roughness were inadequate to satisfy the specification requirement in the fabrication of

electronic devices. These scenarios make ECMP as a research interest less attractive, where ECMP-related research results are also less.

2.4.4 Loose-abrasive and fixed-abrasive polishing

There are two main methods in polishing techniques, namely, loose-abrasive polishing and fixed-abrasive polishing. Loose-abrasive polishing is a type of pressure replication method: it applies loose abrasives and soft polishing pad to polish the surface, hence, generating a small pressure between the specimen and the abrasive particles. Here, almost no mechanical damage is induced to the processed surface, and it becomes easier to obtain a damage-free surface, unlike in the fixed-abrasive polishing; nonetheless, the MRR is small. In addition, with application of the soft polishing pad and with the uneven distribution of the abrasives, pressure distribution in the contact area is impossible to control. As such, this method cannot correct the shape accuracy. Furthermore, the use of slurry increases the polishing costs. It has been reported that the use, management, and post-treatment of slurry account for almost 50% of the total cost of CMP [51].

On the contrary, fixed-abrasive polishing uses a motion transfer method, wherein the surface shape is determined by the tool shape and its motion trajectory, thus, enabling an easy control of the shape accuracy. In addition, only a coolant is needed and no slurry is required, which significantly decreases slurry management and proposal cost. Nonetheless, due to the rigid contact between the abrasives and the specimen, damage is easily induced to the surface. This is the reason why in general, fixed-abrasive polishing is first applied for shape correction, and then loose-abrasive polishing is used for the final finishing of the surface to decrease surface roughness.

In ECMP, the SiC surface is first modified by anodic oxidation, and then the modified layer is removed by soft abrasives. Only the modified layer can be removed as the abrasives are softer

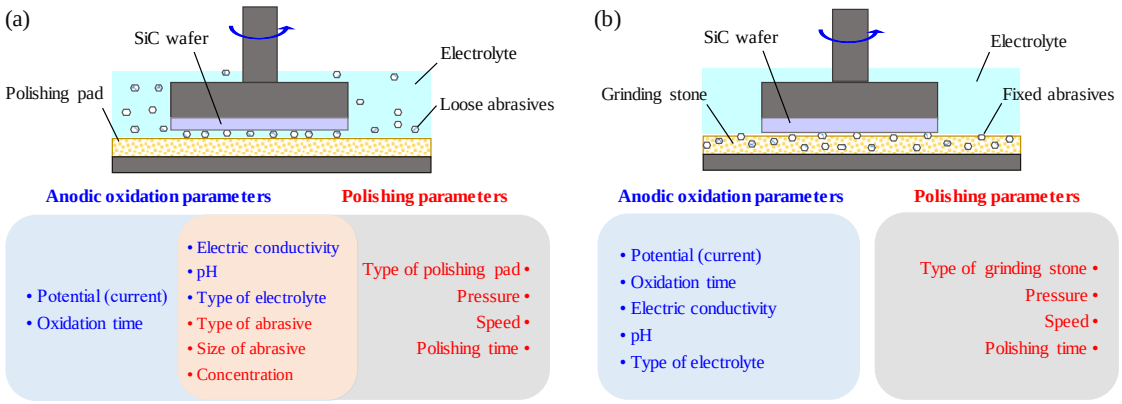

Figure 2.9 Comparison of loose-abrasive and fixed-abrasive polishing for ECMP. (a) Loose-abrasive polishing. (b) Fixed-abrasive polishing.

than SiC. Hence, scratches and SSD are not induced to the SiC surface, making fixed-abrasive polishing with soft abrasives (with hardness lower than SiC) applicable for the ECMP of SiC surfaces. Several other advantages sprout for applying fixed-abrasive polishing method to ECMP. A comparison between loose-abrasive and fixed-abrasive polishing in ECMP is given in Figure 2.9. Note that in ECMP, anodic oxidation of the SiC surface and mechanical polishing of the modified layer are simultaneously conducted. In slurry ECMP, anodic oxidation parameters, i.e., type, pH, and electric conductivity of the electrolyte, and polishing parameters, i.e., type, size, and concentration of the abrasive, cannot be controlled simultaneously, because the electrolyte can be considered as the slurry. Both the anodic oxidation and mechanical polishing of the modified layer have great influences on the surface quality of SiC; therefore, it is very difficult to obtain an atomically smooth surface via ECMP by slurry. With ECMP using fixed-abrasive polishing method, the parameters of abrasives can be decided by the type of grinding stone; thus, the anodic oxidation parameters and abrasive parameters can be separately controlled, and the drastic improvement of ECMP performance is expected.

2.4.5 Strategy of slurryless ECMP for difficult-to-machine materials

Based on the above analysis, slurryless ECMP, which combines anodic oxidation and fixed-abrasive polishing, is proposed as shown in Figure 2.10. For this technique, SiC is fixed on a wafer holder mounted on the tip of a spindle with an insulating layer, and is allowed to contact with a grinding stone. The grinding stone is pasted on a metal plate with many fan-shaped (or other shape) openings. The metal plate is set on a rotary table with an insulating layer. The SiC

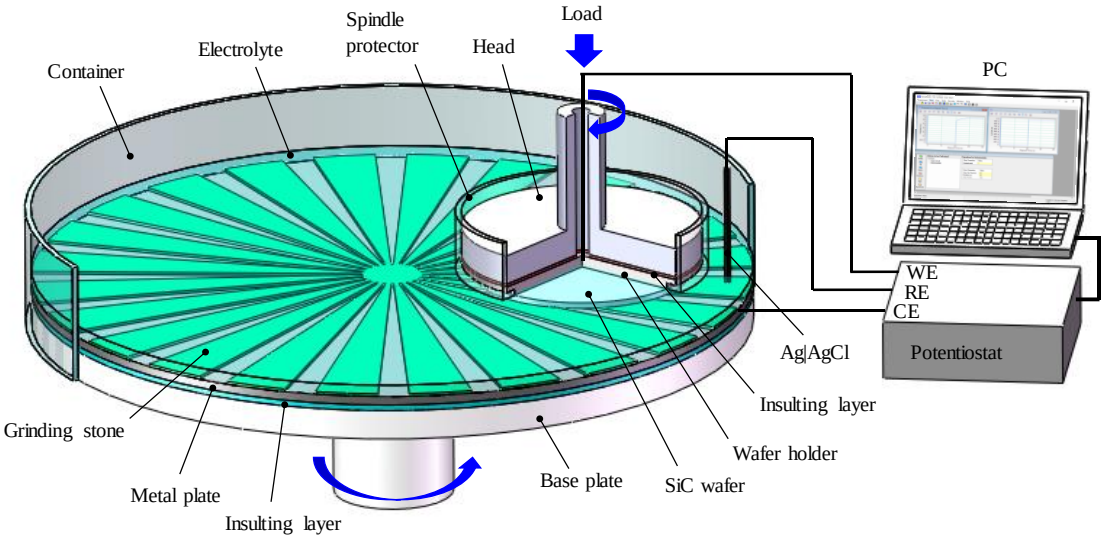

Figure 2.10 Schematic diagram of slurryless ECMP.

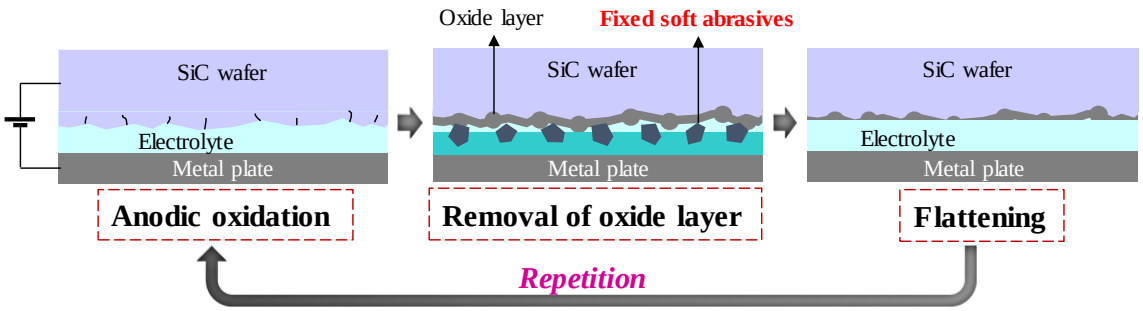

Figure 2.11 Polishing mechanism of slurryless ECMP.

wafer, grinding stone, and metal plate are immersed in an electrolyte. During slurryless ECMP, the SiC wafer is served as a working electrode (WE) and a positive potential is applied on it though the wafer holder, while the metal plate is used as a counter electrode (CE) with a negative potential applied on it. A reference electrode (RE) is used to accurately control the potential applied to the SiC wafer, which is a process controlled by a potentiostat. Wholly, the potentiostat, wafer holder, SiC surface, electrolyte, and metal plate form an electric circuit. SiC surface can be anodically oxidized by the applied positive potential, and the oxidation rate can be adjusted by controlling the potential using the potentiostat.

The polishing mechanism of the proposed slurryless ECMP is shown in Figure 2.11. The SiC surface is first modified by anodic oxidation to generate a modified layer on the surface. Subsequently, the modified layer is removed by the grinding stone. At the initial stage of ECMP, only the convex oxide area on the surface is removed, while the concave area is still covered with the oxide layer. Therefore, the oxidation rate of the convex area should be greater than the concave area owing to the barrier induced by the oxide layer. Repetitive anodic oxidation and removal of oxide results to gradual flattening of the surface and eventually give a damage-free surface. Compared with conventional polishing techniques such as mechanical polishing and CMP, slurryless ECMP exhibits advantages laid out as follows.

First, a highly-efficient polishing can be expected. MRR in slurryless ECMP is mainly controlled by the anodic oxidation rate of SiC surface. Anodic oxidation rate of N-type SiC can reach 53 nm/min [52]; it even reached 1.3 μm/min in the case of P-type SiC [53]. In slurryless ECMP, the MRR can be further improved by the enhanced ion exchange rate and the increased force by the polishing motion and pressure. This is indicative of high MRR. Besides, the anodic oxidation rate is proportional to the electric current, and the MRR can be quantitatively controlled by the electric current, which is a feature that also improves the performance of slurryless ECMP.

Second, damage-free polishing can be expected. In slurryless ECMP, SiC surface is first modified by anodic oxidation, and then the modified layer is removed by fixed soft abrasives.

Because abrasive is far softer than SiC, unlike the case in conventional fixed-abrasive polishing, only the modified layer can be removed and no scratches and SSD is induced to the SiC surface. Therefore, the disadvantages of conventional fixed-abrasive polishing are overcome, but its flattening ability is fully utilized.

Third, reduced production costs can be expected. In slurryless ECMP, only an electrolyte is used; there is no slurry required. In contrast to conventional modification techniques that apply strong oxidants, a neutral electrolyte, i.e., sodium chloride (NaCl), potassium chloride (KCl), and sodium nitride ($NaNO_3$), can be applied to the anodic oxidation of SiC. Furthermore, by the application of the grinding stone, the waste proposal of the electrolyte can be significantly decreased. In addition, unlike the catalyst plate and chemicals in CARE, the gas supply system and generation system in PAP, or the UV and catalytic abrasive in UV-assisted polishing, the slurryless ECMP machine has no additionally expensive parts.

Finally, the manufacturing process of SiC wafers can be simplified. Due to the high MRR and flattening ability of slurryless ECMP, its applicability does not only cover the final finishing of SiC wafers, but is also very promising for processing of sliced or roughly grinded/lapped SiC wafers. A simplified manufacturing process for SiC wafers invites further reduction of their manufacturing costs, and welcomes a significant improvement in their production efficiency.

2.4.6 Pourbaix diagram of SiC in aqueous solutions

For electrochemical reactions, the reaction is generally presented by:

$$\sum \nu_{\mathrm{i}} M_{\mathrm{i}} + ne = 0, \tag{2.4}$$

where M_{i} is the reaction substance, ν_{i} is the chemical quantity of substance i in the reaction, and n is the number of electrons participating in the reaction.

The reaction achieves an equilibrium condition when the sum of electrochemical potentials of the all reacting substances in the electrochemical reactions is zero:

$$\nu_{\mathrm{i}} \bar{\mu}_i = 0, \tag{2.5}$$

where $\bar{\mu}_i$ is the electrochemical potential of substance i.

or

$$\varphi = \varphi^0 + \frac{RT}{nF} \sum \nu_{\mathrm{i}} \ln a_{\mathrm{i}}, \tag{2.6}$$

in which,

$$\varphi^0 = \frac{\sum \nu_{\mathrm{i}} \mu_{\mathrm{i}}^0}{nF}, \tag{2.7}$$

where φ is the absolute potential of the electrochemical reaction, φ^0 is the standard potential of

electrochemical reaction, μ_i^0 is the standard chemical potential of substance *i*, a_i is the activity of substance *i*, that represents the effective concentration of substance *i* in the electrochemical reaction, *R* is the molar gas constant, *T* is the thermodynamic temperature, and *F* is the Faraday constant.

Equations (2.1) and (2.2) describe the anodic oxidation of SiC and generation of amorphous silicon dioxide. Beside SiC anodic oxidation, many other chemical reactions are present, such as the electrolysis of water, chemical reactions between products and water, ionization of substances, and so on. Substances that are taken into consideration in the anodic oxidation system of SiC and their standard free energy are shown in Table 2.1.

Twelve reactions were taken into consideration, and their equilibrium conditions were calculated by Equations (2.6) and (2.7), as shown in Table 2.2. With all equilibrium conditions plotted in one graph, we can obtain the potential-pH equilibrium diagram (Pourbaix diagram), as shown in Figure 2.12. Based on the figure, the anodic oxidation of SiC occurs before the electrolysis of water, which indicates that such process in aqueous solutions is possible. Besides, when the pH of the electrolyte is lower than 10, the oxide layer exists in the form of solid silicon dioxide (SiO_2) with a weak dissolution in water. Therefore, although it is easier to oxidize SiC in strong alkaline electrolytes, such electrolytes should not be used for the anodic oxidation of SiC

Table 2.1 Standard free energy of formation of a given substance [54)]

State	Chemical signal	Standard free energy (kJ/mol)
Solution	H_2O	-237.3
	H^+	0
	OH^-	-157.37
	HCO_3^-	-587.32
Solid	SiC	-109.25
	SiO_2	-786.14
	C	0
Gas	H_2	0
	O_2	0
	CO	-137.34
	CO_2	-394.56
Dissolved substance	H_2SiO_3	-1012.98
	$HSiO_3^-$	-955.88
	SiO_3^{2-}	-887.4

Table 2.2 Equilibrium condition for reactions in anodic oxidation of SiC

Number	Reaction	Equilibrium condition
a	$2H^+ + 2e \leftrightarrow H_2(g)$	$\varphi = -0.0591pH$
b	$4H^+ + 4e + O_2 \leftrightarrow 2H_2O$	$\varphi = 1.229 - 0.0591pH$
1	$SiC + 4OH^- + 4h^+ \leftrightarrow SiO_2 + 2H_2O + C$	$\varphi = -0.5250 - 0.0591pH$
2	$SiC + 6OH^- + 6h^+ \leftrightarrow SiO_2 + 3H_2O + CO(g)$	$\varphi = -0.1777 - 0.0591pH$
3	$SiC + 8OH^- + 8h^+ \leftrightarrow SiO_2 + 4H_2O + CO_2(g)$	$\varphi = -0.1592 - 0.0591pH$
4	$SiO_2 + H_2O \leftrightarrow H_2SiO_3$	$\log(H_2SiO_3) = -1.84$
5	$SiO_2 + H_2O \leftrightarrow HSiO_3^- + H^+$	$\log(HSiO_3^-) = -11.84 + pH$
6	$SiO_2 + H_2O \leftrightarrow SiO_3^{2-} + 2H^+$	$\log(SiO_3^{2-}) = -23.84 + 2pH$
7	$H_2SiO_3 \leftrightarrow HSiO_3^- + H^+$	$\log\frac{(HSiO_3^-)}{(H_2SiO_3)} = -10 + pH$
8	$HSiO_3^- \leftrightarrow SiO_3^{2-} + H^+$	$\log\frac{(SiO_3^{2-})}{(HSiO_3^-)} = -12 + pH$
9	$H_2O \leftrightarrow H^+ + OH^-$	$pH = 7$
10	$H_2O + CO_2 \leftrightarrow HCO_3^- + H^+$	$pH = 8 + \log a_{HCO_3^-}$

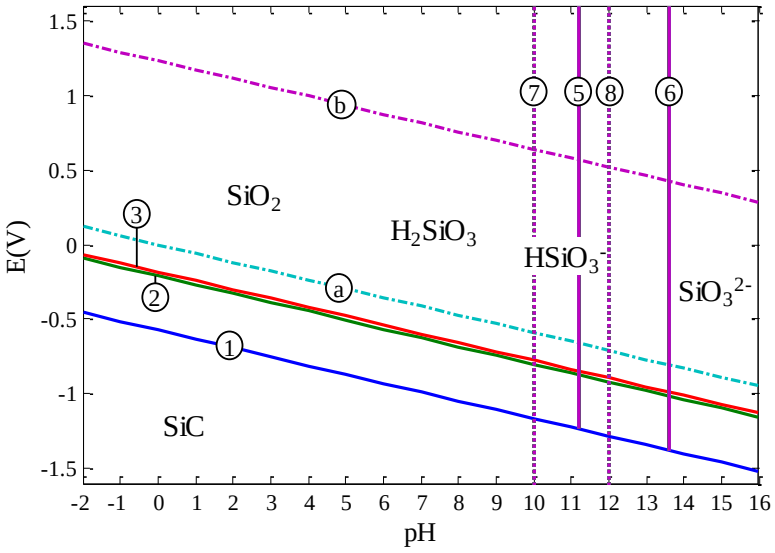

Figure 2.12 Potential-pH equilibrium diagram for the SiC–water system.

as it may cause the etching, not mechanical removal, of the oxide layer, which does not ensure the flattening of the SiC surface. By contrast, anodic oxidation of the SiC in neutral electrolytes is easier than in acid electrolytes, and also ensures the mechanical removal of the oxide layer.

Furthermore, the cost of the electrolytes, waste disposal of the electrolytes, and maintenance of the polishing machine can be significantly reduced and simplified.

2.4.7 Pourbaix diagram of SiC in chloride (Cl^-) aqueous solution

Chlorine neutral salt is a very common substance in our daily life, aside from it being very inexpensive. Figure 2.13 shows the potential-pH equilibrium diagram for the chlorine–water system [55]. Apparently, Cl_2 may be generated by the anodic oxidation of chloride ions (Cl^-) when the pH is low, while ClO_4^- would be generated in the case of a high pH; nonetheless, water electrolysis would preferentially occur due to the system's lower equilibrium potential. These results show that chloride aqueous solution can be used for the anodic oxidation of SiC surface.

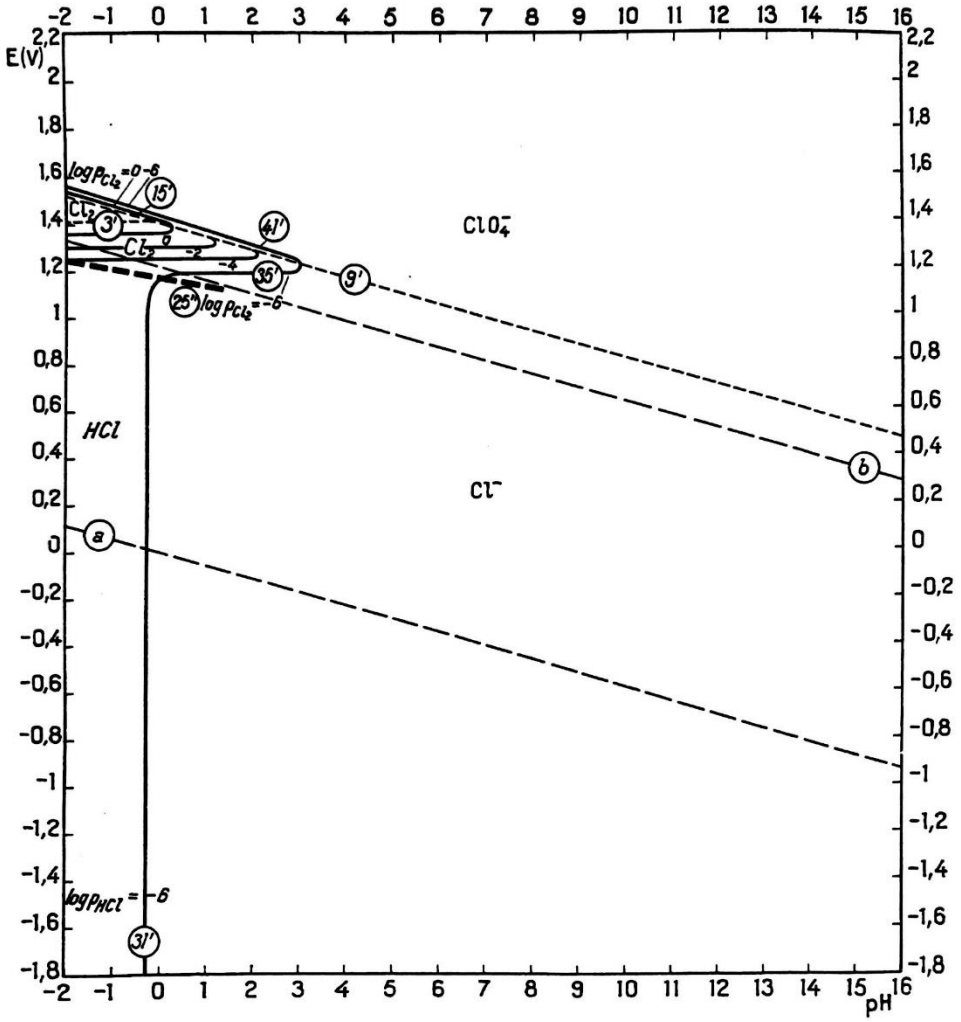

Figure 2.13 Potential-pH equilibrium diagram for the system chlorine–water, at 25 °C [55].

2.4.8 Pourbaix diagram of SiC in nitrate (NO_3^-) aqueous solution

Nitrate solutions were also investigated for the application of electrolyte. Figure 2.14 shows the potential-pH equilibrium diagram for the nitrogen–water system [55]. When a relatively high potential is applied, NO_3^- would not change and remain intact instead, although there are many reactions present when anodizing at a low potential. Because the equilibrium potential of these reactions is lower than that of SiC, the anodic oxidation of SiC also preferentially occurs, where the use of nitrate as electrolyte is possible.

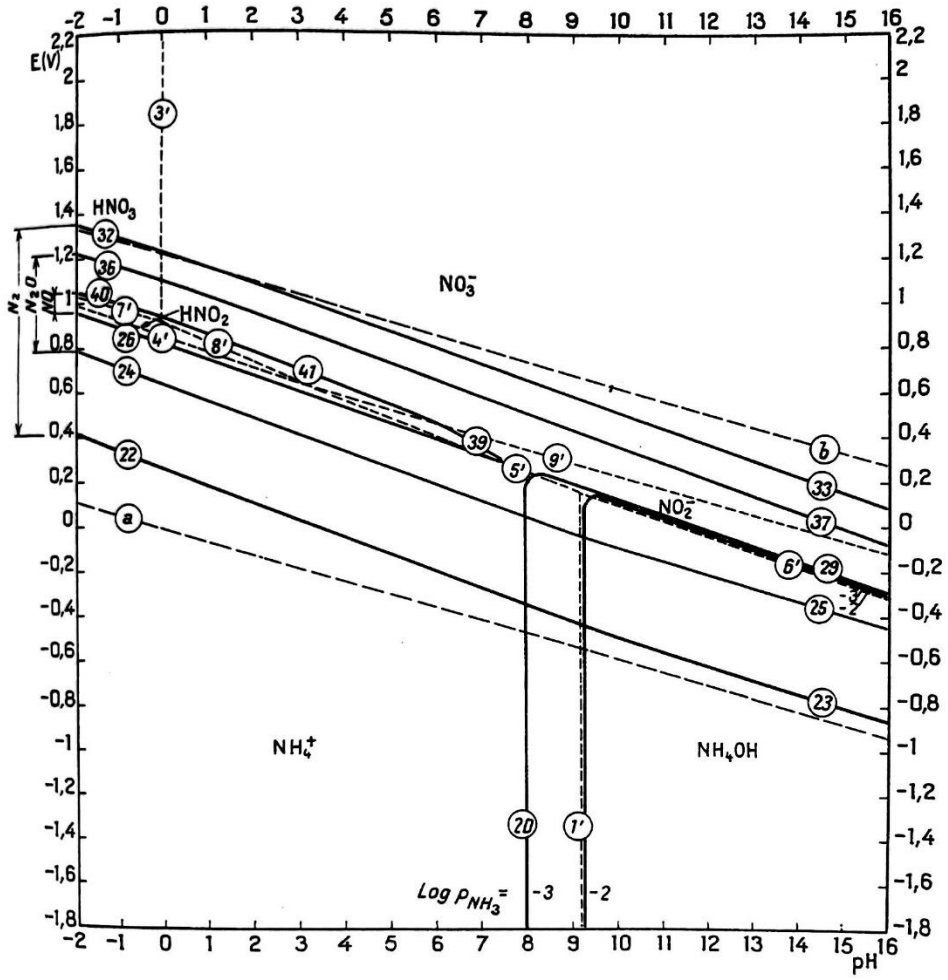

Figure 2.14 Potential-pH equilibrium diagram for the nitrogen–water system, at 25 °C [55].

2.5 Summary

For realizing a highly-efficient, low cost, and damage-free polishing and flattening of SiC wafer, a review of the existing manufacturing processes and polishing techniques of SiC wafers was conducted and the advantages and disadvantages of the polishing techniques were summarized.

Slurryless ECMP was proposed as a solution to solve the problems in these polishing techniques, and to simplify the manufacturing process of SiC wafers. The feasibility of applying neutral electrolytes to slurryless ECMP was also examined. The results of this chapter are summarized as follows.

(1) At present, the manufacturing process of SiC wafer is very complex, and current polishing techniques are unable to simplify it. In general, these techniques cannot realize a highly-efficient, low-cost, and damage-free polishing of SiC wafers: some have low efficiency, some are very costly, and some have insufficient precision. These issues necessitate the development of a new polishing technique.

(2) ECMP using slurry does not produce a flat and atomically smooth surface. In addition, the application of loose abrasive in slurry ECMP make it very difficult to separately control the anodic oxidation and polishing parameters, thereby limiting the polishing performance.

(3) The proposed slurryless ECMP combines surface modification and fixed-abrasive polishing. By this method, the SiC surface is first modified by anodic oxidation, and then the modified layer is removed by fixed soft abrasives. As the abrasive is much softer than SiC, only the modified layer is removed to achieve a damage-free surface. The SiC surface can also be flattened with the fixed-abrasive polishing, eventually leading to an atomically flat and smooth surface.

(4) The possibility of using neutral electrolytes to the slurryless ECMP of SiC wafer was also examined. Here, the equilibrium condition of reactions in the anodic oxidation system of SiC was calculated, and Pourbiax diagram of SiC was obtained. On the basis of the Pourbiax diagram of SiC, chlorine and nitrate solutions were found possible to be used as electrolyte for the anodic oxidation of SiC.

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Chapter 3
Anodic oxidation property and mechanism of 4H-SiC (0001) surface

3.1 Introduction

In slurryless ECMP, the SiC surface is firstly modified by anodic oxidation, and then the modified layer is removed by fixed soft abrasives. Because the abrasive hardness is much lower than that of SiC, only the oxide layer is removed by the soft abrasives. Therefore, it is important to conduct an investigation of the anodic oxidation properties of SiC and clarify the mechanism behind in obtaining a flat and smooth surface by slurryless ECMP. This chapter investigates the effects of anodizing parameters on the anodic oxidation performance of SiC, as well as the accompanying mechanism.

3.2 Anodic oxidation setup

The anodic oxidation setup (Model K0235 Flat Cell supplied by Princeton Applied Research) especially developed to straightforwardly investigate the anodic oxidation mechanism is displayed in Figure 3.1. This three-electrode system consists of a WE (SiC substrate), a RE (Ag|AgCl), and a CE (platinum mesh), together with a potentiostat for controlling the oxidation parameters and for measuring changes in the current and potential during the oxidation process. Commercially available single-crystal 4H-SiC substrates (on-axis, N-type) finished by CMP with a thickness of approximately 341 μm and specific resistance range of 0.015–0.028 Ω·cm supplied by TankeBlue Semiconductor Co. Ltd. were used. Before the anodic oxidation, contamination and native oxides on the SiC substrates were removed by wet chemical cleaning. First, the substrates were dipped into a solution of H_2SO_4 (97 wt%) and H_2O_2 (34 wt%) with a volume ratio of 4:1 for 10 min. Next, they were dipped into concentrated hydrofluoric acid (HF) solution (50 wt%) for 10 min, followed by rinsing with deionized water for another 10 min. Finally, the substrates were blow-dried with pure N_2 gas. All experiments were conducted on the 4H-SiC (0001) face, which is the most commonly used face for power device applications. Oxidation region of the SiC surface assumed a circular shape with an area of 1 cm^2. If not specified, all the anodic oxidation experiments in this chapter were conducted using this anodic oxidation setup.

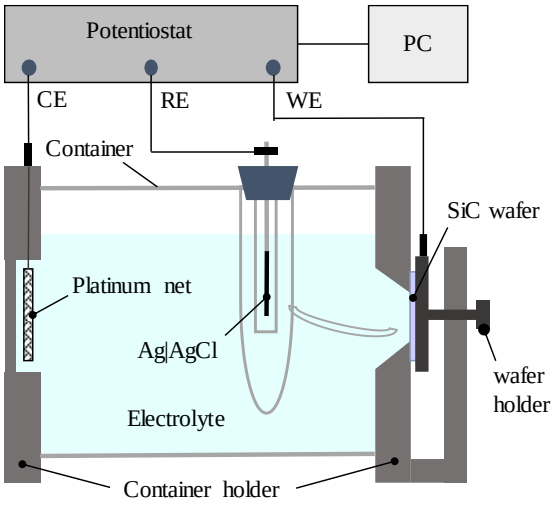

Figure 3.1 Anodic oxidation setup.

3.3 Anodic oxidation of 4H-SiC (0001) surfaces in neutral electrolytes

In Chapter 2, the possibility of applying chloride and nitrate aqueous solutions as electrolyte was examined through a presented Pourbaix diagram. Anodic oxidation experiments were done to verify the possibility, with conditions given in Table 3.1. Specifically, the electrolytes used were NaCl and $NaNO_3$ aqueous solutions with a molar concentration of 0.2 mol/L. CMP-processed 4H-SiC (0001) surfaces were anodically oxidized in both electrolytes at a potential of 9 V for 1, 5, and 10 min respectively. Figure 3.2(a) shows the electric conductivity (EC) of the two electrolytes, in which, although the NaCl solution has greater EC than the $NaNO_3$ solution, the difference is very small. Figures 3.2(b) to (d) show the changes in current during anodic oxidations in these two types of electrolyte. A slight difference appeared during the initial oxidation stage of the SiC surfaces, which disappeared after oxidation for about 1 min. The differences in the initial oxidation stage were presumed to be caused by the differences in the SiC surface, i.e., surface damage, defects, and so on. After the surface was oxidized, such differences disappeared.

Table 3.1 Anodic oxidation conditions

Electrolyte	Molar concentration (mol/L)	Oxidation potential (V)	Oxidation time (min)
NaCl	0.2	9	1, 5, 10
$NaNO_3$	0.2	9	1, 5, 10

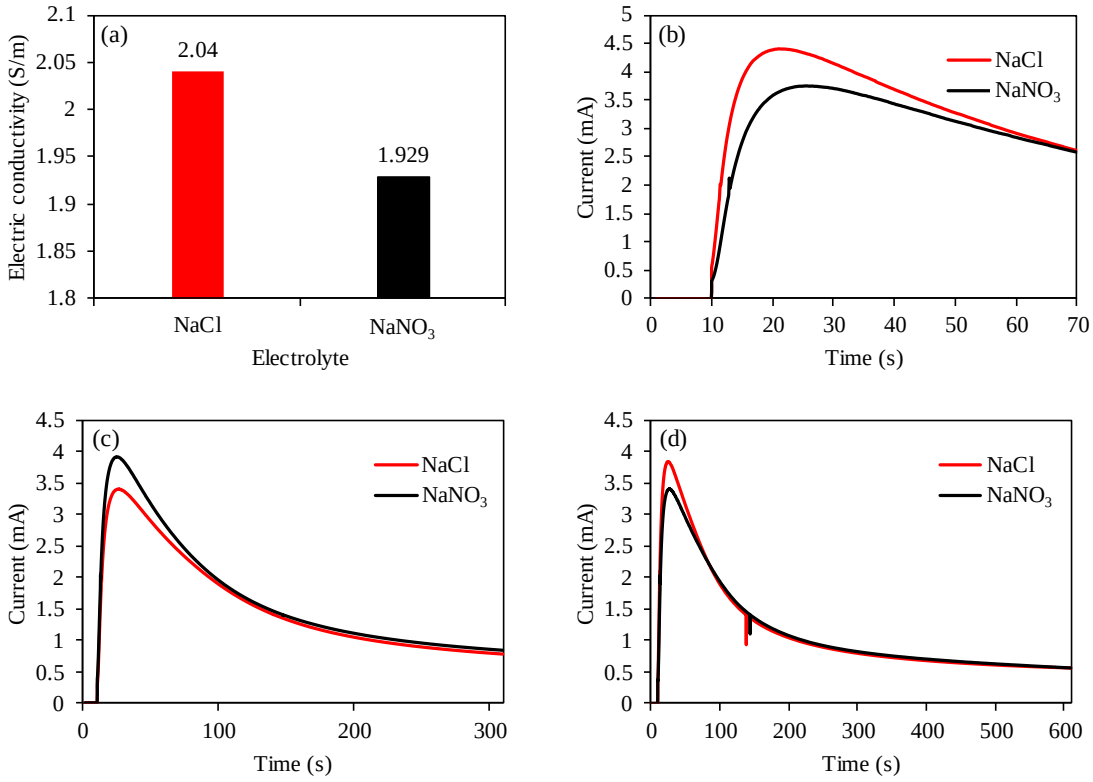

Figure 3.2 Comparison of NaCl and $NaNO_3$ in anodic oxidation of SiC surface. (a) Electric conductivity of 0.2 mol/L NaCl and $NaNO_3$ aqueous solutions, changes in current during anodic oxidation of SiC surface in NaCl and $NaNO_3$ aqueous solution for (b) 1, (c) 5, and (d) 10 min.

Figure 3.3 shows the X-ray photoelectron spectroscopy (XPS) measurement results of the oxidized surfaces at a take-off angle of 45º. Strong peaks corresponding to Si-C bonds were observed in both Si 2p and C 1s spectra in the measurement of as-received surface. In both NaCl and $NaNO_3$ aqueous solutions, after anodic oxidation at 9 V for 1 min, the peak corresponding to Si-C bonds was changed to Si-O bonds in Si 2p spectra, as shown in Figure 3.3(a). At the same time, the peak corresponding to Si-C bonds in C 1s spectrum disappeared after anodic oxidation, as shown in Figure 3.3(b). These results indicate that the SiC surfaces were oxidized to SiO_2 layer in both NaCl and $NaNO_3$ aqueous solutions. Thus, anodic oxidation of SiC in neutral aqueous solutions was realized.

Figure 3.4 shows the topographies of the surfaces oxidized in both electrolytes. After anodic oxidation, many protrusions were generated on the oxidized surface. With the progress of the anodic oxidation, the number of the oxide protrusions increased. In the anodic oxidation of SiC, SiC was changed to SiO_2, and the amount of generated SiO_2 became equal to that of SiC. The molar mass of SiO_2 was 60 g/mol, larger than the 40 g/mol of SiC; reversely, the density of SiC

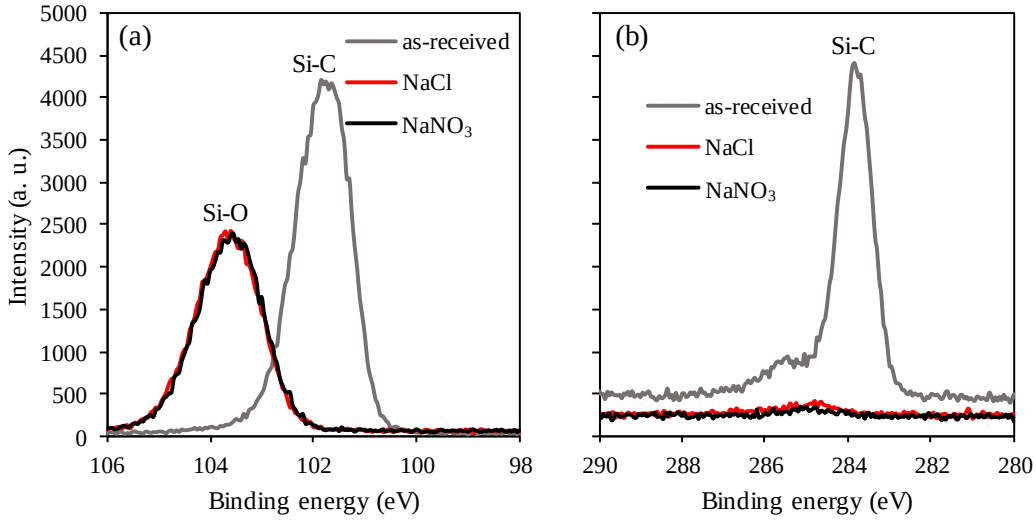

Figure 3.3 XPS measurement results of surface oxidized in NaCl and $NaNO_3$ aqueous solutions at 9 V for 1 min (take-off angle: 45°). (a) Si 2p spectra. (b) C 1s spectra.

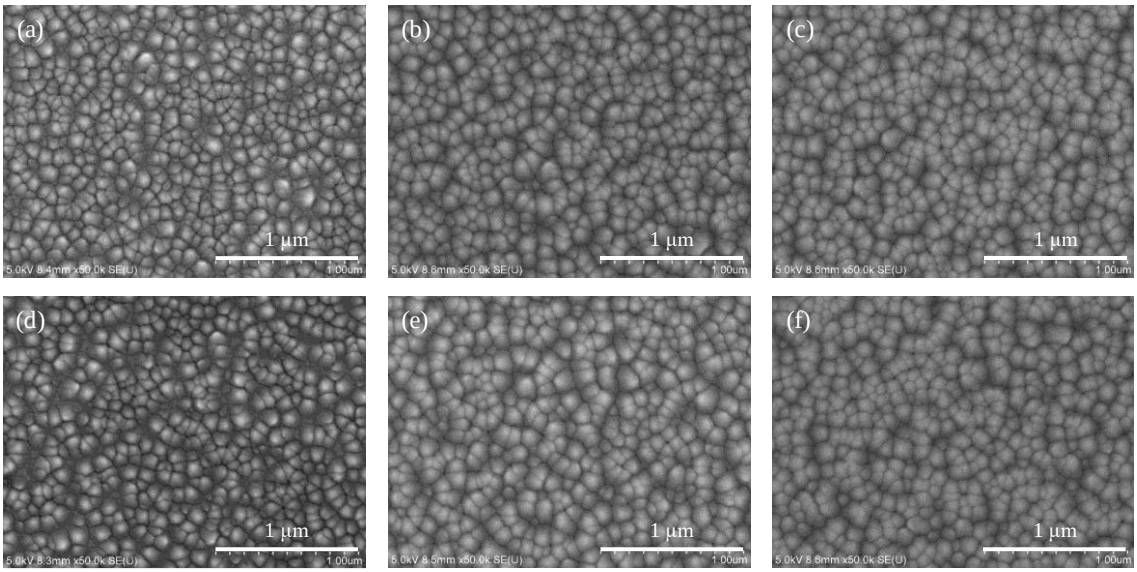

Figure 3.4 SEM images of SiC surfaces oxidized at 9 V in NaCl aqueous solution for (a) 1, (b) 5, and (c) 10 min; and in $NaNO_3$ aqueous solution for (d) 1, (e) 5, and (f) 10 min.

was 3.2 g/cm^3, the density of SiO_2 generated in anodic oxidation was smaller than that of quartz glass (2.32 g/cm^3) owing to its amorphous structure, which was about 1.65 g/cm^3 [1)]; thus, the volume of SiC increased upon oxidization to SiO_2. Moreover, the oxide protrusions were associated with the oxidized sites on the surface, which show the uneven oxidation of the surface. Differences in the topographies of the oxidized surfaces in NaCl and $NaNO_3$ aqueous solutions were not observed.

Subsequently, the oxidized surfaces were dipped into 50 wt% HF solutions for removal of the oxide layer. The oxidation depths were observed by scanning white light interferometer (SWLI), as shown in Figure 3.5(a). A SWLI image of the SiC surface oxidized for 10 min in NaCl and $NaNO_3$ aqueous solutions after removal of the oxide layer is shown in Figure 3.5(b), where the oxidized/etched surfaces were clearly lower than the as-received surface. From a cross-sectional view along A–B in Figure 3.5(c), oxidation depths of 138.69 and 131.72 nm were confirmed on the oxidized surfaces obtained in NaCl and $NaNO_3$ aqueous solutions, respectively. To make the oxidation depth accurate, oxidation depths were measured on the upper, lower, left, and right regions of the circular oxidation area, and the average of these depths was taken as the oxidation depth of the entire circle oxidation area. The measurement results are shown in Figure 3.6(a), which apparently shows the increase in oxidation depth with longer oxidation time. Meanwhile, the differences in oxidation depths obtained in NaCl and $NaNO_3$ aqueous solutions were very small, and showed the same trend with the differences in current shown in Figure 3.4. This result indicates that the anodic oxidation rate is dominated by the oxidation current.

SiC oxidation valences (z_{SiC}) in the two f electrolytes were calculated for further comparison of the oxidation performance of NaCl and $NaNO_3$ aqueous solutions. Specifically, the SiC oxidation valences

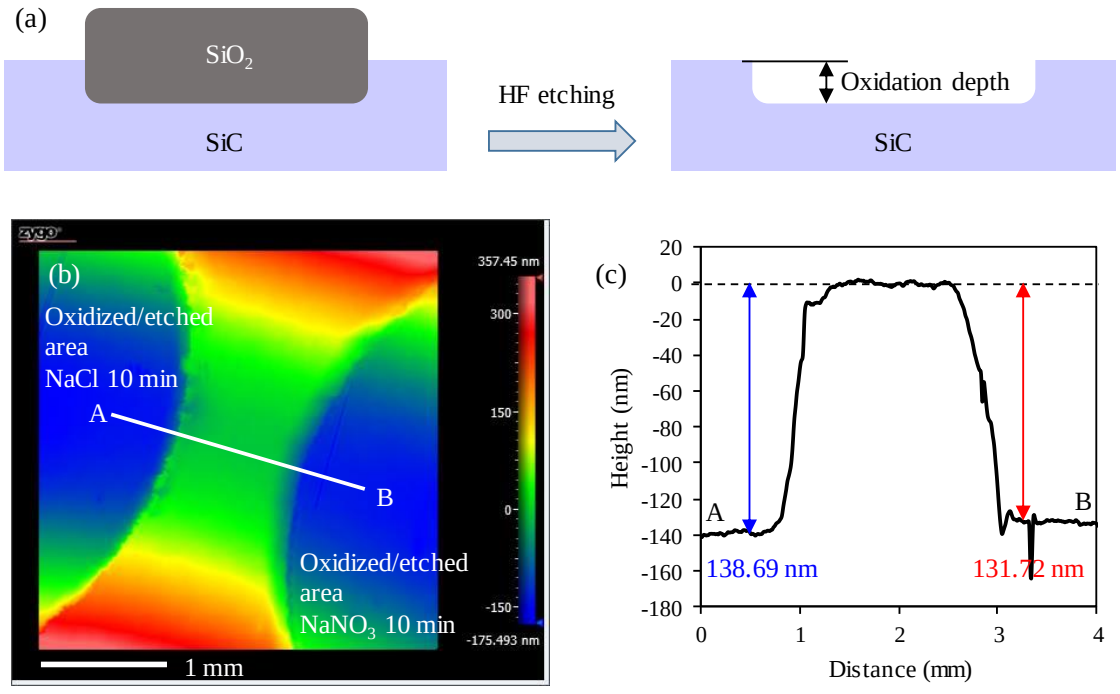

Figure 3.5 Measurement of anodic oxidation depth. (a) Definition of oxidation depth. (b) SWLI image of SiC surface oxidized for 10 min after removing the oxide layer. (c) Cross-sectional view along A–B in (b).

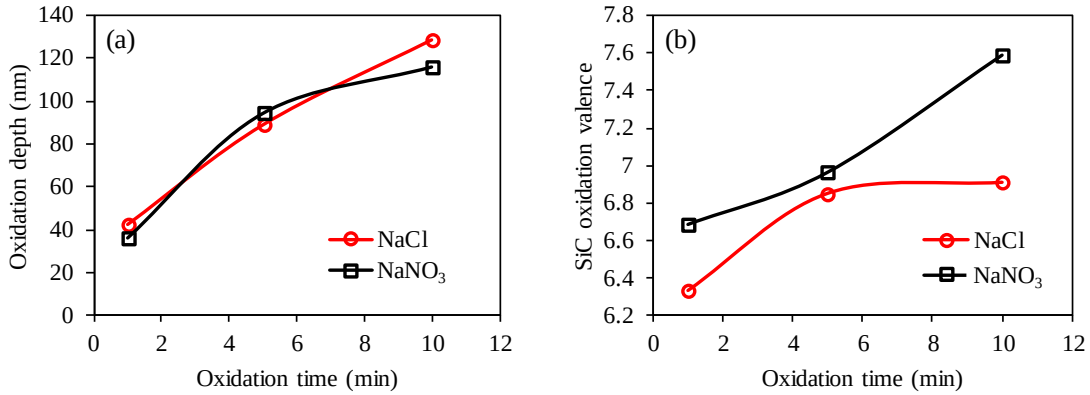

Figure 3.6 (a) Relationship between oxidation depth and oxidation time in NaCl and $NaNO_3$ aqueous solutions. (b) Oxidation valences of SiC in the anodic oxidations with NaCl and $NaNO_3$ aqueous solutions.

(z_{SiC}) was defined as the ratio of the number of consumed elementary charges N_e to the number of oxidized SiC molecules N_{SiC}. It was expressed as

$$z_{SiC} = \frac{N_e}{N_{SiC}} = \frac{Q/F}{\rho S d/M}, \tag{3.1}$$

where Q is the amount of charge that passed in the anodic oxidation process, F is the Faraday's constant, ρ is the density of SiC, S is the oxidation area, d is the oxidation depth, and M is the molar mass of SiC.

Equation (3.1) was employed for determining the SiC oxidation valences of the anodic oxidation experiments, as shown in Figure 3.6(b). In both anodic oxidations in NaCl and $NaNO_3$ aqueous solutions, an increasing trend of SiC oxidation valences was observed with increasing oxidation time. This phenomenon was presumably a result of an increase in the barrier effect of the oxide layer with longer oxidation time. By contrast, it was clear that the SiC oxidation valences in the anodic oxidation with NaCl aqueous solution was always smaller than that of $NaNO_3$ aqueous solution.

After oxide removal via HF etching, the surface became very rough, as shown in Figure 3.7. A large number of etch pits corresponding to the oxide protrusions [2)] were distributed on the surface and significantly increased the surface roughness. The surface roughness result of this experiment is displayed in Figure 3.8. Note that after anodic oxidation and HF etching, the surface roughness significantly increased, but the difference between surfaces oxidized by NaCl and $NaNO_3$ aqueous solutions were not clear. Because of the greater efficiency of electric energy in NaCl aqueous solution than in $NaNO_3$ aqueous solution, NaCl was used as electrolyte in the investigation that follows.

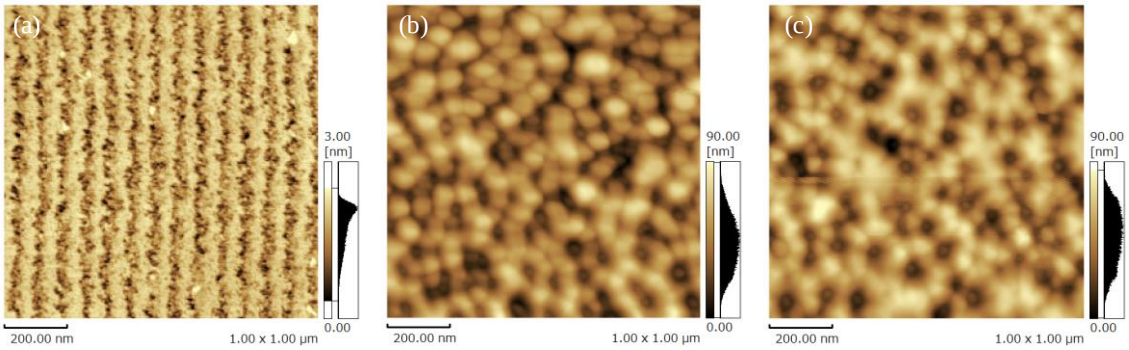

Figure 3.7 AFM images of surfaces after removal of the oxide layer by HF etching. (a) As-received CMP-processed surface. Surfaces oxidized in (b) NaCl and (c) $NaNO_3$ aqueous solutions for 1 min after removal of the oxide layer by HF etching.

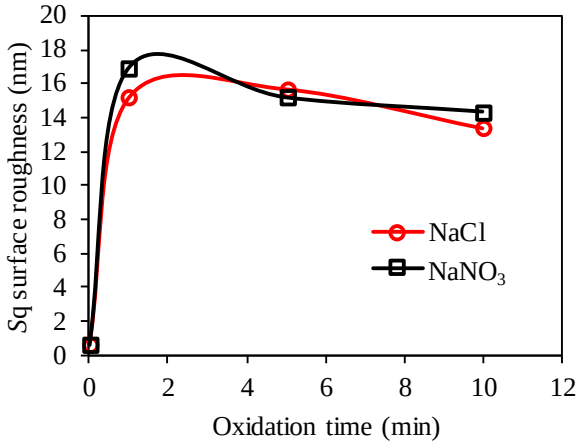

Figure 3.8 Comparison of the surface roughness obtained by anodic oxidation in NaCl and $NaNO_3$ solutions after removal of the oxide layer by HF etching.

During the ECMP process, anodic oxidation softens the SiC surface, enabling the surface to be polished by a soft abrasive, such as CeO_2. Nanoindentation tests were conducted on the surfaces of as-received SiC (CMP polished), synthetic quartz glass, borosilicate glass, and anodically oxidized SiC for comparison of their surface hardness. The typical load–displacement curves of these four surfaces measured by the nanoindentation method are presented in Figure 3.9(a). Here, a Berkovich-type indenter made of diamond was used, and the surface hardness was calculated by the Oliver–Pharr method [3]. Figure 3.9(b) shows the results of the nanoindentation tests calculated from the load–displacement curves. Interestingly, after anodic oxidation, the surface hardness of SiC significantly decreased from 41.98 to 3.59 GPa. Although the anodic oxide layer was of synthetic quartz glass and borosilicate glass mainly composed of SiO_2, the anodically

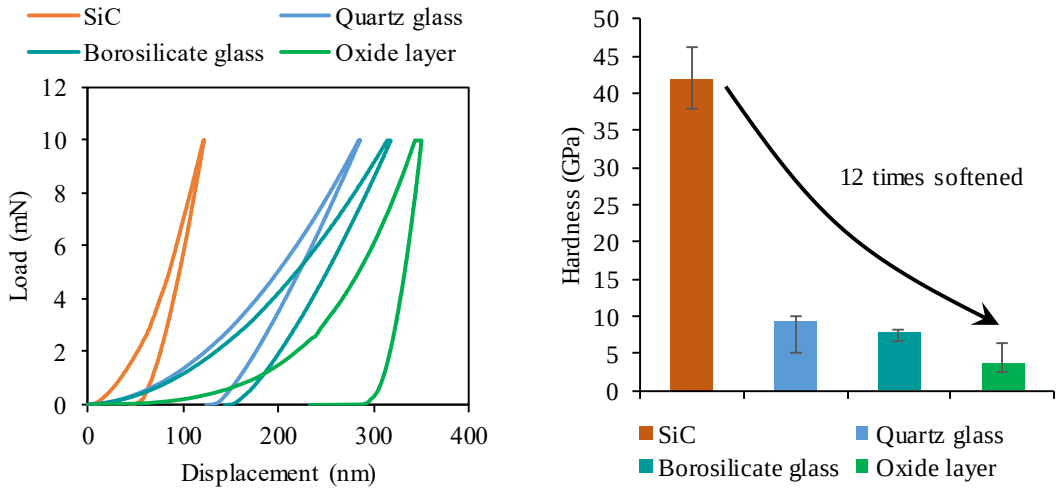

Figure 3.9 Hardness of various materials measured by nanoindentation method. (a) Load–displacement curves. (b) Hardness calculated from data (a).

oxidized SiC surface was found to be softer than these glass types. Thus, anodic oxidation was confirmed very useful for the surface softening of SiC.

3.4 Anodic oxidation properties of 4H-SiC (0001) surface

3.4.1 Potential dependence

Linear sweep voltammetry (LSV) was employed to investigate the relationship between the oxide protrusions and the oxidation potential. The oxidation setup is shown in Figure 3.1. Here, the oxidation potential was accurately controlled by referring to an Ag|AgCl electrode. Figure 3.10 shows the LSV result for a 4H-SiC substrate obtained at a scanning rate of 5 mV/s with an oxidation potential of 0 to 9.8 V; the inset shows an enlargement of the graph from 0 to 5 V. The result revealed an *I–V* curve similar to that for general metal anodization with five oxidation periods [4], a–b (0–1.9 V): unoxidized state; b–c (1.9–2.4 V): active state; c–d (2.4–3.5 V): passive state; d–e (3.5–6.0 V): transient state; and e–f (6–9.8 V): transpassive state. This indicates that anodic oxidation occurs when the potential is larger than 1.9 V, that a passive film inhibits the oxidation between 1.9 and 3.5 V, and that the breakdown of the passive film occurs when the potential is larger than 3.5 V.

An anodic oxidation experiment was conducted to verify the result by the LSV. SiC substrates were anodically oxidized at potentials of 1 (unoxidized state), 3 (passive state), 5 (transient state), and 7 and 9 V (transpassive state) for 2 min, as shown in Table 3.2. The oxidized surfaces were then observed by AFM. Figure 3.11 shows the changes in the oxidation current during the

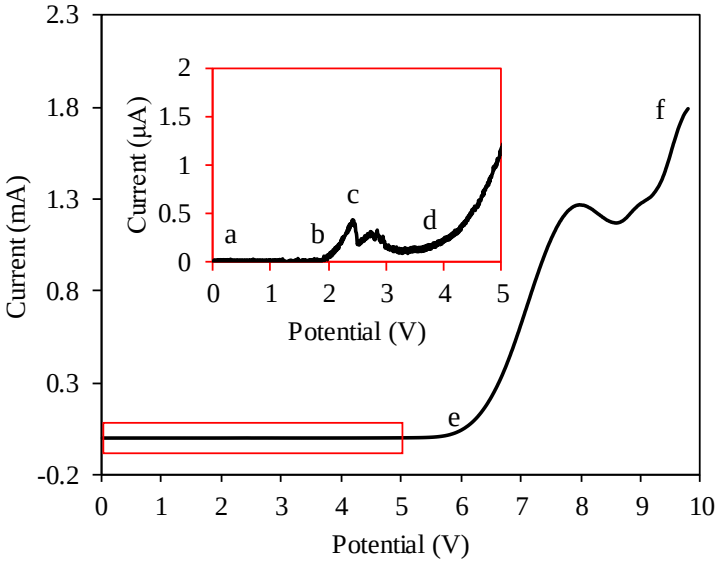

Figure 3.10 LSV result for 4H-SiC in 1 wt% NaCl solution with a scanning rate of 5 mV/s.

Table 3.2 Anodic oxidation of 4H-SiC (0001) surfaces with different potentials for 2 min

Experimental No.	①	②	③	④	⑤
Potential (V)	1	3	5	7	9

oxidation process. Oxidation did not occur at 1 V as no current flowed. The current decreased with increasing oxidation time at 3 V, which indicates that the oxidation was hindered by the passive film. The current first decreased with oxidation time, and then increased at 5, 7, and 9 V, indicating the breakdown of the passive film. These results are consistent with the LSV result.

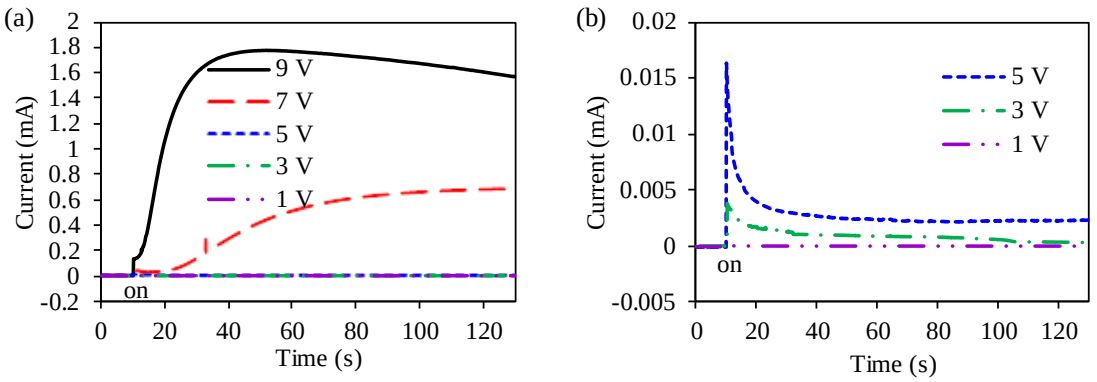

Figure 3.11 Changes in current at different oxidation potentials. (a) Overall view. (b) Enlargement of changes in current at 1, 3 and 5 V.

Figure 3.12 shows the surface morphologies before and after oxidation. It was found that the surface morphology hardly changed after oxidation at 1 V, whereas the terraces became smoother at 3 and 5 V, but no oxide protrusions were observed. Oxide protrusions were generated on the surface oxidized at 7 and 9 V. Since the changes of surface oxidized at 3 and 5 V were not clear, anodic oxidation experiments with longer times were conducted at 3 and 5 V to confirm the oxidation of the SiC surfaces. Figure 3.13 shows the topographies of SiC surfaces after oxidized at 3 V for 60 min and 5 V for 10 min. After anodic oxidation at 3 V for 60 min, the step-terrace structure disappeared but no oxide protrusions were generated, as shown in Figure 3.13(a), the surface roughness decreased after the anodic oxidation, which is attribute to the passivation of the surface. On the surface oxidized at 5 V for 10 min, many oxide protrusions were generated, as shown in Figure 3.13(b). Combining these phenomena with the LSV result, the oxide protrusions were generated by the breakdown of the passive film.

On the basis of the above results, the changes in current during the potential-controlled oxidation process, as shown in Figure 3.11, is better explained as follows. The initial decrease in the current was caused by the passivation of the surface. Further oxidation of the surface was

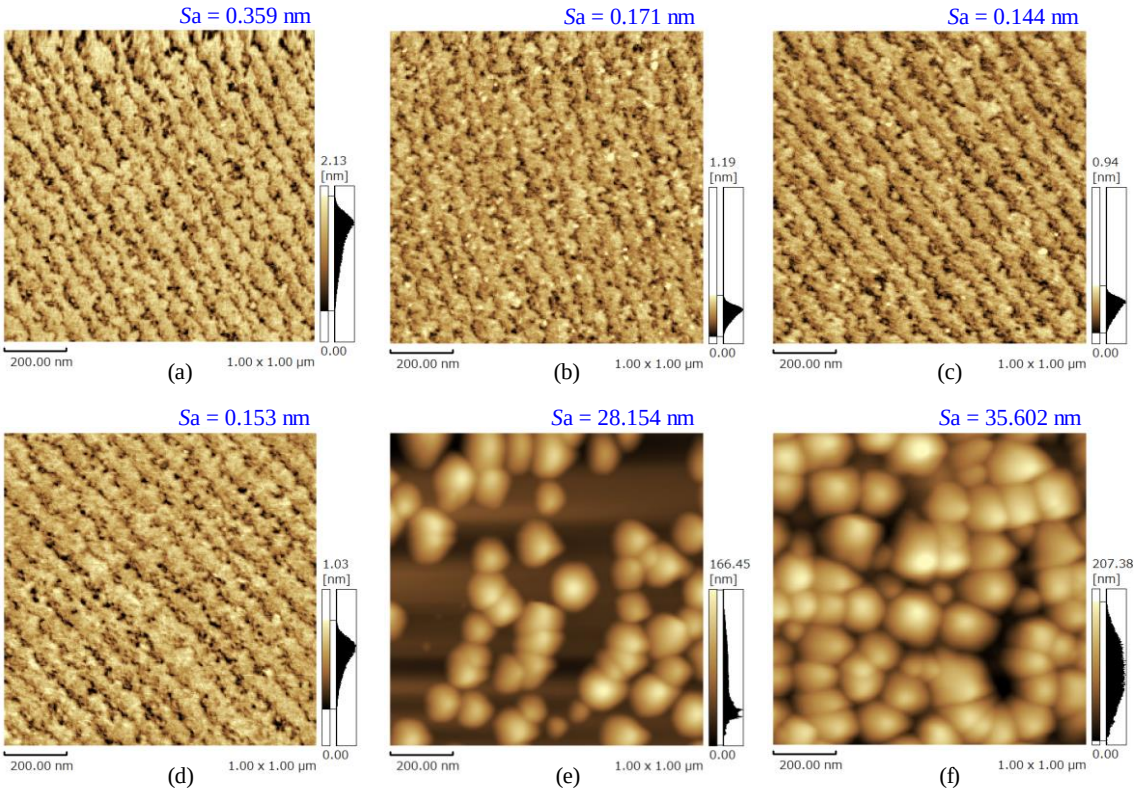

Figure 3.12 AFM images of surfaces oxidized in 1 wt% NaCl solution for 2 min at different potentials. (a) As-received. (b) 1 V. (c) 3 V. (d) 5 V. (e) 7 V. (f) 9 V.

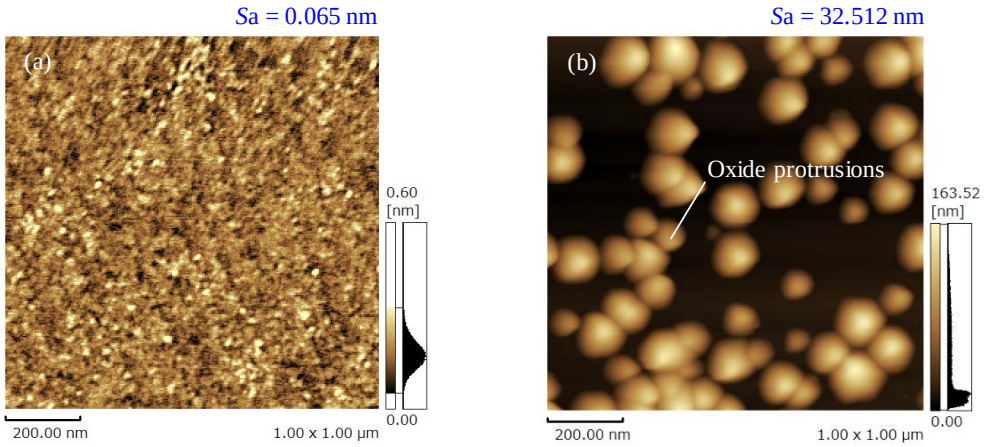

Figure 3.13 AFM images of surfaces oxidized in 1 wt% NaCl solution at (a) 3 V for 60 min, and (b) 5 V for 10 min.

hindered when the potential was 3 V, which was insufficient to break down the passive film. The initial decease in the current followed by the increase suggests the breakdown of the passive film followed by the growth of the oxide at the breakdown sites. The current subsequently decreased with the merging of the oxide protrusions, which occurred at 9 V.

3.4.2 Current dependence

To study the current dependence of anodic oxidation of the SiC surface, SiC surfaces were oxidized at the same charge of 60 mC for different currents of 5 µA, 50 µA, 100 µA, 1 mA, and 2 mA, as shown in Table 3.3. Figure 3.14 shows the AFM images of SiC surfaces oxidized with different currents. The amount of oxide should be the same for the same amount of charge on the basis of Faraday's laws of electrolysis, while the oxidation rate should be proportional to the current density according to Coulomb's law. It was found that the frequency and size of the oxide protrusions changed with the current density: the frequency of oxide protrusions decreased while their size increased with lower current density. Given the small AFM observation area of 1 µm ×

Table 3.3 Anodic oxidation of 4H-SiC (0001) surface with a constant charge of 60 mC at different current density

Experimental No.	①	②	③	④	⑤	⑥
Current density (mA/cm^2)	0.005	0.05	0.1	1	2	5
Oxidation time (min)	200	20	10	1	0.5	0.2
Electrolyte	1 wt% NaCl aqueous solution					

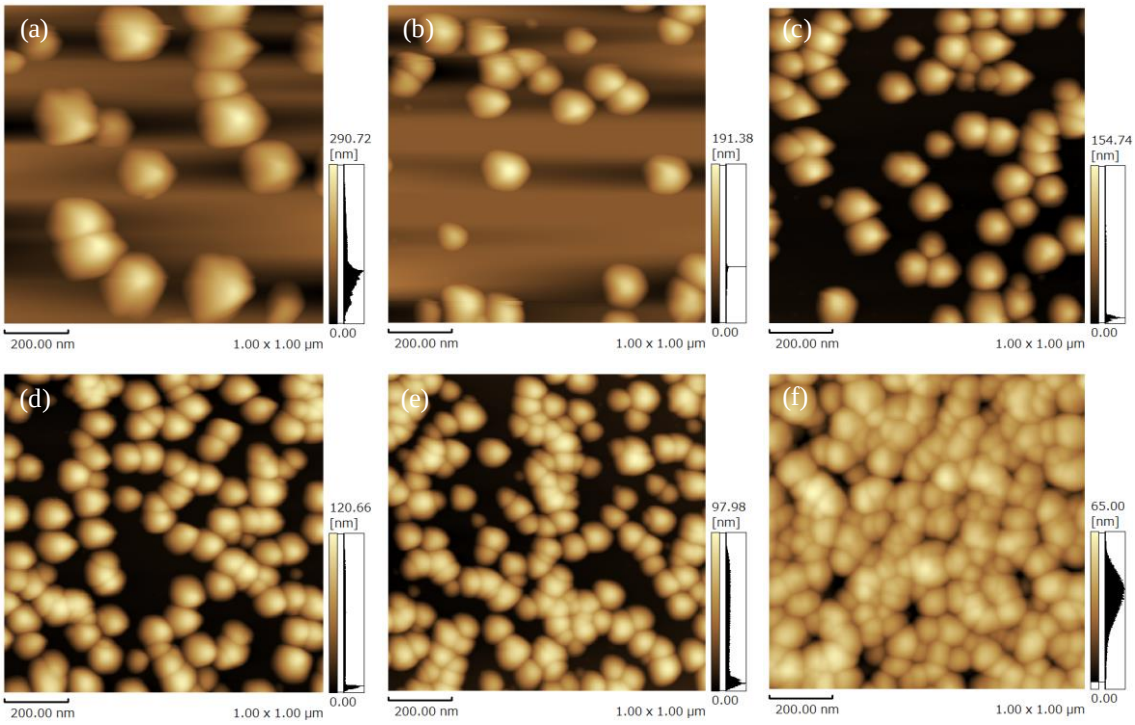

Figure 3.14 AFM images of oxidized SiC surfaces at the same charge of 60 mC with different currents. (a) 5 µA, 200 min. (b) 50 µA, 20 min. (c) 100 µA, 10 min. (d) 1 mA, 1 min. (e) 2 mA, 0.5 min. (f) 5 mA, 0.2 min.

1 µm (relative to the oxidation area of 1 cm^2), it was necessary to evaluate the distribution of the oxide protrusions on the entire oxidized surface after the anodic oxidation. For each specimen, 10 points uniformly distributed over the oxidation area were observed using AFM. The frequency, diameter, and volume of the oxide protrusions were statistically calculated using particle analysis software supplied by Shimadzu Corporation, as shown in Figure 3.15.

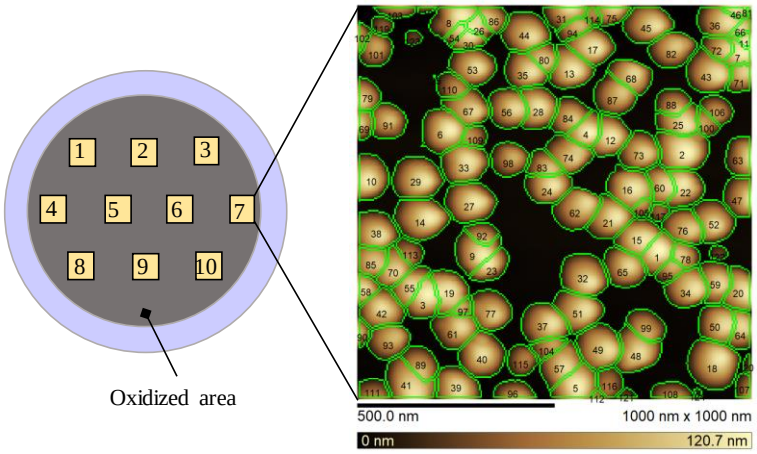

Figure 3.15 Analysis of oxide protrusions by particle analysis software.

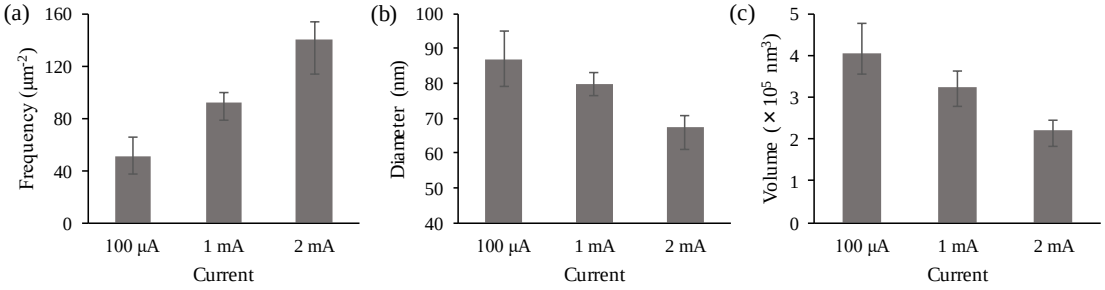

Figure 3.16 Relationship between the oxide protrusions and the oxidation current. (a) Frequency *vs.* oxidation current. (b) Diameter *vs.* oxidation current. (c) Volume *vs.* oxidation current.

The obtained average frequency, diameter, and volume of the oxide protrusions are given in Figure 3.16. Apparently, the frequency of oxide protrusions increased while the diameter and volume decreased, as the current increased. These results show that a relationship exists between the oxide protrusions (etch pits) and the oxidation current (potential). Oxidation of the scratches on these oxidized surfaces was observed via scanning electron microscopy (SEM), as shown in Figure 3.17. The scratch was completely oxidized when the current density was small; however, there was uneven oxidation of the place without the scratch and the area of the oxidized region was small. In contrast, when the current density was high, the areas other than the scratch region were oxidized to the same extent as the scratch. Moreover, oxidation in the place without scratch

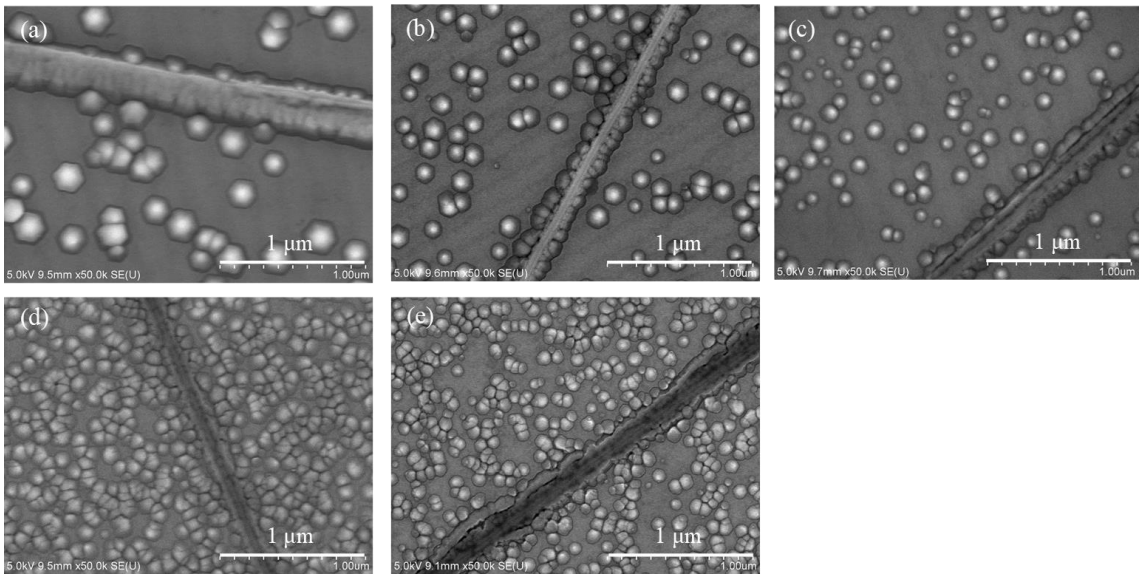

Figure 3.17 SEM images of SiC surfaces oxidized at the same charge of 60 mC with different currents a. (a) 5 μA, 200 min. (b) 50 μA, 20 min. (c) 100 μA, 10 min. (d) 1 mA, 1 min. (e) 2 mA, 0.5 min.

was not uniform, but surface oxidation was more uniform at a high current density compared to that at a low current density.

Figure 3.18 shows the changes in potential during the anodic oxidation of SiC surfaces with different currents. The potentials were firstly increased and then decreased with the increasing oxidation time, which is attribute to the passivation of the SiC surface and the breakdown of the passive film, respectively. Besides, a higher current was corresponding to a higher potential. With the breakdown of the passive film, many minor changes occurred in the potentials, these minor changes were more and larger at a higher current, while less and smaller at a lower current, as shown in Figures 3.18(c) to (e), which is corresponding to the frequency of the breakdown. In the anodic oxidation of N-type SiC, potential plays a decisive role in the formation of the space charge layer and the gathering of holes in the space charge layer, and the breakdown of the passive film

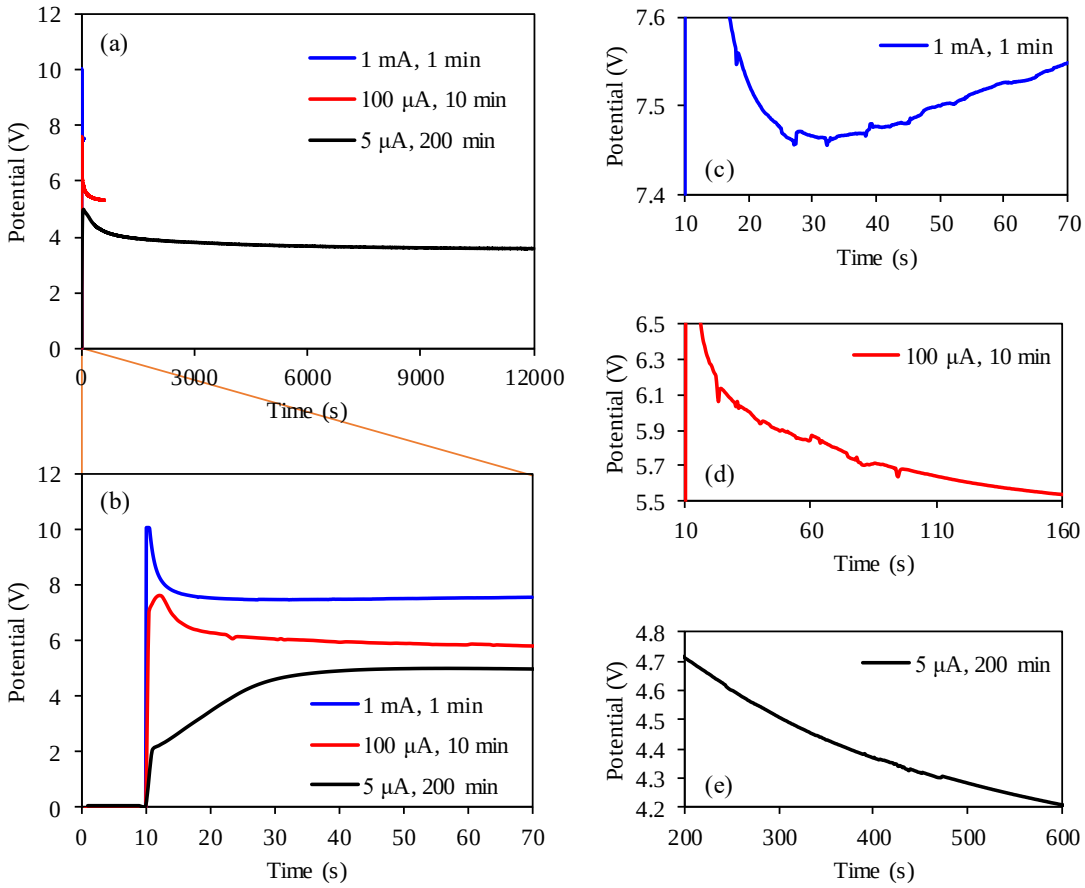

Figure 3.18 (a) Changes in potentials during the anodic oxidations of SiC surfaces with different currents. (b) Enlargement of the changes in potentials in the oxidation time of 1 min. Partially enlarged views of the changes in potentials in the anodic oxidations at (c) 1 mA for 1 min, (d) 100 µA for 10 min, and (d) 5 µA for 200 min.

is also directly related to the applied potential. Therefore, the differences in the anodic oxidation at different currents were attribute to the difference in the oxidation potential. Distribution of the space charge region on the SiC surface was more uniform under a higher potential, which resulted in a more uniform oxidation of the SiC surface.

Surface roughness of these oxidized surfaces after oxide removal by HF etching was evaluated, as shown in Figure 3.19. In Figure 3.19(b), although the *Sz* surface roughness of the surface oxidized at 2 mA/cm^2 increased compared to the current density of 1 mA/cm^2, the *Sz* surface roughness of the oxidized/etched surfaces decreased with an increase in oxidation current density. Figures 3.19(c) to (f) respectively show the AFM images and the cross-sectional views of the surfaces oxidized at the current of 5 μA and 2 mA after removal of the oxide. When the current density was low, the pits were less but deeper, as opposed to when the current density was high, wherein there were many but shallower pits. Based on the above results, it is considered that when the SiC is oxidized using a large current density, the surface oxidation area becomes large and the *Sz* surface roughness become low; thus, damage on the SiC surface can be more uniformly and efficiently removed.

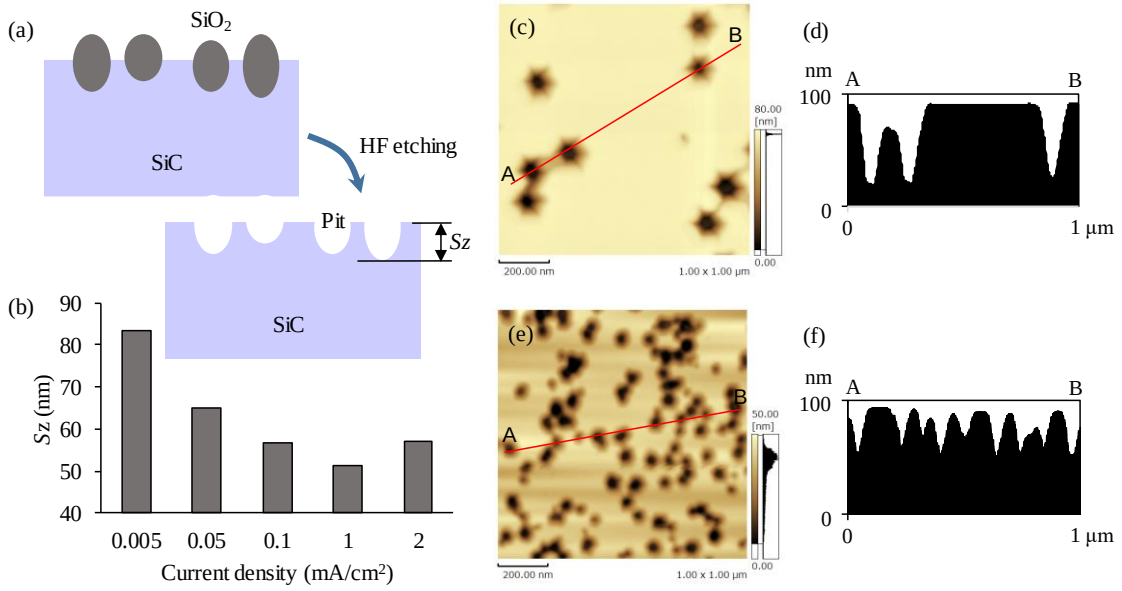

Figure 3.19 Evaluation of oxidized surface after removal of the oxide layer. (a) Schematic diagram of the oxide removal. (b) *Sz* surface roughness of surfaces oxidized with different current densities after removal of the oxide layer. (c) AFM image of surface oxidized at 5 μA after removal of the oxide layer. (d) Cross-sectional view of A–B in (c). (e) AFM image of surface oxidized at 2 mA after removal of the oxide layer. (f) Cross-sectional view of A–B in (e).

3.4.3 Time dependence

To study the time dependence of anodic oxidation, anodic oxidations of 4H-SiC (0001) surfaces at a constant potential of 9 V with different oxidation times from 1 to 600 min were conducted, as shown in Table 3.4. Evaluation method of the oxidation depth was as shown in Figure 3.5. This method was employed to evaluate the oxidation depths of different oxidation times, as depicted in Figure 3.20(a). Note that the oxidation depth increased as oxidation time increased; the rate of increase can be divided into three periods, namely, 1–10, 10–180, and 180–600 min. Oxidation depths grew rapidly at oxidation time lower than 10 min, while it slightly decreased at oxidation time greater than 10 min but less than 180 min. The growth rate further decreased as the oxidation time exceeded 180 min; nonetheless, growth in oxidation depth continued with increasing oxidation time.

The rapid increase in oxidation depth in initial oxidation stage was attributed to the rapid oxidation of the surface damage, as shown in Figures 3.21(a) and (b). The topographies of the oxide layers still exhibited the same pattern of the diamond-lapped surface, which shows the preferential oxidation of surface damage. Further oxidation of the surface after 10 min was attributed to the porosity of the oxide layer [5-6], wherein cracks generated during the growth of the oxide layer, as shown in Figures 3.21(d) to (h). Specifically, cracks generated after the surface was oxidized for 30 min, as shown in Figure 3.21(d), and expanded beyond that, causing some

Table 3.4 Anodic oxidation of 4H-SiC (0001) surfaces at 9 V with different oxidation times

Experimental No.	①	②	③	④	⑤	⑥	⑦	⑧
Oxidation time (min)	1	5	10	30	60	180	300	600

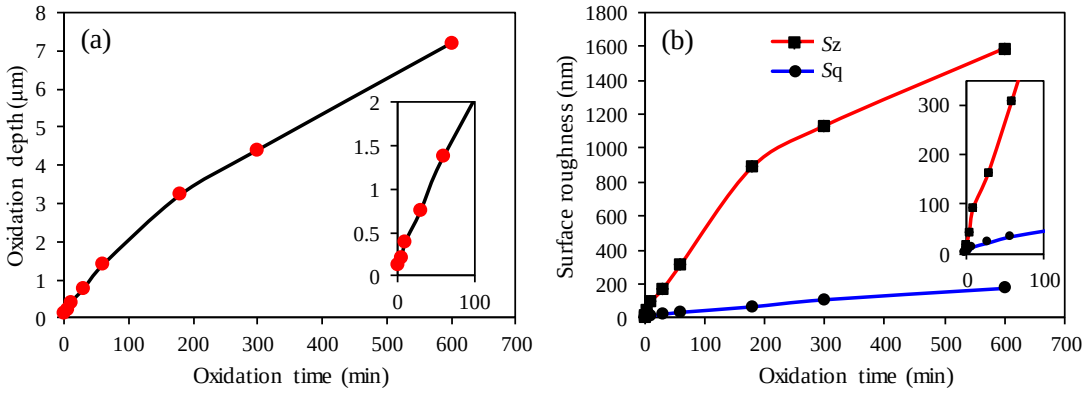

Figure 3.20 Constant potential oxidation of 4H-SiC (0001) surface. Relationship between (a) oxidation depth and oxidation time, and (b) surface roughness and oxidation time. The insets show the enlarged images of the results obtained with oxidation times of less than 100 min.

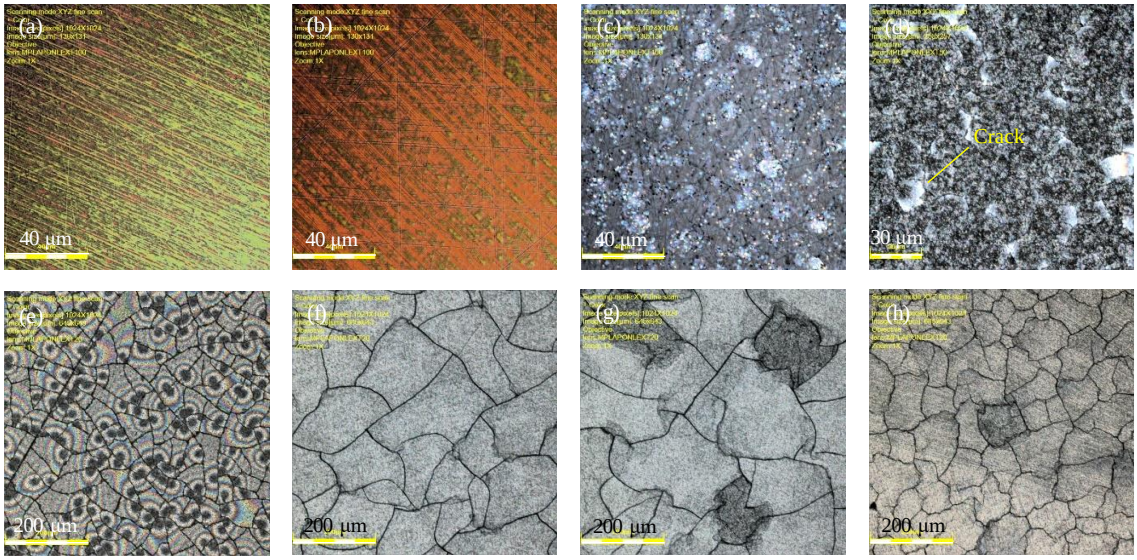

Figure 3.21 Laser microscopy images of SiC surfaces oxidized for (a) 1, (b) 5, (c) 10, (d) 30, (e) 60, (f) 180, (g) 300, and (h) 600 min.

oxide to peel off at the intersection of cracks on the surfaces oxidized for 300 and 600 min, as shown in Figures 3.21(g) and (h). Moreover, these phenomena increased the permeability of the oxide layer, allowing the oxidation species pass through the oxide layer and reach the interface between the oxide layer and bulk SiC, which then results in the continuous oxidation of SiC. The difference in the oxidation from 10 to 180 min and from 180 to 600 min may be caused by the thickening of the oxide layer and the changes in the oxide/SiC interface.

Figure 3.20(b) shows the changes in surface roughness of the oxidized surface after removal of the oxide layer. Note the increased surface roughness with longer oxidation time. Changes in the increase rate of the surface roughness were the same with the changes in growth rate of the oxidation depth. After anodic oxidation for 600 min, the *S*q surface roughness increased from 0.955 to 175.094 nm, whereas the *S*z surface roughness increased relatively more, from 8.606 to 1585.315 nm. These results show that smooth SiC surfaces cannot be obtained by long-time anodic oxidation.

Furthermore, the time dependence of constant current anodic oxidation was also studied, with particular conduct of anodic oxidation with constant current density for different oxidation times. The anodic oxidation parameters are shown in Table 3.5. Diamond-lapped surfaces were anodically oxidized using a two-electrode system at a constant current density of 10 mA/cm^2 in 1 wt% NaCl aqueous solution for 2, 10, and 30 min. Afterward, the oxide layers were removed by dipping the surfaces into 50 wt% HF solution. The changes in oxidation depth with an increase in oxidation time are illustrated in Figure 3.22(a), in which oxidation depth apparently increased

Table 3.5 Anodic oxidation of 4H-SiC (0001) surfaces at a constant current density of 10 mA/cm^2 with different oxidation times.

Experimental No.	①	②	③
Oxidation time (min)	2	10	30

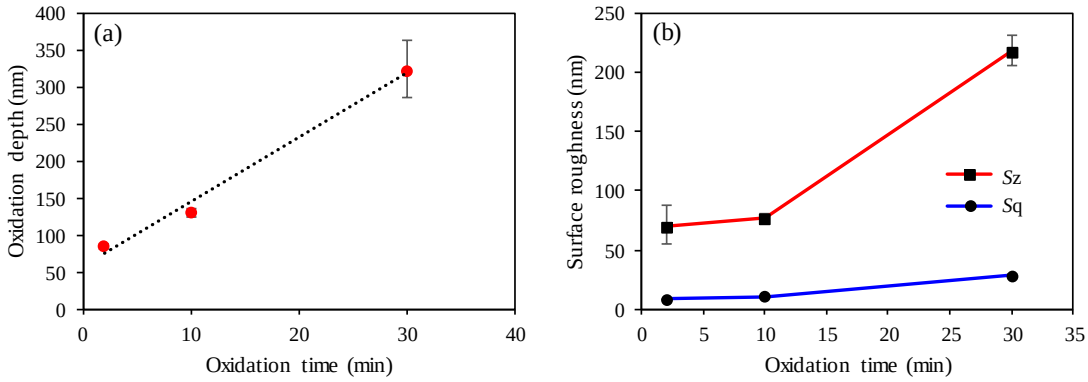

Figure 3.22 Constant current oxidation of 4H-SiC (0001) surface. Relationship between (a) oxidation depth and oxidation time, and (b) surface roughness and oxidation time.

with the increase in oxidation time. Such is consistent with the Coulomb's law, which states that the amount of oxide is proportional to the amount of electric charge.

After removal of the oxide layer, five areas on the surfaces were measured via SWLI. Typical SWLI images of these surfaces are shown in Figure 3.23. Figure 3.22(b) shows the surface roughness of these surfaces calculated from the five observed areas for each sample. The surfaces oxidized for 2 and 10 min exhibited similar topography pattern to the diamond-lapped surface, as shown in Figures 3.23(a) and (b), but with the *S*z and *S*q surface roughnesses increased, as shown in Figure 3.22(b). This is attributed to the preferential oxidation of the surface damage on the

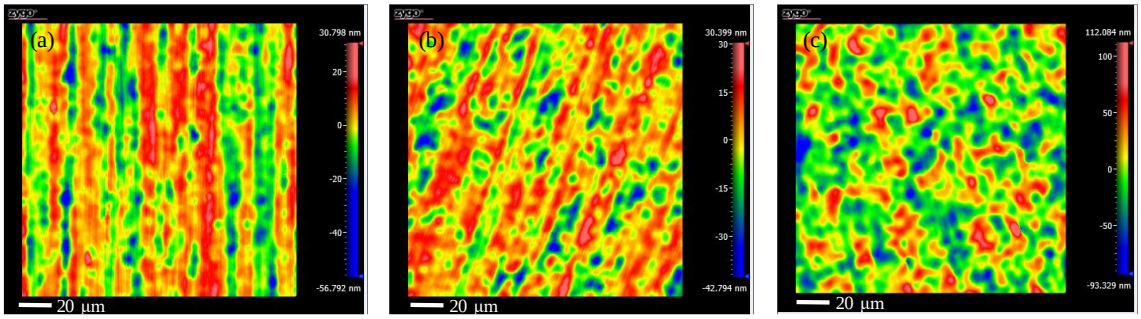

Figure 3.23 SWLI images of SiC surfaces oxidized at a current density of 10 mA/cm^2 at oxidation times of (a) 2, (b) 10, and (c) 30 min after removal of the oxide layer by HF etching.

diamond-lapped surface: the regions of scratches and pits on the surface were preferentially oxidized, resulting in deepening and widening of the scratches and pits and an increase in the *Sz* surface roughness [7]. Figure 3.23(c) shows the surface oxidized for 30 min after removal of the oxide layer by HF dipping. The surface structure found on the diamond-lapped surface was not observed, whereas many pits and fibrous protrusions were randomly distributed on the surface. This is attributed to the anisotropic oxidation of the SiC surface [8]. Therefore, the initial oxidation period of the SiC surface was dominated by the distribution of subsurface damage on the SiC wafer, and then by the anisotropy of single-crystal 4H-SiC after the subsurface damage. For both oxidation types, SiC surface roughness increased as oxidation time increased.

3.4.4 Off-angle dependence

The off-angle of SiC on the anodic oxidation properties of SiC surface was also investigated. On-axis and 4°-off CMP-processed SiC surfaces were anodically oxidized at constant potentials of 7 and 9 V in 1 wt% NaCl aqueous solution for 1 min. The oxidized surfaces were then observed by SEM. Figure 3.24 shows the changes in currents during the anodic oxidation. Apparently, the current in the oxidation of 4°-off SiC surface was always greater than that of the on-axis surface. Figure 3.25 shows the SEM images of the surfaces oxidized at 9 V for 1 min. It is clear that a part of the on-axis SiC surface remained uncovered with oxide, whereas, all of the surface was covered with oxide on the oxidized 4°-off SiC surface. These results suggest that the oxidation rate of 4°-off SiC surface is greater than that of on-axis SiC surface.

To understand these differences, the initial anodic oxidation morphology of an on-axis 4H-SiC (0001) surface was observed via AFM. For easy control of the oxidation process, the SiC surface was anodically oxidized under a very low constant current density of 5 μA/cm^2, and then observed

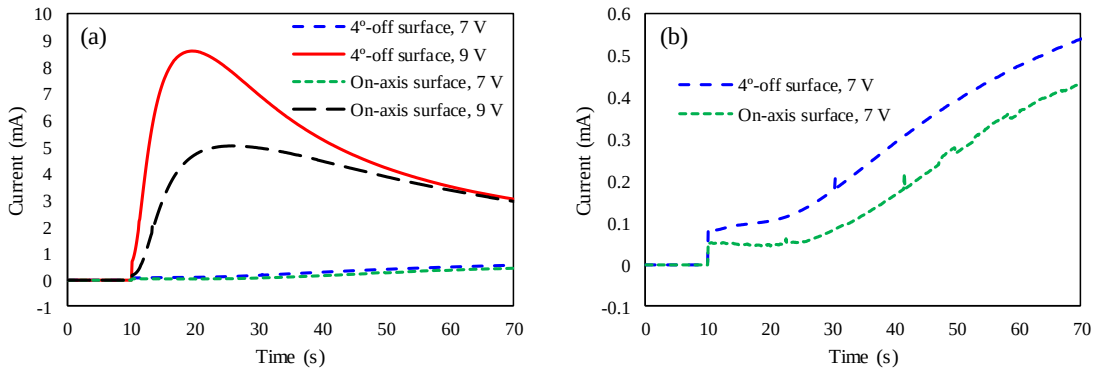

Figure 3.24 Changes of current in anodic oxidation of on-axis and 4°-off SiC wafers at different oxidation potentials. (a) Overall view. (b) Enlargement of changes in current at 7 V.

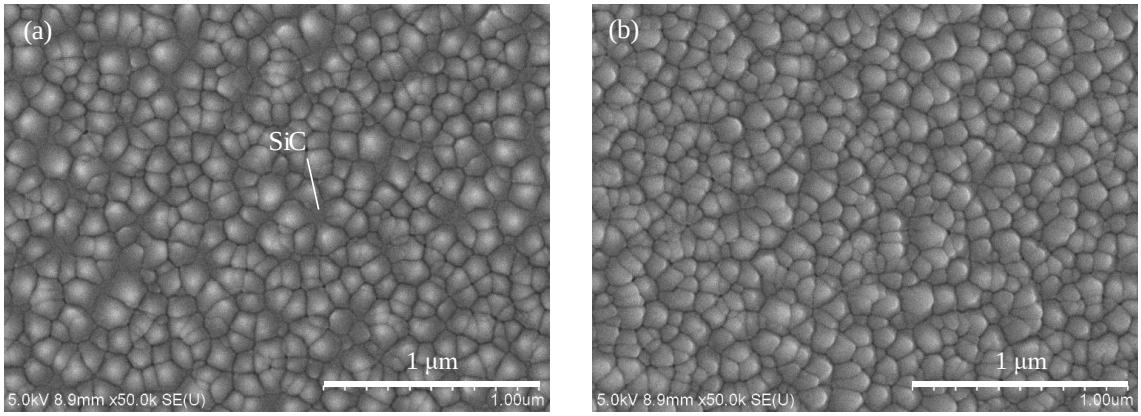

Figure 3.25 SEM images of oxidized (a) on-axis and (b) 4°-off SiC surfaces at 9 V for 1 min.

by AFM after oxidation for intervals of 1 min. The oxidation state of the surface was confirmed by analyzing the SiC substrate under using XPS after oxidation for 2 min.

Changes in the surface morphology of the 4H-SiC substrate during the first 2 min of anodic oxidation are depicted in Figure 3.26. In Figure 3.26(a), the as-received CMP-finished SiC surface had a clear terrace-step structure, although the step edges were rough. Moreover, its cross-sectional view with tilt correction showed having a step height of 0.25 nm (Figure 3.26(d)), which is consistent with the ideal height of a single 4H-SiC bilayer.

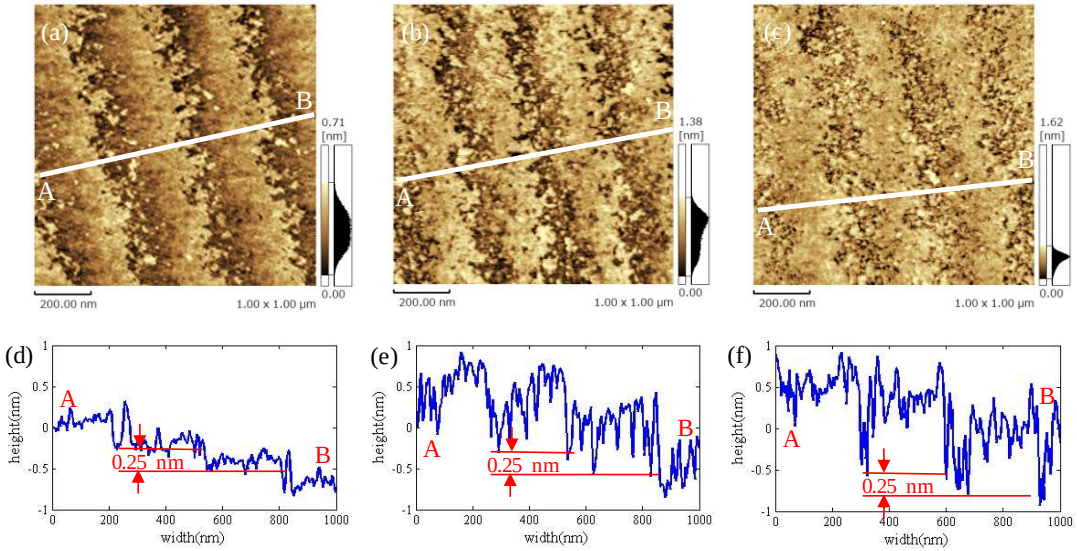

Figure 3.26 Surface morphology of SiC substrate before and after oxidation. (a) As-received surface. (b) Surface oxidized for 1 min. (c) Surface oxidized for 2 min. (d) Terrace step of as-received surface. (e) Terrace step of surface oxidized for 1 min. (f) Terrace step of surface oxidized for 2 min.

After anodic oxidation for 1 min, the surface became rougher, as indicated in Figure 3.26(b). A cross-sectional view of the AFM image, which was tilt-corrected under the same conditions as used in Figure 3.26(d), is shown in Figure 3.26(e). Here, it is clear that the terraces became inclined and their edges went higher than the terrace bottoms. In the anodic oxidation of SiC, SiC was changed to SiO_2, which has lower density and greater molar mass than SiC; thus, the volume of SiC would increase when oxidized to SiO_2. This result implies that the terrace edges were oxidized, but not the terrace bottoms, as the step height between the bottoms of two adjacent terraces was still 0.25 nm. With the oxidation time reaching 2 min, the terraces became rougher, as shown in Figures 3.26(c) and (f), yet the terrace bottoms remained unoxidized with the unchanged step height between the bottoms of the two adjacent terraces.

To confirm whether this phenomenon was caused by the surface oxidation, XPS analysis was carried out on the substrate that was oxidized for 2 min. Figure 3.27 shows the Si 2p and C 1s spectra of the surface detected with a take-off angle of the specimen platen of 15°. From Figures 3.27(a) and (b), the spectrum of Si 2p changed after oxidation. The results of peak separation in Figure 3.27(b) showed weak peaks corresponding to intermediate oxide (SiC_xO_y) [9] after oxidation for 2 min. Moreover, the spectrum of C 1s was also changed, as shown in Figures 3.27(c) and (d), wherein the C–OH bonds decreased, the C–C/C–H bonds increased, and bonds corresponding to SiC_xO_y appeared after oxidation. It has been reported that SiC surface was terminated with OH after removal of the oxide layer by HF etching [10]. Since HF was applied to remove the native oxide on the SiC wafer before anodic oxidation, thus, the decrease in C–OH bonds is attribute to the oxidation of the SiC surface. Whereas, the increase in C–C/C–H bonds is attribute to the contamination during the anodic oxidation [11].These results indicate that the surface was oxidized

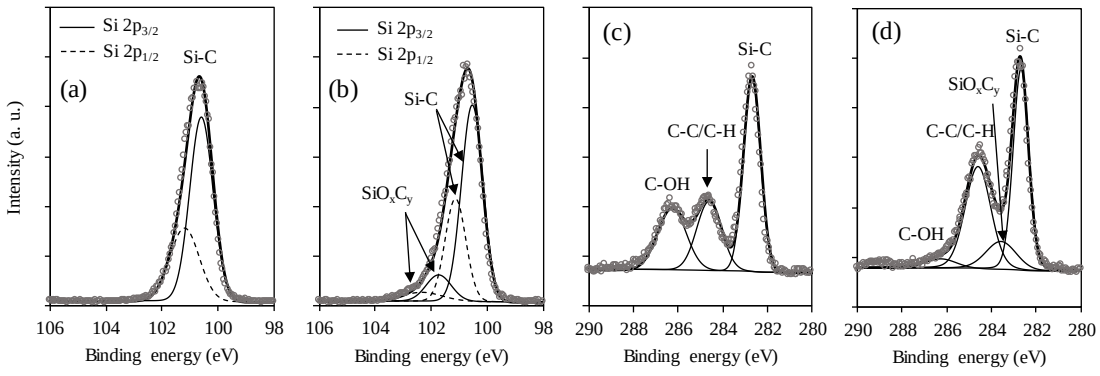

Figure 3.27 Results of XPS after oxidation for 2 min (take-off angle 15°). (a) Si2p peak separation of as-received surface. (b) Si2p peak separation of surface oxidized for 2 min. (c) C1s peak separation of as-received surface. (d) C1s peak separation of surface oxidized for 2 min.

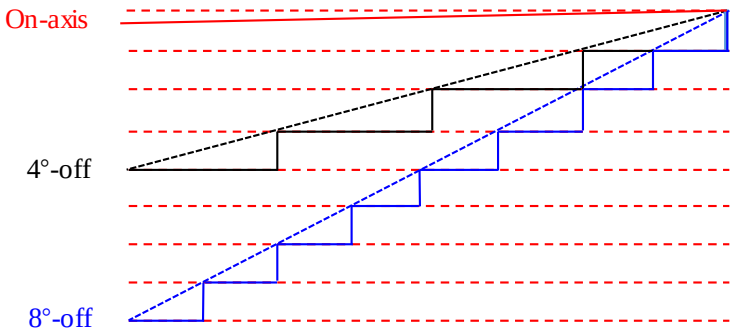

Figure 3.28 Schematic diagram of SiC surfaces with different off-angles.

to intermediate oxide with a small thickness, that the changes in the terrace steps shown in Figure 3.26 originated from the oxidation of the surface, and that the anodic oxidation of SiC surface initiated from the terrace edges.

A schematic diagram of SiC surfaces with different off-angles is illustrated in Figure 3.28. Note the increase in the density of step terrace at the increase of off-angle, which means that there were more step edges on the 4°-off SiC surface than on the on-axis SiC surface. Since the anodic oxidation of SiC surface started from the step edges, under the same condition the oxidation rate of 4°-off SiC surface must be greater than that of on-axis SiC surface.

3.5 Origin of oxide protrusions in anodic oxidation process

To investigate the origin of the oxide protrusions in the anodic oxidation process of SiC surface, AFM observation of the anodic oxidation process was performed. In determining the origin of the oxide protrusions, it is very important to observe the changes in the same area on the surface during the oxidation process. However, it is very difficult to find the same place on the surface after each oxidation process due to the small observation area of AFM. Therefore, a nanoindenter (ENT-2100, Elionix Inc.) was used in forming some indents on the surface, which proved helpful for finding the same area in the AFM observation. Four hundred indents (20 × 20) separated by an interval of 5 μm were formed with a force of 100 mN. An image of the indents obtained using the charge-coupled device (CCD) camera of the microscope is displayed in Figure 3.27(a). Using these indents as a reference, four indents located in the upper right corner of the indented area were observed via AFM, as demonstrated in Figure 3.29(b). Moreover, surface morphology changes after each oxidation process was observed in the same square area of 1 μm × 1 μm.

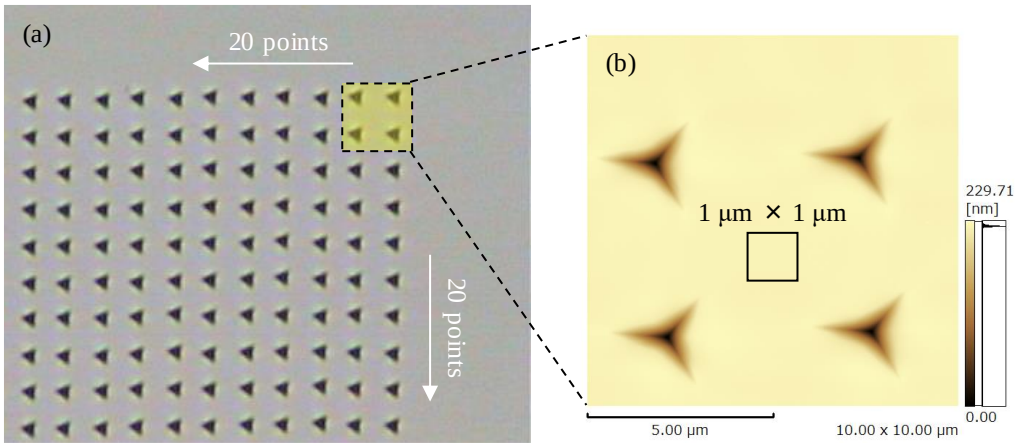

Figure 3.29 Indents on the SiC surface formed using a nanoindenter with a force of 100 mN. (a) CCD image of the indents. (b) AFM image of four indents in the upper right corner of the indented area.

Oxidation rate was precisely controlled through the employment of current-controlled oxidation on the indented SiC surface at a constant current of 10 μA for a total oxidation time of 1.5 min, during which the oxidized surface was observed every 0.5 min by AFM. Figure 3.30 shows the surface morphologies after different oxidation times, as well as changes in the current and potential during the oxidation process. After the as-received SiC substrate was finished by CMP, a terrace-step structure was observed on the as-received surface, as shown in Figure 3.30(a). After oxidation for 0.5 min, the terrace-step structure became unclear, and small oxide protrusions began to form on the surface, as can be seen in Figure 3.30(b). With the oxidation progress, the terrace-step structure became less clear, while more oxide protrusions were generated, as shown in Figure 3.30(c). In the final 0.5 min, the oxide protrusions became large and almost no new oxide protrusions were generated, as depicted in Figure 3.30(d). This result indicates that the number of oxide protrusions has a limit, which is determined by the oxidation condition (potential).

The origin of the oxide protrusions was investigated by using the location indicated by a red circle in Figure 3.30 as a benchmark on the surface. Five oxide protrusions, numbered from 1 to 5 and marked by arrows with different colors in Figure 3.30(d), were taken as the target subjects. The observation showed that the oxide protrusions originated from atomic pits on the as-received CMP-finished surface, as demonstrated in Figure 3.30(a). Moreover, the CMP of a 4H-SiC (0001) surface based on the study by Shi *et al.* showed that atomic pits were introduced by the utilization of large abrasive particles or a high polishing pressure during the CMP process [12]. Therefore, those atomic pits are considered as mechanical damage in atomic level introduced during CMP.

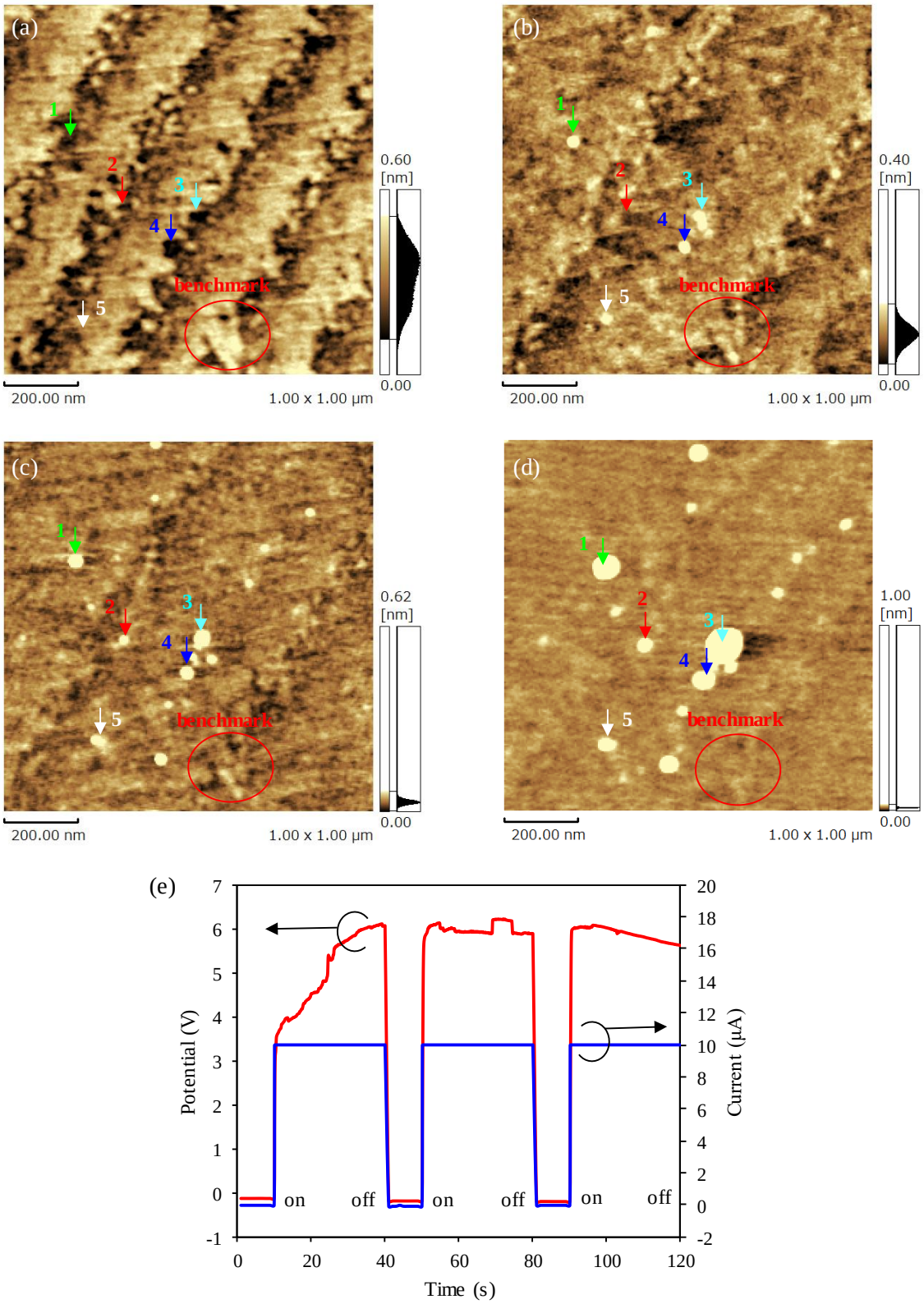

Figure 3.30 AFM observation of the anodic oxidation process of SiC at a current of 10 μA in 1 wt% NaCl solution. (a) As-received surface ad surfaces oxidized for (b) 0.5 min, (c) 1 min, (d) 1.5 min. (e) Changes in the current and potential during the oxidation process.

Also, in Figure 3.30(a), these atomic pits were randomly located on the terraces, but had larger frequency on the terrace edges presumably due to the preferential polishing of higher locations on the surface in CMP. However, not all the atomic pits became oxide protrusions after oxidation, as evidenced in Figure 3.30. Referring back to Figure 3.14, the frequency of oxide protrusions increased with increasing oxidation current (potential), which indicates that the atomic pits had different breakdown potential thresholds, and that more atomic pits were broken down at a higher potential. In other words, the oxide protrusions should be distributed in lines along the terrace edges if most of the atomic pits were broken down in the oxidation process. As mentioned earlier, the observation area of AFM is very small, thus, it becomes difficult to observe the distribution of oxide protrusions. To overcome this, SEM was employed for observation of the surface oxidized at currents of 2 and 1 mA, as shown in Figure 3.14. It is believed that most of the atomic pits were broken down at both oxidation rates. Figure 3.31 shows the SEM images of the two oxidized surfaces, where the insets are AFM images of the as-received surfaces. Apparently, the oxide protrusions were distributed in lines along with step direction, and the distance between the lines was consistent with the width of the terraces, verifying our supposition.

There are two reasons for the breakdown at the atomic pits. First, the breakdown is related to the geometry of the atomic pits. The electric field is more easily focused at a sharp position on the surface because of the repulsive force between carriers with the same charge, which are holes in the anodic oxidation of SiC. Therefore, breakdown would more easily occur at deep and narrow pits than at wide and shallow ones. This could alternatively state that the deep and narrow pit has lower breakdown threshold than the wide and shallow pit, and thus, is preferentially broken down during the oxidation process. Second, there are more broken Si–C bonds at the atomic pits,

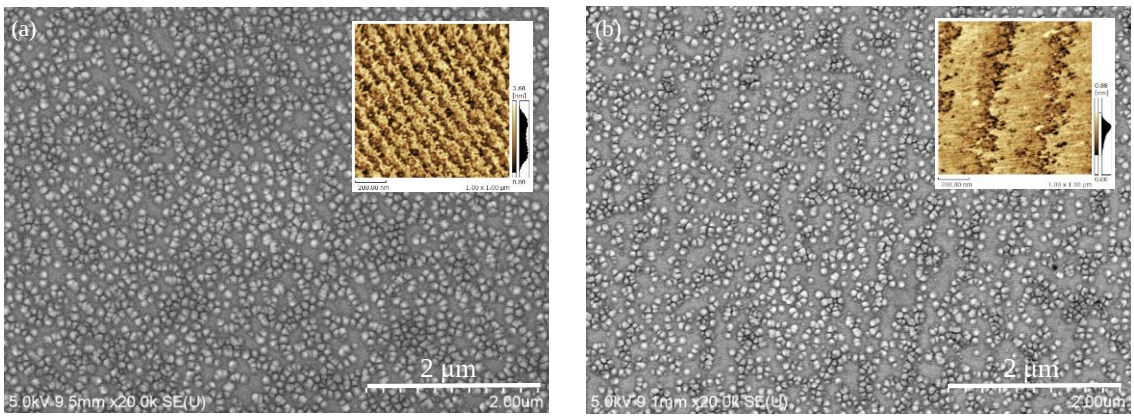

Figure 3.31 SEM images of surfaces oxidized in 1 wt% NaCl solution with the same charge of 60 mC. (a) Surface oxidized at a current of 1 mA for 1 min. (b) Surface oxidized at a current of 2 mA for 0.5 min. The insets are AFM images of the as-received surface of area 1 μm × 1 μm.

resulting in more dangling bonds. Therefore, oxidation rate at these locations is greater than that at locations without pits [13].

Figure 3.30(e) shows the changes in the potential during the current-controlled oxidation process. As in the potential-controlled oxidation process, changes in the potential in the current-controlled oxidation process also reflect the oxidation stage of the SiC surface. Based on the figure, the potential could be seen to increase during the first 0.5 min, which can be accounted to the passivation of the SiC surface as the oxide protrusions had just been generated, as demonstrated in Figure 3.30(b). In the final minute, the potential decreased. In combination with the surface morphologies shown in Figures 3.30(c) and (d), this result corresponds to the breakdown of the passive film and the growth of the oxide protrusions.

Figure 3.30 also shows that two adjacent terraces merged after oxidation for 0.5 min. It has been reported that two types of Si–C terrace exists on 4H-SiC, namely, 4H1 and 4H2 terraces, depending on the physical relationship with the bilayers below [14,15]. The stability of these terraces is different. Calculation results from previous studies indicate that the extra energy required to deposit a new layer on a 4H1 terrace is much greater than that for a 4H2 terrace [16-18], which reflects that a 4H1 terrace is more stable than a 4H2 terrace. Research on the finishing of 4H-SiC [13,19] have demonstrated that the oxidation rate of 4H2 terraces is greater than that of 4H1 terraces, which results in different types of terrace-step structure. Similarly, since 4H2 terraces have a higher oxidation rate than 4H1 terraces in the oxidation process the rate of volume increase of the former should be greater than that of the latter. Such conviction leads to the edges of 4H1 terraces being covered by the oxidized 4H2 terraces, and the merging of the both types of terrace, as shown in Figures 3.30(b) and (c).

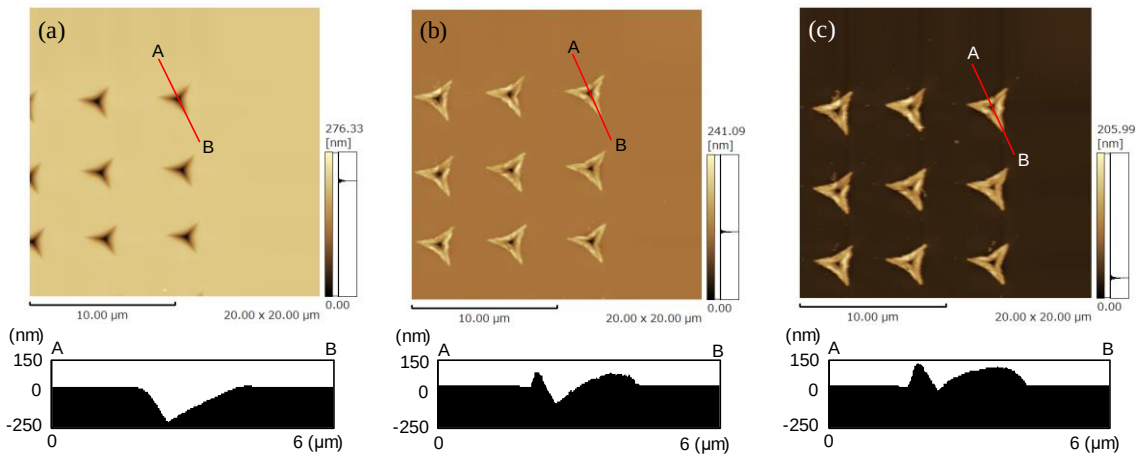

Figure 3.32 AFM images and cross-sectional views of (a) unoxidized indents and indents oxidized for (b) 0.5 min and (c) 1 min.

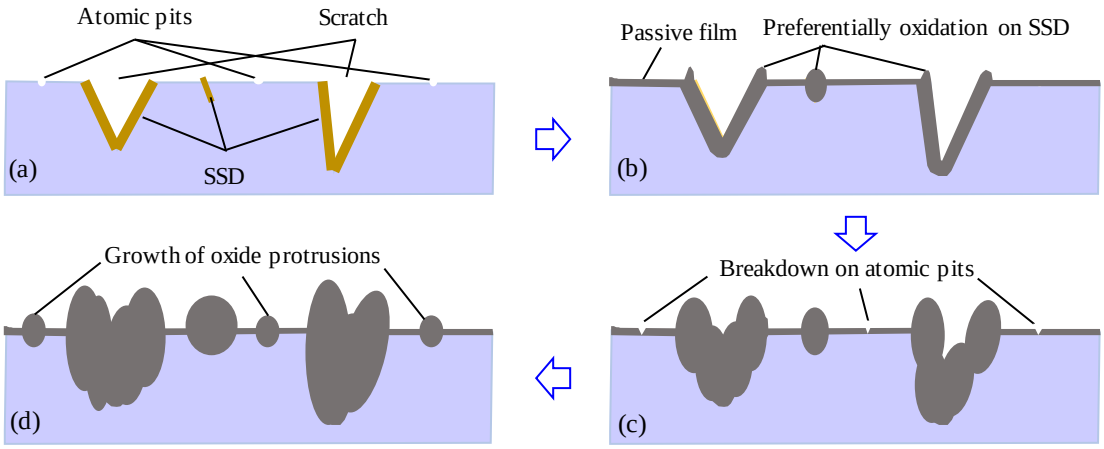

Figure 3.33 Modeling of the anodic oxidation process of 4H-SiC surface.

Changes in the indents in the anodic oxidation process are shown in Figure 3.32. Indents were oxidized at the first 0.5 min of the oxidation, and oxidation started from the entire surface of the indents, as shown in Figure 3.32(b). Additionally, the oxidation rate of the indents was very high, the height of oxide protrusions located at the edges of the indents reached more than 100 nm within 1 min, as depicted in Figure 3.32(c). Figure 3.30 shows that the oxidation rate of the area indicated in Figure 3.29 was very low, with the height of the oxide protrusions herein only reaching approximately 30 nm after oxidation for 1.5 min. This result indicates that the indents were preferentially oxidized in the anodic oxidation process. Nonetheless, because these indents were mechanically formed with a nanoindenter, the damaged layer was undoubtedly introduced on and just under the surface of the indents, which reveals that the damaged layer had lower breakdown potential and higher oxidation rate than the atomic pits.

On the basis of the above results, the anodic oxidation process of a SiC substrate with scratches, SSD, and atomic pits can be modeled, as shown in Figure 3.33. In the initial oxidation step, the edges of the scratches and SSD were preferentially oxidized, while the remaining part of the surface was passivated, as shown in Figure 3.33(b). If the oxidation potential is insufficient to break down the passivation film, the film hinders further surface oxidation, where instead, only the scratches and SSD are oxidized. In contrast, the passivation film is broken down at the atomic pits, as shown in Figure 3.33(c), followed by current concentration on the breakdown sites due to lower resistance, which eventually leads to the generation of oxide protrusions (etch pits).

3.6 Growth process of oxide protrusions

As explained above, generation of etch pits during anodic oxidation leads to serious deterioration of the surface roughness; thus, it is very important to clarify the growth process of

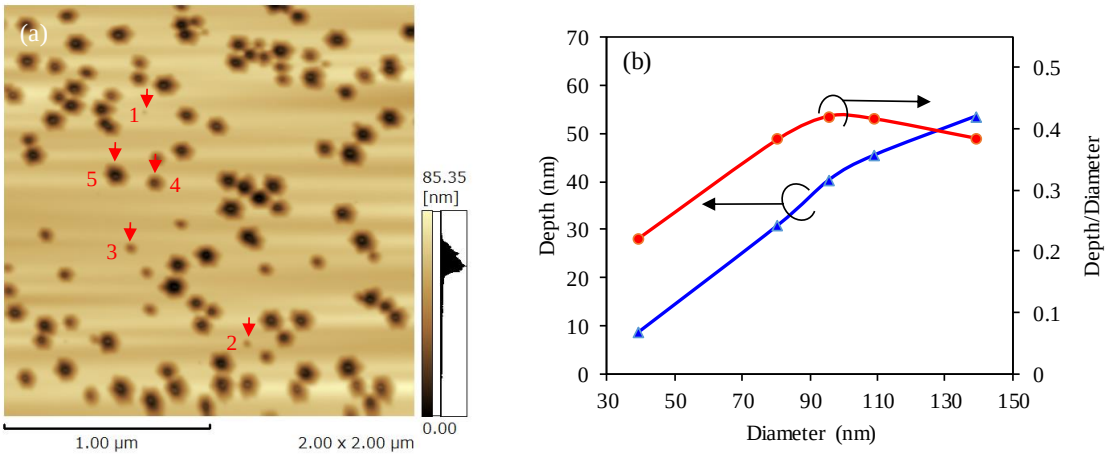

Figure 3.34 (a) Etch pits on an oxidized surface with the oxide layer removed by HF solution. (b) Relationship between the depth and diameter of the etch pits marked by arrows in (a).

etch pits. Merging of the etch pits together was avoided by applying a potential of 7 V to oxidize the SiC substrate for 1 min, the oxidized surface was then dipped into a 50 wt% HF solution for 30 min, for removal of the oxide layer. Figure 3.34(a) shows an AFM image of the surface after the oxide layer has been removed, and reveals many etch pits with different sizes that were randomly distributed on the surface. To investigate the growth process of the etch pits, five etch pits with different sizes were specifically analyzed using particle analysis software. The relationship between the diameter and depth of the five etch pits is described in Figure 3.34(b). On one hand, the depth of the pits increased as their diameter increased, which indicates a thicker oxide layer over the larger etch pits. On the other hand, the depth-to-diameter ratio first increased, and then decreased with increasing diameter. Such pattern reveals a longitudinal growth of the etch pits in the early growth stage and lateral growth in the late growth stage.

In parallel, the growth process of the oxide protrusions was modeled using the Deal-Grove model, which mathematically describes the growth of an oxide layer on the surface of a material

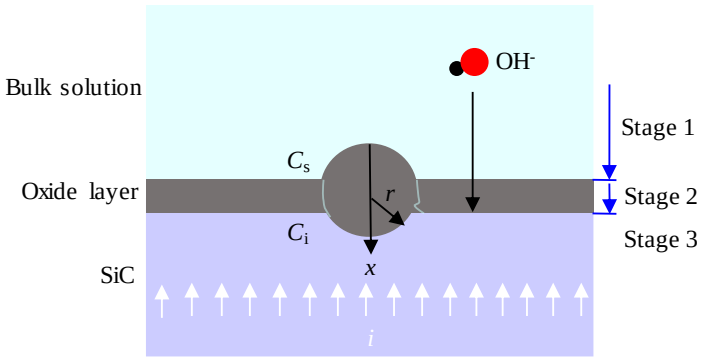

Figure 3.35 Modeling of the growth process of oxide protrusions using the Deal-Grove model.

[20-21]. The Deal-Grove model of anodic oxidation for SiC is particularly shown in Figure 3.35. Hypothetically, the oxidizing species, considered to be hydroxyl groups (OH^-) in the anodic oxidation of SiC, undergoes three processes [22-23]. Initially, the hydroxyl groups diffuse from the bulk electrolyte to the SiC surface. Next, they diffuse through the existing oxide layer to the oxide-SiC interface. Finally, they react with SiC. Each of these stages proceeds at a rate proportional to the concentration of hydroxyl groups. In practice, stage 1 does not limit the reaction rate at a sufficiently low potential for a short oxidation time, which means that the growth process of etch pits is mainly controlled by stages 2 and 3. Stage 2 is a diffusion process that obeys Fick's Law. Thus, the diffusion flux of hydroxyl groups J_{ox} in the oxide layer can be expressed as

$$J_{\mathrm{ox}} = D_{\mathrm{ox}} \frac{C_{\mathrm{s}} - C_{\mathrm{i}}}{x}, \tag{3.2}$$

and the rate of mass transfer in the x direction is governed by:

$$\frac{\partial m}{\partial t} = D_{\mathrm{ox}} A_{\mathrm{x}} \frac{C_{\mathrm{s}} - C_{\mathrm{i}}}{x}. \tag{3.3}$$

Because $\frac{\partial m}{\partial t} = \frac{I}{zF}$ and $I = 2\pi r^2 i$, the following formula can be derived:

$$C_{\mathrm{i}} = C_{\mathrm{s}} - \frac{i}{zDF} x, \tag{3.4}$$

where C_s is the concentration of hydroxyl groups on the surface of the SiC substrate and is approximately equal to that in the bulk solution, C_{i} is the concentration of hydroxyl groups on the oxide-SiC interface with an oxide layer of depth x, A_{x} is the area perpendicular to the x direction through which diffusion takes place, i is the current density at which the oxide protrusions are generated, z is the chemical valence of hydroxyl groups, F is the Faraday constant, and D_{ox} is the diffusion coefficient of hydroxyl groups in the oxide layer.

Meanwhile, stage 3 is a charge transfer process. Here, the current density of the electrochemical reaction is given by:

$$i = nFkC_{\mathrm{i}}, \tag{3.5}$$

where n is the number of electrons consumed by the reaction and k is the rate constant. Therefore, C_{i} determines the oxidation rate in a potential-controlled electrochemical reaction. For a current-controlled reaction, the distribution of C_{i} determines the distribution of the current density on the SiC surface.

It is clear in Equation (3.4) that C_i decreases as the oxide thickness increases. This means that oxidation rate is smallest at the center of the pits, having the thickest oxide layer, as reflected from Equation (3.5). Figure 3.34 describes that the longitudinal growth of pits occurs in the early growth stage, indicating that the growth of the pits was controlled by stage 3 (charge-controlled). Diffusion of hydroxyl groups is not significantly hindered by oxide protrusions with relatively

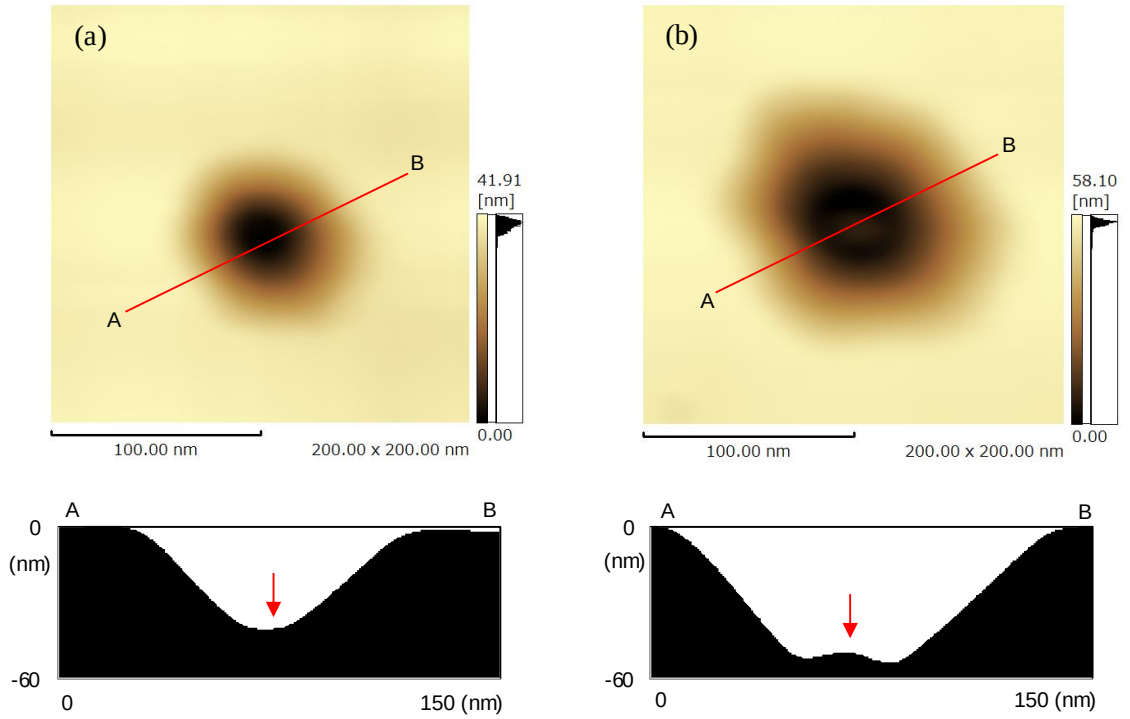

Figure 3.36 AFM images and cross-sectional views of small and large etch pits.

small thickness. With increasing thickness of oxide protrusions in the late growth stage, diffusion of hydroxyl groups in the oxide layer becomes increasingly difficult, particularly at the center of the pits, resulting in the lateral growth of the pits. High-resolution AFM images and cross-sectional views of small and large pits are displayed in Figure 3.34, wherein an apparent SiC protrusion at the bottom center of the large etch pit could be observed, but not in the small pit. This is indicative of a lower oxidation rate at the center of the large pit, thereby verifying the proposed model of pit growth.

3.7 Repeated anodic oxidation and HF etching of SiC surface

The above results verify that a smooth SiC surface cannot be obtained because of the preferential anodic oxidation of surface damage. To understand if this scenario works for the anodic oxidation of a damage-free surface, attempts were done to obtaining a uniform oxidation of SiC surface. A CMP-finished single-crystal 4H-SiC substrate (on-axis, N-type) supplied by TankeBlue Semiconductor Co. Ltd. with 350-μm thickness and specific resistance within 0.015–0.028 Ω·cm was used for this investigation. Oxidation and etching experiments were performed on the (0001) face, the face most commonly used in electric power devices. NaCl aqueous solution was the electrolyte used, with concentration and EC of 1 wt% and 1.8 S/m, respectively. Before

the oxidation and etching experiments, the substrate was observed by X-ray diffraction (XRD) to confirm its purity. The XRD spectrum is presented in Figure 3.37, wherein only an intense X-ray peak at 35.6° corresponding to hexagonal 4H-SiC was observed, which thus, confirmed the purity of the 4H-SiC substrate.

A constant potential of 7 V referred to an Ag|AgCl RE was applied to induce anodic oxidation. Two sets of experiments were conducted to investigate the repeatability of oxidation/etching and the effects of oxidation time on the surface topography of the oxidized/etched surface. The experimental procedure is shown in Figure 3.38. In both sets of experiments, the SiC substrate was first oxidized for 10 min, before it was dipped into an HF solution for 60 min to remove the surface damage formed during the wafer manufacturing process. Subsequently in the first set, after removal of the surface damage, the surface was alternately processed by anodic oxidation (for 1 min) and HF etching (for 30 min) four times. In the second set, the surface was alternately processed by a combination of anodic oxidation (for 1 min) and HF etching (for 30 min) twice, followed by a combination of anodic oxidation (for 10 min) and HF etching (for 60 min) twice.

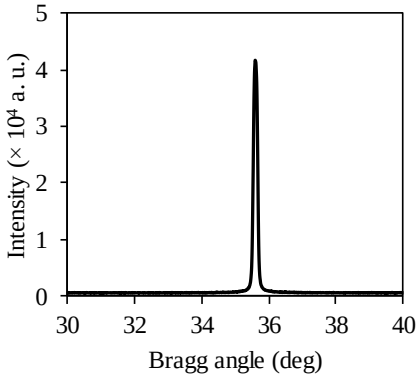

Figure 3.37 X-ray diffraction (XRD) spectra of as-received 4H-SiC substrate. The (0001) surface is irradiated with X-rays and the Bragg angle is varied from 30° to 40°.

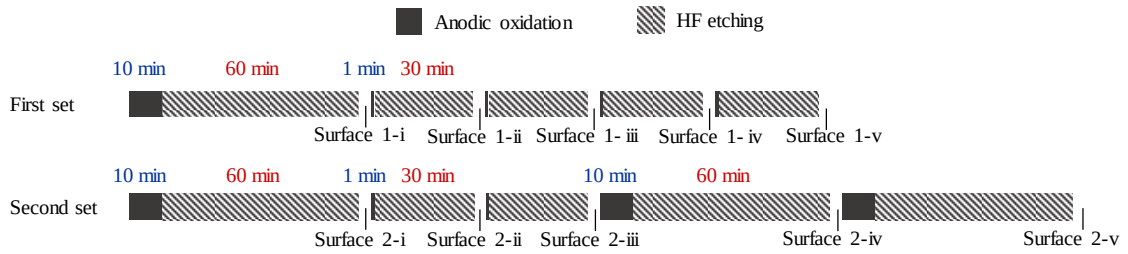

Figure 3.38 Experimental procedure. Two sets of experiments conducted. The oxidized/etched surfaces are denoted as surfaces 1-i to 1-v in the first set of experiments and surfaces 2-i to 2-v in the second set of experiments.

The oxidized/etched surfaces were denoted as surfaces 1-i to 1-v in the first set of experiments, and surfaces 2-i to 2-v in the second set. The surface morphologies were observed via AFM (SPM 9700), and SEM (Hitachi S-4800) after every anodic oxidation or HF etching. Oxygen distribution on the oxidized surfaces was observed by energy dispersive X-ray spectrometry (EDX).

3.7.1 Effects of surface damage on the oxidation performance of SiC

Results of the first two oxidation/etching steps are presented in Figure 3.39. From Figure 3.39(a), note that although the as-received surface used in this study had a clear terrace-step structure, the terraces were not straight and had many defects, and a subsurface damage layer existed on them. These structural defects were preferentially oxidized in the anodic oxidation process, leading to the generation of oxide protrusions [7,24]. Additionally, the SiC surface was fully covered by oxide protrusions after oxidation for 10 min, as shown in Figure 3.39(b), suggesting that the structural defects on the surface were fully oxidized. The oxidation depth after removing the oxide layer reached 70 nm, as shown in Figure 3.40. The depth of the damage layer generated during mechanical polishing by diamond abrasives was approximately 50 nm, whereas almost no surface damage was observed on the CMP-processed surface, except for some slight

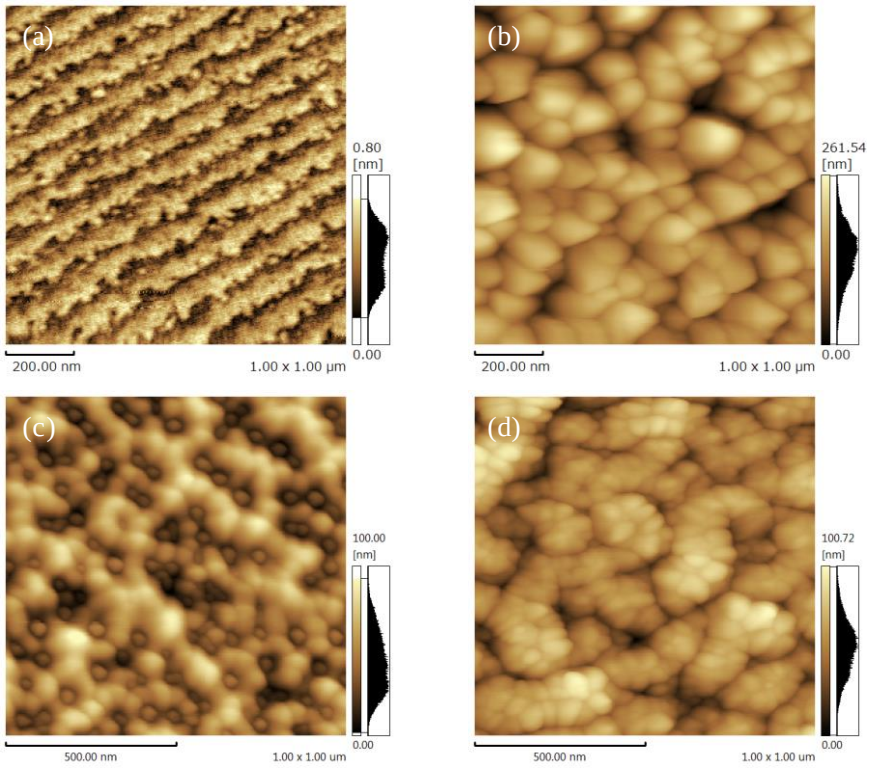

Figure 3.39 AFM images of SiC surfaces. (a) As-received surface. (b) Surface oxidized for 10 min. (c) Surface 1-i. (d) Surface 1-i oxidized for 1 min.

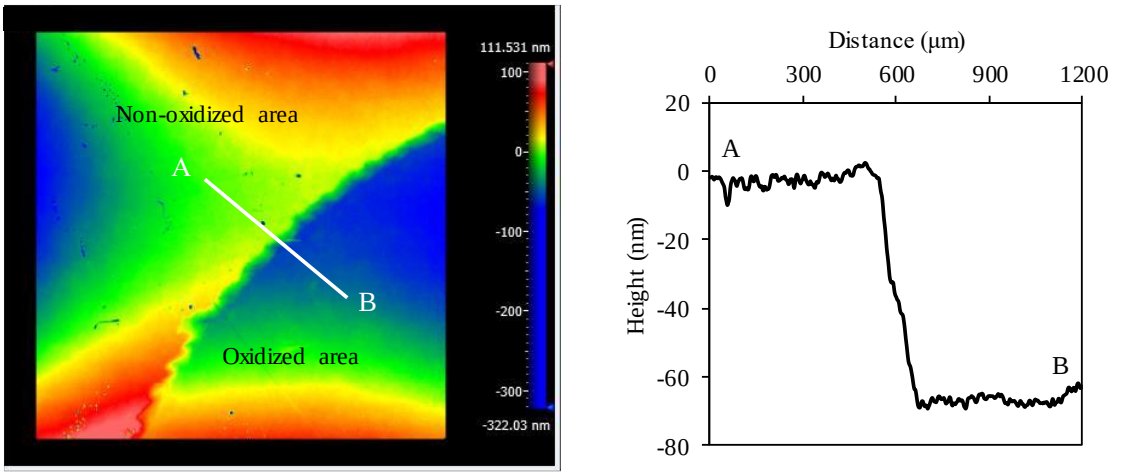

Figure 3.40 Oxidation depth of as-received surface after oxidation for 10 min. The surface after removing the oxide is observed by a scanning white light interferometer (SWLI). The oxidation depth is about 70 nm according to the cross-sectional view along A–B.

crystallographic damages [25-27]. Therefore, surface 1-i in Figure 3.39(c) was presumably a "damage-free" surface, regardless of the presence of several etch pits on it. After re-oxidization of surface 1-i for 1 min, as indicated in Figure 3.39(d), many small oxide protrusions were generated, which were distributed uniformly on the oxidized surface.

Figure 3.41 shows the EDX measurement results for the oxidized surfaces obtained by the oxidation of an as-received surface and surface 1-i at 7 V for 1 min. As shown in Figures 3.41(a) and (b), oxidation of the as-received surface was not uniform due to the generation of large oxide protrusions, and similarly, oxygen distribution on the oxidized surface was not uniform and instead was concentrated at the sites of the oxide protrusions and the lines corresponding to subsurface damage. On the contrary, as shown in Figures 3.41(d) and (e), oxidation of surface 1-i was relatively uniform, oxygen was uniformly distributed on the surface, and no preferential oxidation occurred even in the regions of scratches. This result indicates that the surface was uniformly oxidized after removal of the surface damage.

Generally, surface damage, i.e., scratches, on a SiC surface is always accompanied by a series of edge dislocations, screw dislocations [28], deformations, microcracks [29], and stacking faults [30]. These defects induce residual strain and change the material properties of SiC. Jia *et al.* demonstrated that the atomic bonding at dislocation sites is weaker than that in a perfect SiC crystal, and that the activation energies of dislocations are lower than those in a perfect SiC crystal, resulting in a higher etching rate at the dislocation sites [31]. Moreover, oxidation rate at the defect sites is higher than at the defect-free sites in the dry thermal oxidation of SiC [32]; the difference is greater in wet thermal oxidation using a water vapor and oxygen flow, owing to the influence of

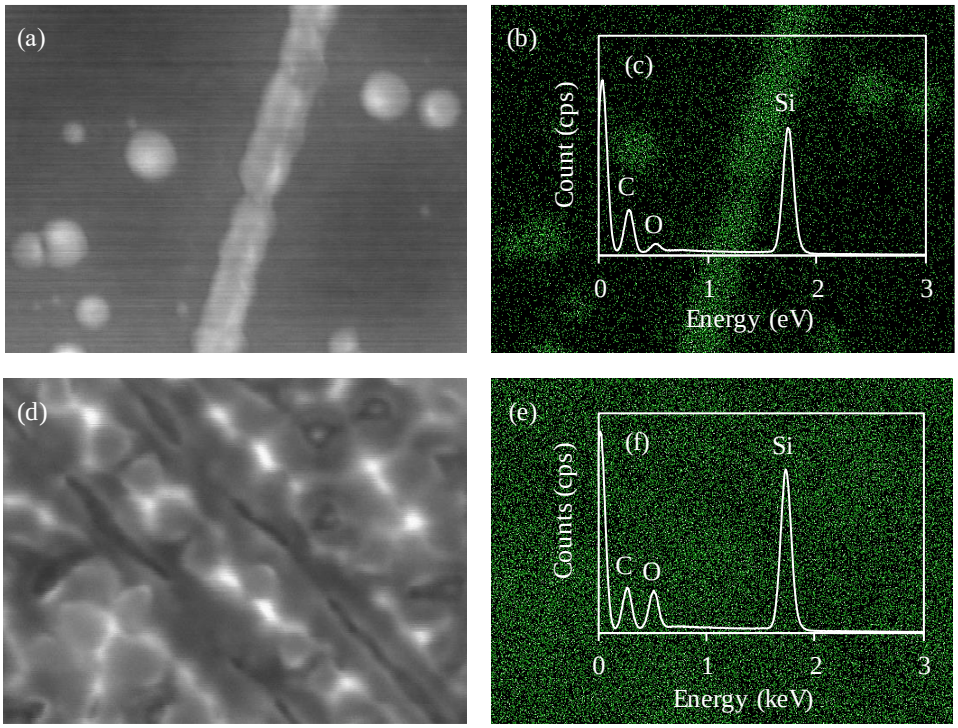

Figure 3.41 EDX measurement results of as-received surface and surface 1-i after oxidation for 1 min. (a) SEM image of as-received surface after oxidation, its (b) distribution map of oxygen and (c) element spectrum. (d) SEM image of surface 1-i after oxidation, its (e) distribution map of oxygen and (f) element spectrum. The oxidation of the as-received surface is not uniform whereas the oxidation of surface 1-i is uniform.

weaker atomic bonding and local polarity inversion at the defect sites [33]. Defects weaken the bonds between atoms and affect the material properties of SiC, resulting in the defect sites exhibiting higher chemical activity than the defect-free areas. These effects occurred in the anodic oxidation of SiC, thereby resulting in the preferential oxidation of defects, as shown in Figures 3.41(a) and (b).

Figure 3.42 shows the changes in current during the oxidation of the as-received surface and surface 1-i. The current during the oxidation of surface 1-i was greater than during the oxidation of the as-received surface in the initial oxidation stage, and current trends during the two oxidations were different. The spectra shown in Figures 3.41(c) and (f) suggest that the amount of oxide on the as-received surface after oxidation was less than that on surface 1-i after oxidation due to the appearance of a smaller oxygen peak. In the oxidation of the as-received surface, the change in the current can be divided into three stages: an initial decrease, followed by an increase, and a secondary decrease. Combining this with the EDX measurement result shown in Figure 3.41(b), it was deduced that the region of subsurface damage was preferentially oxidized, with

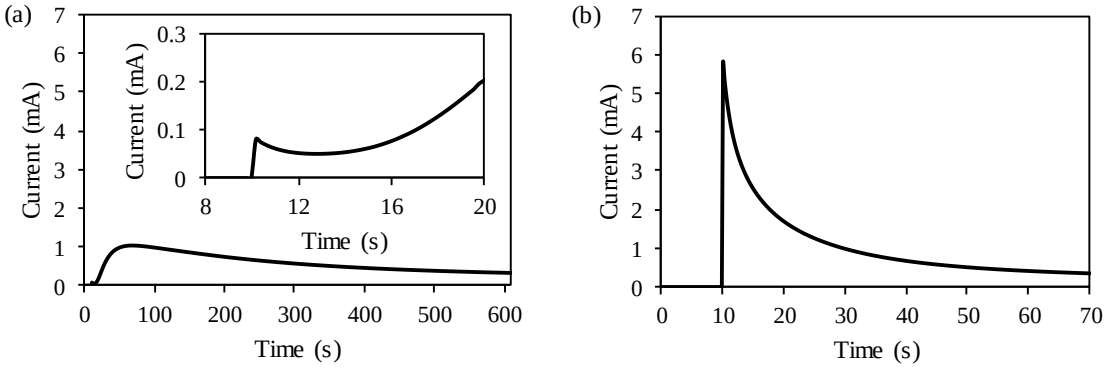

Figure 3.42 Changes in current during anodic oxidation of (a) as-received surface; the inset shows an enlarged image of the changes in the current during the initial oxidation stage, and (b) surface 1-i. Both anodic oxidations are started at 10 s. The trends of the current during the two oxidations are different.

the initial decrease in the current being considered to correspond to the oxidation of the subsurface damage and the passivation of the region without subsurface damage [7]. The resistance increased after the region of subsurface damage was covered with an oxide layer, and the current flowed to the region without subsurface damage, which led to the breakdown of the passivation film and the subsequent increase in the current. When the entire surface was covered with oxide layer, the current decreased for the second time. During oxidation of surface 1-i, the current decreased monotonically with oxidation time. As there was no subsurface damage on surface 1-i, only a single stage of oxidation occurred in the surface. Moreover, oxidation of the whole surface was simultaneous as the current decreased monotonically with the oxide layer growth.

The difference in oxidation rate between the two oxidations was investigated through the electrochemical impedance method, as shown in Figure 3.43. The impedance of the anodic oxidation system of SiC can be expressed by Equation (3.6), which includes three parts, namely, those of the electrolyte Z_E, the SiC surface Z_{SS}, and the bulk SiC Z_{BS},

$$Z = Z_E + Z_{SS} + Z_{BS}, \tag{3.6}$$

Similarly, the impedance of the SiC surface Z_{SS} can be divided into three parts, namely, the impedance of the oxide layer, that of the interface between the oxide layer and the bulk SiC, and that of the space charge layer:

$$Z_{SS} = R_{ox} + R_{IF} + \frac{1}{j\omega C_{scl} + \frac{1}{R_{ct}}}, \tag{3.7}$$

where, R_{ox} is the resistance of the oxide layer that takes the form of Equation (3.8), C_{scl} is the capacitance of the space charge layer, and is expressed by Equation (3.9), R_{ct} is the resistance of

the space charge layer, and R_{IF} is the resistance of the interface between the oxide layer and the bulk SiC. Since 4H-SiC is an anisotropic crystal, the oxidation rate changes with the orientation, and after generation of etch pits, not only the (0001) face but also the other faces were exposed to the electrolyte. Therefore, the area of the other faces exposed to the electrolyte also increases with an increase in the surface area, resulting to a change in R_{IF}.

Accordingly, R_{IF} can be expressed as a function of surface area by Equation (3.10).

$$R_{ox} = \rho \frac{d_{ox}}{S}, \tag{3.8}$$

$$C_{scl} = \frac{\varepsilon_0 \varepsilon S}{d_{scl}}, \tag{3.9}$$

$$R_{IF} = \alpha \frac{R_{IF0}}{S}, \tag{3.10}$$

where S is the oxidized area of the surface, d_{ox} is the thickness of the oxide layer, ρ is the resistivity of the oxide layer, ε_0 is the dielectric constant of vacuum, ε is the dielectric constant of the space charge layer, d_{scl} is the thickness of the space charge layer, R_{IF0} is the initial resistance of the interface, and α is the scaling factor.

The impedance of the anodic oxidation system can be expressed as

$$Z = R_{SiC} + R_{sol} + \rho \frac{d_{ox}}{S} + \alpha \frac{R_{IF0}}{S} + \frac{d_{scl}^2 R_{ct}}{d_{scl}^2 + (\omega \varepsilon_0 \varepsilon S R_{ct})^2} - j \frac{\omega \varepsilon_0 \varepsilon S d_{scl} R_{ct}^2}{d_{scl}^2 + (\omega \varepsilon_0 \varepsilon S R_{ct})^2}, \tag{3.11}$$

$$|Z| = \sqrt{\left[R_{SiC} + R_{sol} + \rho \frac{d_{ox}}{S} + \alpha \frac{R_{IF0}}{S} + \frac{d_{scl}^2 R_{ct}}{d_{scl}^2 + (\omega \varepsilon_0 \varepsilon S R_{ct})^2}\right]^2 + \left[\frac{\omega \varepsilon_0 \varepsilon S d_{scl} R_{ct}^2}{d_{scl}^2 + (\omega \varepsilon_0 \varepsilon S R_{ct})^2}\right]^2}, \tag{3.12}$$

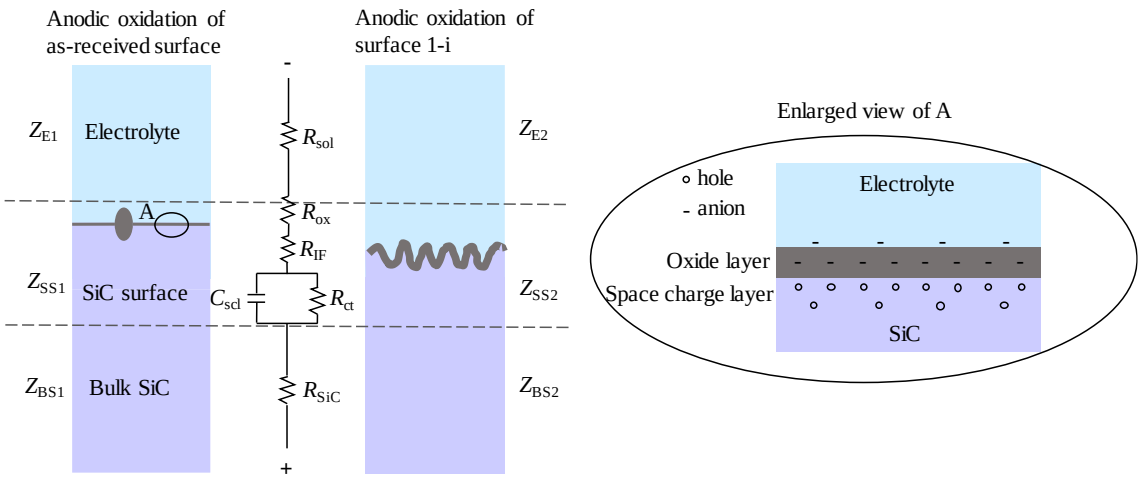

Figure 3.43 Model of anodic oxidation of SiC using the electrochemical impedance method.

where R_{SiC} and R_{sol} are the resistances of the bulk SiC and the electrolyte, respectively, and can be considered as constants in the anodic oxidation process; and ω is the angular frequency of the alternating current, which is 0 in our experiment because a direct current was applied in this study. Further, the impedance transforms to:

$$|Z| = R_{SiC} + R_{sol} + \rho\frac{d_{ox}}{S} + \alpha\frac{R_{IF0}}{S} + R_{ct}, \tag{3.13}$$

Equation (3.13) reflects that the impedance of the anodic oxidation system decreases with an increase in surface area. On account of Ohm's law, the current density also decreases with increasing surface area. During the initial oxidation stage of the as-received surface, the current was very small with the limited damage on the CMP-processed surface, whereas the oxidation area expanded to the whole surface, increasing the current. In the oxidation of surface 1-i, the increase in oxidation area, as shown in Figure 3.43, resulted to a decrease in the impedance of the SiC surface $Z_{SS2,}$ and thus, inducing much higher oxidation rate. The relationship between surface area and current density was investigated in all the oxidation experiments. The area of the oxidized/etched surface was considered as the oxidation area at the end of the final oxidation step, which was calculated using the AFM data processing software over the observation area of 1 μm × 1 μm. The relationship between the surface area and oxidation current density at the end of each oxidation step is displayed in Figure 3.44. The same trend was observed in both sets of experiments, that is, current density changed with the oxidation area, which suggests that the oxidation area has dominant effect on the oxidation rate. The minor differences between the first and second set of experiments in the values of surface areas and current densities may be attributed to the differences in the doping concentrations of the SiC wafers.

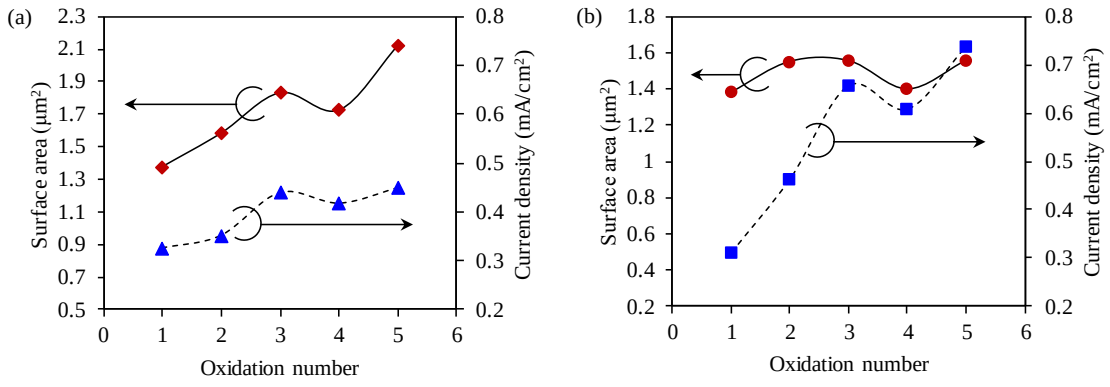

Figure 3.44 Relationship between surface area and oxidation current density. (a) First set. (b) Second set. The surface area is calculated from the AFM images using AFM data processing software, where the observation area is 1 μm × 1 μm.

3.7.2 Formation of porous SiC in the oxidation/etching process

Changes in the surface morphology with the repeated anodic oxidation and HF etching are shown in Figure 3.46. Many etch pits and fibers were observed on the surface. With the progress of oxidation and etching, the fibers became thinner and small etch pits generated in the original etch pits caused the generation of new fibers. Figure 3.46 shows the EDX measurement results of surface 1-i shown in Figure 3.45(a), which clearly indicated the absence of oxide on the surface. Instead, fibers among the etch pits and protrusions at the centers of the etch pits of SiC formed, with such etch pits and SiC fibers constituting the porous SiC. This is suggestive that the pit size and fiber size of porous SiC can be controlled via the anodic oxidation parameters.

Figure 3.47 shows a SEM image of surface 1-ii. Small etch pits were mainly generated along (green arrows) or in the opposite direction (red arrows) to the <1000>, <0100>, and <0010> directions on the SiC protrusions located in the etch pits. 4H-SiC is an anisotropic crystal with higher oxidation rate along these three directions, which results in the generation of hexagonal etch pits in the oxidation/etching process [34–36]. After the first oxidation/etching process, faces (11–20), (−2110), and (1–210) were exposed to the electrolyte with the generation of the etch pits. Moreover, these faces were rapidly oxidized in the second oxidation process, thereby resulting in the expansion of the etch pits and the generation of small etch pits on the SiC protrusions. The generation of small oxide protrusions during the oxidation of surface 1-i, as shown in Figure 3.39(d), was presumed to originate from the preferential oxidation on these faces. This mechanism dominated all the oxidation/etching processes. As a result, porous SiC was still

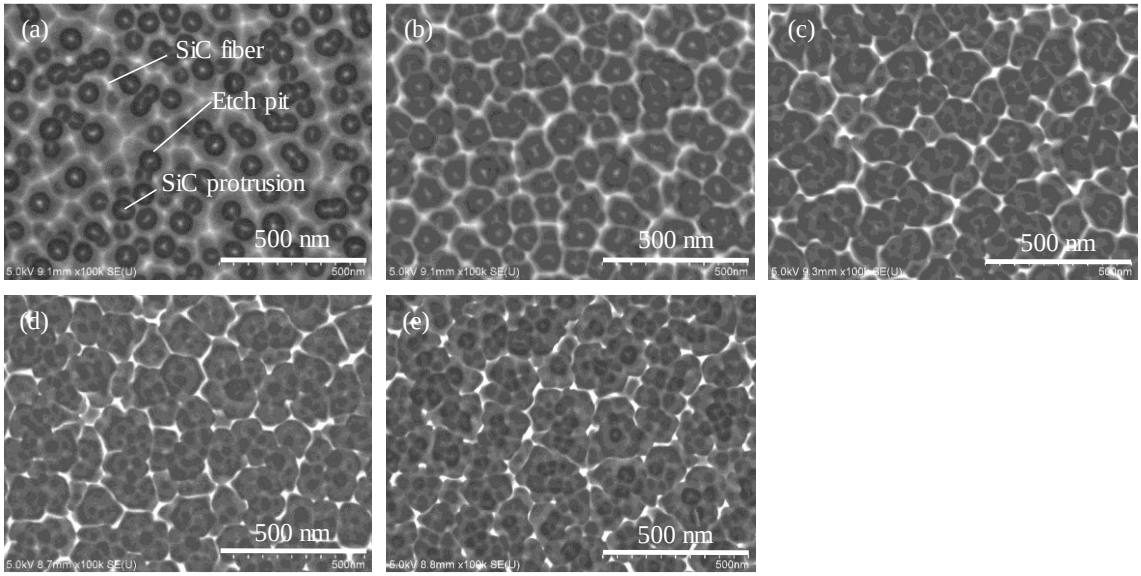

Figure 3.45 SEM images of oxidized/etched surfaces. (a) Surface 1-i. (b) Surface 1-ii. (c) Surface 1-iii. (d) Surface 1-iv. (e) Surface 1-v. Porous SiC is observed.

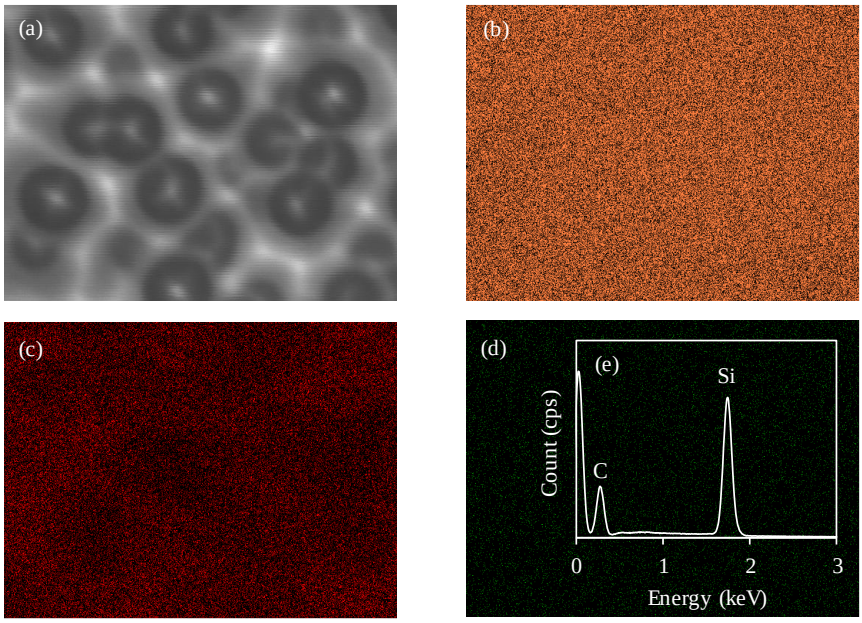

Figure 3.46 EDX measurement results of surface 1-i. (a) SEM image of surface 1-i. (b) Distribution map of silicon element. (c) Distribution of carbon element. (d) Distribution of oxygen element. (e) Element spectrum of surface 1-i. Oxygen is not observed on surface 1-i.

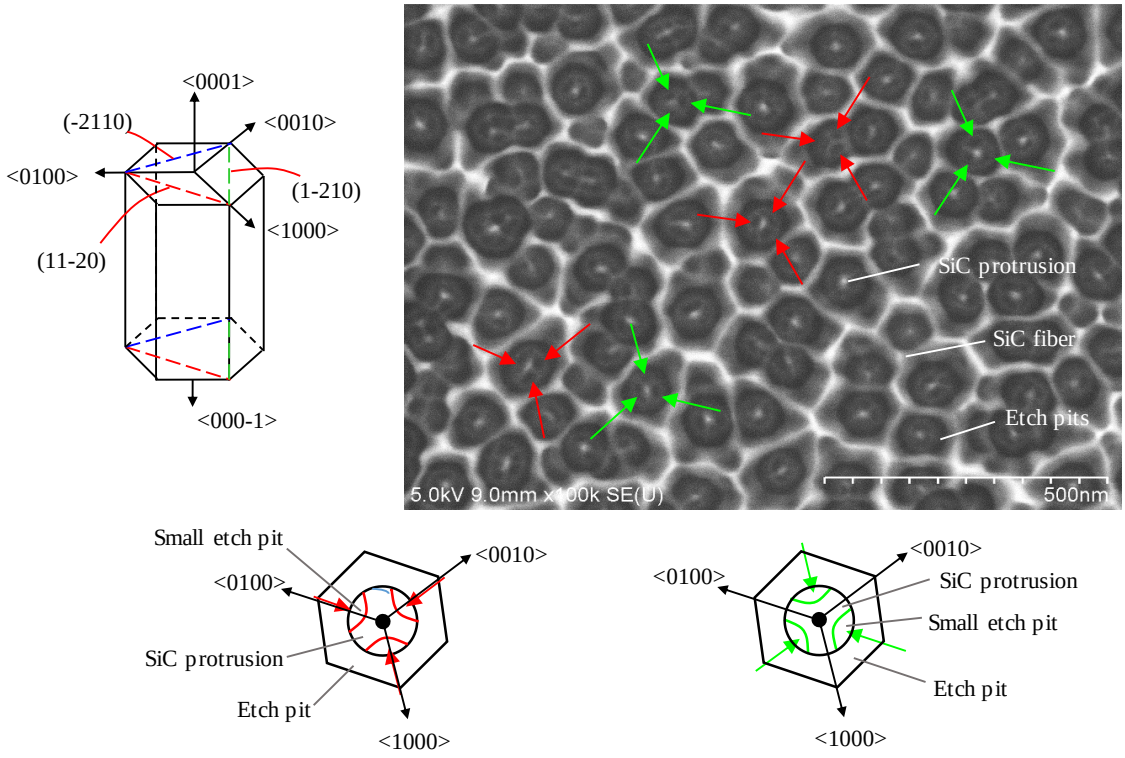

Figure 3.47 SEM image of surface 1-ii. Small etch pits are mainly generated along (green arrows) or in the opposite direction (red arrows) to the <1000>, <0100>, and <0010> directions on the SiC protrusions.

observed even after five times of oxidation/etching, as shown in Figure 3.45(e), which suggests that the structure of porous SiC is significantly dependent on the etch pits generated at the beginning of the oxidation process, and that an atomically smooth surface cannot be obtained by repeated anodic oxidation and etching.

Changes in the surface roughness *Sz* with the progress of oxidation and etching observed by AFM are shown in Figure 3.48. Apparently, *Sz* increased during the entire experiment due to a few remaining unchanged SiC fibers with the repeated anodic oxidation and etching. Figure 3.49 shows the SEM images of surfaces 2-iv and 2-v. Although these surfaces were oxidized for a longer time of 10 min, a few high height of SiC fibers were still observed on the surface, and the surface roughness *Sz* was greater than that of surfaces 1-iv and 1-v that were oxidized for only 1 min. These results reflect the difficulty in oxidizing the SiC fibers.

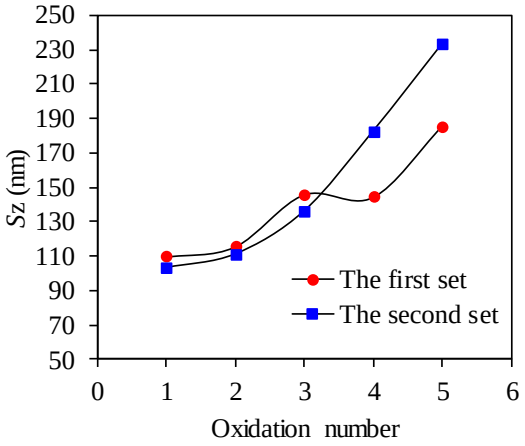

Figure 3.48 Changes in surface roughness with the progress of oxidation and etching obtained by AFM over an observation area of 1 μm × 1 μm. The surface roughness increases with the progress of oxidation and etching.

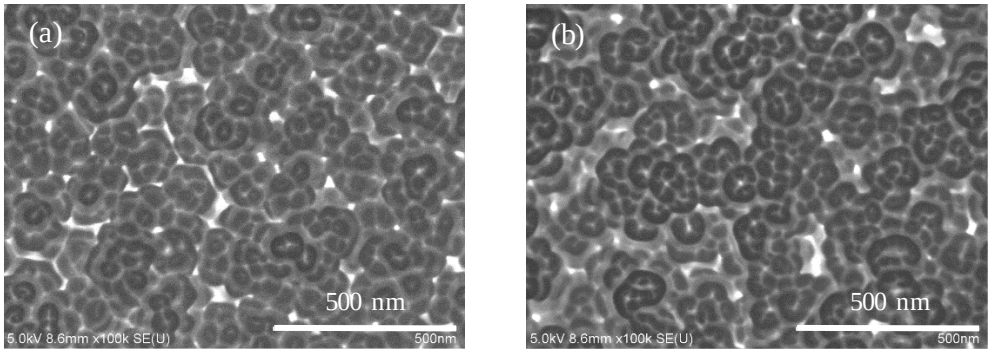

Figure 3.49 SEM images of oxidized/etched surfaces in the second set of experiments. (a) Surface 2-iv. (b) Surface 2-v. Many SiC fibers remain on the surface and are difficult to oxidize.

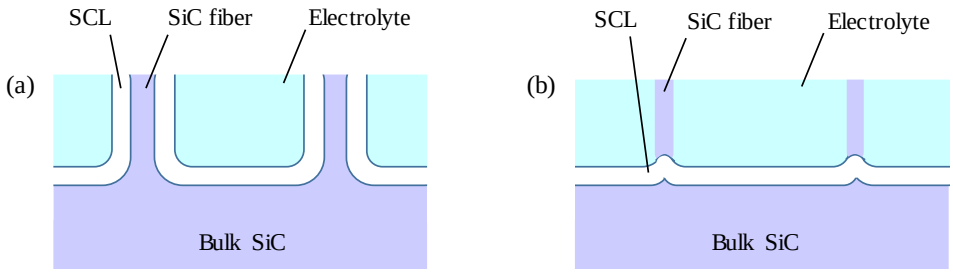

Figure 3.50 Structure of the space charge layer (SCL) when the thickness of the SiC fiber is (a) large and (b) small [37].

Such difficulty in dissolving nanometer-thick SiC fibers was attributed to the Fermi level pinning on the fibers [37], as shown in Figure 3.50. As soon as each SiC fiber became thin, the space charge layer on both sides of the SiC fiber merged and formed a space charge layer passing through the bottom of the SiC fiber, which then caused electrical isolation of the main part of the SiC fiber from the crystal. Therefore, further fiber oxidation became impossible, and the thin SiC fiber remained stable. Thus, the porous SiC was presumed to have formed from the anisotropic oxidation of SiC and the difficulty of dissolving nanometer-thick fibers.

3.8 Strategy for obtaining smooth SiC surface using slurryless ECMP

The results in the preceding subsections reflect that generation of oxide protrusions is inevitable, regardless of whether the anodic oxidation type is constant potential or constant current. Besides, the surface roughness of the oxidized SiC surface after removal of the oxide layer went worse with longer oxidation time, and became rough with repeated anodic oxidation and HF etching. The initial oxidation period of the SiC surface was dominated by the distribution of subsurface damage on the SiC wafer, then was dominated by the anisotropy of single-crystal 4H-SiC after the subsurface damage had been completely oxidized. For both types of oxidation, the surface roughness increased with increase in oxidation time. These results indicate that a smooth SiC surface cannot be obtained by anodic oxidation, and the combination of anodic oxidation and mechanical polishing is very important to obtain smooth SiC surfaces.

Accordingly, because the soft abrasives only remove the oxide layer in ECMP, the smoothness of the interface between the oxide layer and bulk SiC is critical for obtaining a smooth SiC surface. Moreover, as the surface roughness of oxidized SiC becomes rougher with increasing oxidation time, the oxide layer on the SiC surface should be removed immediately if a smooth surface is to be obtained. The strategy for obtaining a smooth SiC surface by slurryless ECMP is

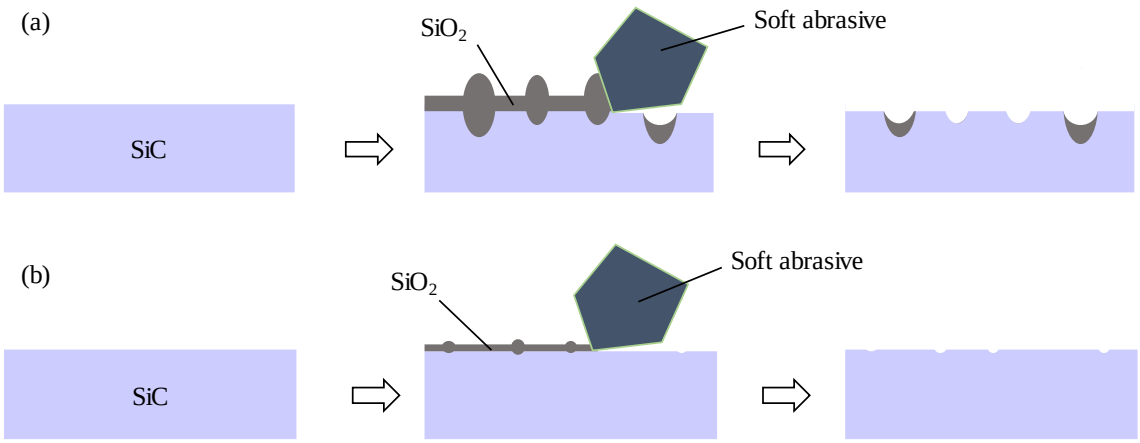

Figure 3.51 Strategy for obtaining smooth SiC surface by slurryless ECMP. Model of ECMP process in the conditions of (a) oxidation rate > polishing rate of oxide layer, and (b) oxidation rate <= polishing rate of oxide layer.

introduced in Figure 3.51. Here, if the oxide layer becomes thicker during the ECMP process, a rough surface is normally obtained, as depicted in Figure 3.51(a). On the contrary, a smooth surface would be obtained, if the oxide layer is removed when it is very thin, as shown in Figure 3.51(b). Thus, it is essentially important to control the balance between the anodic oxidation rate and the removal rate of the oxide layer to obtain a smooth SiC surface via slurryless ECMP.

3.9 Summary

This chapter presented and confirmed the anodic oxidation of 4H-SiC (0001) surfaces in neutral electrolytes, as well as the softening effect of anodic oxidation. It also detailed on the investigation of the anodic oxidation properties and mechanism of 4H-SiC (0001) surface. The results of these investigations were taken into account to formulate a strategy for obtaining a smooth SiC surface with slurryless ECMP. The main points of the chapter can be generalized as follows.

(1) Anodic oxidations of 4H-SiC (0001) surfaces were performed in NaCl and $NaNO_3$ aqueous solutions. XPS analysis confirmed that the surfaces were anodically oxidized in both solutions, although oxidation was not uniform and resulted to the increase in surface roughness after removal of the oxide layer. The difference between the anodic oxidations in these two electrolytes was very small and an oxidation rate of approximately 40 nm/min was obtained, but the NaCl solution exhibited higher efficiency of electric energy.

(2) The softening effect of anodic oxidation was confirmed, with SiC hardness significantly decreasing from 41.98 to 3.59 GPa after anodic oxidation. Although the anodic oxide layer, synthetic quartz glass, and borosilicate glass mainly composed of SiO_2, it was found that the anodically oxidized surface was softer than these glass materials.

(3) LSV measurement was applied to investigate the relationship between the oxide protrusions and the oxidation potential. It revealed an *I–V* curve for SiC that is similar to that of general metal anodization having five oxidation periods, namely, unoxidized state, active state, passive state, transient state, and transpassive state.

(4) Oxide protrusions were observed as SiC was oxidized in the transient and transpassive states. These were generated from the sites of breakdown on the passivation film. Moreover, their density increased while their diameter and volume decreased, with an increase in potential (current). Besides, almost the same oxidation degree of scratches and areas without scratches were obtained in high oxidation current densities. This points out that for an abrasive-polished SiC substrate subjected to the ECMP process, the surface should be oxidized under high oxidation rate to fully remove the damaged layer on the surface. Subsequently, the surface should be polished at a low potential corresponding to the passive state, to avoid the generation of etch pits, as well as to obtain an atomically smooth surface.

(5) Investigation of the time dependence of anodic oxidation of SiC revealed that the anodic oxidation of SiC continues with oxidation time, even lasting for 10 h. This was because the outer oxide layer becomes porous and accommodates several cracks with the volume expansion of SiC after anodic oxidation for a certain time. The surface roughness of the oxidized surface after the oxide layer has been removed increased with oxidation time in both constant potential and constant current anodic oxidation.

(6) Results of the investigation of the off-angle dependence of anodic oxidation of SiC confirmed that the oxidation rate of 4H-SiC increases with greater off-angle as the oxidation of SiC surface originates from the terrace edges. Additionally, 4H2 terraces demonstrated higher oxidation rate than 4H1 terraces.

(7) The oxide protrusions originated from atomic pits introduced by large abrasive particles or a high polishing pressure during the CMP process. Depending on their geometric structure, these atomic pits could have different breakdown thresholds. The SSD induced by indenter was preferentially oxidized compared with the atomic pits.

(8) Through modeling of the growth process of the oxide protrusions, the growth process was found to be controlled by the charge transfer process at the initial stage, which changed to a diffusion process after the oxide protrusions grew to the size order of 100 nm.

(9) Repeated anodic oxidation and HF etching were conducted on a 4H-SiC (0001) face, with which the effects of surface damage on the anodic oxidation properties were investigated. Anodic oxidation proved very effective for removing the surface damage formed by mechanical polishing. The surface was easier to oxidize after removal of the surface damage by oxidation/etching; moreover, the oxidation became relatively uniform. This is favorable for obtaining a SiC substrate with a smooth surface by slurryless ECMP.

(10) Changes in current were different in the anodic oxidations of surfaces with and without SSD. A model based on the electrochemical impedance method was built to dig deeper on such differences; the results of such investigation revealed that the oxidation area and the anisotropy of 4H-SiC plays a dominant role in determining the oxidation rate of the SiC surface.

(11) Porous SiC was generated in the repeated anodic oxidation and etching of 4H-SiC (0001) surfaces. It was mainly caused by the anisotropy of the SiC crystal and the Fermi level pinning that occurred on the nanometer-thick SiC fibers. The structure of the porous SiC was significantly dependent on the etch pits generated at the beginning of the oxidation, and can be controlled via the anodic oxidation parameters.

(12) Surface roughness increased with repeated anodic oxidation and HF etching. The initial oxidation period of the SiC surface was dominated by the distribution of SSD on the SiC wafer, and then by the anisotropy of single-crystal 4H-SiC after the subsurface damage had been completely oxidized. For both types of oxidation, the surface roughness increased with longer oxidation time.

(13) A strategy has been proposed for obtaining smooth SiC surface using slurryless ECMP, as a smooth surface is not attainable by a combination of anodic oxidation and HF etching alone, and because the surface roughness of oxidized/etched surface increases with oxidation time. To obtain a smooth surface, it is presumed that the oxide layer should be immediately removed after its generation, that is, the removal rate of the oxide layer should be greater than the anodic oxidation rate in slurryless ECMP.

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Chapter 4
Application of slurryless ECMP to 4H-SiC wafers

4.1 Introduction

As a brief review, an investigation of the oxidation properties and mechanism of 4H-SiC (0001) surface in Chapter 3 demonstrated that anodic oxidation of SiC is not uniform, and that an atomically smooth surface is not attainable with only a combination of anodic oxidation and HF etching. The proposed strategy then is to remove the oxide layer immediately after its generation. To verify this assumption and realize the effectiveness of slurryless ECMP of SiC wafers, the present chapter presents the development of a slurryless ECMP machine, followed by a comparison of the performance of two-step and simultaneous ECMP using this machine. A suitable grinding stone is selected for the slurryless ECMP of SiC surfaces. Due to the high efficiency of slurryless ECMP, it is applied to sliced 4H-SiC (0001) surfaces, and then its performance is evaluated. Finally, the ECMP process is optimized in order to deliver an atomically smooth surface.

4.2 Development of slurryless ECMP machine

Anodic oxidation and mechanical polishing are two basic but essential functions for realizing the slurryless ECMP of SiC wafers, and should be organically combined when utilizing the ECMP machine. In addition, electrolyte leakage must be completely eliminated, in order to validate the anodic oxidation of SiC wafers. The proposed slurryless ECMP meeting such requirements is shown in Figure 4.1. The SiC wafer was fixed on a copper plate installed on an insulating base to serve as a WE. The tip of a spindle was used as a CE. A grinding stone was mounted on the tip of the spindle and in contact with the SiC surface. The SiC surface, grinding stone, and the tip of the spindle were immersed in the electrolyte. A potentiostat was applied to control the anodic oxidation parameters to anodizing the SiC surface. A load was applied on the spindle as the grinding stone was rotated with a specific speed to remove the oxide layer during the anodization process. This way, slurryless ECMP could be realized.

The designed prototype slurryless ECMP machine is as shown in Figure 4.2. Its polishing section was placed on a base plate, and the load system and motion system were installed on a sliding board, which can vertically move up and down using a screw. The spindle was set in a

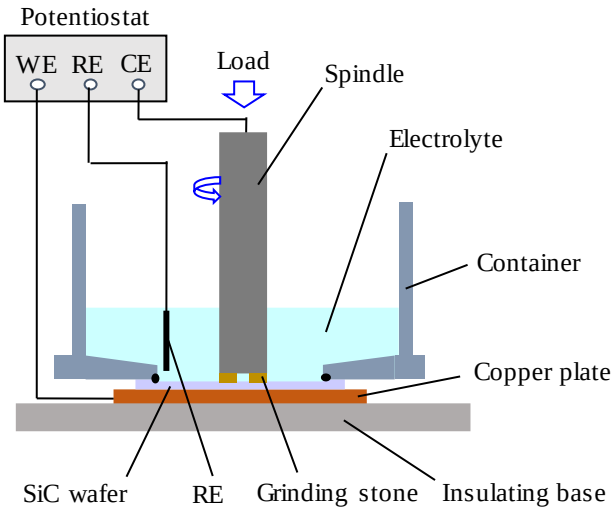

Figure 4.1 Schematic diagram of slurryless ECMP.

sleeve, its radial position fixed by spline with clearance fit; thus, it can move in the sleeve freely along the axial direction, as shown in Figure 4.2(b). The sleeve was driven by a motor through a conveyor belt. Thus, the spindle can rotate with the sleeve at the same rotation speed as it moves freely along the vertical direction, which allows the polishing pressure to be applied by placing weight on the fixed weight placement on the spindle's top. To accurately control the polishing pressure, the weight of spindle system was balanced by a counter weight.

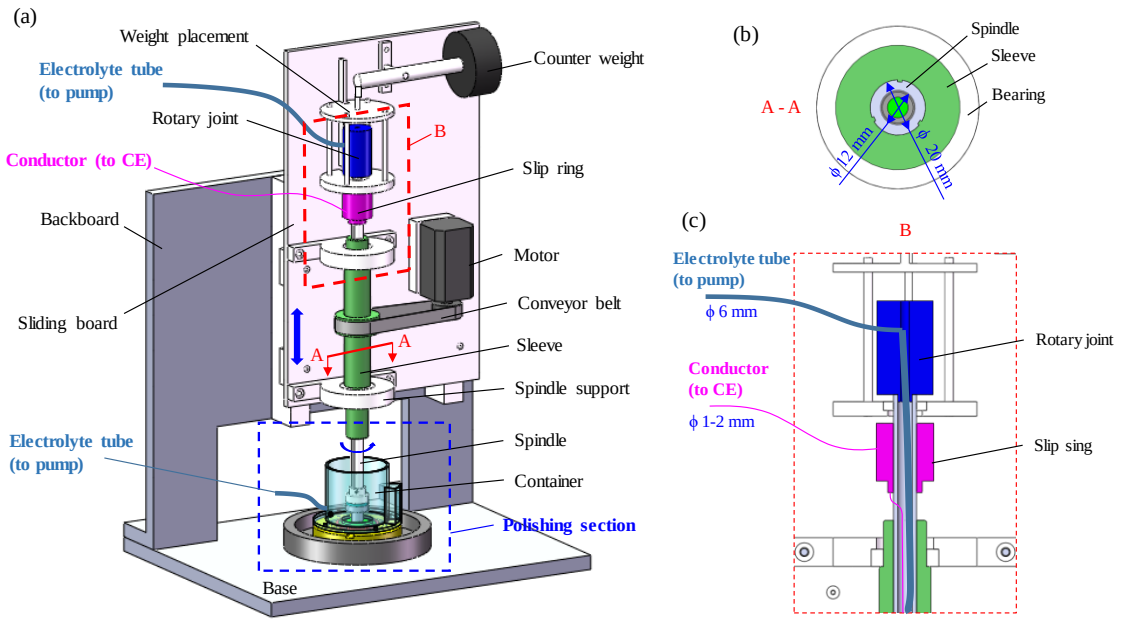

Figure 4.2 Schematic of prototype slurryless ECMP machine. (a) Schematic diagram of slurryless ECMP machine. Cross-sectional views (b) along A–A in (a), and (c) of part B in (a).

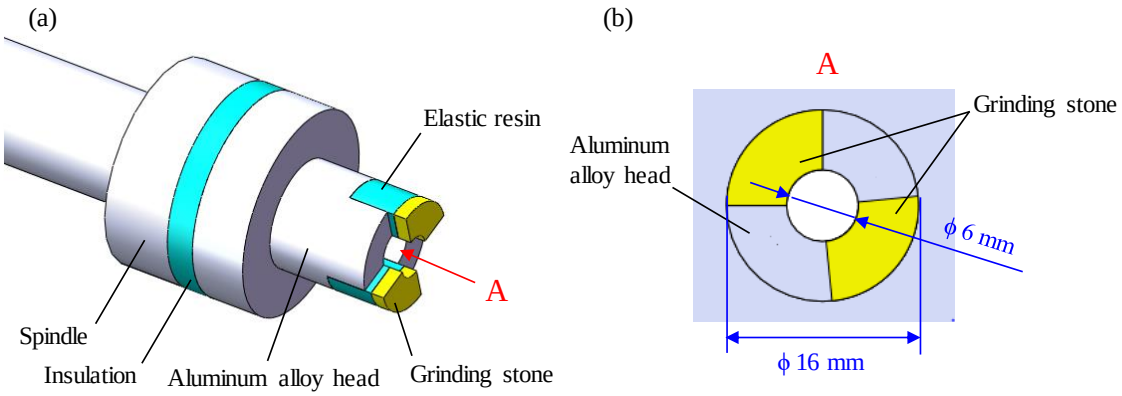

Figure 4.3 The polishing head. (a) Overall view of the polishing head. (b) View of the polishing head in direction A.

The tip of the spindle was used as CE; it rotates with the spindle during ECMP. Therefore, a hollow spindle and a slip ring were applied to prevent the electrolyte from being ejected from the polishing area by the centrifugal force of the spindle. During ECMP, the electrolyte was circulated by a peristaltic pump and supplied from the spindle's center. Moreover, a rotary joint for supplying the electrolyte, as shown in Figure 4.2(c), was used.

The polishing head of the prototype slurryless ECMP machine is displayed in Figure 4.3. An insulation material was applied between the spindle and the polishing head serving as the CE. Two elastic resins with quarter-circle shape were set between the polishing head and the grinding stone, to automatically adjust the tilt between the SiC substrate and the grinding stone.

Figure 4.4 shows the cross-sectional view of the polishing section. The SiC wafer was fixed on a copper plate installed on an insulating base and served as a WE. A part of the wafer was exposed through the aperture of the machining base plate and was allowed to be in contact with the electrolyte. The electrolyte was kept by a container, with O rings applied to prevent it from leaking. To keep the solution in RE clean, RE was set out of the container; it was connected to the electrolyte through a small hole in the machining base plate. The electrolyte was supplied from the tube set in the center of the spindle, and drained from the side of the container. This way, the anodic oxidation of SiC surface could be realized via an application of a positive potential on the copper plate, and accurately controlled by the potentiostat. By controlling the load and rotation speed of the spindle, anodic oxidation and mechanical polishing could be effectively combined.

Figure 4.5 shows the developed slurryless ECMP machine.

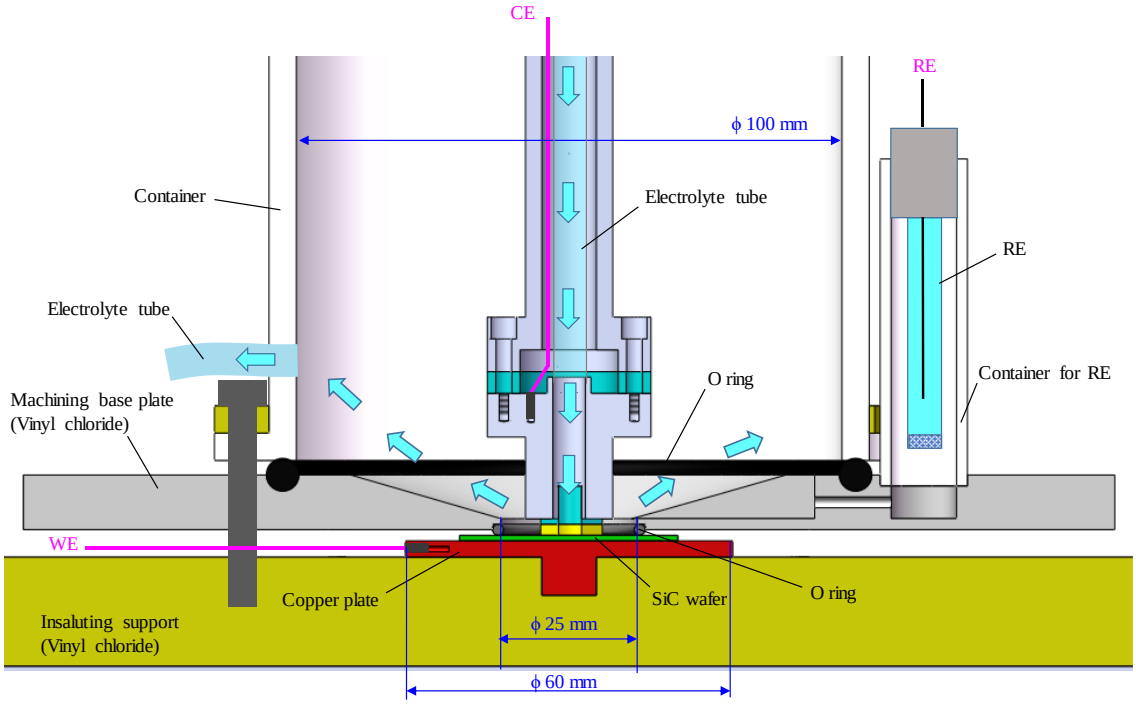

Figure 4.4 Specific design of the polishing head.

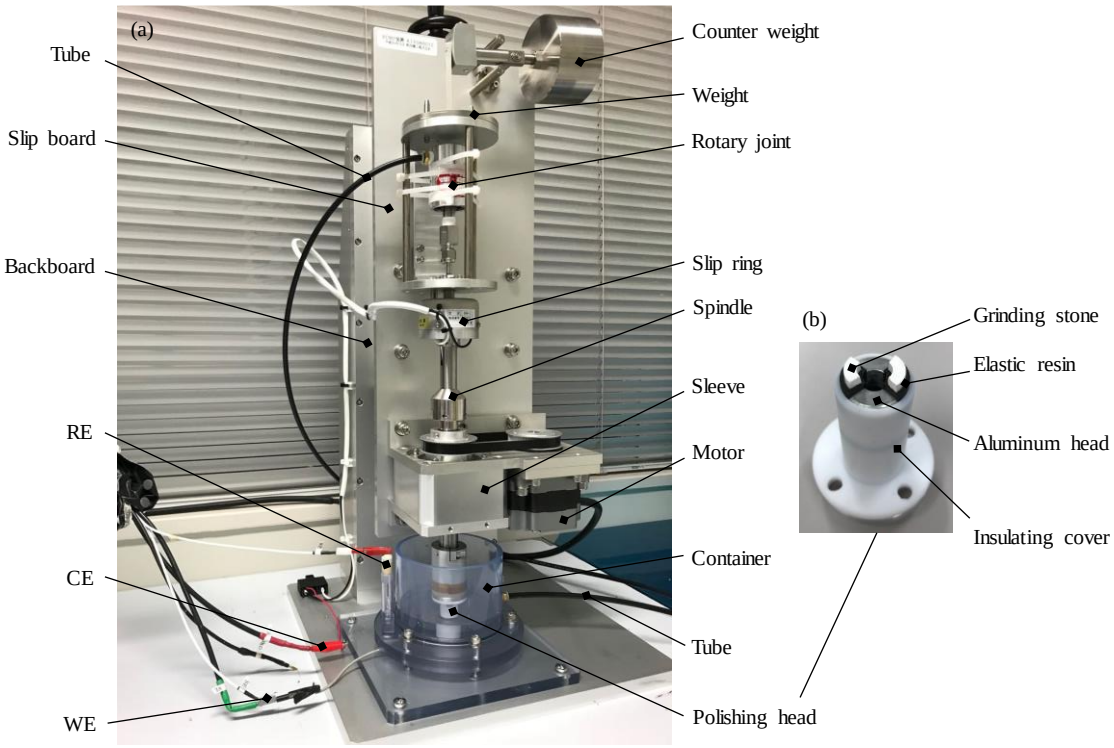

Figure 4.5 Photographs of (a) developed slurryless ECMP machine and (b) its polishing head.

4.3 Two-step and simultaneous slurryless ECMP

Using the developed ECMP machine, two-step and simultaneous ECMP were conducted to verify the results and assumptions laid out in Chapter 3. In the two-step ECMP, the anodic oxidation of SiC surface and the mechanical polishing of the oxide layer were conducted separately. In contrast, they were simultaneously conducted in the simultaneous ECMP. Commercially available single-crystal 4H-SiC substrates (3 inch, 4°-off, N-type) were employed in this study. Both faces of each substrate were prepared by two-step diamond lapping. Each face was primarily lapped with a #4000 diamond grinding plate (average particle size of 3 μm) for 10 min at a pressure of 19.6 kPa; it was secondarily lapped with a #20000 diamond grinding plate (average particle size of 0.3 μm) for 30 min at the same pressure. ECMP was conducted on the Si face of the substrate. Table 4.1 shows the simultaneous ECMP parameters. Sodium chloride (NaCl) aqueous solution with 1-wt% concentration and 1.8-S/m electrical conductivity was used as the electrolyte, and a current of constant density of 0.2 mA/cm^2 was applied during the anodic oxidation. Polishing was performed at 140 kPa of pressure and 500 rpm of spindle rotation speed. The anodic oxidation and polishing parameters in the two-step ECMP were same as in the simultaneous ECMP, but the processes were conducted separately, as shown in Tables 4.2 and 4.3.

Table 4.1 Simultaneous ECMP parameters

Current density (mA/cm^2)	0.2
Spindle rotation speed (rpm)	500
Polishing pressure (kPa)	140
Polishing time (min)	30
Grinding stone	Vitrified-bonded ceria (#8000)
Electrolyte	1 wt% NaCl aqueous solution

Table 4.2 Oxidation parameters for two-step ECMP

Current density (mA/cm^2)	0.2
Spindle rotation speed (rpm)	500
Polishing pressure (kPa)	0
Polishing time (min)	30
Electrolyte	1 wt% NaCl aqueous solution

Table 4.3 Polishing parameters for two-step ECMP

Current density (mA/cm^2)	0
Spindle rotation speed (rpm)	500
Polishing pressure (kPa)	140
Polishing time (min)	30
Grinding stone	Vitrified-bonded ceria (#8000)
Electrolyte	1 wt% NaCl aqueous solution

Figure 4.6 shows the scanning white microscopic interferometry (SWLI) images of the surface after the simultaneous ECMP and the two-step ECMP, as well as their cross-sectional views. It can be observed that although the removal of the SiC surface in the simultaneous ECMP was uneven, the cross-section along the polishing direction suggests the formation of small surface roughness. In the case of two-step ECMP, several pits formed on the surface; as shown in the B–B' sectional view in Figure 3(d), the surface was very rough compared to that obtained by the simultaneous ECMP.

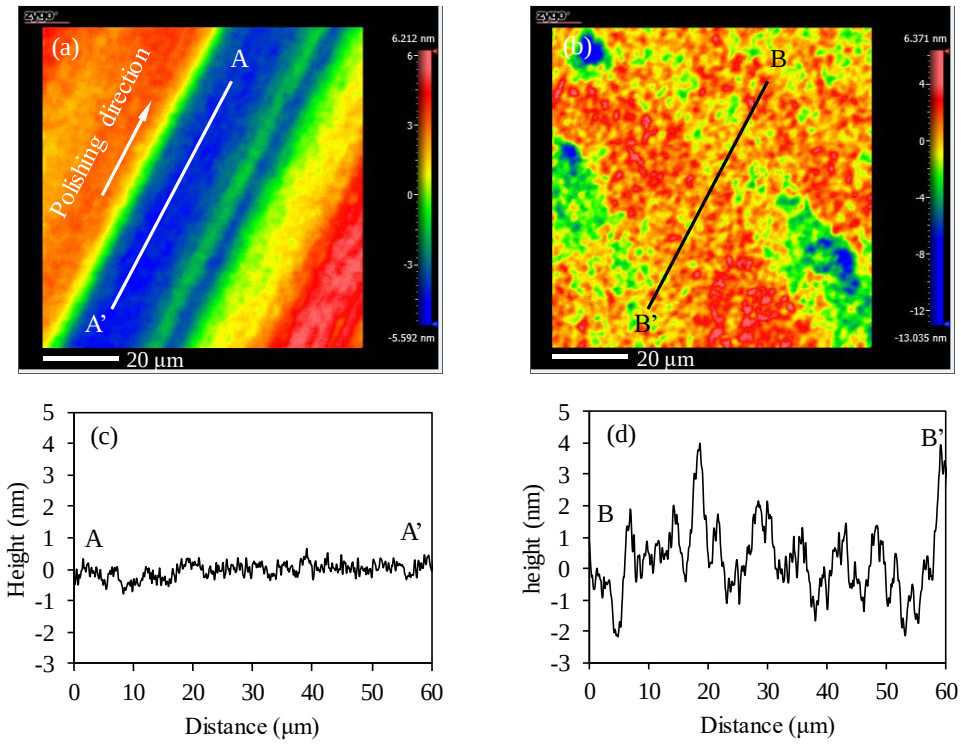

Figure 4.6 Results of simultaneous ECMP and two-step ECMP. SWLI images of surface processed by (a) simultaneous and (b) two-step ECMP. Cross-sectional views of (c) simultaneous ECMP-processed surface along A–A' and (d) two-step ECMP processed surface along B–B'.

To further investigate the surfaces obtained by the simultaneous and two-step ECMPs, the processed surfaces were measured by AFM for an observation area of 5 μm × 5 μm. AFM images of the surfaces processed by both ECMP methods are illustrated in Figure 4.7. Note that although global flatening of the SiC surface was not obtained, local flatterning of the surface, with a *S*q surface roughness of 1.191 nm, was obtained in simultaneous ECMP, as evidenced in Figure 4.7(a). In the case of the two-step ECMP, a rough surface, with a *S*q surface roughness of 7.611 nm, was still observed even in the small observation area. These results verify those results in Chapter 3 stressing that a smooth surface is unattainable using only a combination of anodic oxidation and etching, which necessitates the mechanical polishing of the oxide layer in order to obtain a smooth SiC surface.

Accordingly, Figure 4.8 shows the XPS measurement results of the surfaces processed by both ECMP methods. Removal of oxide layers was similar in each ECMP. A weak peak corresponding to Si–C bonds was obseved in both ECMP-processed surfaces, whereas, a strong peak and a relatively stronge peak corresponding to Si–C–O and Si–O bonds were also observed, indicating that the oxide layer was not completely removed. Highly magnified SEM images of the polished surfaces are presented in Figure 4.9. Several pits appeared on both surfaces processed by the simultaneous and two-step ECMP; nonetheless, the size of the pits on the surface polished by simultaneous ECMP was smaller and the density of the pits was higher, as compared to those on the surface polished by two-step ECMP, thus, the simultaneous ECMP achieved a smoother surface. Moreover, as fixed soft abrasives were applied to remove the oxide layer, the removal of oxide in the pits was more difficult than in the other areas due to the lower polishing pressure. This factor made it difficult to completely remove the oxide layer.

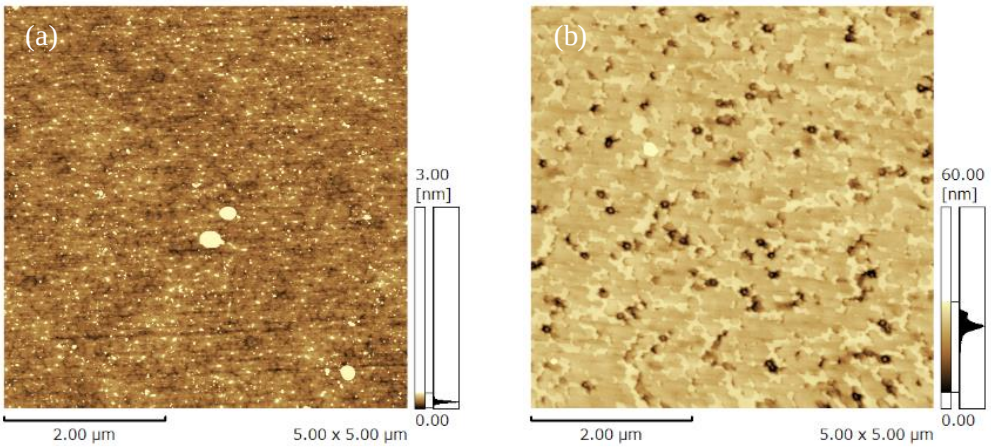

Figure 4.7 AFM images of surfaces processed by (a) simultaneous ECMP, *S*a = 0.366 nm, *S*q = 1.191 nm, *S*z = 42.313 nm, and (b) two-step ECMP, *S*a = 4.854 nm, *S*q = 7.611 nm, *S*z = 133.626 nm.

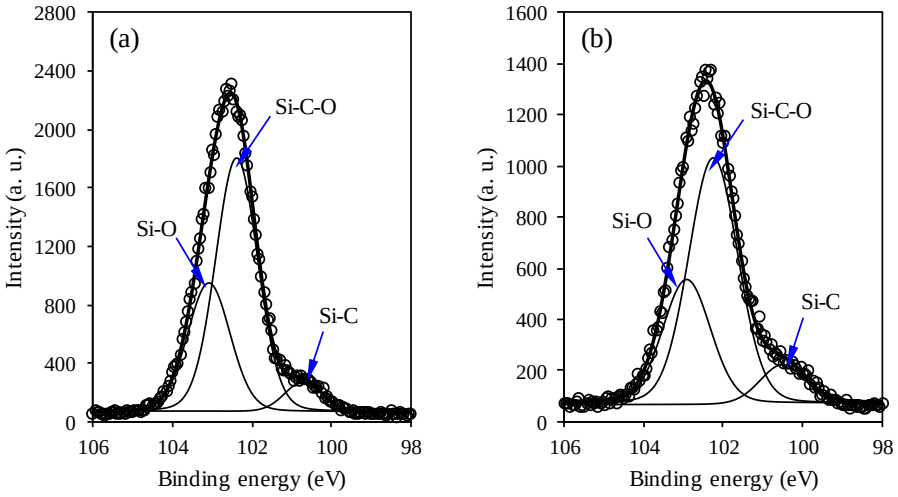

Figure 4.8 Si 2p XPS spectra of surfaces processed by (a) simultaneous ECMP and (b) two-step ECMP measured with a take-off angle of 45°.

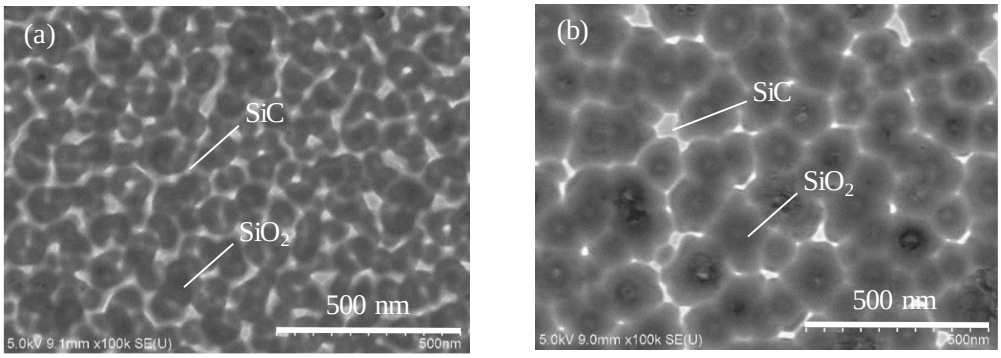

Figure 4.9 SEM images of surfaces processed by (a) simultaneous ECMP and (b) two-step ECMP.

Laser microscopy images of the ceria grinding stone before and after ECMP are shown in Figure 4.10. Prior to ECMP, many scratches appeared on the surface of grinding stone, as reflected in Figure 4.10(a). Such scratches were induced as the grinding stone was dressed by a diamond dresser (#100). After ECMP, some areas on the surface of the grinding stone appeared white, as indicated in Figure 4.10(b). The enlarged laser microscopy images of areas A and B (the white area) are displayed in Figures 4.10(c) and (d), respectively, the *S*q and *S*z surface roughness that were greatly decreased, which indicates that the white area became flat and smooth after ECMP. In particular, only the white areas were in contact with the SiC surface during ECMP, thereby resulting to the non-uniform polishing of the SiC surfaces, and to the difficulty in removing the oxide on the surface. Hence, there is a need to optimize the polishing motion in the ECMP machine to realize the uniform polishing of the SiC surface.

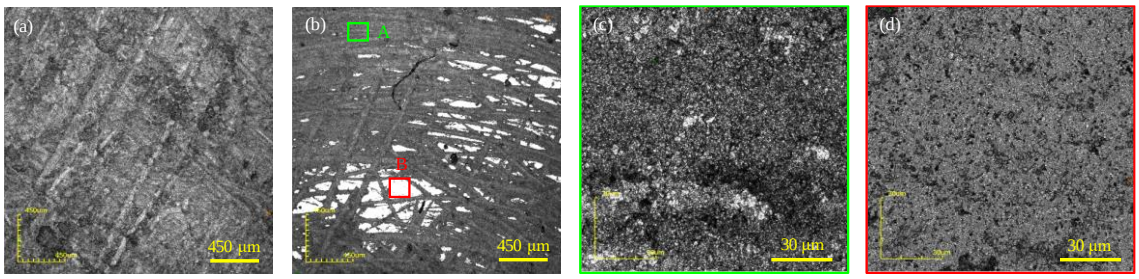

Figure 4.10 Laser microscopy images of the ceria grinding stone (a) before ECMP and (b) after ECMP. Enlarged images of (c) area A, *Sq* = 1.991 μm, *Sz* = 13.629 μm, and (d) area B, *Sq* = 0.175 μm, *Sz* = 4.559 μm, in (b).

The polishing motion should be complex for the SiC surface to be more uniformly polished. With this notion, X and Y stages were added under the base plate of the ECMP machine, as shown in Figure 4.11. During ECMP, the SiC wafer can move along the *x* or *y* direction, while the grinding stone rotates with the spindle, thus, the shape of the area polished by the grinding stone can be changed to different shapes by controlling the motion of both the X and Y stages. This way, improvements in polishing uniformity and removal of oxide layer can be expected.

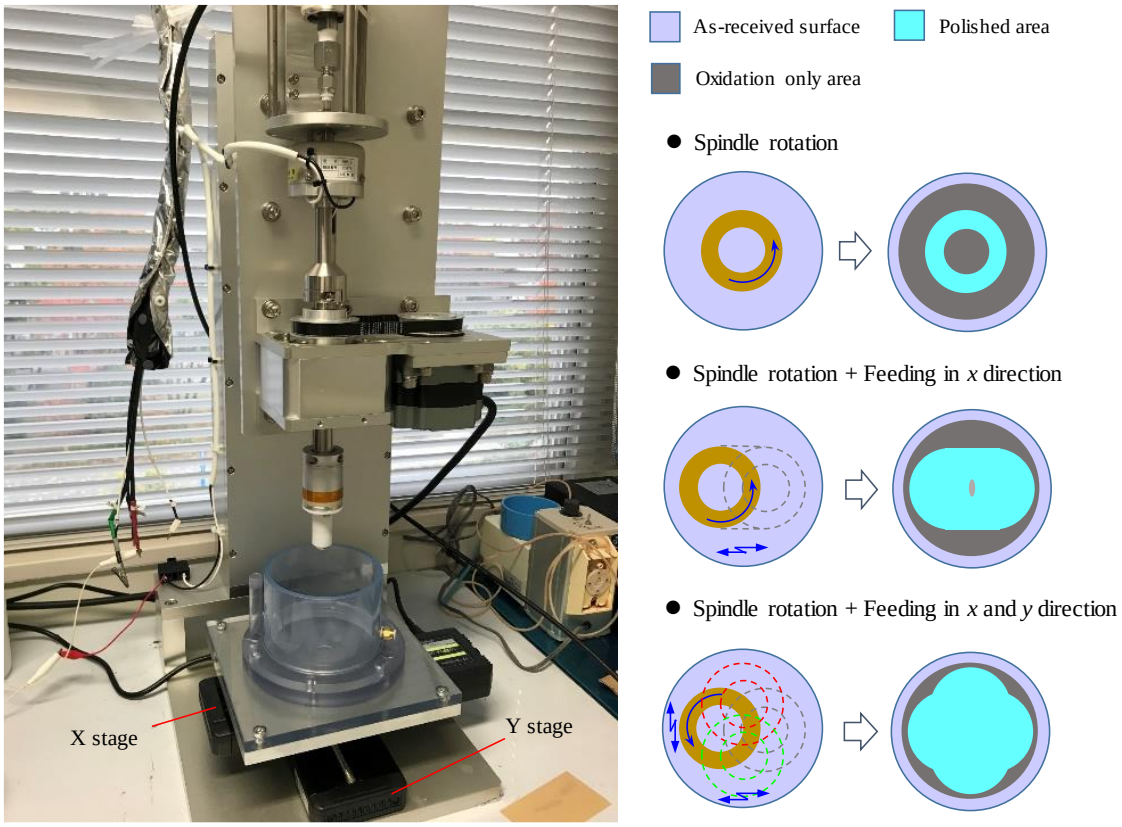

Figure 4.11 Optimization of relative motion in ECMP machine.

4.4 Polishing properties of different grinding stones

Three types of grinding stone, namely, ceria, silica, and alumina, were applied to polish the diamond-lapped 4H-SiC (0001) surfaces. The purpose is to determine which grinding stone is suitable for the slurryless ECMP of the SiC surface. The 4H-SiC substrates (on-axis, N-type) were supplied by TankeBlue Semiconductor Co., Ltd.; they had a thickness of 360 μm and a specific resistance in the range of 0.015–0.028 Ω·cm. The grinding stones with an average particle size of 1 μm (#8000) were vitrified bonded and supplied by MIZUHO Co., Ltd. A two-electrode system controlled by a DC power source was applied to control the anodic oxidation parameters. The ECMP parameters are shown in Table 4.4. ECMP with a constant current density of 2 mA/cm^2 were performed on the diamond-lapped surfaces for 90 min.

In this experiment and the other polishing experiments in this study, since the polished areas in each individual experiment were the same, the material removal rate (MRR) is defined by the removal depth of the processed surface per unit of time as

$$\mathrm{MRR} = \frac{d_\mathrm{p}}{t}, \tag{4.1}$$

where d_p is the polishing depth of the polished area, and t is the polishing time.

Figure 4.12 shows the results of ECMP with different grinding stones. The polished surfaces were measured by SWLI and the depths of polishing areas were measured using the stylus profiler. Figures 4.12(a), (b), and (c) show the SWLI images of surfaces polished with ceria, alumina, and silica grinding stones, respectively. It is clear that the surface polished with the ceria grinding stone had the smallest surface roughness. Several polishing marks appeared on the surface polished with the alumina grinding stone that significantly increased the surface roughness. From the cross-sectional views of the areas polished with the three types of grinding stone shown in Figure 4.12(d), polishing depths of, respectively, 2–3 and 4–5 μm, were obtained using the ceria and alumina grinding stones, whereas the oxide layer was hardly removed with the silica grinding stone.

The Vickers hardness of alumina was 12–23 GPa [1)], much greater than that of ceria (5–7.5 GPa [2)]) and silica (7.6 GPa [3)]) but comparable to that of SiC (24–28 GPa [4)]). Therefore, in the case of using the alumina grinding stone, scratches were presumably formed on the SiC wafer due to the hardness of alumina being close to that of SiC, as shown in Figure 4.12(b). On the other hand, although silica and ceria have equivalent hardness, the MRR with the former was much lower than with the latter. Also, because SiC was oxidized to silicon dioxide and silicon oxycarbides during anodic oxidation [5)], the characteristics of the oxide layer are considered similar to those of quartz glass. Therefore, to study their differences, a polishing experiment was performed on a

Table 4.4 ECMP of 4H-SiC (0001) surfaces with different grinding stones

Current density (mA/cm^2)	2 (two-electrode system)
Spindle rotation speed (rpm)	1000
Polishing pressure (kPa)	140
Polishing time (min)	90
Grinding stone	Vitrified-bonded ceria, alumina, silica
Particle size (μm)	1 (#8000)
Electrolyte	1 wt% NaCl aqueous solution

quartz glass substrate under the same conditions (Table 4.4) without electricity for 30 min, using the three types of grinding stone.

The polishing results for the quartz glass substrates are shown in Figure 4.13. Note that the alumina grinding stone yielded the highest MRR of approximately 36 μm/h, which was twice

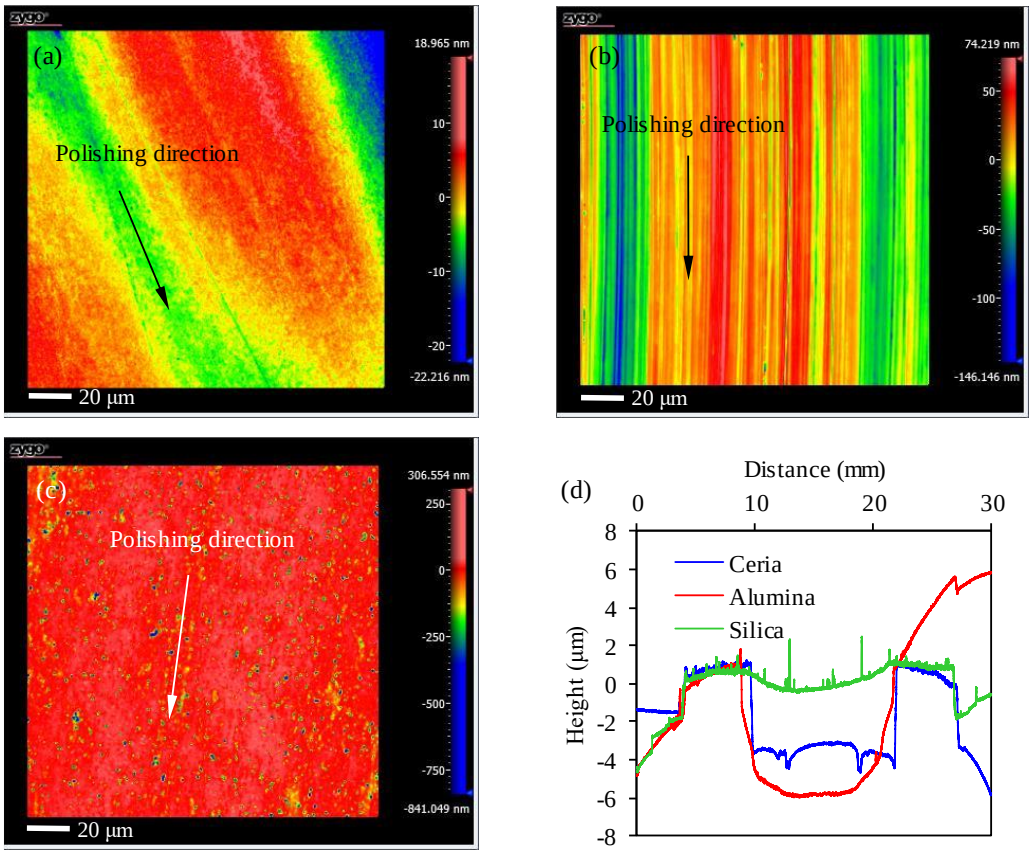

Figure 4.12 SWLI images of 4H–SiC surfaces processed using (a) ceria, *S*q = 4.229 nm; (b) alumina, *S*q = 56.649 nm; and (c) silica, *S*q = 32.914 nm as grinding stones. (d) Cross-sectional views of polishing areas after ECMP with the three grinding stones.

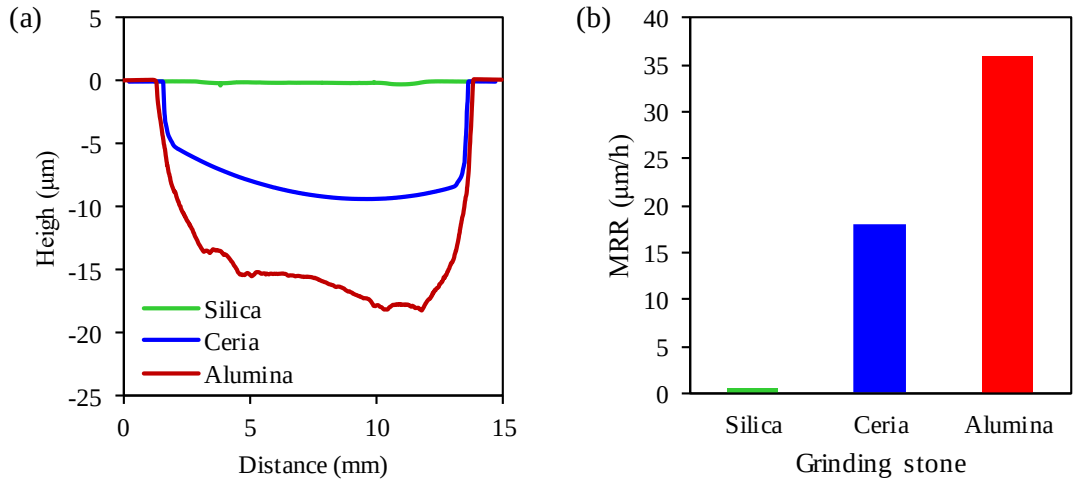

Figure 4.13 MP of quartz glass substrates using ceria, alumina, and silica grinding stones. (a) Cross-sectional views of polishing areas obtained using the three grinding stones. (b) MRRs for the three grinding stones.

that when the ceria grinding stone (18 μm/h) was used. In contrast, the MRR with the silica grinding stone was very low, at about 0.6 μm/h. Ceria-based slurries are more capable of silicon dioxide polishing than silica slurries, because a chemical interaction occurs at the ceria-silicon dioxide interface, which increases the MRR, although the specific chemical interaction mechanism is still being debated [6,7]. Chemical interactions also occur during the polishing of silicon dioxide with silica-based slurries, but they are much weaker than those with ceria-based slurries [8]. On this basis, it is assumed that the difference in the chemical interactions led to the higher MRR of the oxide layer for ceria than for silica, regardless of the relatively low hardness of ceria. The highest MRR obtained when using alumina was attributed to its high hardness, which led to the rapid mechanical removal of the oxide layer.

Although the alumina grinding stone has higher MRR than the ceria grinding stone, it has high hardness that contributes to the formation of SSD on the ECMP-processed surface. Thus, the ceria grinding stone was deemed more suitable for ECMP of SiC than the alumina grinding stone, in obtaining a damage-free surface. As such, the subsequent experiments were conducted using the ceria grinding stone.

4.5 Balance between the anodic oxidation rate and removal rate of the oxide layer

In this study, NaCl aqueous solution with 1 wt% concentration was used as the electrolyte. For

the removal of the oxide layer, a vitrified bonded ceria grinding stone supplied by Mizuho Co., Ltd., with an average particle size of 1 μm (#8000) was applied. During ECMP, the ceria grinding stone was rotated with the spindle and the SiC wafer underwent reciprocating motion along the *x* axis at a set feeding rate. Therefore, on the basis of the polishing motion pattern, when a part of the SiC surface was being polished during the ECMP process, another area was being oxidized whose oxidation duration could be controlled by the feeding rate of the X stage. That is, the balance between the anodic oxidation rate and the removal rate of the oxide layer was controlled by the feeding rate. ECMP experiments were conducted at different feeding rates; the experimental parameters are shown in Table 4.5. Diamond-lapped 4H-SiC wafers (on-axis, N-type) with a thickness of about 360 μm and a specific resistance range of 0.015–0.028 Ω·cm were used for the ECMP experiments. All experiments were performed on the (0001) face.

An SWLI (NewView 8300, Zygo) image of an as-received diamond-lapped surface used for the ECMP experiments is shown in Figure 4.14. The surface was lapped with a #4000 diamond grinding plate (with an average particle size of 3 μm) for 10 min at a pressure of 19.6 kPa. Scratches and pits were observed owing to the mechanical removal of the material by the diamond abrasives. It had a relatively large *S*q surface roughness of 4.290 nm.

Table 4.5 ECMP parameters

Current density (mA/cm^2)	10
Spindle rotation speed (rpm)	1500
Polishing pressure (kPa)	140
Feeding rate (mm/s)	① 1, ② 2, ③ 5, ④ 10
Reciprocating distance (mm)	5
Polishing time (min)	30
Flow rate (mL/min)	380

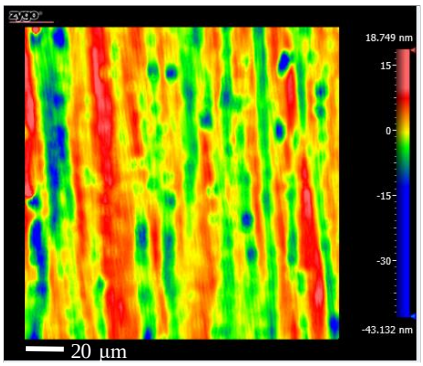

Figure 4.14 SWLI image of as-received diamond-lapped surface, *S*q = 4.290 nm, *S*z = 61.881 nm.

SWLI images of surfaces processed by ECMP at different feeding rates are displayed in Figure 4.15. It is clear that scratches on the as-received diamond-lapped surface were removed and the surface roughness was decreased at all feeding rates; however, many etch pits were observed on the surface polished with feeding rates of 1 and 2 mm/s. As the feeding rate increased, the number of pits decreased, completely disappearing at 10 mm/s. Figure 4.16 shows the relationship between surface roughness and feeding rate. Note the decreasing surface roughness with higher feeding rate. With the disappearance of the pits, both the *S*z and *S*q surface roughness decreased on a dramatic scale, which indicates that surface roughness was mainly influenced by the generation of pits.

To determine the reason for the generation of pits, the removal depths of the SiC surfaces were measured by a stylus profiler. Figure 4.17 shows the cross-sectional views of polished grooves obtained by ECMP at different feeding rates. Almost the same removal depth of approximately 5 μm was observed from the surface of the as-received SiC in 30 min at different feeding rates, as shown in Figure 4.17(b). Therefore, the MRR of SiC was about 10 μm/h, regardless of the feeding rates. Since the removal depths of all samples were similar, the degrees of subsurface damage removal were also similar for all samples. These results indicate that the pits on the surface polished at low feeding rates did not originate from diamond lapping, but from the ECMP process.

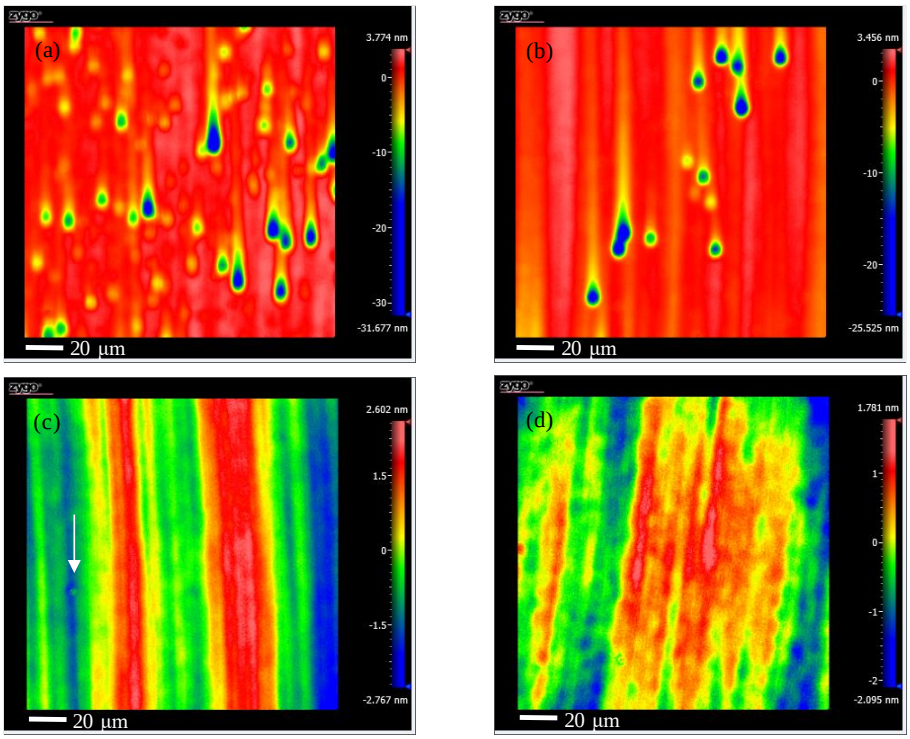

Figure 4.15 SWLI images of SiC surfaces polished at feeding rates of (a) 1, (b) 2, (c) 5, and (d) 10 mm/s.

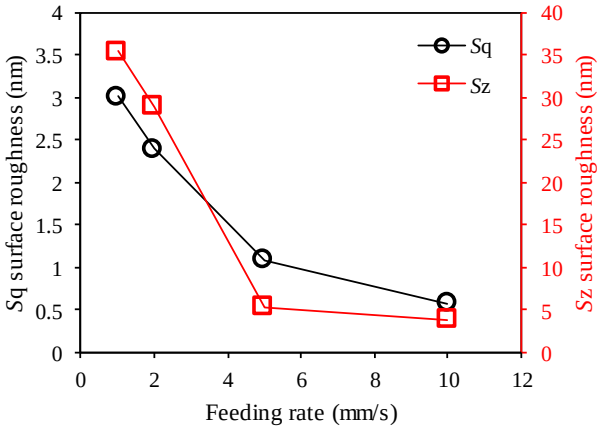

Figure 4.16 Relationship between surface roughness and feeding rate.

It was also observed that the overall cross-sectional views of the polished grooves were different, and the removal uniformity of the polishing areas worsened with increasing feeding rate, as shown in Figure 4.17. The differences in the overall cross-sectional views of the polished grooves were caused by the warp of the thin SiC wafers that was inevitably induced by their manufacturing process, whereas changes in the removal uniformity of the polishing areas were attributed to the polishing motion during the ECMP process. Moreover, during ECMP, the ceria grinding stone was rotated with the spindle and the SiC wafer underwent reciprocating motion along the *x* axis at a set feeding rate, and a ring-like ceria grinding stone was applied, as shown in Figure 4.17. The grinding stone momentarily stopped at both left and right sides of the polishing

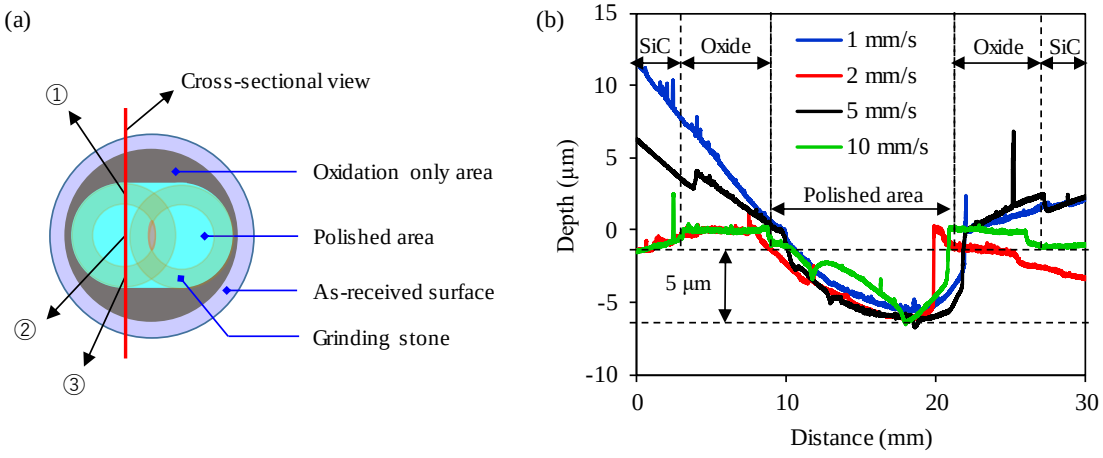

Figure 4.17 Observation of cross-sectional view. (a) Observation schematic graph, grinding stone on the left and right sides are shown. (b) Cross-sectional views of polished areas obtained at different feeding rates.

area, owing to the reciprocating motion of the X stage; thus, a relatively higher removal amount with a ring-like shape would be obtained at both sides due to longer polishing time. On this regard, the center of the cross-sectional view (position ② in Figure 4.17(a)) would be a little higher than the two sides (positions ① and ③ in Figure 4.17(a)). With higher feeding rates, the moving time between the two stopping sites decreased, thereby increasing the difference in the removal amount between the two stopping sites and other areas and deteriorating the removal uniformity. Furthermore, the contact status between the SiC surface and the grinding stone also affected the polishing result. These problems could be solved by improving the ECMP machine for polishing the entire wafer.

XPS measurement results of the as-received diamond-lapped surface are shown in Figure 4.18(a), where a small amount of oxide could be observed. Figures 4.18(b) to (e) present the XPS

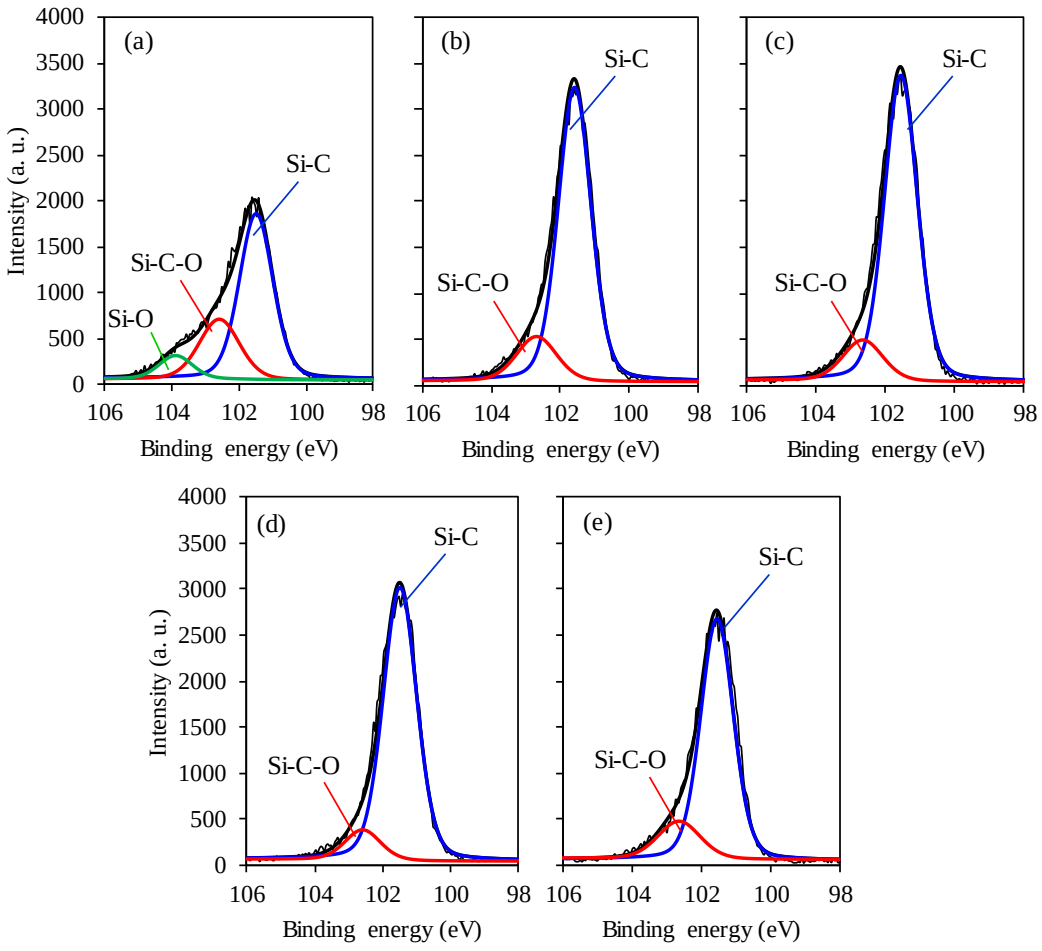

Figure 4.18 Si 2p spectra of (a) as-received diamond-lapped surface, and surfaces polished at feeding rates of (b) 1, (c) 2, (d) 5, and (e) 10 mm/s obtained by XPS measurement with a take-off angle of 45°.

measurement results of the SiC surfaces polished at different feeding rates. Strong peaks corresponding to Si–C bonds and weak peaks corresponding to Si–C–O bonds were observed, which indicates that a small amount of silicon oxycarbide remained on the polished surface; nonetheless, the removal states of the anodic oxide of the four surfaces polished at different feeding rates were almost the same. Silicon oxycarbide is an intermediate product of the oxidation of SiC; although it is more difficult to remove than silicon oxide, it can be completely removed by additional mechanical polishing [9].

On the basis of the above analysis, the removal depth and the removal states of the oxide of the four surfaces were almost the same. The difference in the ECMP of the four SiC surfaces, thus, could be attributed to the difference in the feeding rate, as modeled in Figure 4.19. In the case of a low feeding rate, for instance, the oxidation time of the SiC surface was long as a longer time was required to complete the reciprocating motion of the SiC wafer. With a constant current being applied in the ECMP experiments, the oxidation rate at the different feeding rates is presumably the same on account of Faraday's electrolysis law. With this, the thickness of the oxide layer prior to its removal by the grinding stone, was proportional to the oxidation time and inversely proportional to the feeding rate. As such, the thicknesses of the oxide layer at a feeding rate of 1 mm/s could be estimated as 2, 5, and 10 times greater than those at the feeding rates of 2, 5, and 10 mm/s, respectively, as indicated in Figure 4.19. Chemical oxidation/etching of a 4H-SiC surface is an anisotropic process. During the electrochemical process, in particular, current density

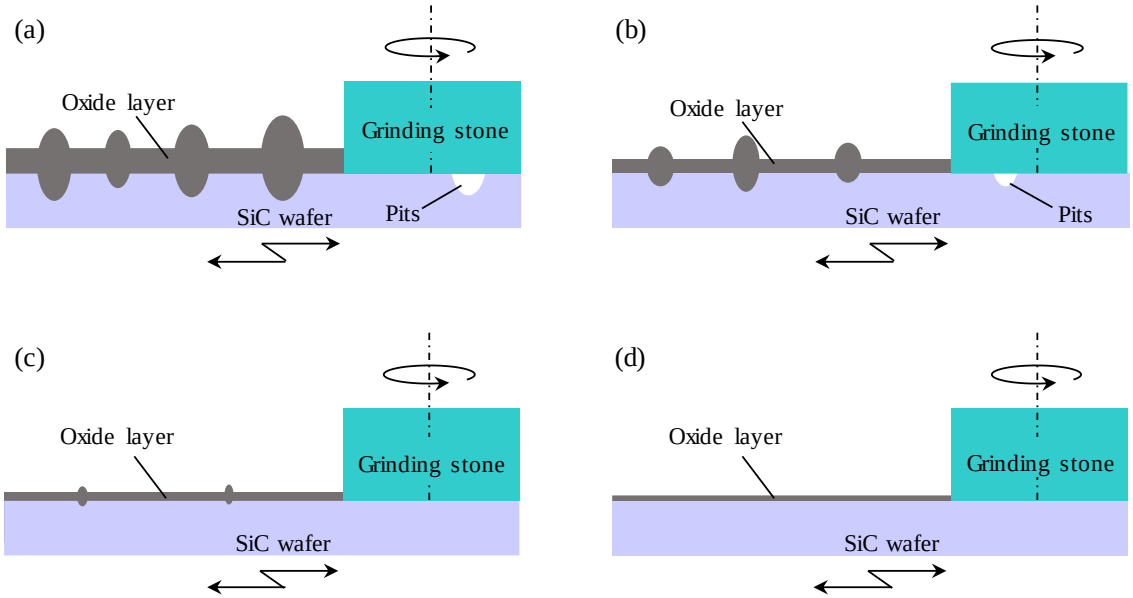

Figure 4.19 Modeling of ECMP process at feeding rates of (a) 1, (b) 2, (c) 5, and (d) 10 mm/s.

distribution on the SiC surface also affected the oxidation uniformity, as that described in Chapter 3. Additionally, the anodic oxidation of SiC did not stop with the progress of oxidation, owing to the porosity of the oxide layer [10].

Accordingly, the interface between the bulk SiC and the oxide layer may have become rough with the thickening of the oxide layer, because the ceria grinding stone can only remove the oxide layer, as shown in Figure 4.19. After the oxide layer removal, a rough surface with pits was obtained at the feeding rate of 1 mm/s, with the formation of the thick oxide layer. The oxide layer thickness decreased and the interface between the bulk SiC and the oxide layer became smoother with an increase in feeding rate. At a feeding rate of 10 mm/s, a smooth surface without pits was obtained.

4.6 Application of ECMP to sliced 4H-SiC (0001) surfaces

Figure 4.20 shows the morphologies of a sliced 4H-SiC (0001) (on-axis, N-type) surface supplied by Mizuho Corporation that was sliced with a diamond saw of 0.12-mm wire diameter and with diamond particles whose diameter ranged 20–30 μm. Figure 4.20(a) displays the formation of low-spatial-frequency saw marks via slicing, and indicates obtained surface roughness of 1.156-μm *S*q and 7.578-μm *S*z. The cross-sectional view in Figure 4.20(b) reflects that the spatial wavelength of the periodical saw marks was approximately 640 μm. Many high-spatial-frequency structures appeared on the surface aside from the low-spatial-frequency saw marks, as shown in Figure 4.20(c). Moreover, the observed damage on the surface reached a depth of 5 μm, but the SSD was assumed to be much deeper.

The sliced surfaces were processed by ECMP, with the ECMP parameters as shown in Table 4.6. Figure 4.21 shows the surface topography after ECMP at a current density of 2 mA/cm^2 and

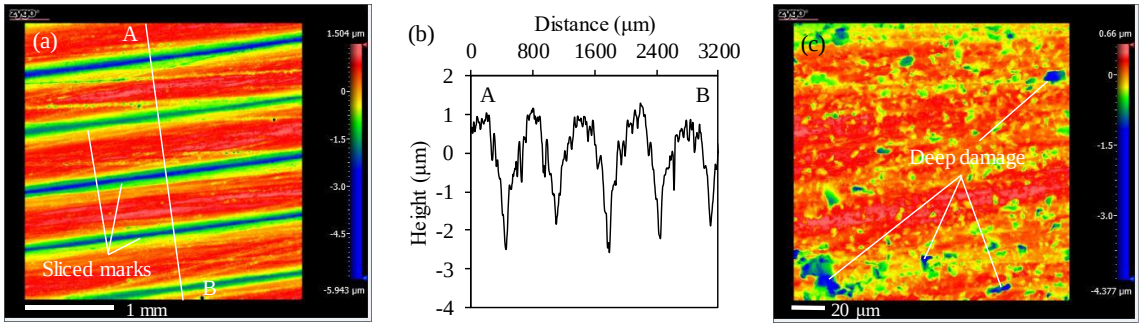

Figure 4.20 Sliced 4H–SiC (0001) surface. (a) SWLI image with a magnification of 2.8, *S*q = 0.869 μm, and *S*z = 7.447 μm. (b) Cross-sectional view along A–B in (a). (c) SWLI image with a magnification of 50, *S*q = 0.286 μm, and *S*z = 5.037 μm.

a spindle rotation speed of 1000 rpm for 1 h 40 min. From the surface topography of polished area 1 in Figure 4.21(a), high-spatial-frequency saw marks formed by slicing were removed, and the *Sq* surface roughness was decreased from 0.286 μm to 7.525 nm. Although most of the surface was very smooth, some low-spatial-frequency saw marks remained, therein deteriorating the surface roughness, as shown in Figure 4.21(b). Logically, this indicates that the removal depth was not sufficient to remove the SSD formed by wire saw slicing. XPS measurement results of the ECMP-processed SiC surface are shown in Figure 4.22. Strong peaks corresponding to Si–O and Si–C–O bonds were observed, which revealed that the oxide on the polished surface was not completely removed.

Table 4.6 ECMP parameters

Current density (mA/cm^2)	2
Spindle rotation speed (rpm)	1000
Polishing pressure (kPa)	140
Feeding rate (mm/s)	10
Reciprocating distance (mm)	5
Polishing time (min)	100
Electrolyte	1 wt% NaCl aqueous solution
Flow rate (mL/min)	380
Grinding stone	Vitrified bond ceria (#8000)

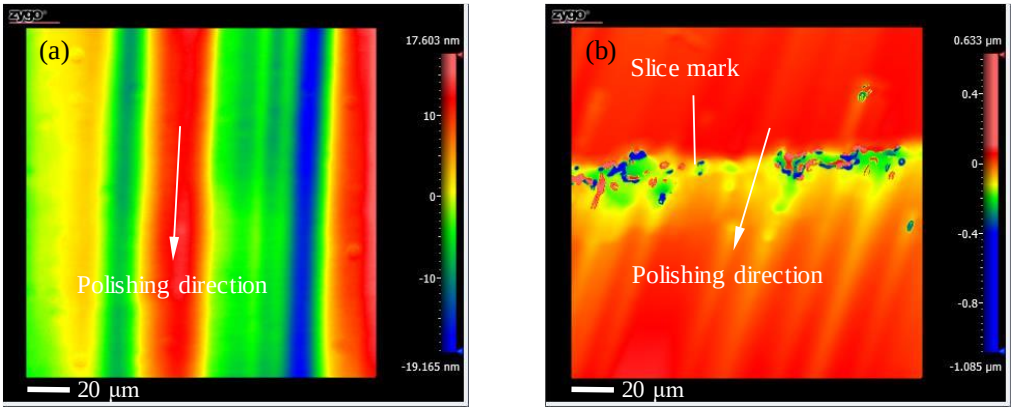

Figure 4.21 SWLI image of surface after ECMP at 2 mA/cm^2 and 1000 rpm for 1 h 40 min. (a) Polished area 1: *Sq* = 7.525 nm and *Sz* = 36.769 nm. (b) Polished area 2: *Sq* = 0.072 μm and *Sz* = 1.717 μm.

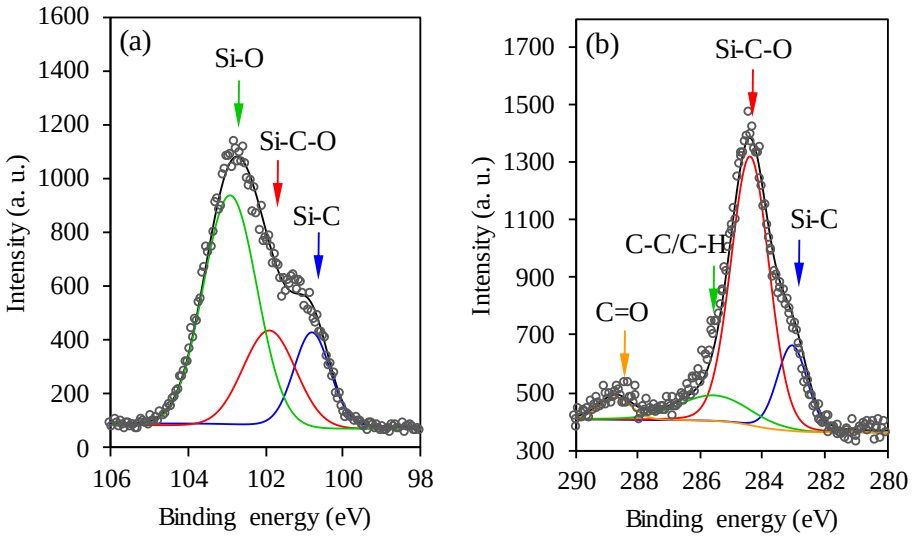

Figure 4.22 XPS measurement results of SiC surface after ECMP at 2 mA/cm^2 and 1000 rpm for 1 h 40 min with a take-off angle of 45°, (a) Si 2p, (b) C 1s.

For complete removal of the saw marks and the residual oxide on the ECMP-processed surface, a sliced surface was processed by ECMP for 3 h and an additional Mechanical polishing (MP) without anodic oxidation for 30 min. The other polishing parameters were the same as those in Figure 4.21. Figures 4.23(a) and (b) show a low-magnification SWLI image of the polished surface and its cross-sectional view, respectively. The saw marks were completely removed, as shown in Figure 4.23(a), and the surface was markedly flattened, in comparison to the sliced surface shown in Figures 4.20(a) and (b). The ring-like surface structure that formed could be

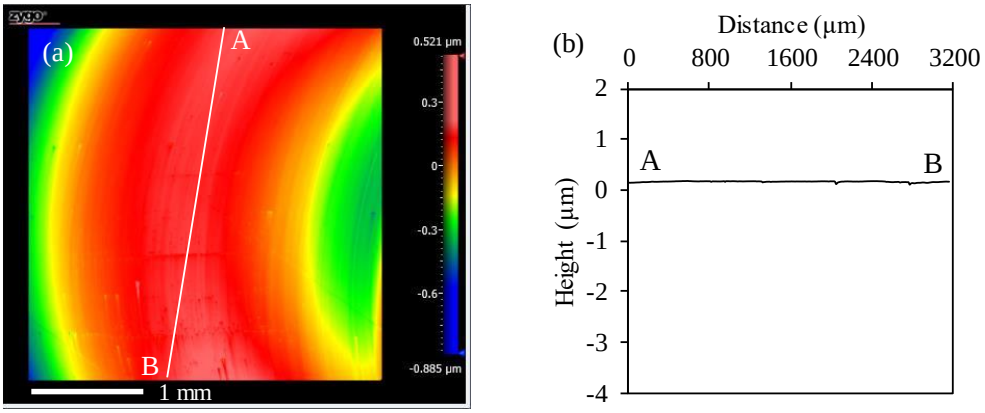

Figure 4.23 Sliced 4H–SiC (0001) surface after ECMP at 2 mA/cm^2 and 1000 rpm for 3 h and an additional MP for 30 min. (a) SWLI image enlarged 2.8 times. (b) Cross-sectional view along A–B in (a).

attributed to the rotation and uniaxial oscillation patterns of the grindstone in the prototype ECMP machine.

A high-magnification SWLI image of the polished area is given in Figure 4.24. The *Sq* roughness was 3.128 nm, which is comparable to that of a traditional diamond-lapped surface. However, there were many polishing marks along the polishing direction on the processed surface, as shown in Figures 4.21(a) and 4.24. The marks presumably formed by the mismatch of the spindle rotation speed and the feeding rate in the X direction, as shown in Figure 4.25. During ECMP, abrasives in the grinding stone rotated with the spindle, and the SiC wafer underwent a reciprocating motion along the X direction. One abrasive particle moved the same distance along the X direction in the same period of time during the polishing, because the feeding rate remained at 10 mm/s. Moreover, during this same period of time, there was a small number of rotations of the abrasive particle in the case of a low spindle rotation speed, which resulted in wide and large

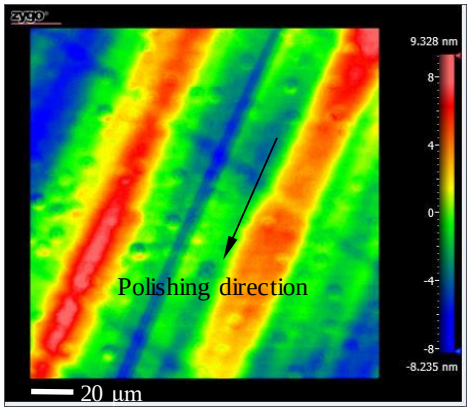

Figure 4.24 SWLI image of surface after ECMP for 3 h and an additional MP for 30 min at a spindle rotation speed of 1000 rpm, *Sq* = 3.128 nm.

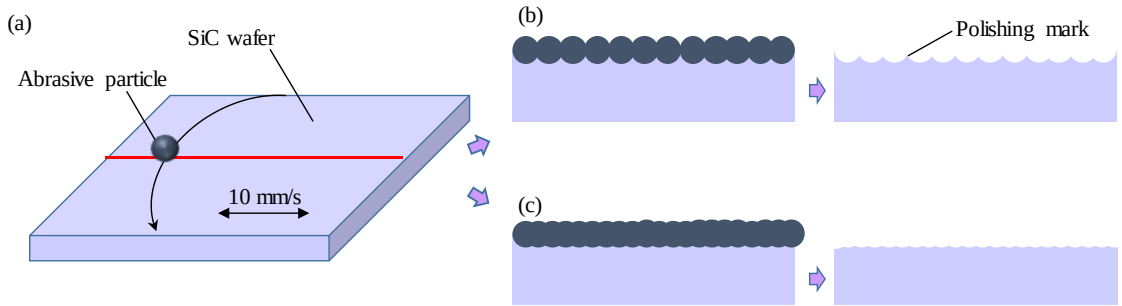

Figure 4.25 Modeling of ECMP process. (a) Positional relationship between abrasive and SiC wafer in ECMP process. Cross-sectional view of SiC surface in ECMP with a (b) low and (c) high spindle rotation speed.

height polishing marks, thereby increasing the surface roughness, as shown in Figure 4.25(b). In the case of a high spindle rotation speed, the number of rotations of the abrasive particle increased, leading to the overlapping of the polishing marks that eventually resulted to their shallowing and narrowing and a decrease in the surface roughness, as shown in Figure 4.25(c). These results suggest that the combination between the feeding rate and spindle rotation speed in ECMP is very important for obtaining smooth SiC surfaces, where higher spindle rotation speed can obtain a smoother surface given the same feeding rate.

These polishing marks were removed by increasing the spindle rotation speed from 1000 to 1500 rpm. Also, a sliced wafer surface was polished for 3 h under the same conditions. Figure 4.26 shows an SWLI image of the surface polished at a spindle rotation speed of 1500 rpm. After the polishing marks were removed, a smoother surface (1.969 nm *S*q) was obtained. This result indicates that the combination of the spindle rotation speed and the feeding rate plays an important role in the morphology of the ECMP-processed surface.

Moreover, although the low-spatial-frequency saw and polishing marks were removed by increasing the polishing time and spindle rotation speed, many pits and some line-shaped defects that are perpendicular to the polishing direction could be observed on the polished surface, as shown in Figure 4.24. The pits and line-shaped defects were randomly distributed, as in the case of deep surface damages on the as-sliced SiC surface, as shown in Figure 4.20. In the anodic oxidation of SiC, the sites of defects and SSD were preferentially oxidized and had higher oxidation rate, as described in Chapter 3. Thus, pits would be generated on the sites of the defects and SSD after removal of the oxide layer. The pits on the ECMP-processed surface in Figures 4.24 and 4.26 were seemingly formed by the residual SSD, which were induced by the slicing of the SiC wafer.

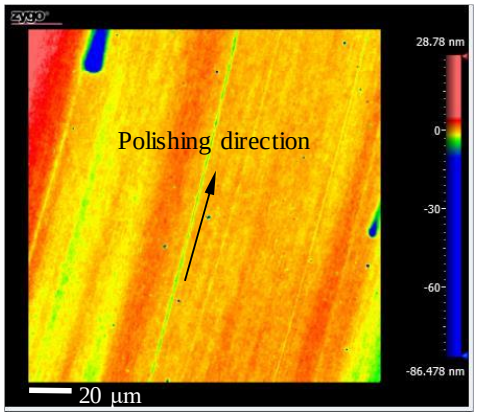

Figure 4.26 SWLI image of surface after ECMP for 3 h at a spindle rotation speed of 1500 rpm, *S*q = 1.969 nm.

XPS results of these two ECMP-processed surfaces are shown in Figure 4.27. Here, both Si–O and Si–C–O bonds appeared on both surfaces. More specifically, on the surface after ECMP for 3 h and an additional MP for 30 min, peaks of Si–O and Si–C–O bonds were clearly weaker than that of Si–C bonds. On the opposite, on the surface only after ECMP for 3 h, stronger peaks corresponding to Si–O and Si–C–O bonds were observed. These results indicate that the additional MP can remove the residual oxide on the polished surface. Meanwhile, the polishing depths in Figures 4.24 and 4.26 were measured using a stylus profiler. The depths of removal in both figures were about 15 μm, as shown in Figure 4.28, while the MRRs were 5 μm/h at both spindle rotation speeds of 1000 and 1500 rpm. By contrast, the MRR of quartz glass was 18 μm/h

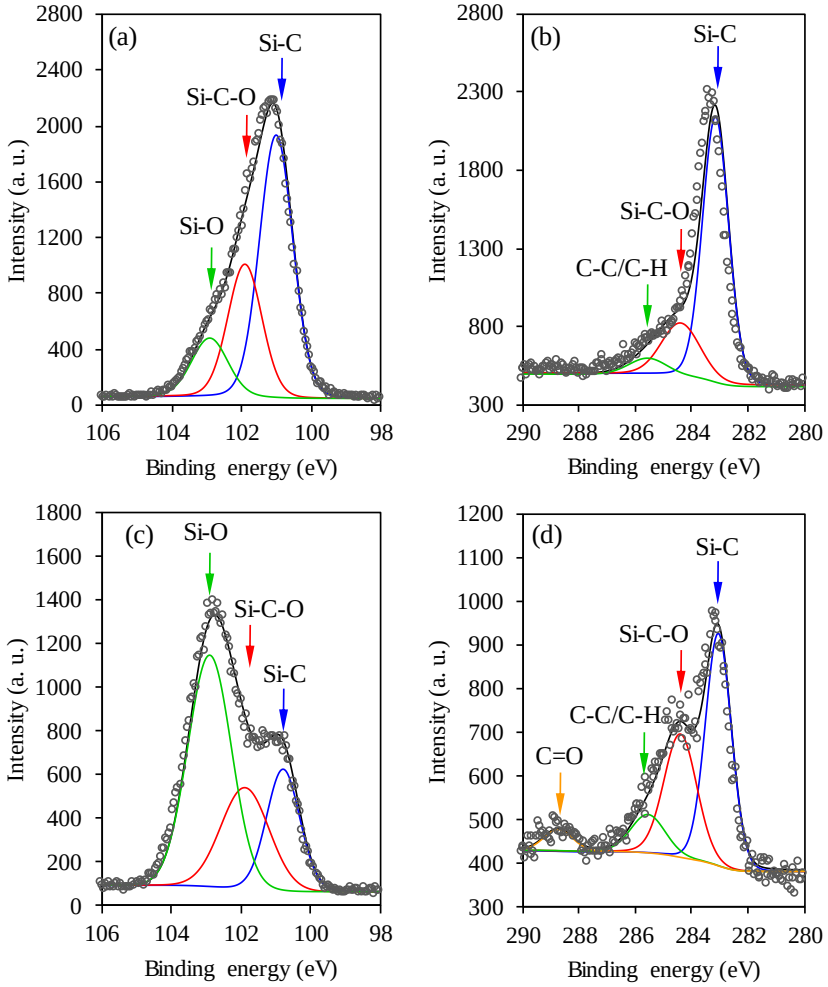

Figure 4.27 XPS measurement results of ECMP-processed SiC surfaces with a take-off angle of 45°. (a) Si 2p and (b) C 1s spectra of SiC surface after ECMP at 2 mA/cm^2 and 1000 rpm for 3 h and an additional MP for 30 min. (c) Si 2p and (d) C 1s spectra of SiC surface after ECMP at 2 mA/cm^2 and 1500 rpm for 3 h.

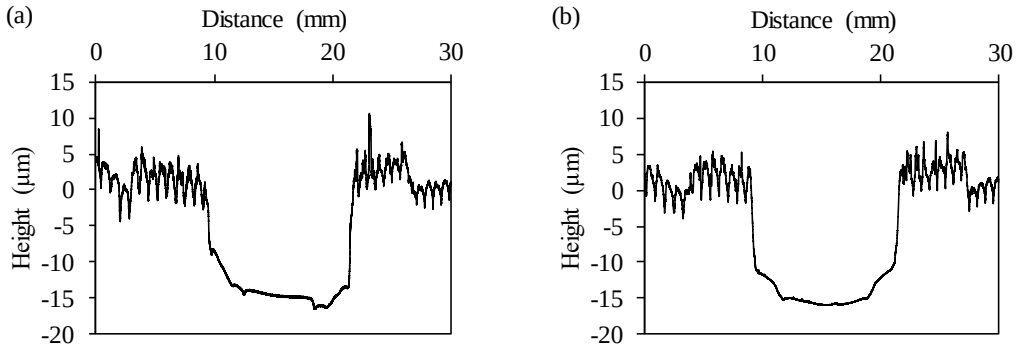

Figure 4.28 Cross-sectional views of polishing areas obtained with spindle rotation speeds of (c) 1000 rpm and (d) 1500 rpm.

at 1000 rpm, as shown in Figure 4.13. The MRR of the anodic oxide layer of 4H–SiC (0001) should be higher than that of quartz glass, as the hardness of the oxide layer of the SiC generated by anodic oxidation was found to be much lower than that of quartz glass. Correspondingly, the MRR of the oxide layer was much greater than the MRR obtained in the two ECMP experiments, which indicates that the current density of 2 mA/cm^2 limited the oxidation rate that dominated the MRR in ECMP. Moreover, the residual oxide on the polished surface was presumably located on the sites of pits. Complete removal of the residual oxide was challenging due to the use of fixed abrasives, as the fixed-abrasive faces difficulty to extend into the bottom of pit for removing the residual oxide due to shielding by the convex SiC area. Therefore, it was essential to increase the anodic oxidation rate so as to effectively remove deep damage existing beneath the sliced surface.

On the basis of Faraday's law of electrolysis, the mass of the oxidized SiC is directly proportional to the quantity of charge passed, as expressed by:

$$m = M\frac{Q}{zF}, \tag{4.2}$$

where m is the mass of the oxidized SiC, M is the molar mass of SiC, Q is the total electric charge during slurryless ECMP, F is the Faraday constant, and z is the valence of the ion.

With a constant current density being applied to the slurryless ECMP, the total electric charge during the process can be expressed as

$$Q = Sit, \tag{4.3}$$

where S is the polishing area, i is the current density, and t is the polishing time.

Thus, in terms of thickness, the MRR can be given by:

$$\text{MRR} = \frac{m}{S\rho t} = \frac{Mi}{zF\rho}, \tag{4.4}$$

where ρ is the density of SiC.

Equation (4.4) suggests that the MRR in slurryless ECMP is directly proportional to current density, that is, an increase in current density should improve the MRR. Thus, to obtain a higher MRR, the current density was increased from 2 to 10 mA/cm^2. Figure 4.29 shows the topography and polishing depth of a sliced 4H-SiC (0001) surface after ECMP, with the parameters shown in Table 4.7 Saw marks, surface damage, and polishing marks were removed, therein achieving a smooth surface with *S*q roughness of 1.352 nm, as shown in Figure 4.29(a), which is comparable to that of a conventional diamond-lapped SiC surface. A cross-sectional view of the polished area in this experiment is shown in Figure 4.29(b), with high MRR of 23 μm/h, almost 5 times which obtained at a current density of 2 mA/cm^2. This result is consistent with Equation (4.4).

Figure 4.30 shows the XPS spectra of the ECMP-processed surface in Figure 4.29. Strong peaks corresponding to the Si–C bond were observed in both the Si 2p and C 1s spectra, whereas only a weak peak corresponding to the Si–O–C bond was observed in the Si 2p spectrum. Moreover, the residual oxide on the surface in Figure 4.29 was found to be much less than that on the surfaces

Table 4.7 ECMP parameters

Current density (mA/cm^2)	10
Spindle rotation speed (rpm)	1500
Polishing pressure (kPa)	140
Feeding rate (mm/s)	10
Reciprocating distance (mm)	5
Polishing time (min)	120

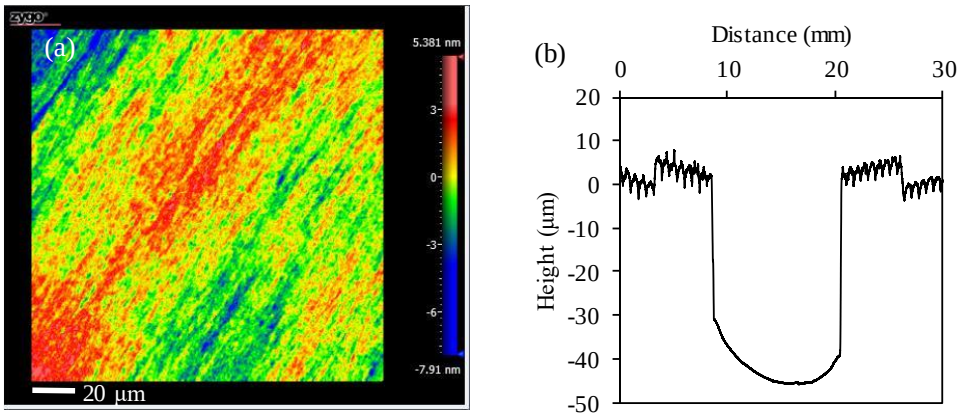

Figure 4.29 Sliced surface after ECMP at 10 mA/cm^2 and 1500 rpm for 2 h. (a) SWLI image: *S*q = 1.352 nm and *S*z = 13.291 nm. (b) Cross-sectional view of the polished area observed using the stylus profiler.

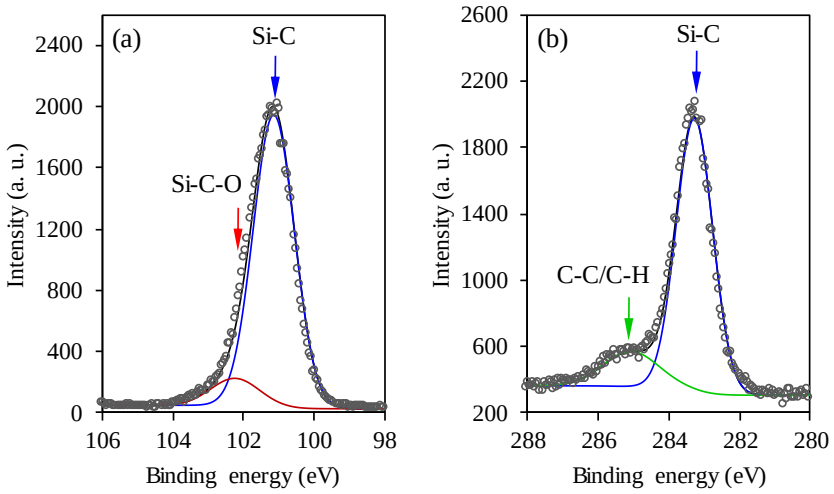

Figure 4.30 XPS spectra of the surface obtained by ECMP at a current density of 10 mA/cm^2 measured with a take-off angle of 45°. (a) Si 2p and (b) C 1s spectra.

in Figures 4.24 and 4.26. This result reveals that the oxide layer was sufficiently removed after removal of the deep damage, and that the small amount of residual oxide on the surface can be removed by a short additional MP, which is the same as the ECMP but without electricity.

The above results were considered for the modeling the ECMP process of the sliced SiC surface, as depicted in Figure 4.31. On the sliced SiC surface, note the appearance of several saw marks and SSD just beneath. During ECMP, the whole SiC surface was oxidized and the SSD sites were preferentially oxidized. In the initial polishing stage, only the convex oxide area on the surface was removed, whereas the concave area remained covered with the oxide layer. As such, the oxidation rate of the convex area should be greater than that of the concave area owing to the barrier induced by the oxide layer. With repeated anodic oxidation and removal of the oxide layer, the saw marks were gradually removed and the SiC surface gradually became flat. After the saw marks were removed, many SSD remained below the SiC surface and pits were generated on the SSD sites due to higher oxidation rate. During this polishing period, it was difficult for the fixed

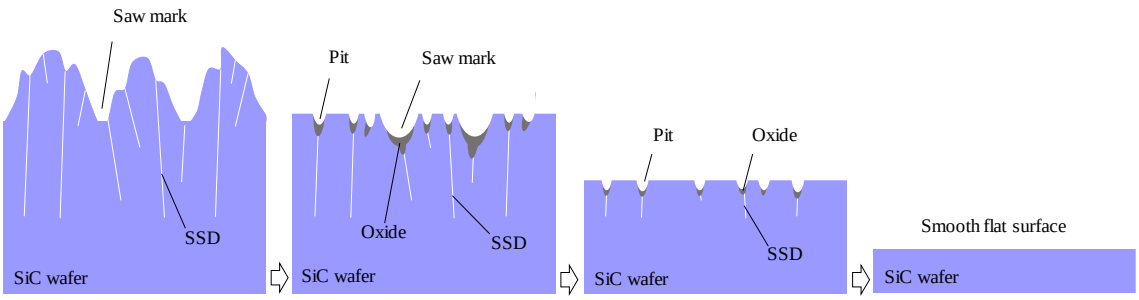

Figure 4.31 Flattening of sliced SiC surface using slurryless ECMP.

abrasive to extend into the pit bottom in order to remove the residual oxide, due to shielding by the convex SiC area. As a result, residual oxide settled on the bottom of the pits. After the SSD was completely removed, a relatively uniform oxidation occurred, as descried in Chapter 3, thereto resulting in a flat and smooth surface with almost no residual oxide. This property of slurryless ECMP makes it possible to estimate the removal status of the SSD.

4.7 Evaluation of subsurface damage of SiC processed by ECMP

Raman spectroscopy (RAMANtouch, Nanophoton) measurements on the sliced surface, the ECMP-processed surface, and a diamond-lapped surface were carried out to evaluate the performance of ECMP in the removal of SSD. The laser used in the Raman spectroscopy has 532-nm wavelength. The change in the nominal focus position (NFP) of the laser during the observation was 8 μm. However, considering the refractive index of SiC, the change in actual focus position, which refers to the actual depth of observation for the SiC surfaces, was approximately calculated to as much as 2.7 times that in NFP [11-13]. Residual stress on the SiC surfaces was derived from the shift of the FTO(2/4)E2 (776 cm^{-1}) peak of SiC, whereas the tensile and compressive stresses were calculated using a ratio of −510 MPa/cm^{-1} based on the Raman shift from 776 cm^{-1} [14].

Figure 4.32 shows the optical microscopy images of surfaces processed by slicing, ECMP, and diamond lapping, as well as their residual stress along the depth direction, as observed via

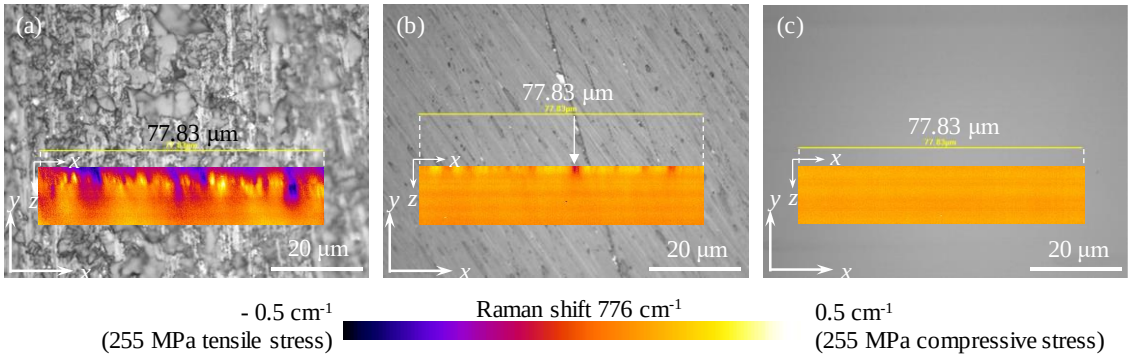

Figure 4.32 Optical microscopy images of (a) sliced surface, (b) diamond-lapped surface, and (c) ECMP-processed surface at 10 mA/cm^2 for 2 h. The insets show the residual stress distributions of different surfaces along the depth direction (*z* direction) measured by confocal Raman microscopy with an observation width of 77.83 μm. The change in the NFP of the laser during the observation is 8 μm.

confocal Raman microscopy. As shown in Figure 4.32(a), many irregular cracks and granular SiC could be observed on the sliced surface. The two-dimensional distribution image of residual stress showed the occurrence of tensile and compressive stresses on the sliced surface, reaching greater than 200 MPa at maximum, whereas the tensile stress on the examined line reached a maximum depth of about 16.2 μm from the surface. On the surface processed by conventional lapping using a #4000 diamond lapping plate (within the average particle size range of 2–4 μm) at a polishing pressure of 19.6 kPa, several scratches and pits appeared by the mechanical removal of SiC, as shown in Figure 4.32(b). Residual stress on the diamond-lapped surface concentrated at the positions of scratches and pits, and the residual stress and the maximum depth at which it existed (about 3.8 μm) were clearly less than those on the sliced surface. In contrast, a scratch-free surface was achieved after ECMP at the current density of 10 mA/cm^2 for 2 h, because only the anodically oxidized layer was removed by the soft ceria grinding stone. The inset residual stress image shows that no SSD existed on and beneath the surface, which indicates that a damage-free surface was obtained. Therefore, the surface processed by ECMP is more preferable for the final finishing step of the surface.

4.8 Influence of current density on the performance of slurryless ECMP

As described in Chapter 2, the oxidation state of the SiC surface changes with oxidation current density. Therefore, current density was optimized to obtain the best polishing performance. Slurryless ECMP with different current densities were conducted on on-axis N-type sliced 4H-SiC (0001) surfaces, as shown in Table 4.8. The polishing performance of ECMP was then evaluated by MRR and surface roughness. The sliced surface (supplied by TankeBlue Corporation) is displayed in Figure 4.33. Observe the presence of low-spatial-frequency saw marks and high-spatial-frequency pits on the surface. The MRR was calculated from the polishing depth of the polished grooves that were measured by a stylus profiler. Figure 4.34 shows the changes in MRR as current density was increased. The MRR linearly increased with higher current density of less than 5 mA/cm^2, while it saturated at approximately 12.5 μm/h at greater than 5 mA/cm^2. During the ECMP with 5 mA/cm^2, the potential was greater than 10 V. Although occurring of the anodic oxidation of SiC is the easiest in the ECMP system, the other electrochemical reactions, ie. Water electrolysis and oxidation of chloride ions, would occur under the relatively high potential (10 V), because the potentials for these reactions are much lower than 10 V, as shown in Sections 2.4.6, 2.4.7 and 2.4.8. The occurring of other electrochemical reactions decreased the efficiency of the current density. Likewise, it indicates that the anodic oxidation rate of the SiC surface has a limit.

Table 4.8 Slurryless ECMP of sliced SiC wafers with different current densities

Experimental number	Current density (mA/cm^2)	Polishing time (h)	Removal depth (μm)
①	2	3	15
②	3	3	24
③	4	3	28.8
④	5	2	25
⑤	10	2	24
⑥	20	1	13

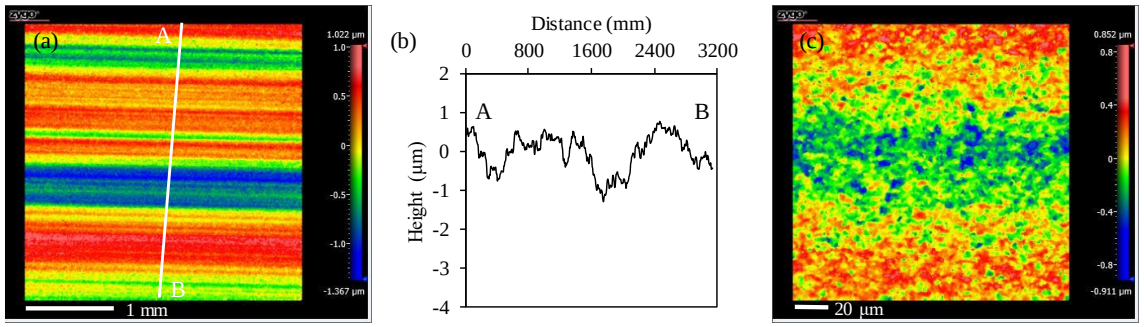

Figure 4.33 Sliced 4H-SiC (0001) surface supplied by TankeBlue Corporation. (a) SWLI image with a magnification of 2.8, *S*q = 0.468 μm, and *S*z = 2.389 μm. (b) Cross-sectional view along A–B in (a). (c) SWLI image with a magnification of 50, *S*q = 0.204 μm, and *S*z = 1.763 μm.

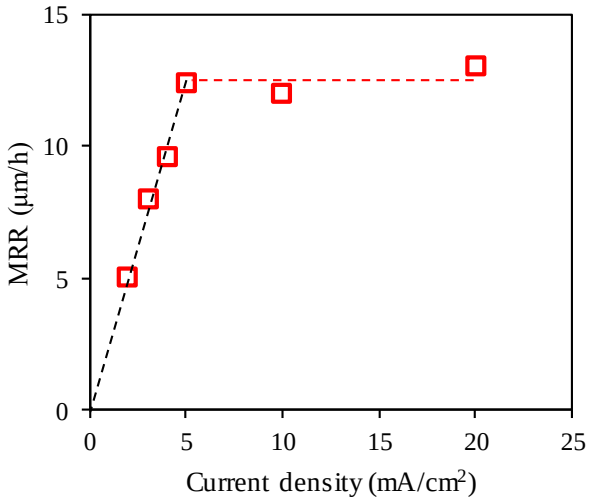

Figure 4.34 Relationship between MRR and current density.

To find the limit of the anodic oxidation rate, anodic oxidations of diamond-lapped 4H-SiC surfaces with different current densities were investigated, with anodic oxidation parameters as listed in Table 4.9. After anodic oxidation, the oxide layers were removed by HF etching, and the oxidation depths were observed by SWLI. The average value of the four oxidation depths of the up, down, left, and right sides of the oxidation spots was the final oxidation depth used for the oxidation spots. Changes of the oxidation depth with current density are presented in Figure 4.35(a), in which a relationship that was almost the same as that between the MRR and current density depicted in Figure 4.34 was obtained. However, during anodic oxidation, the oxidation rate reached a maximum with the current density reaching 2 mA/cm^2, much lower than that of the in ECMP (5 mA/cm^2). Two reasons were considered for this difference, the first being the difference in the surface damage. Recall in Chapter 3 that during the anodic oxidation of the SiC surface, the sites of scratches and surface damage were preferentially oxidized, with the oxidation rate of the surface damage being greater than the damage-free area. Logically, the oxidation rate of the sliced SiC surface would be greater than that of diamond-lapped SiC surface because of the shallower damage layer, which would then result to a lower limit oxidation rate. The second reason was the difference in the oxidation conditions between the ECMP and anodic oxidation. In ECMP, the oxide layer was removed immediately after its generation; thus, oxidation was always conducted on a fresh SiC surface. On the contrary, in anodic oxidation, the oxide layer remained on the SiC surface, which potentially inhibited the anodic oxidation of the SiC surface. Furthermore, in ECMP, the polishing motion could promote the exchange of reactive species during anodic oxidation, add to it the friction and pressure between the grinding stone and the SiC surface that enhance the anodic oxidation of the SiC surface.

Table 4.9 Anodic oxidation parameters of diamond-lapped 4H-SiC (0001) surfaces

Experimental number	Current density (mA/cm^2)	Oxidation time (min)
①	0.2	10
②	0.5	10
③	1	10
④	2	10
⑤	3	10
⑥	4	10
⑦	5	10
⑧	10	10

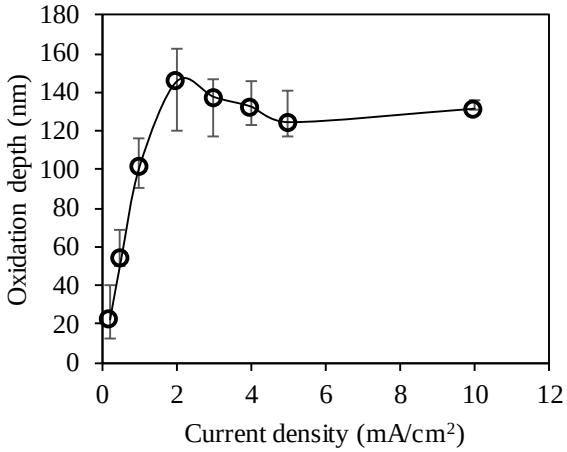

Figure 4.35 Relationship between oxidation depth and current density in anodic oxidation of diamond-lapped 4H-SiC (0001) surfaces.

To study the limits of the MRR and oxidation rate, two nitrogen-doped 4H-SiC wafers (samples A and B) with different doping concentrations were subjected to anodic oxidation. Figure 4.36(a) shows the nitrogen concentration of these two SiC wafers, as obtained by secondary ion mass spectroscopy (SIMS, IMS-7f) at measurement depth of 2 μm. Doping concentration of 1.50×10^{19} atoms/cc was observed for sample A, which was 1.92×10^{19} atoms/cc for sample B, the concentration of sample B was 1.28 times greater than that of sample A. These two wafers were anodically oxidized at a current density of 10 mA/cm^2 for 10 min, prior to the oxide layer getting removed by HF etching. The oxidation depths of both surfaces are shown in Figure 4.36(b). Specifically, the low-doped SiC (sample A) surface had an oxidation depth of about 132 nm, which is the limit of oxidation rate shown in Figure 4.35. It was 177 nm on the highly doped SiC surface (sample B), up by 1.34 times. The differences in oxidation depths and doping concentrations between the two wafers were similar, which indicates that the limit of oxidation rate at high current densities was broken by higher doping concentration.

In the anodic oxidation of SiC, the holes had participation in the oxidation reactions, which suggests that there were much more holes in the highly doped SiC than in the low-doped one, under the same anodic oxidation condition. Nonetheless, with N-type SiC wafers applied in these experiments, the holes that participated in the oxidation reactions should not be generated by the dopant (nitrogen) in SiC, they should be gathered or generated by the electric field caused by the band bending in the space charge layer. The band bending of SiC surface significantly depends on the difference of the Fermi levels of SiC and the redox pair in the electrolyte. The Fermi level of N-type semiconductor increases with increasing doping concentration. Therefore, the Fermi

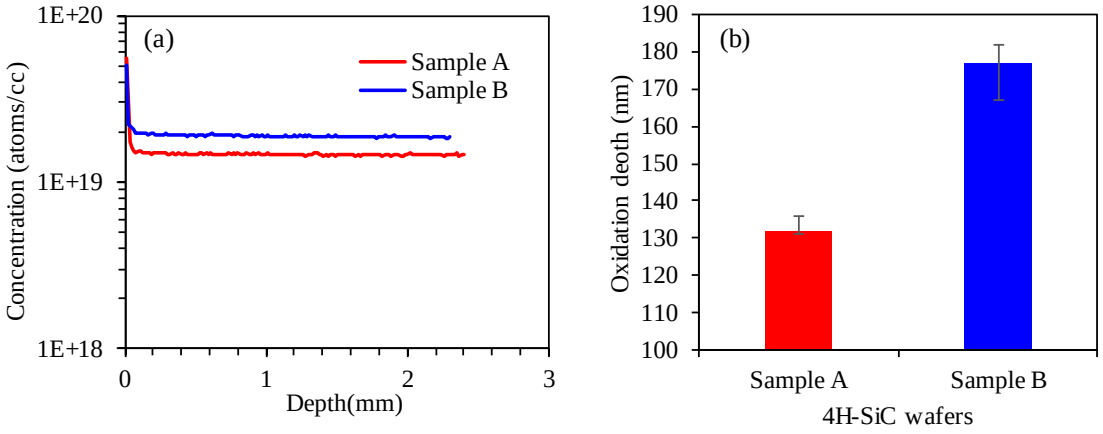

Figure 4.36 Anodic oxidation of diamond-lapped 4H-SiC (0001) surfaces with different doping concentration (dopant: nitrogen). (a) Doping concentration of the high-doped and low-doped SiC wafers. (b) Oxidation depths of the high-doped and low-doped SiC surfaces with a current density of 10 mA/cm^2 for 10 min.

level of high-doped SiC surface is greater than that of low-doped SiC surface, which increased the band bending of the SiC, resulted in the gathering and generation of more holes in the space charge layer.

On the other hand, dopant in SiC mainly exists as substitutional impurity, which distorts the lattice of SiC and induces tensile or compressive stress in the dopant sites. In general, the bandgap of the strained sites would be larger than that of the unstrained layer when under compressive strain, and smaller under tensile strain [15,16]. In addition, it has also been reported that doping narrowed the bandgaps of 3C-, 4H-, 6H-SiC, and Si [17]. Therefore, there were more holes generate in the space charge layer of the high-doped SiC surface, because electrons in the valence band were easier to be drove to the conduction band by the electric field caused by the band bending. The combined effects of the increase in band bending and narrowing in bandgap increased the limit anodic oxidation rate of the high-doped SiC surface.

SWLI images of ECMP-processed SiC surfaces with different current densities are presented in Figure 4.37. Under low current densities, the SiC surfaces were not flat; eventually, they became flat as the current density exceeded 10 mA/cm^2. Besides, although it was very difficult to evaluate the surface roughness of the polished surface by its flatness, the smoothest surface was obtained at 10 mA/cm^2. Such positioned 10 mA/cm^2 to be the most suitable current density for the ECMP of SiC wafers.

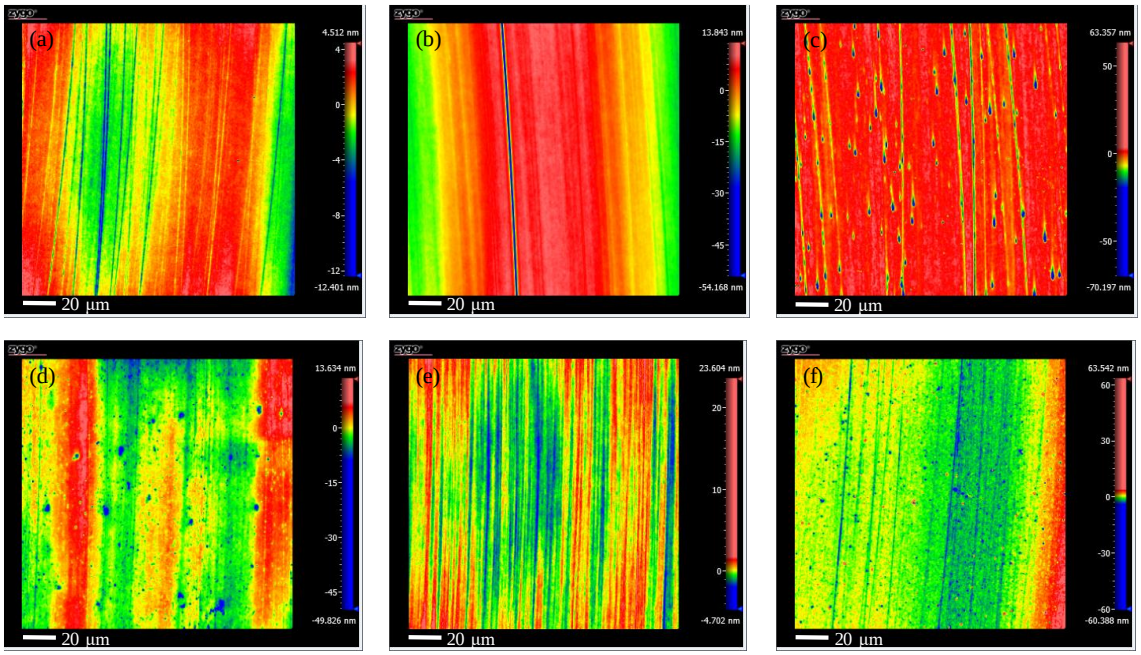

Figure 4.37 SWLI images of ECMP-processed SiC surfaces with current densities of (a) 2 mA/cm^2, *S*q = 1.802 nm, *S*z = 16.912 nm, (b) 3 mA/cm^2, *S*q = 8.168 nm, *S*z = 68.011 nm, (c) 4 mA/cm^2, *S*q = 3.604 nm, *S*z = 133.554 nm, (d) 5 mA/cm^2, *S*q = 3.165 nm, *S*z = 63.460 nm, (e) 10 mA/cm^2, *S*q = 0.770 nm, *S*z = 28.306 nm, and (f) 20 mA/cm^2, *S*q = 1.439 nm, *S*z = 123.930 nm.

4.9 Optimization of slurryless ECMP process

4.9.1 Optimization of polishing motion in slurryless ECMP

Based on the discussions in Sections 4.7 and 4.8, 10 mA/cm^2 is the current density that yields the smoothest SiC surfaces. Nevertheless, at such density there still were many polishing marks on the polished surfaces, which significantly increased the surface roughness. Consequently, removing such polishing marks would considerably reduce the roughness of the polished surface. With such objective, the motion along Y direction was added to make the polishing motion complicated, as shown in Figure 4.38. In particular, three kinds of polishing motion were used to polish sliced 4H-SiC surfaces. For the first one, the SiC wafer only underwent a linear reciprocating motion along the X direction. For the second one, the motion along Y direction was added, with the SiC wafer undergoing a square motion, as shown in Figure 4.38(b). Here, at the center of the SiC surface, fixed abrasives were applied to remove the oxide on the SiC surface in four mutually perpendicular directions. Lastly, for the third one, the SiC wafer underwent cross motion with the linkage of XY stage, as shown in Figure 4.38(c). Moreover, two other motions 45° to the four mutually perpendicular directions were added. As such, the path of the fixed

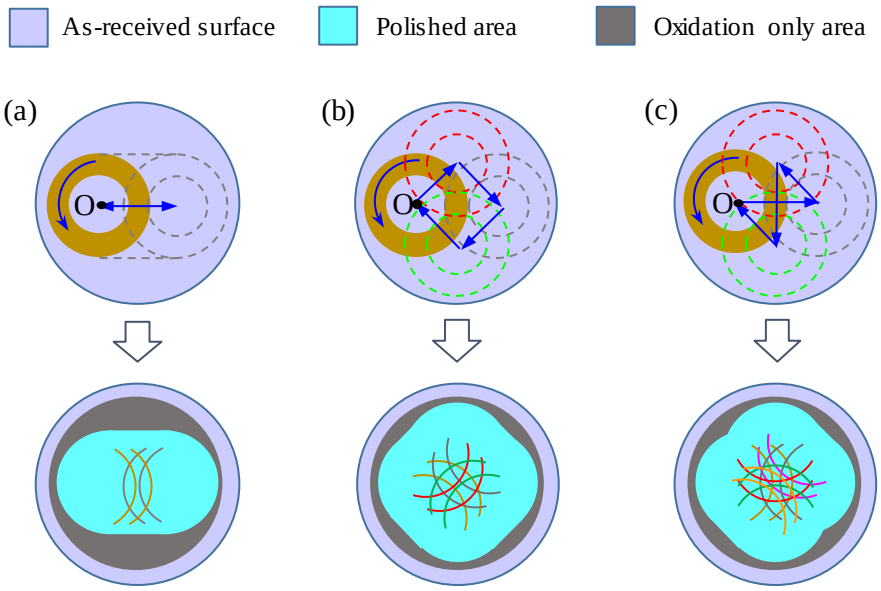

Figure 4.38 Polishing spots and polishing paths of ECMP with (a) linear reciprocating motion of X stage, (b) square motion of XY stages, and (c) cross motion of XY stage.

Table 4.10 Parameters of ECMP with different polishing motions

Parameters	Linear motion	Square motion	Cross motion
Current density (mA/cm^2)	10	10	10
Spindle rotation speed (rpm)	1500	1500	1500
Polishing pressure (kPa)	140	140	140
Feeding rate X (mm/s)	10	10	10
Feeding rate Y (mm/s)		10	10
Reciprocating distance X (mm)	8	4+4	8
Reciprocating distance Y (mm)		4+4	8
Polishing time (min)	120	120	120
Flow rate (mL/min)	380	380	380

abrasives became more complicated. Sliced 4H-SiC (0001) surfaces (on-axis, N-type) shown in Figure 4.33 were polished by ECMP with these three polishing motion patterns, with the ECMP parameters as shown in Table 4.10.

Topographies of the polished surfaces by these three polishing motion patterns are illustrated in Figure 4.39. In the ECMP with linear reciprocating motion, the surface roughness of the sliced surface went down from 0.468 μm to 0.770 nm *Sq*, with many polishing marks observed along the rotation direction of the spindle, as shown in Figure 4.39(a). On the surface polished with

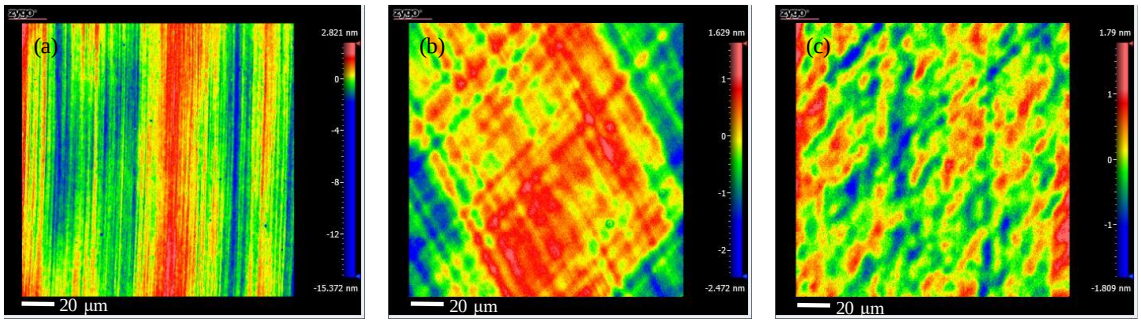

Figure 4.39 SWLI images of SiC surfaces obtained by ECMP with (a) linear reciprocating motion along X direction, *S*q = 0.778 nm, *S*z = 18.194 nm; (b) square motion of XY stages, *S*q = 0.551 nm, *S*z = 4.101 nm; and (c) cross motion of XY stage, *S*q = 0.397 nm, *S*z = 3.599 nm.

square motion, crossed polishing marks were observed, and the surface roughness dropped to 0.551 nm *S*q, as depicted in Figure 4.39(b). These polishing marks were almost completely removed in ECMP with cross motion, as displayed in Figure 4.39(c), in which the surface roughness of the polished surface further decreased to 0.397 nm. Indeed, surface roughness was greatly reduced by the complication of the polishing motion.

Figure 4.40 shows the cross-sectional view of polishing spots obtained by ECMP with different polishing motion patterns. Polishing depths of 11.9, 11.2, and 10.8 µm/h were obtained by linear reciprocating motion, square motion, and cross motion, respectively. Although the difference among these polishing depths was very small, a decreasing trend was observed, which is attributed to the difference in the periods of the different polishing motions that determines the polishing

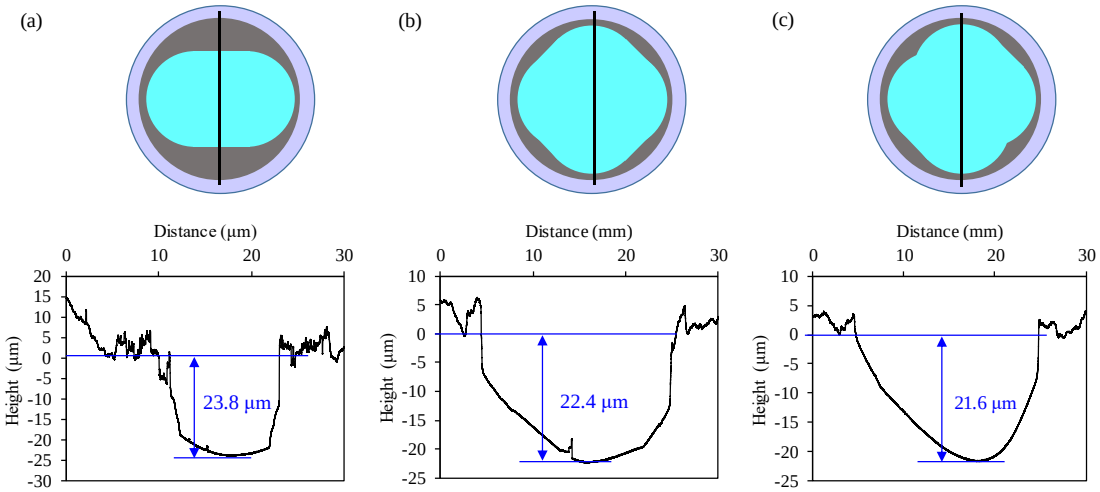

Figure 4.40 Cross-sectional view of polishing spots obtained by ECMP with (a) linear reciprocating motion of X stage, (b) square motion of XY stages, and (c) cross motion of XY stage.

time of a local area on the polished region. The moving distance and feeding rate along either X or Y direction were the same (d = 8 mm, f = 10 mm/s) in these three polishing motions. Therefore, if the time when the worktable changed its moving direction is ignored, then the period of linear reciprocating motion can be expressed as

$$T_{\mathrm{L}} = \frac{2d}{f}, \tag{4.5}$$

while periods of the square polishing motion T_{S} and cross polishing motion T_{C} can be expressed as

$$T_{\mathrm{S}} = \frac{2\sqrt{2}d}{f}, \tag{4.6}$$

$$T_{\mathrm{C}} = \frac{(2+\sqrt{2})d}{f}. \tag{4.7}$$

It is clear that the period of linear reciprocating polishing motion was smaller than that of square polishing motion, but the period of cross polishing motion was the largest. That is, polishing time of the local area was longest in the ECMP with linear reciprocating polishing motion, and shortest in the ECMP with cross polishing motion, which resulted to the difference in the polishing depths. This problem would be solved in the full-size ECMP.

4.9.2 Improvement of surface roughness by optimizing anodic oxidation parameters

Although SiC surfaces with surface roughness of sub-nanoscale order were obtained, many high-frequency features on the polished surface were still visible. Chapter 3 confirmed the anodic oxidation of SiC surface becoming uniform with an increase in oxidation current density, but with several small pits forming on the oxidized surface. If an atomically smooth surface is to be obtained, then no oxide protrusions should form during anodic oxidation. Regarding the LSV study in Chapter 3, the result clarified that a potential of 2.4–3.5 V leads to passivation of the SiC surface, where oxide protrusions would not generate. On such basis, an additional ECMP with a constant potential in the passivation state is considered to be available at the finishing of the surface obtained by ECMP with high current densities.

Accordingly, an ECMP with high current density can be taken as a rough ECMP, for which rapid removal of SSD and significant decrease of surface roughness occur to yield an overall flattening of the SiC surface. Subsequently, an ECMP with low potential can be used as a finish ECMP, in order to remove the micron-sized high-frequency features on the surface generated by the rough ECMP, so as to further decrease the surface roughness. In order to verify the feasibility

of this sequential ECMP process, rough ECMP and finish ECMP were conducted on the sliced 4H-SiC (0001) surface (on-axis, N-type). The experimental parameters are as shown in Table 4.11. Here, the SiC surface was first roughly polished by ECMP with current density of 10 mA/cm^2 for 2 h, and then, the finish ECMP with a potential of 3 V for 1 h was performed on the roughly polished surface. The surface obtained by rough ECMP is presented in Figure 4.41(a), whereas SWLI images of the SiC surface after being polished by finish ECMP are shown in Figure 4.41(b). Based on both figures, the high-frequency feature on the surface obtained by

Table 4.11 Conditions of rough and finish ECMP

	Rough ECMP	Finish ECMP
Current density (mA/cm^2)	10	
Potential (V)		3
Spindle rotation speed (rpm)	1500	1500
Polishing pressure (kPa)	140	140
Feeding rate X (mm/s)	10	10
Feeding rate Y (mm/s)	10	10
Reciprocating distance X (mm)	8	8
Reciprocating distance Y (mm)	8	8
Polishing time (min)	120	60
Flow rate (mL/min)	380	380
Grinding stone	Ceria (#8000)	Ceria (#8000)

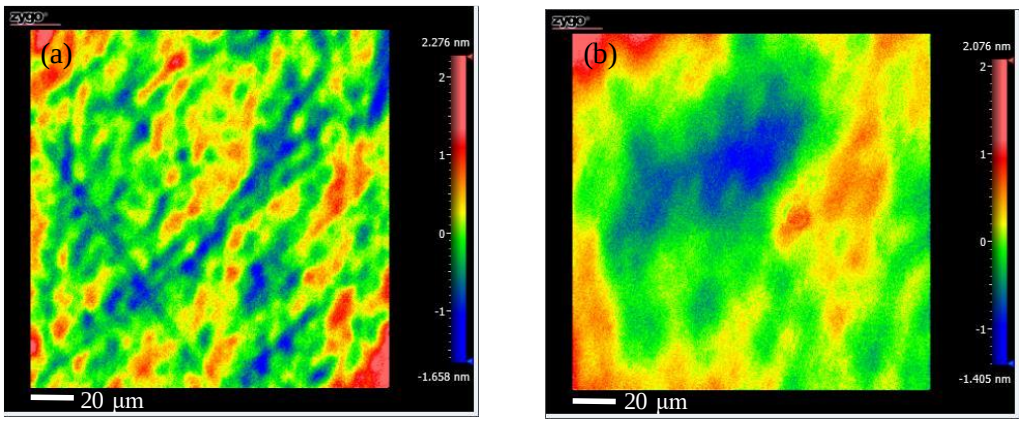

Figure 4.41 SWLI images of (a) SiC surface obtained by ECMP at a current density of 10 mA/cm^2 for 2 h with cross motion of XY stage, *S*q = 0.428 nm, *S*z = 3. 934 nm; and (b) the surface in (a) after an additional ECMP with a constant potential of 3 V for 1 h, *S*q = 0.370 nm, *S*z = 3.481 nm.

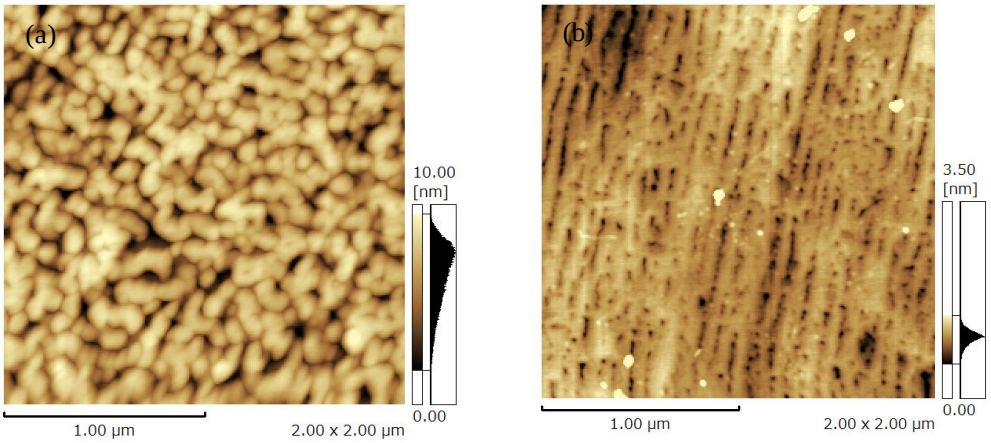

Figure 4.42 AFM images of (a) SiC surface obtained by rough ECMP at a current density of 10 mA/cm^2 for 2 h with cross motion of XY stage, *S*q = 1.956 nm; and (b) the surface in (a) after a finish ECMP with a constant potential of 3 V for 1 h, *S*q = 0.620 nm.

rough ECMP was removed by finish ECMP, yielding an atomically smooth surface with *S*q surface roughness of 0.428 nm and *S*z surface roughness of 3.481 nm.

AFM images of the surfaces obtained by rough ECMP and finish ECMP are illustrated in Figure 4.42. Note that the micron-sized high-frequency features on the SiC surface were completely removed by the additional finish ECMP, resulting to an atomically smooth surface. These results show that slurryless ECMP is very effective in the manufacture of SiC wafers, both in the rough and fine polishing processes.

4.10 Summary

This chapter presented the development of a prototype slurryless ECMP machine, and discussed the application of slurryless ECMP into 4H-SiC wafers with such machine. Also, the polishing mechanism of ECMP was investigated, along with the performance of slurryless ECMP in the polishing of sliced SiC wafers. Moreover, parameters of slurryless ECMP were optimized to obtain the smoothest surface. In general, this chapter presented these main points.

(1) The developed local slurryless ECMP machine pinpoints the efficient utilization of the combination of anodic oxidation and MP. Practically speaking, ECMP utilizing only spindle rotation cannot completely remove the oxide layer, thereby resulting to rough surfaces. By adding X and Y stages to the ECMP machine, an ECMP with different polishing motion patterns was realized.

(2) Simultaneous ECMP and two-step ECMP were conducted. The former obtained a much smoother surface, and confirmed that a smooth surface cannot be obtained by separation of anodic oxidation and mechanical removal or etching of the oxide layer. Simultaneous MP of the oxide layer is thus essential for obtaining smooth SiC surfaces.

(3) Among ceria, alumina, and silica grinding stones, ceria can be applied to give the smoothest surface with relatively high MRR that is attributable to its low hardness and its chemical interactions with the oxide layer. Alumina grinding stone has the highest MRR due to the relatively high hardness, but induces scratches and SSD on the polished surface. Silica grinding stone was almost inefficient in removing the oxide layer. Ceria grinding stone exhibited the best performance in the ECMP of SiC wafers.

(4) The balance between anodic oxidation rate and removal rate of the oxide layer was investigated in the ECMP. Results indicated that the removal rate of the oxide layer should be greater than the oxidation rate so as to obtain an atomically smooth surface, as the interface between the bulk SiC and the oxide layer becomes rough with the thickening of the oxide layer.

(5) Although the grinding stone only removes the oxide layer in ECMP, a combination of feeding rate and spindle rotation speed in ECMP is a critical factor for obtaining smooth SiC surfaces. Moreover, a higher spindle rotation speed yields to a smoother surface given the same feeding rate.

(6) Highly-efficient damage-free polishing of SiC wafers was realized with slurryless ECMP, after application to sliced 4H-SiC (0001) wafers. In particular, after ECMP for 2 h at a current density of 10 mA/cm^2 in NaCl aqueous solution using a #8000 ceria vitrified grinding stone, a scratch-free mirror surface was obtained, with the *S*q roughness of the SiC surface decreased from 286 to 1.352 nm. The MRR was approximately 23 μm/h, and saw marks and surface damage on the sliced surface were completely removed. The flattening and smoothing abilities of slurryless ECMP were confirmed.

(7) The influence of current density on the performance of slurryless ECMP, especially on the MRR, was confirmed. For the sliced SiC wafers supplied by TankeBlue Corporation, the MRR linearly increased as current density increased within less than 5 mA/cm^2, while it saturated at a certain value (of roughly 12.5 μm/h) when the current density exceeded 5 mA/cm^2. The limit of MRR was also found to increase with higher doping concentration. A

possible mechanism pertains to the band bending of SiC being increased while the bandgap of SiC being narrowed by the doping-induced defects (strain) in the bulk SiC; however, further study should confirm this. Moreover, surface flatness and roughness best achieved with the ECMP at current density of 10 mA/cm^2.

(8) Polishing motion in slurryless ECMP was optimized to obtain the smoothest surface. Polishing marks formed in ECMP with linear reciprocating and square motions, but disappeared by application of cross polishing motion to the ECMP process. It was confirmed that the surface roughness decreased with the complexity of polishing motion.

(9) Manufacturing process with rough and finish ECMP was proposed to directly polish the sliced SiC surfaces and yield atomically smooth surfaces. In rough ECMP, SiC wafer was polished with high current density to rapidly remove the SSD on the surface, and then to obtain overall flatness and smoothness of the surface. In finish ECMP, the high-frequency features that formed in the rough ECMP was removed by polishing with a constant potential located in the passive state of the SiC surface. It was also confirmed that a surface with step-terrace structure was obtained by this manufacturing process. The conventional manufacturing process of SiC wafers, which consists of slicing, grinding, lapping, and CMP, can be possibly simplified to slurryless ECMP.

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Chapter 5
Slurryless ECMP with hard grinding stones

5.1 Introduction

In Chapter 3, it was confirmed that scratches and subsurface damage (SSD) on the SiC surface are preferentially oxidized and require higher anodic oxidation rate than the damage-free area during the anodic oxidation process. It was expected that the material removal rate (MRR) of slurryless ECMP can be further improved via introduction of minor SSD on the SiC surface during ECMP. In this chapter, ECMP with fixed-hard abrasives is proposed for the rapid removal and flattening of the sliced SiC wafers in the initial polishing stage. With this ECMP, the hard abrasive particles can be expected to both remove the oxide layer and form minor SSD on the SiC surface, which necessarily increase the MRR.

5.2 The relationship between MRR and SSD in slurryless ECMP

The relationship between SSD and MRR in ECMP was investigated by performing ECMP of 4H-SiC (0001) surfaces (on-axis, N-type) with different surface damages. Sliced SiC wafers supplied by Mizuho Corporation and TankeBlue Semiconductor Co. Ltd., diamond-lapped, and CMP-processed SiC wafers were processed with ECMP. The ECMP parameters used are listed

Table 5.1 ECMP parameters

Current density (mA/cm^2)	10
Spindle rotation speed (rpm)	1500
Polishing pressure (kPa)	140
Feeding rate (mm/s)	10
Reciprocating distance (mm)	5
Polishing time (min)	120
Electrolyte	1 wt% NaCl aqueous solution
Flow rate (mL/min)	380
Grinding stone	Vitrified-bonded ceria (#8000)

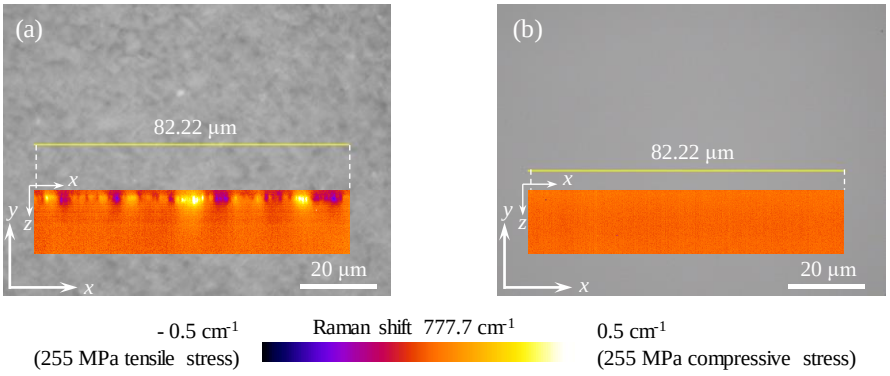

Figure 5.1 Raman spectroscopy measurement results of (a) sliced surface supplied by TankeBlue Semiconductor Co. Ltd. and (b) CMP-processed surface. The insets show the residual stress distributions of surface along the depth direction (*z* direction) measured by confocal Raman microscopy with an observation width of 82.22 μm. The change in the NFP of the laser during the observation is 8 μm.

in Table 5.1; here, linear reciprocating polishing motion along the X direction was applied. Prior to the conduct of ECMP, SSD on these surfaces were evaluated by Raman spectroscopy. As shown in Figure 4.32, residual stress layers with thickness of approximately 16.2 and 3.8 μm were observed on the sliced wafer supplied by Mizuho Corporation and diamond-lapped surface, respectively. Meanwhile, a residual stress layer about 10-μm thick was observed on the sliced surface supplied by TankeBlue Semiconductor Co. Ltd., while no residual stress layer was observed on the CMP-processed surface, as shown in Figure 5.1.

The MRR in the ECMP of SiC surfaces prepared by different machining techniques is shown in Figure 5.2, which was evaluated from the polishing depth of the polished area that measured by a stylus profiler. The sliced surface supplied by Mizuho Corporation exhibited the largest MRR of about 23 μm/h, followed by the sliced surface supplied by TankeBlue Semiconductor Co. Ltd. with MRR of about 12 μm/h, and then by the diamond-lapped surface with MRR of about 8.2 μm/h, and lastly, by the CMP-processed surface having the smallest MRR of about 6.3 μm/h. These results suggest that the MRRs of the SiC wafers decreased with the thinning of the SSD layer. SWLI images of the surfaces obtained after slurryless ECMP are displayed in Figure 5.3. Similar surface topographies were observed for all surfaces, but the sliced surface supplied by Mizuho Corporation after ECMP demonstrated the largest *S*q surface roughness of 1.870 nm. There was a slight difference among the sliced surface supplied by TankeBlue Semiconductor Co. Ltd., the diamond-lapped surface, and CMP-processed surface, of *S*q surface roughness less than 1 nm. These results show that the ECMP of the sliced surface supplied by Mizuho Corporation might need longer time to obtain a smooth surface compared to the others.

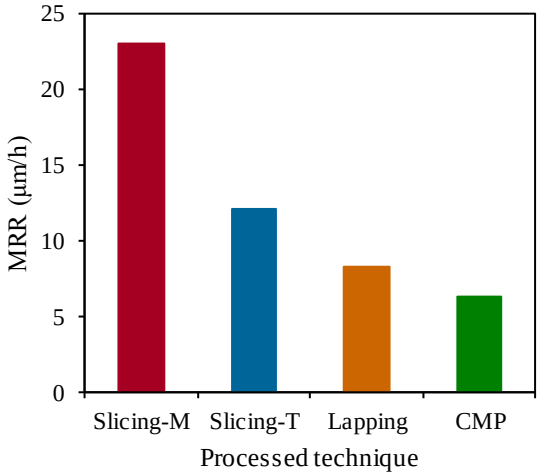

Figure 5.2 MRR in slurryless ECMP of SiC surfaces prepared by different machining techniques. (Slicing-M: sliced surface supplied by Mizuho Corporation, Slicing-T: sliced surface supplied by TankeBlue Semiconductor Co. Ltd.)

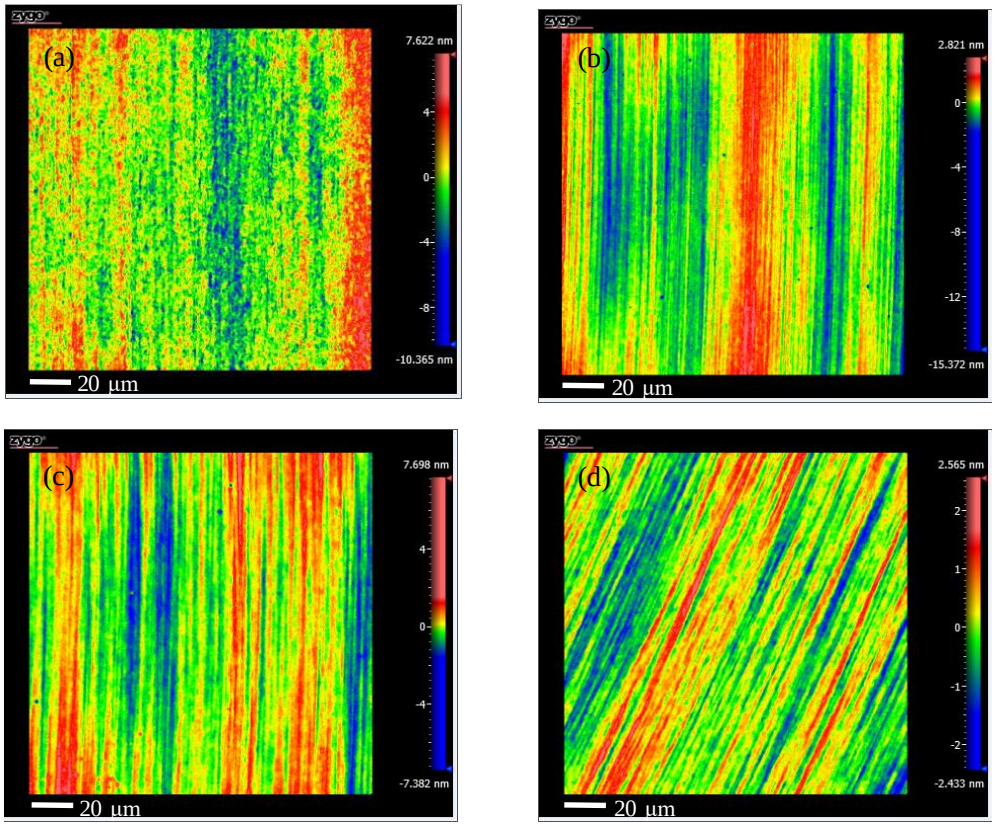

Figure 5.3 SWLI images of SiC surfaces obtained by slurryless ECMP of (a) sliced surface supplied by Mizuho Corporation, *Sq* = 1.870 nm, *Sz* = 17.987 nm, (b) sliced surface supplied by TankeBlue Semiconductor Co. Ltd, *Sq* = 0.778 nm, *Sz* = 18.194 nm, (c) diamond-lapped surface, *Sq* = 0.625 nm, *Sz* = 15.079 nm, and (d) CMP-processed surface, *Sq* = 0.624 nm, *Sz* = 4.998 nm.

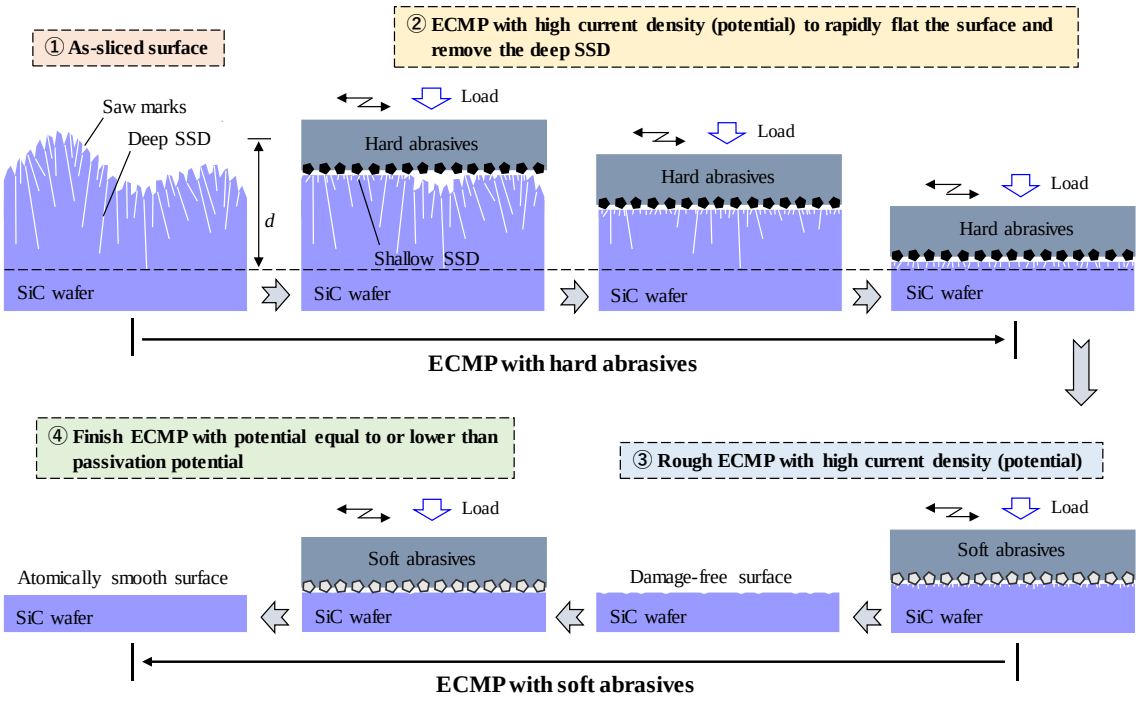

Figure 5.4 Strategy for improving the performance of slurryless ECMP in the polishing of sliced SiC wafers by applying hard abrasives.

The above analysis confirmed that the SiC surface with a thicker SSD layer would most likely exhibit higher MRR in ECMP. As such, the MRR of slurryless ECMP in the polishing of sliced wafers can be deemed to improve further via induction of shallow SSD on the SiC surface during ECMP, as shown in Figure 5.4. Here, the ECMP process is divided into two stages: ECMP with hard abrasives and with soft abrasives. Since the sliced surface have waviness and very thick SSD layer on it, a shallow SSD induced by hard abrasives during ECMP is very effective for rapidly flattening the surface and removing the deep SSD. After the deep SSD with a depth of *d* has been removed, only a shallow SSD layer remains on the SiC surface. Then, rough and finish ECMP with soft abrasives are applied to remove the residual shallow SSD layer and finish the SiC surface. It is expected that a new highly-efficient manufacturing process for SiC wafers can be established by the proposed slurryless ECMP process.

5.3 SSD of surfaces processed by different grinding stones

5.3.1 Introduction

To induce shallow SSD layer on the SiC surface, a suitable abrasive should be selected. The Vickers hardness of common abrasive materials is presented in Table 5.2. Diamond is the hardest, and therefore, is the most promising abrasive. Alumina (Al_2O_3) abrasive is a little harder than SiC,

Table 5.2 Vickers harnesses of common abrasive materials [1-4)]

Materials	Vickers Hardness (GPa)
Diamond	70 - 110
Slicon carbide (SiC)	24 - 28
Sapphire (Al_2O_3)	12 - 23
Silica (SiO_2)	7.6
Ceria (CeO_2)	5 - 7.5

making it feasible for forming shallow SSD on the SiC surface. Silica was confirmed inefficient in such regard, as confirmed in Chapter 4.

5.3.2 MP of 4H-SiC surfaces with different grinding stones

MP of CMP-processed 4H-SiC (0001) surfaces (4°-off, N-type) was carried out to confirm the SSD induced by different abrasives. The SSD induced by ceria abrasives was taken as the standard to evaluate the SSD induced by the other abrasives. Particularly, vitrified-bonded ceria and alumina grinding stones with average particle sizes of 1.0 μm (range of 0.5–2.0 μm, #8000), and diamond grinding stone with an average particle size of 0.2 μm (range of 0–0.5 μm, #20000) were applied for polishing of the SiC surface. The MP parameters are as shown in Table 5.3. Cross polishing motion was used in the MP experiment, with the SiC surfaces being polished for 30 min.

SWLI images of the SiC surfaces mechanically polished with different grinding stones are shown in Figure 5.5. Several large scratches were formed on the surface polished by ceria grinding stone, but these were very shallow so that the surface had relatively small surface

Table 5.3 MP parameters

Spindle rotation speed (rpm)	1500
Polishing pressure (kPa)	140
Feeding rate X (mm/s)	10
Feeding rate Y (mm/s)	10
Reciprocating distance X (mm)	8
Reciprocating distance Y (mm)	8
Polishing time (min)	30
Flow rate (mL/min)	380
Electrolyte	1 wt% NaCl aqueous solution

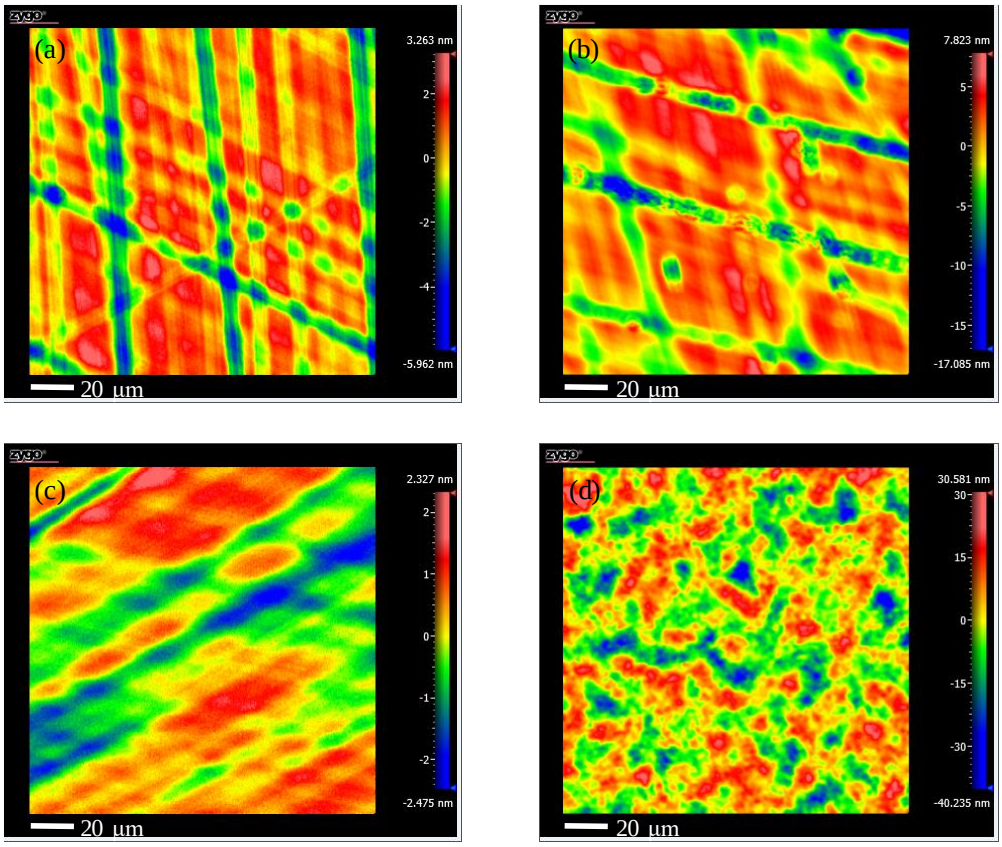

Figure 5.5 SWLI images of CMP-processed 4H-SiC surfaces after MP with grinding stone of (a) ceria, *S*q = 1.385 nm, *S*z = 9.226 nm; (b) Alumina, *S*q = 3.154 nm, *S*z = 24.098 nm; (c) #20000 diamond, *S*q = 0.747 nm, *S*z = 4.802 nm; and (d) #8000 diamond, *S*q = 9.471 nm, *S*z = 70.816 nm.

roughness without microcracks, as shown in Figure 5.5(a). The surface polished by alumina grinding stone in Figure 5.5(b) showed a similar result, where many large scratches appeared after MP, but there were many microcracks, indicating that brittle removal of the SiC surface occurred. Where the abrasives had very small particles (less than 2 µm), the large scratches on the surfaces polished by ceria and alumina grinding stones were attributed from the abrasives aggregation. These results indicate that a single, tiny ceria and alumina abrasive particle was almost unable to remove the SiC surface, thus, a uniform SSD layer was difficult to achieve via application of ceria and alumina grinding stones.

Figure 5.5(c) shows the surface polished with #20000 diamond grinding stone. No obvious scratch was observed, and its surface roughness was much smaller than with the ceria grinding stone. The surface obtained by MP with #8000 diamond grinding stone in Figure 5.5(d) showed many pits, but with no scratches, or alternatively, the observation scale would have been too large to observe the scratches due to their small sizes. The surface was rougher compared with the other

surfaces, but much smaller than that of sliced SiC surface. Additionally, the defects were very uniform on the surface polished by #8000 diamond grinding stone, which is a favorable feature for ECMP to obtain a smooth surface.

Figure 5.6 shows the Raman spectroscopy measurement results of the surfaces mechanically polished by these grinding stones. On the surface polished by ceria grinding stone, it was very difficult to observe the scratches, with very few small residual stresses, as shown in Figure 5.6(a). On the surface polished by alumina grinding stone, the scratches were visible, together the residual stress corresponding to these scratches. Moreover, the residual stress was not uniformly distributed as the scratches themselves were unevenly distributed on the polished surface. The deepest SSD on the observed line reached about 4 μm, although damage-free areas were likewise

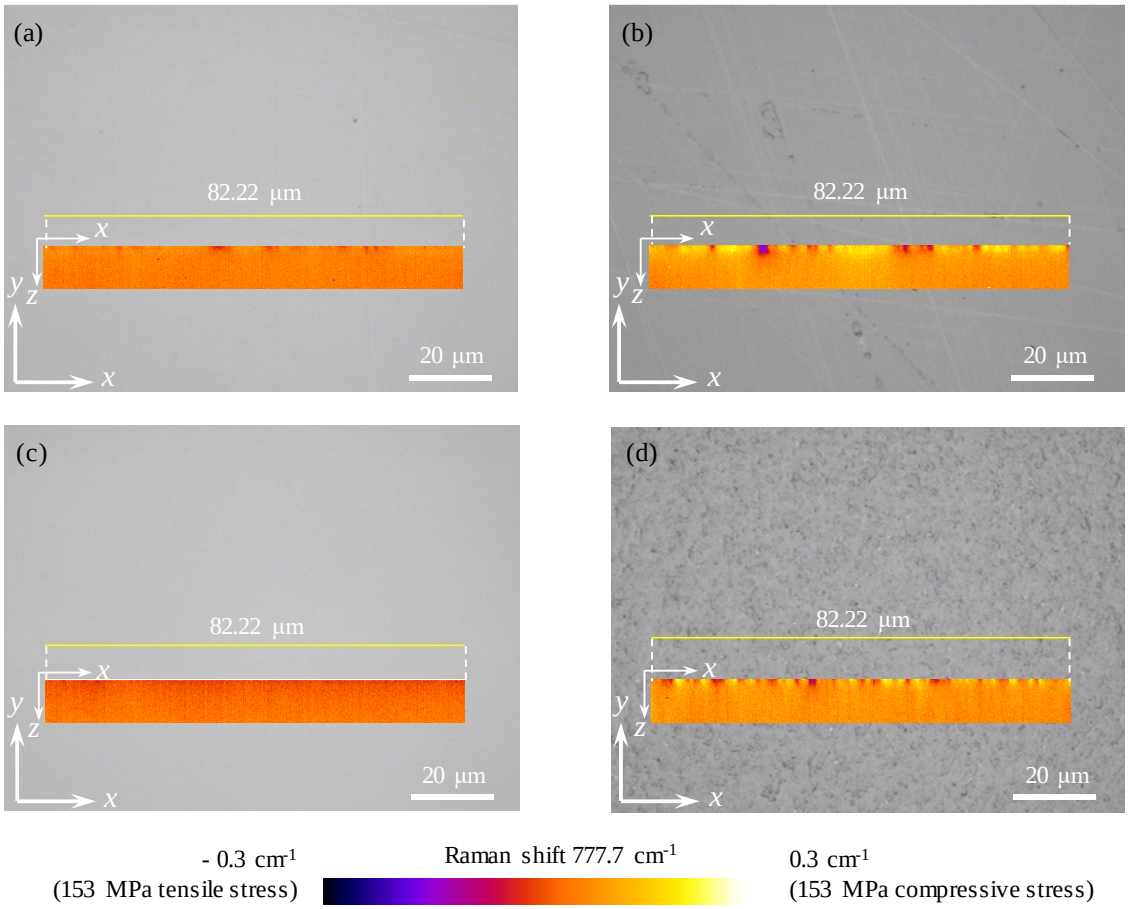

Figure 5.6 Raman spectroscopy measurement results of surfaces obtained by MP with grinding stones of (a) ceria, (b) alumina, (c) diamond #20000, and (d) diamond #8000. The insets show the residual stress distributions of different surfaces along the depth direction (*z* direction) measured by confocal Raman microscopy with an observation width of 82.22 μm. The change in the NFP of the laser during the observation is 4 μm.

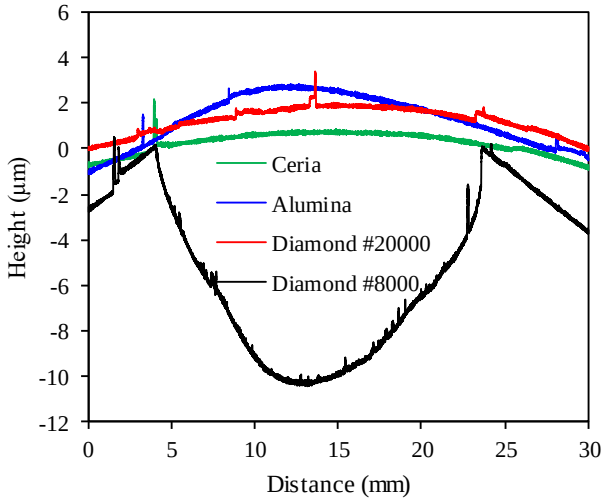

Figure 5.7 Cross-sectional view of polishing area obtained by MP with different grinding stones.

observed. Figure 5.6(c) shows the surface polished by #20000 diamond grinding stone. Although the surface was slightly removed as shown in the SWLI image in Figure 5.5(c), no residual stress was observed. That is, the thickness of the residual stress layer was presumably too thin for the Raman spectroscopy to measure. On the contrary, a uniform residual stress layer about 3-μm thick was observed on the surface polished by #8000 diamond grinding stone, as shown in Figure 5.6(d). The residual stress layer was much thinner than that of the sliced surface, which means that the #8000 grinding stone might be suitable for rapid removal of the thick SSD layer on the sliced surface in ECMP.

Cross-sectional views of the polished areas by MP with different grinding stones are given in Figure 5.7. The SiC surfaces were almost not removed by ceria, alumina, and #20000 diamond grinding stones, but were only induced with some scratches. Nonetheless, a polishing depth of about 10.4 μm was observed in the MP with #8000 diamond grinding stone, with MRR of 20.8 μm/h. The #8000 diamond grinding stone is thus, a very promising abrasive in deep SSD removal on the SiC surface and in improving the MRR of slurryless ECMP.

5.3.3 Slurryless ECMP of 4H-SiC surfaces with different grinding stones

ECMP with ceria, alumina, #20000 diamond, and #8000 diamond grinding stones were conducted on CMP-processed surfaces (4°-off, N-type) to investigate their performance in enhancing the MRR of slurryless ECMP. The ECMP parameters are listed in Table 5.4, where a cross polishing motion was used in ECMP to polish the CMP-processed surfaces for 30 min. Figure 5.8 shows the cross-sectional views of the polished areas and MRRs obtained with the different grinding stones. After the application of anodic oxidation, the SiC surfaces were

Table 5.4 ECMP parameters

Sample	CMP-processed 4H-SiC (0001) wafer (4°-off, N-type)
Current density (mA/cm^2)	10
Spindle rotation speed (rpm)	1500
Polishing pressure (kPa)	140
Feeding rate X (mm/s)	10
Feeding rate Y (mm/s)	10
Reciprocating distance X (mm)	8
Reciprocating distance Y (mm)	8
Polishing time (min)	30
Electrolyte	1 wt% NaCl aqueous solution
Flow rate (mL/min)	380

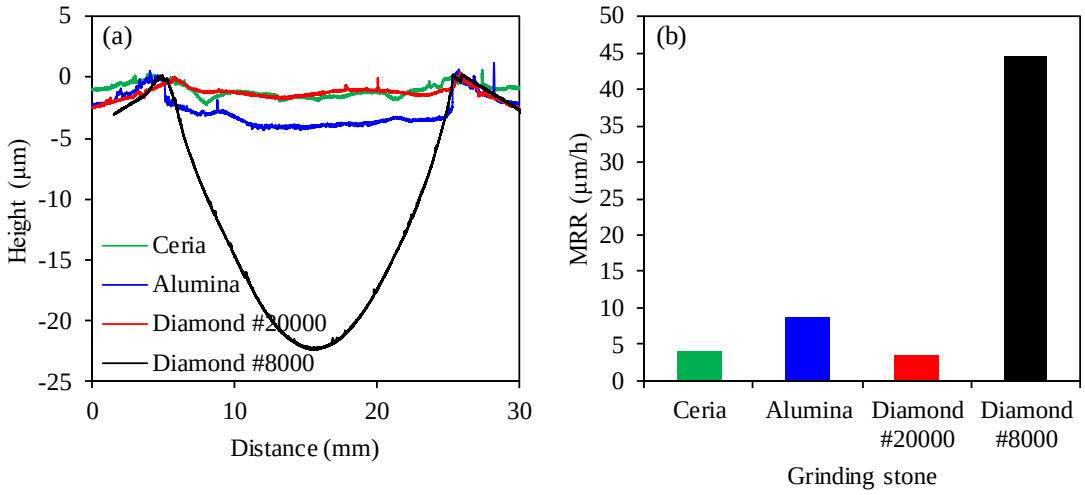

Figure 5.8 (a) Cross-sectional views of polished areas obtained by ECMP with different grinding stones. (b) MRRs of these grinding stones.

removed by all the four grinding stones. Polishing depths obtained by application of #20000 diamond, ceria, and alumina grinding stones were 1.8, 2.0, and 4.2 μm, respectively. These, however, were much smaller than that obtained by #8000 diamond grinding stone that reached about 22.3 μm, for MRR of approximately 44.6 μm/h, which is more than two times the result in MP. Because the SiC surfaces were almost not removed by ceria, alumina, and #20000 diamond grinding stone in MP, as indicated in Figure 5.7, these results suggest that the increase in MRRs

was caused by anodic oxidation of the SiC surface, and that the difference in the increasing amounts was attributed to the difference in SSD induced by the different grinding stones. Moreover, as the SSD layer induced by #8000 diamond grinding stone was a little thinner but more uniform than that induced by alumina grinding stone, much higher MRR was obtained by #8000 diamond grinding stone. Further, the MRR in ECMP was increased by more than twice that in MP for the #8000 diamond grinding stone, which suggests that the softening of the SiC surface by anodic oxidation was also very effective in improving the MRR of ECMP with diamond grinding stones.

SWLI images of SiC surfaces processed by slurryless ECMP with different grinding stones are shown in Figure 5.9. In the case of ceria grinding stone, a smooth surface with *S*q surface roughness of 0.624 nm and *S*z surface roughness of 5.457 nm was obtained. With the alumina grinding stone, a surface with large pits and wide scratches resulted from the ECMP, which is

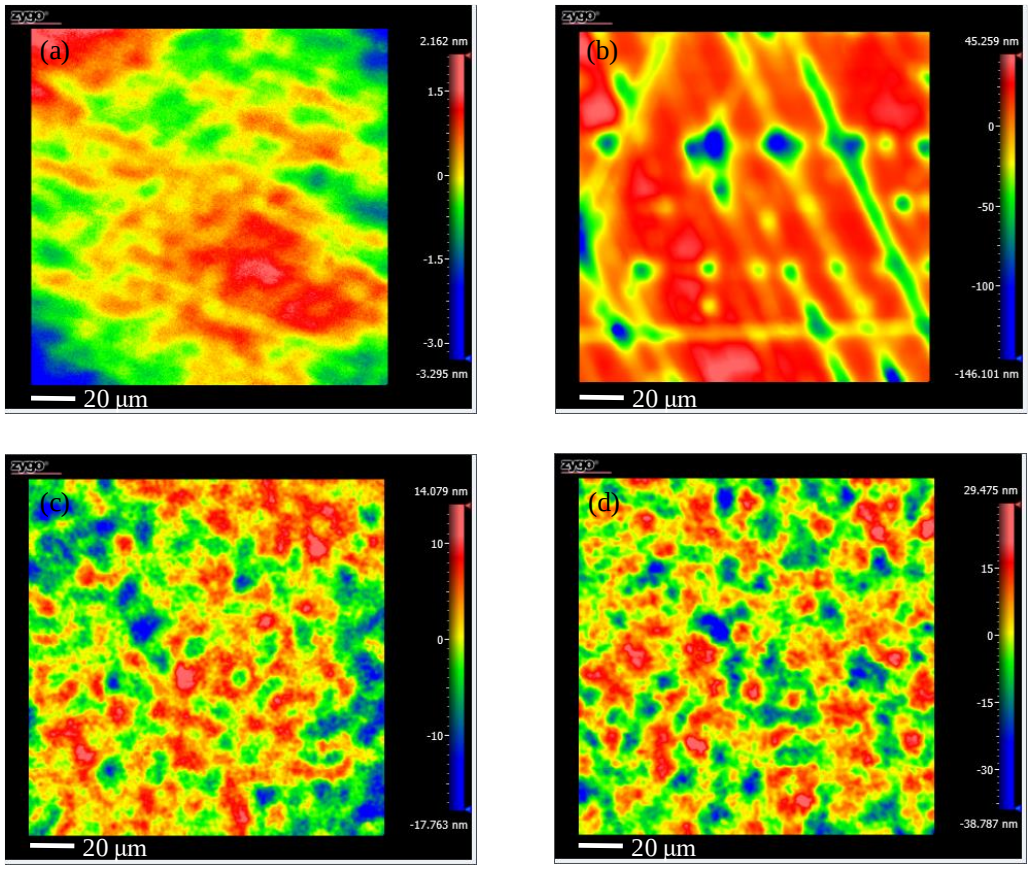

Figure 5.9 SWLI images of SiC surfaces obtained by ECMP with (a) ceria grinding stone, *S*q = 0.624 nm, *S*z = 5.457 nm; (b) Alumina grinding stone, *S*q = 24.757 nm, *S*z = 191.360 nm; (c) #20000 diamond grinding stone, *S*q = 4.643 nm, *S*z = 31.842 nm; (d) #8000 diamond grinding stone, *S*q = 8.691 nm, *S*z = 68.262 nm.

similar to the surface obtained in the MP of CMP-processed surface with the same abrasive, as shown in Figure 5.5(b). As the SSD induced on the SiC surface was not uniform by the alumina grinding stone, as shown in Figure 5.6(b), the SSD sites were preferentially oxidized causing a rough surface with *S*q surface roughness reaching 24.757 nm and *S*z surface roughness reaching 191.360 nm. These roughness values were unfavorable for the subsequent final polishing of the SiC surface. The topography of the surface processed by ECMP with #20000 diamond grinding stone was similar to that obtained by #8000 diamond grinding stone, as shown in Figures 5.9(c) and (d), but had lower surface roughness. It is considered that the oxide layer was not completely removed by #20000 diamond grinding stone as it had the shallowest polishing depth, as shown in Figure 5.8(a). The surface processed by ECMP with #8000 diamond grinding stone was almost the same with that obtained in MP, as shown in Figure 5.9(d), which is suggestive of mechanical removal of the SiC surface during ECMP with the #8000 diamond grinding stone, so that the oxide generated by anodic oxidation in the ECMP process almost had no effect on the mechanical removal, due to the lower hardness.

Figure 5.10 shows the changes in potential during ECMP with different grinding stones. The smallest potential was observed in the ECMP with #8000 diamond grinding stone. With constant current density applied in the ECMP, the potential reflected difficulty in the anodic oxidation of the SiC surfaces. Thus, this result suggests that the anodic oxidation of the SiC surface during ECMP with #8000 diamond grinding stone was the easiest among the other grinding stones. Applying #8000 diamond grinding stone promoted the mechanical removal of the SiC surface via the anodic oxidation; conversely, the anodic oxidation was promoted by the mechanical removal of the SiC surface.

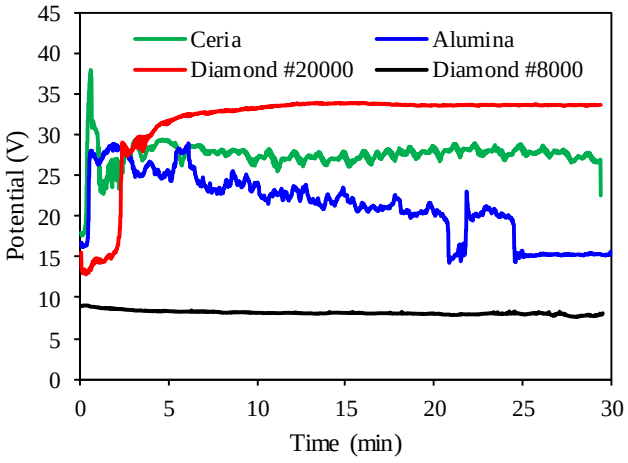

Figure 5.10 Changes in potential during constant current ECMP of CMP-processed SiC surfaces with different grinding stones.

5.4 Improvement of MRR of slurryless ECMP by applying hard abrasives

Based on the results in the preceding Sections, #8000 diamond grinding stone was selected to improve the MRR of ECMP in the initial polishing stage of a sliced SiC surface (on-axis, N-type) supplied by TankeBlue Semiconductor Co. Ltd. Table 5.5 shows the ECMP parameters. Here, cross polishing motion was applied. The sliced SiC surface was firstly polished by ECMP with #8000 diamond grinding stone for 20 min to rapidly remove the deep SSD, and then the obtained surface was polished by ECMP with ceria grinding stone for 30 min to remove the shallow SSD layer.

SWLI images of the sliced SiC surface is shown in Figure 5.11(a). The surface was very rough, with *S*q surface roughness of 0.110 μm and *S*z surface roughness of 1.081 μm. After ECMP with #8000 diamond grinding stone for only 20 min, the *S*q and *S*z surface roughness went down to 9.768 and 79.910 nm, respectively, as shown in Figure 5.11(b), very close to those obtained after ECMP of the CMP-processed surface shown in Figure 5.9(d). After an additional ECMP with ceria grinding stone for only 30 min, the *S*q and *S*z surface roughness dropped to 0.429 and 3.399 nm, respectively, which is comparable to those of the surface after a direct ECMP with ceria grinding stone for 2 h, as discussed in Chapter 4. These results show that the flattering and smoothening of the sliced surfaces were realized with the proposed ECMP process. The obtained SiC surface can be further smoothened by application of finish ECMP described in Section 4.9.

Table 5.5 ECMP parameters for a sliced SiC surface

	ECMP with hard abrasives	ECMP with soft abrasives
Current density (mA/cm^2)	10	10
Spindle rotation speed (rpm)	1500	1500
Polishing pressure (kPa)	140	140
Feeding rate X (mm/s)	10	10
Feeding rate Y (mm/s)	10	10
Reciprocating distance X (mm)	8	8
Reciprocating distance Y (mm)	8	8
Polishing time (min)	20	30
Flow rate (mL/min)	380	380
Grinding stone	Diamond (#8000)	Ceria (#8000)

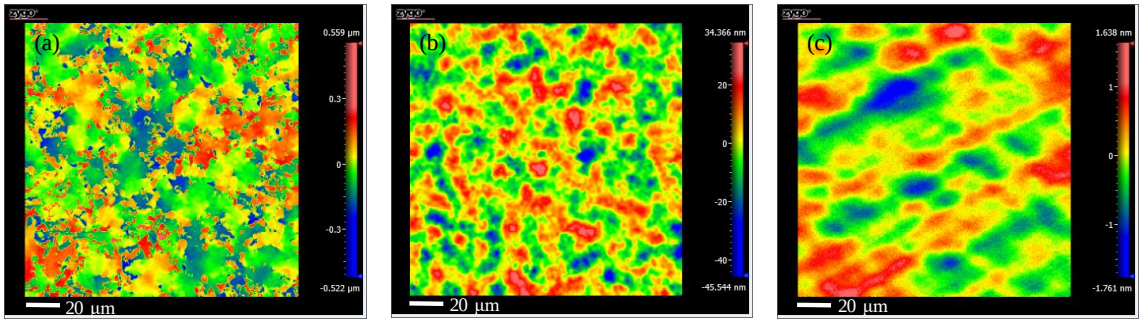

Figure 5.11 SWLI images of (a) sliced SiC surface, *S*q = 0.110 μm, *S*z = 1.081 μm; (b) the sliced surface after ECMP with #8000 diamond grinding stone for 20 min, *S*q = 9.768 nm, *S*z = 79.910; and (c) after an addition ECMP with ceria grinding stone for 30 min, *S*q = 0.429 nm, *S*z = 3.399 nm.

Figure 5.12 shows the Raman spectroscopy measurement results of the surfaces after ECMP with #8000 diamond grinding stone for 20 min, and after an additional ECMP with ceria grinding stone for 30 min. A residual stress layer similar to that obtained in the MP of the CMP-processed SiC surface with #8000 diamond grinding stone, was observed on the surface after ECMP with #8000 diamond grinding stone for 20 min, as shown in Figure 5.12(a). This result suggests that the mechanical removal of the oxide layer and the bulk SiC occurred simultaneously during ECMP with the diamond grinding stone. After an additional ECMP with ceria grinding stone for

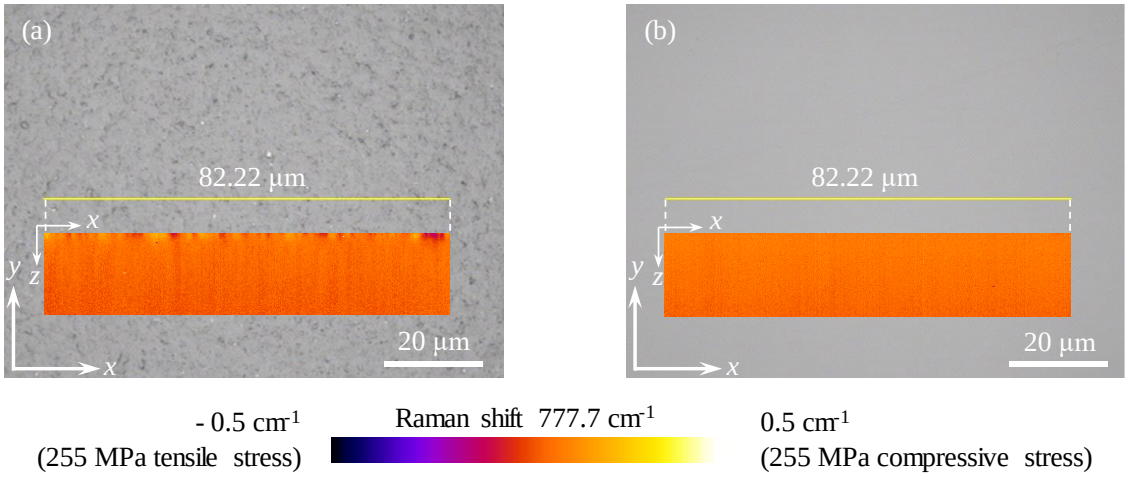

Figure 5.12 Raman spectroscopy measurement results of surfaces obtained by (a) ECMP with #8000 diamond grinding stone for 20 min, and (b) after an additional ECMP with ceria grinding stone for 30 min. The insets show the residual stress distributions of different surfaces along the depth direction (*z* direction) measured by confocal Raman microscopy with an observation width of 82.22 μm. The change in the NFP of the laser during the observation is 8 μm.

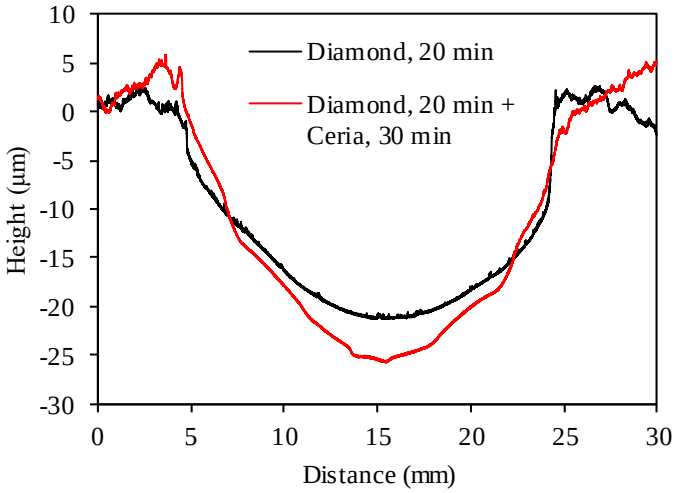

Figure 5.13 Cross-sectional view of the polished area in different ECMP stages.

30 min, the residual SSD layer on the surface polished by ECMP with diamond grinding stone was removed and a damage-free surface was obtained, as shown in Figure 5.12 (b). These results indicate that deep SSD layer on the sliced surface was completely removed by these two ECMP processes.

Figure 5.13 shows the cross-sectional views of the polished areas under different ECMP stages. A polishing depth of approximately 21 μm was obtained after ECMP with #8000 diamond grinding stone for 20 min, which increased to about 25.6 μm after an additional ECMP with the ceria grinding stone for 30 min. MRRs of 63 and 9.2 μm/h resulted from the ECMP with #8000 diamond and ceria grinding stones, respectively. These results show that the performance of slurryless ECMP significantly improved via the application of #8000 diamond grinding stone. Moreover, the *S*q surface roughness of the sliced wafer decreased from 0.11 μm to less than 0.5 nm within 50 min, which is comparable to the polishing results obtained by ECMP with ceria grinding stone for 2 h, as shown in Section 4.9.

5.5 Summary

This chapter highlighted the proposal of slurryless ECMP with hard abrasives for further improvement of the performance of slurryless ECMP. It conducted an investigation of the relationship between MRR and SSD on the SiC surface, as well as that of the SSD induced by different grinding stones. In the last part, it presented an evaluation of the performance of ECMP with hard abrasives via ECMP experiments on a sliced 4H-SiC (0001) surface. The main points are presented below.

(1) Based on the investigation of the relationship between MRR and SSD on the SiC surface, the MRR of slurryless ECMP decreases when there are less SSDs on the SiC surface. Hard abrasives were favorable to keep the MRR in the polishing process of the sliced SiC surfaces. Shallow SSD was induced during the ECMP with hard abrasives, keeping a high MRR for rapid removal of deep SSD on the sliced SiC surface. After removal of the deep SSD, only a shallow SSD layer existed on the SiC surface, which can be removed for a short time by an additional ECMP with soft abrasives.

(2) Different grinding stones exhibited different performances in inducing SSD on the SiC surface. Ceria and #20000 diamond grinding stones were almost unable to induce SSD on the SiC surface and alumina grinding stone formed an uneven SSD, whereas #8000 diamond grinding stone induced a uniform SSD layer on the SiC surface, thus, is preferable for the subsequent, additional ECMP with soft abrasives for removal of the SSD layer.

(3) CMP-processed SiC surfaces were subjected to ECMP with different grinding stones. Ceria and #20000 diamond grinding stones yielded the lowest MRR, which is considered to be the same with the oxidation rate. SSD formed by alumina grinding stone enhanced the anodic oxidation rate, which resulted in relatively high MRR; nonetheless, the polished surface was very rough due to the non-uniform SSD. ECMP with #8000 diamond grinding stone exhibited simultaneous mechanical removal of SiC surface and removal of the oxide layer, which resulted in high MRR of 20.8 μm/h, more than two times greater than that of MP. Thus, by applying #8000 diamond grinding stone, mechanical removal of the SiC surface was promoted by the anodic oxidation, and conversely, the anodic oxidation was promoted by the mechanical removal of the SiC surface.

(4) The performance of the proposed combination in ECMP process was evaluated through ECMP experiments with #8000 diamond and ceria grinding stones on a sliced SiC surface. A smooth damage-free surface obtained, which is comparable with the surface obtained by ECMP with ceria grinding stone for 2 h, was attained with the proposed ECMP process for only 50 min.

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Chapter 6
Summary

Slurryless electrochemical mechanical polishing (ECMP), which uses anodic oxidation to modify the surfaces to a soft oxide layer, and fixed soft abrasives to remove the oxide layer, was developed for the highly-efficient, low-cost, and damage-free polishing of SiC wafers. The anodic oxidation properties and mechanism of 4H-SiC (0001) surface were studied through a series of anodic oxidation experiments. The performance of slurryless ECMP was investigated using the developed prototype slurryless ECMP machine, and the ECMP process was optimized to obtain the smoothest SiC surfaces. Subsequently, the manufacturing process of SiC wafer using slurryless ECMP was established. The efficiency of ECMP was further improved to reduce time and cost in the manufacture of SiC wafers.

Chapter 1 described the background of the study, current issues in the manufacture of SiC wafers, the performance, properties, and applications of SiC, and the aim of the study.

In Chapter 2, for realizing a highly-efficient, low cost, and damage-free polishing and flattening of SiC wafer, a review of the existing manufacturing processes and polishing techniques of SiC wafers was conducted and the advantages and disadvantages of the polishing techniques were summarized. Slurryless ECMP was proposed as a solution to solve the problems in these polishing techniques, and to simplify the manufacturing process of SiC wafers. The feasibility of applying neutral electrolytes to slurryless ECMP was also examined.

(1) At present, the manufacturing process of SiC wafer is very complex, and current polishing techniques are unable to simplify it. In general, these techniques cannot realize a highly-efficient, low-cost, and damage-free polishing of SiC wafers: some have low efficiency, some are very costly, and some have insufficient precision. These issues necessitate the development of a new polishing technique.

(2) ECMP using slurry does not produce a flat and atomically smooth surface. In addition, the application of loose abrasive in slurry ECMP make it very difficult to separately control the anodic oxidation and polishing parameters, thereby limiting the polishing performance.

(3) The proposed slurryless ECMP combines surface modification and fixed-abrasive polishing. By this method, the SiC surface is first modified by anodic oxidation, and then the modified layer is removed by fixed soft abrasives. As the abrasive is much softer than SiC, only the modified layer is removed to achieve a damage-free surface. The SiC surface can also be flattened with the fixed-abrasive polishing, eventually leading to an atomically flat and smooth surface.

(4) The possibility of using neutral electrolytes to the slurryless ECMP of SiC wafer was also examined. Here, the equilibrium condition of reactions in the anodic oxidation system of SiC was calculated, and Pourbiax diagram of SiC was obtained. On the basis of the Pourbiax diagram of SiC, chlorine and nitrate solutions were found possible to be used as electrolyte for the anodic oxidation of SiC.

In Chapter 3, anodic oxidation of 4H-SiC (0001) surfaces were conducted in neutral electrolytes. The anodic oxidation of 4H-SiC (0001) surface in neutral electrolytes and the softening effect of anodic oxidation were confirmed. Besides, the anodic oxidation property and mechanism of 4H-SiC (0001) surface were investigated. On the basis of these results, strategy for obtaining smooth SiC surfaces using slurryless ECMP was proposed.

(1) Anodic oxidations of 4H-SiC (0001) surfaces were performed in NaCl and $NaNO_3$ aqueous solutions. XPS analysis confirmed that the surfaces were anodically oxidized in both solutions, although oxidation was not uniform and resulted to the increase in surface roughness after removal of the oxide layer. The difference between the anodic oxidations in these two electrolytes was very small and an oxidation rate of approximately 40 nm/min was obtained, but the NaCl solution exhibited higher efficiency of electric energy.

(2) The softening effect of anodic oxidation was confirmed, with SiC hardness significantly decreasing from 41.98 to 3.59 GPa after anodic oxidation. Although the anodic oxide layer, synthetic quartz glass, and borosilicate glass mainly composed of SiO_2, it was found that the anodically oxidized surface was softer than these glass materials.

(3) LSV measurement was applied to investigate the relationship between the oxide protrusions and the oxidation potential. It revealed an *I–V* curve for SiC that is similar to that of general metal anodization having five oxidation periods, namely, unoxidized state, active state, passive state, transient state, and transpassive state.

(4) Oxide protrusions were observed as SiC was oxidized in the transient and transpassive states. These were generated from the sites of breakdown on the passivation film. Moreover, their density increased while their diameter and volume decreased, with an increase in potential (current). Besides, almost the same oxidation degree of scratches and areas without scratches were obtained in high oxidation current densities. This points out that for an abrasive-polished SiC substrate subjected to the ECMP process, the surface should be oxidized under high oxidation rate to fully remove the damaged layer on the surface. Subsequently, the surface should be polished at a low potential corresponding to the passive state, to avoid the generation of etch pits, as well as to obtain an atomically smooth surface.

(5) Investigation of the time dependence of anodic oxidation of SiC revealed that the anodic oxidation of SiC continues with oxidation time, even lasting for 10 h. This was because the outer oxide layer becomes porous and accommodates several cracks with the volume expansion of SiC after anodic oxidation for a certain time. The surface roughness of the oxidized surface after the oxide layer has been removed increased with oxidation time in both constant potential and constant current anodic oxidation.

(6) Results of the investigation of the off-angle dependence of anodic oxidation of SiC confirmed that the oxidation rate of 4H-SiC increases with greater off-angle as the oxidation of SiC surface originates from the terrace edges. Additionally, 4H2 terraces demonstrated higher oxidation rate than 4H1 terraces.

(7) The oxide protrusions originated from atomic pits introduced by large abrasive particles or a high polishing pressure during the CMP process. Depending on their geometric structure, these atomic pits could have different breakdown thresholds. The SSD induced by indenter was preferentially oxidized compared with the atomic pits.

(8) Through modeling of the growth process of the oxide protrusions, the growth process was found to be controlled by the charge transfer process at the initial stage, which changed to a diffusion process after the oxide protrusions grew to the size order of 100 nm.

(9) Repeated anodic oxidation and HF etching were conducted on a 4H-SiC (0001) face, with which the effects of surface damage on the anodic oxidation properties were investigated. Anodic oxidation proved very effective for removing the surface damage formed by mechanical polishing. The surface was easier to oxidize after removal of the surface damage by oxidation/etching; moreover, the oxidation became relatively uniform. This is favorable for obtaining a SiC substrate with a smooth surface by slurryless ECMP.

(10) Changes in current were different in the anodic oxidations of surfaces with and without SSD. A model based on the electrochemical impedance method was built to dig deeper on such differences; the results of such investigation revealed that the oxidation area and the anisotropy of 4H-SiC plays a dominant role in determining the oxidation rate of the SiC surface.

(11) Porous SiC was generated in the repeated anodic oxidation and etching of 4H-SiC (0001) surfaces. It was mainly caused by the anisotropy of the SiC crystal and the Fermi level pinning that occurred on the nanometer-thick SiC fibers. The structure of the porous SiC was significantly dependent on the etch pits generated at the beginning of the oxidation, and can be controlled via the anodic oxidation parameters.

(12) Surface roughness increased with repeated anodic oxidation and HF etching. The initial oxidation period of the SiC surface was dominated by the distribution of SSD on the SiC wafer, and then by the anisotropy of single-crystal 4H-SiC after the subsurface damage had been completely oxidized. For both types of oxidation, the surface roughness increased with longer oxidation time.

(13) A strategy has been proposed for obtaining smooth SiC surface using slurryless ECMP, as a smooth surface is not attainable by a combination of anodic oxidation and HF etching alone, and because the surface roughness of oxidized/etched surface increases with oxidation time. To obtain a smooth surface, it is presumed that the oxide layer should be immediately removed after its generation, that is, the removal rate of the oxide layer should be greater than the anodic oxidation rate in slurryless ECMP.

In Chapter 4, a prototype slurryless ECMP machine was developed to realize the polishing of SiC wafers, the structure and polishing properties of this slurryless ECMP machine were introduced. Then, slurryless ECMP was applied to 4H-SiC wafers. The polishing properties of different grinding stones and the performance of two-step ECMP and simultaneous ECMP were investigated. The application results of slurryless ECMP to the sliced SiC wafers were introduced and analyzed. Besides, the polishing motions and polishing process of slurryless ECMP were optimized. A novel manufacturing process for 4H-SiC wafers was established by applying slurryless ECMP.

(1) The developed local slurryless ECMP machine pinpoints the efficient utilization of the combination of anodic oxidation and MP. Practically speaking, ECMP utilizing only spindle rotation cannot completely remove the oxide layer, thereby resulting to rough surfaces. By adding X and Y stages to the ECMP machine, an ECMP with different polishing motion patterns was realized.

(2) Simultaneous ECMP and two-step ECMP were conducted. The former obtained a much smoother surface, and confirmed that a smooth surface cannot be obtained by separation of anodic oxidation and mechanical removal or etching of the oxide layer. Simultaneous MP of the oxide layer is thus essential for obtaining smooth SiC surfaces.

(3) Among ceria, alumina, and silica grinding stones, ceria can be applied to give the smoothest surface with relatively high MRR that is attributable to its low hardness and its chemical interactions with the oxide layer. Alumina grinding stone has the highest MRR due to the relatively high hardness, but induces scratches and SSD on the polished surface. Silica grinding stone was almost inefficient in removing the oxide layer. Ceria grinding stone exhibited the best performance in the ECMP of SiC wafers.

(4) The balance between anodic oxidation rate and removal rate of the oxide layer was investigated in the ECMP. Results indicated that the removal rate of the oxide layer should be greater than the oxidation rate so as to obtain an atomically smooth surface, as the interface between the bulk SiC and the oxide layer becomes rough with the thickening of the oxide layer.

(5) Although the grinding stone only removes the oxide layer in ECMP, a combination of feeding rate and spindle rotation speed in ECMP is a critical factor for obtaining smooth SiC surfaces. Moreover, a higher spindle rotation speed yields to a smoother surface given the same feeding rate.

(6) Highly-efficient damage-free polishing of SiC wafers was realized with slurryless ECMP, after application to sliced 4H-SiC (0001) wafers. In particular, after ECMP for 2 h at a current density of 10 mA/cm^2 in NaCl aqueous solution using a #8000 ceria vitrified grinding stone, a scratch-free mirror surface was obtained, with the *S*q roughness of the SiC surface decreased from 286 to 1.352 nm. The MRR was approximately 23 μm/h, and saw marks and surface damage on the sliced surface were completely removed. The flattening and smoothing abilities of slurryless ECMP were confirmed.

(7) The influence of current density on the performance of slurryless ECMP, especially on the MRR, was confirmed. For the sliced SiC wafers supplied by TankeBlue Corporation, the MRR linearly increased as current density increased within less than 5 mA/cm^2, while it saturated at a certain value (of roughly 12.5 μm/h) when the current density exceeded 5 mA/cm^2. The limit of MRR was also found to increase with higher doping concentration. A possible mechanism pertains to the band bending of SiC being increased while the bandgap of SiC being narrowed by the doping-induced defects (strain) in the bulk SiC; however, further study should confirm this. Moreover, surface flatness and roughness best achieved with the ECMP at current density of 10 mA/cm^2.

(8) Polishing motion in slurryless ECMP was optimized to obtain the smoothest surface. Polishing marks formed in ECMP with linear reciprocating and square motions, but disappeared by application of cross polishing motion to the ECMP process. It was confirmed that the surface roughness decreased with the complexity of polishing motion.

(9) Manufacturing process with rough and finish ECMP was proposed to directly polish the sliced SiC surfaces and yield atomically smooth surfaces. In rough ECMP, SiC wafer was polished with high current density to rapidly remove the SSD on the surface, and then to obtain overall flatness and smoothness of the surface. In finish ECMP, the high-frequency features that formed in the rough ECMP was removed by polishing with a constant potential located in the passive state of the SiC surface. It was also confirmed that a surface with step-terrace structure was obtained by this manufacturing process. The conventional manufacturing process of SiC wafers, which consists of slicing, grinding, lapping, and CMP, can be possibly simplified to slurryless ECMP.

In Chapter 5, slurryless ECMP with hard abrasives was proposed to further improve the MRR of slurryless ECMP. The relationship between MRR and SSD on the SiC surface was investigated, and the SSD induced by different grinding stones were also studied. Finally, the performance of ECMP with hard abrasives was evaluated by conducting slurryless ECMP on a sliced 4H-SiC (0001) surface.

(1) Based on the investigation of the relationship between MRR and SSD on the SiC surface, the MRR of slurryless ECMP decreases when there are less SSDs on the SiC surface. Hard abrasives were favorable to keep the MRR in the polishing process of the sliced SiC surfaces. Shallow SSD was induced during the ECMP with hard abrasives, keeping a high MRR for

rapid removal of deep SSD on the sliced SiC surface. After removal of the deep SSD, only a shallow SSD layer existed on the SiC surface, which can be removed for a short time by an additional ECMP with soft abrasives.

(2) Different grinding stones exhibited different performances in inducing SSD on the SiC surface. Ceria and #20000 diamond grinding stones were almost unable to induce SSD on the SiC surface and alumina grinding stone formed an uneven SSD, whereas #8000 diamond grinding stone induced a uniform SSD layer on the SiC surface, thus, is preferable for the subsequent, additional ECMP with soft abrasives for removal of the SSD layer.

(3) CMP-processed SiC surfaces were subjected to ECMP with different grinding stones. Ceria and #20000 diamond grinding stones yielded the lowest MRR, which is considered to be the same with the oxidation rate. SSD formed by alumina grinding stone enhanced the anodic oxidation rate, which resulted in relatively high MRR; nonetheless, the polished surface was very rough due to the non-uniform SSD. ECMP with #8000 diamond grinding stone exhibited simultaneous mechanical removal of SiC surface and removal of the oxide layer, which resulted in high MRR of 20.8 μm/h, more than two times greater than that of MP. Thus, by applying #8000 diamond grinding stone, mechanical removal of the SiC surface was promoted by the anodic oxidation, and conversely, the anodic oxidation was promoted by the mechanical removal of the SiC surface.

(4) The performance of the proposed combination in ECMP process was evaluated through ECMP experiments with #8000 diamond and ceria grinding stones on a sliced SiC surface. A smooth damage-free surface obtained, which is comparable with the surface obtained by ECMP with ceria grinding stone for 2 h, was attained with the proposed ECMP process for only 50 min.

In this study, the proposed slurryless ECMP was developed and applied to 4H-SiC wafers. This included an investigation and understanding of the anodic oxidation property and mechanism of 4H-SiC (0001) surface and the polishing mechanism of slurryless ECMP. Upon application of slurryless ECMP to sliced 4H-SiC (0001) surfaces, MRRs ranging from 10 to 23 μm/h and damage-free surfaces with *S*q surface roughness of less than 1 nm were obtained. Optimizing the polishing motion and the ECMP process yielded an atomically smooth surface, and led to the establishment of the manufacturing process of 4H-SiC wafers using the proposed method. Applying ECMP with hard-fixed abrasives for sliced SiC surfaces significantly reduced the

polishing time of ECMP from 2 h to 50 min to obtain a smooth surface with *S*q surface roughness of less than 0.5 nm.

Furthermore, slurryless ECMP abolishes the use of slurry and strong chemicals, so that SiC wafers are polished in an environment-friendly manner and at low cost. Additionally, the application of grinding stones smoothens and flattens the processed SiC surfaces, thereto expanding the application of ECMP from final polishing to flattening. Based on the findings laid out in this study, the current manufacturing process of SiC wafer can be simplified with slurryless ECMP. The industrial application of slurryless ECMP is strongly expected, and will be attempted for discussion in future studies.

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