論 文 内 容 の 要 旨

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論文題名	Proactive Supply Noise Mitigation and Design Methodology for Robust VLSI Power Distribution (予測的電源ノイズ低減とロバストなVLSI電源分配網設計手法)

論文内容の要旨

With the scaling down of the technology node, both power consumption, and supply noise are continuously increasing in modern VLSI designs. The emergent power supply noise through the power delivery network (PDN) can eventually degrade the chip timing performance or even cause malfunction. Therefore, an effective supply noise mitigation system and PDN design methodology are critically important to ensure robust VLSI power distribution.

Designing a high-quality low noise PDN system is a complex and challenging task, which requires many efforts from PDN design stage to operation stage and extensive consideration throughout PDN components. For example, using switched capacitor voltage regulator (SCVR) as the power supply solution involves supply voltage ripple. Parasitic resistance and inductance of PDN can induce dynamic voltage drop by load current variation. At the chip load stage, supply noise degrades chip operation performance. Meanwhile, chip operation variation brings load current variation, which in turn, causes supply noise. Jointly considering these interdependent and heterogeneous aspects is the major difficulty in PDN design and noise mitigation.

Traditionally, PDN designers rely on a simple voltage guard bound as design guidance. Following such guidance, designers assume a max allowed voltage drop, and then determine the parameters of PDN components to meet the voltage drop constraints. To explore PDN parameters and verify the performance, considerable design time and run-time efforts are necessary. Next, a reactive noise mitigation system is introduced to dynamically regulate the load voltage such that the voltage guard bound is maintained during the operation stage. Nevertheless, designers just blindly believe the chip performance is ensured if voltage guard bound guidance is followed.

However, for large VLSI designs such as many-core systems, activity variation among multiple cores can result in considerable emergent large power requirements within tens of clock cycles. Therefore, the traditional voltage guard bound guidance is very difficult to meet at the PDN design stage because the allowed PDN impedance can be as small as micro Ohms across the wide frequency range. Moreover, during the system operation stage, the traditional reactive noise mitigation system fails to compensate such emergent supply noise due to systematic issues such as voltage sensing latency, voltage boosting latency through PDN, and limited voltage scaling capability. Finally, even with a dedicated noise mitigation control system and PDN design, the actual chip performance impact is still invisible to PDN designers due to using the over-simplified load model. Such an issue can, in turn, mislead the PDN and noise mitigation system design, resulting in under- or over-designed PDN system and unexpected supply noise impact. Besides, with the rising popularity of machine learning technology, the proactive noise mitigation system based on chip load power/current prediction instead of reactive one is discussed to conceal the PDN latency. However, the mitigation solution either suffers from high hardware overhead or low prediction accuracy. Hence, the practical proactive supply noise mitigation and design methodology for off-chip PDN remains an open problem.

To put proactive noise mitigation into practical and improve the PDN design methodology, there are two major challenges need to be addressed. The first is negative loop challenge of proactive noise mitigation. A proactive noise mitigation controller requires a long-term accurate power/current prediction to conceal the PDN voltage setup latency. However, existing long-term prediction requires high computation cost and consequently long computation latency. Besides, traditional switched capacitor voltage regulator (SCVR) is a common off-chip power supply solution, but off-chip SCVR has limited voltage scaling flexibility and long response time. These two bottlenecks demand further longer-term prediction. Such a negative loop makes proactive noise mitigation suffer from either high hardware overhead or low prediction accuracy. Various works are proposed to address this challenge. For example, low dropout (LDO) voltage regulator is proposed to achieve fast noise mitigation response, but at the cost of heat generation and low energy efficiency. Multi-ratio SCVRs are also studied but the output ripple and limited voltage scaling level remain open problems. Till now, practical methodology to design a proactive noise mitigation system has not been established.

The second challenge is the design gaps in PDN design methodology. The first gap exists between PDN design constraints and target impedance design. Target impedance methodology is a common practice to bridge the PDN impedance with voltage drop constraints. However, actual PDN impedance is defined in the frequency domain while the voltage drop constraints are given in the time domain. Although the current spectrum tells us that dynamic power noise distributes within a certain frequency range, how to determine detailed frequency-dependent target impedance remains an open problem. The second gap exists between on-chip timing information, and off-chip PDN verification and exploration. Conventionally, very simple load models are provided to off-chip PDN designers, and hence on-chip behavior cannot be analyzed by them for PDN verification. Besides, supply voltage and clock frequency may be controlled for each core or a group of cores. Such a system behavior affects the power supply noise significantly, but due to its complexity, it is difficult for on-chip designers to construct even a simple chip load model for PDN configuration exploration purposes. Without the critical on-chip timing information, existing over-simplified PDN design methodology can mislead the PDN design, resulting in under- or over-designed PDN, and under- or over-estimated supply noise impact.

This dissertation proposes the proactive supply noise mitigation and PDN design methodology by addressing the above two challenges. For the first negative loop challenge, this dissertation manages to break the negative loop from two aspects. The first is to lighten the prediction cost by developing a lightweight short-term average current predictor. The second is to relieve the prediction length requirement by introducing a scalable major-minor voltage regulator (MMVR) structure. For the second design gap challenge, this dissertation proposes a frequency-dependent target impedance design methodology that considers the constraints of both average and dynamic voltage drops. A concept of magnitude equivalent frequency (MEF) is proposed to simplify the frequency-dependent target impedance design. To validate and explore the noise impact, this dissertation proposes a chip load model that can provide the on-chip timing information, replay detailed voltage-dependent current profile, and extensively explore the inter-core operation mode variation within a short run-time.

With the proposed methods, firstly a lightweight current predictor is derived, which consists of six-layer decision tree regressor and achieves over 0.99 correlation for 50-cycle-ahead prediction. Secondly, the proposed MMVR power supply solution achieved over 3X voltage scaling range compared with traditional SCVR while the ripple is within 16mV, which is 1.6¥% of load voltage. The proactive noise mitigation system is constructed using MMVR and predictor. Experimental results with a multi-core RISC-V design show that the proposed proactive mitigation system can mitigate the supply noise within 30mV while the noise exceeds 70mV with the conventional reactive mitigation. Also, the average supply voltage is compensated during the full operation period. Thirdly, the frequency-dependent target impedance is obtained which fulfills the voltage drop constraints. Experiments confirm that the synthesized target impedance satisfied the constraints with less than 0.1¥% error in the actual processor load case. Fourthly, a compact chip load model is derived, which is mostly described by Verilog-A. Experimental results show that the proposed model reproduces the current profile, current peak, and timing data well even while it achieves over 300X run-time reduction compared to a transistor-level model. It is also experimentally demonstrated that land side capacitor is helpful to improve processor timing performance in test cases.

The proactive noise mitigation methodology discussed in this dissertation helps to relieve the emergent supply noise so that the robustness for VLSI power distribution can be ensured. The methods proposed in this dissertation are also helpful for PDN designers to mitigate the over- or under-designed PDN impacts, and reduce the design cost and iteration time by facilitating the PDN verification and exploration process.

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論文審査の結果の要旨及び担当者

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論文審査の結果の要旨

本論文は、予測的電源ノイズ低減とロバストなVLSI電源分配網設計手法に関する研究の成果をまとめたものであり、以下の主要な結果を得ている。

1．予測的電源ノイズ低減システムの提案

将来の電源変動を予測してノイズを低減するシステムでは、電源の昇圧に必要な応答時間を隠ぺいするため、長期にわたる正確な電力/電流予測が求められる。しかし、長期予測には高い計算コストが必要となるため、予測に長い計算時間が必要となり、結果として長期予測が実現できないというジレンマがある。また、従来のスイッチドキャパシタ電圧レギュレータ（SCVR）では、電圧スケーリングの柔軟性が制限され、応答時間が長い問題があった。本論文では、50サイクル先の電流に対して0.99以上の相関をもつ予測が可能な、深さ6の小さな決定木で構成された軽量電流予測回路を開発した。スケーラブルなメジャー-マイナー電圧レギュレータ（MMVR）構造を導入して、短い応答時間と広い電圧スケーリング範囲を実現した。これらを組み合わせた提案予測的電源ノイズ低減システムの効果を実験的に確認したところ、従来のリアクティブなシステムと比較して、40 mVを超える電圧降下マージン削減が達成できることを確認した。

２．ロバストな電源分配網(PDN)設計手法の提案

従来のPDN設計には2つの課題がある。第一の課題は、時間領域の設計制約を周波数領域で定義される目標インピーダンスに反映させる方法が存在しないため、周波数依存の目標インピーダンスの適切な決定が困難であることである。第二の課題は、オフチップPDNの設計がチップの性能に与える影響を直接的に評価する方法がないため、PDNが過大・過小設計になりやすいことである。本論文では、第一の課題に対して、時間領域の平均電圧降下と動的電圧降下の制約を考慮する周波数依存目標インピーダンス設計手法を提案した。目標インピーダンスを効率的に求めるため、振幅等価周波数（MEF）を考案した。実験により、プロセッサ負荷に対して時間領域の制約が0.1%未満の誤差で満足できることを確認した。第二の課題に対しては、チップ内のタイミング情報が提供でき、コアの動作モードの変動も含めて正確に電圧依存電流波形が再現できるチップ負荷モデルを開発した。実験により、提案モデルが、トランジスタレベルのモデルと比較して実行時間を300倍以上短縮しながらも、電流波形、電流ピーク値、およびタイミング情報が正確に再現できることを確認した。また、提案モデルの活用により、ランドサイドキャパシタを用いたプロセッサの性能向上が定量的に評価可能であることも確認した。

以上のように、本論文ではロバストなVLSI電力分配網設計を実現し、緊急的な電源ノイズを予測して軽減することに成功している。PDNの設計検証と最適化を支援することで、PDN設計者が過剰・過小な設計に陥る問題を解決し、設計コストや時間が削減できると期待できる。緊急的なノイズに対して確保していた電源電圧マージンを削減し、チップの低消費電力化にも貢献する。よって、博士（情報科学）の学位論文として価値のあるものと認める。