Doctoral Dissertation

Studies on Thermal Design Evaluation Method of SiC Power Module

SiCパワーモジュールの熱設計評価法に関する研究

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Abstract

Fast switching operation of SiC unipolar power devices enables to make more efficient and to miniaturize power conversion systems, which achieves a high power density power conversion system. High di/dt in fast switching operation, however, induces a switching surge voltage associated with the parasitic inductance in the circuit wiring, then it is required to minimize the parasitic inductance with maintaining the circuit topology. Thermal design is another key factor for the safety and reliable operation of high power density circuits. Then, thermal characteristics of power module packages should be evaluated for thermal management of power conversion systems.

The objective of this research is the development of thermal design evaluation methods for power module packages to realize a high power density SiC power conversion system. This thesis develops an algorithm to accurately identify the transient thermal network model of power module packages. And this thesis proposes a modified static test method to evaluate transient thermal characteristics of power module packages with SiC MOSFETs. The significant parameters to improve heat spreading performance of SiC power modules are revealed using the developed transient thermal network model identification method in order to design transient thermal characteristics of SiC power modules.

This thesis consists of the following six chapters. Chapter 1 is the introduction. The background and objective of this research are introduced. The problems to achieve a high power density power conversion system with SiC power devices are also explained in this chapter.

Chapter 2 treats fundamentals of SiC power devices and power modules. Electrical characteristics and its temperature dependency of SiC SBD and SiC MOSFET are derived in section 2.2. Recent and next generation structure and technology of power

module package are described in section 2.3. Section 2.3 also shows the developed multi-layered ceramic substrate in this study and evaluates the parasitic inductance of the developed SiC power module using the multi-layered ceramic substrate.

Chapter 3 develops a signal processing algorithm to identify the accurate transient thermal network model for power module packages. The conventional algorithm for identifying the transient thermal network model has difficulty in eliminating noise on the measured result. The modified algorithm for identifying the transient thermal network model is explained and performs some numerical validations for a known numerical model in the frequency domain. Moreover, the developed algorithm is experimentally validated for a discrete power device and power module with an active metal bonding (AMB) substrate.

Chapter 4 proposes a junction temperature (T_{J}) estimation method for SiC MOSFETs in the transient thermal characterization. SiC MOSFET has still concern about the dynamic gate threshold voltage shift due to the trap in the oxide/semiconductor interface, which violates the estimated time response of T_{J}. The proposed method, which advances the conventional static test method, is performed and validated using the embedded temperature sense diode on SiC MOSFET. The time response of T_{J} is also evaluated for the developed SiC MOSFET with built-in Schottky barrier diode (SBD) named as SWITCH-MOS.

Chapter 5 evaluates the thermal design of SiC power module substrates for various types of module constitutions using the transient thermal network model. Finite volume method (FVM) simulation is performed to evaluate the validity of obtained transient thermal characteristics. Section 5.3 and 5.4 reveal the significant parameters for improving transient thermal characteristics of power module packages based on an AMB substrate.

Conclusions, industrial impacts and suggestions of future work are provided in Chapter 6.

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Contents

Chapter 1

Introduction

1.1 Background

Electrical power is generated and consumed in a variety of voltage and current levels in modern society. Power electronics, which was defined by W. E. Newell in 1974 [1], is a key technology to efficiently use a electrical power by changing voltage and current amplitude and/or frequency using power conversion systems. Switching operation of power conversion systems is realized by using power semiconductor devices such as power diode, metal-oxide semiconductor field effect transistor (MOSFET), insulated gate bipolar transistor (IGBT), and gate turn off thyristor (GTO). Power conversion systems are widely adopted for industrial application (motor drive, factory automation, data center), renewable energy conversion system (solar, wind, geothermal heat), transportation (hybrid or electrical car, railway, aerospace), home appliance (air conditioner, robot cleaner), and so on.

As extending the adopted field of power conversion systems and increasing amount of consumed electrical power in the world, power conversion systems are required to be more efficient operation and reduce size, weight and cost. Fast switching operation of power conversion systems realizes low switching loss in operation and allows high frequency switching operation. This enables to miniaturize and accomplish a high power density power conversion system. While some breakthroughs have been occurred for developing device structure such as Si super junction (SJ) MOSFET [2], the conventional Si-based power semiconductor device is approaching to the theoretical limitation,

which is derived from the physical property of Si and its device structures.

Wide bandgap (WBG) semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) attract attention as next generation power semiconductor devices [3]-[10]. Table 1.1 lists the major physical properties of WBG and conventional semiconductor materials for power semiconductor devices. Here, Baliga figure of merit (BFOM) shows the performance index of conduction loss assuming the specific on-state resistance of power MOSFET at low switching frequency operation [11]. Reference [12] is adopted for high frequency operation of power conversion systems, which considers switching loss of each switching transient. As shown in Table 1.1, WBG semiconductor materials are superior to the conventional Si semiconductor in terms of wide bandgap, high critical breakdown, high electron mobility and thermal stability. These features accomplish the high breakdown voltage unipolar power device with low on resistance, fast switching and high temperature operation capability.

Table 1.1 Physical properties of WBG and conventional semiconductor materials

	Si	GaAs	4H-SiC	GaN	Diamond
Bandgap E_{G} [eV]	1.12	1.43	3.26	3.39	5.47
Breakdown electric field E_{c} [MV/cm]	0.3	0.4	3.0	3.3	10.0
Electron mobility μ_{e} [cm^2/Vs]	1400	8500	1000	900	2200
Saturated electron mobility v [cm/s]	1.0	2.0	2.2	2.7	2.7
Thermal conductivity λ [W/cm/K]	1.5	0.5	4.9	2.0	20.0
Relative dielectric constant ε	11.8	12.8	9.7	9.0	5.5
BFOM($=\varepsilon\mu_{\mathrm{e}}E_{\mathrm{G}}^3$)	1	13.7	14.5	13.6	85.3

Fig. 1.1 shows the major territories of WBG and conventional power semiconductor devices for a variety of applications. GaN power semiconductor devices have the equal or better potential than SiC power semiconductor devices [13]. But it is difficult to fabricate insulation layer like Si, thus they are expected to adopt a small or middle power and high switching frequency operation application using the lateral structure such as high electron mobility transistor (HEMT) [14] [15]. Wireless power transfer (WPT) applications over MHz switching frequency using GaN power semiconductor devices were already reported [16]-[18]. Reference [19] developed high switching fre-

quency gate driver using GaN HEMT to operate synchronous DC-DC converter at 10MHz. Diamond is the most promising material as power semiconductor devices, and some Schottky barrier diodes (SBD) and MOSFETs have been enthusiastically studied [20]-[23]. But since doping on pure diamond crystal is difficult due to its wide bandgap, a practical rated power device is still not realized. In regard to SiC power semiconductor devices, SiC crystal growth had break through by epitaxial growth method in Japan [24]. And the vertical SiC power devices like MOSFET and IGBT are easily fabricated using SiC single crystal because SiC can be thermally oxidized in the same manner as silicon and SiO_2 forms a native passivation layer on SiC crystal [25]. Moreover, SiC power semiconductor devices can operate over 300 °C due to its wide bandgap and high thermal conductivity [26] [27]. Thus SiC power semiconductor devices are expected to adopt for high power rated applications. Researchers have reported many application using SiC power semiconductor devices [28]-[31], and some are already commercialized.

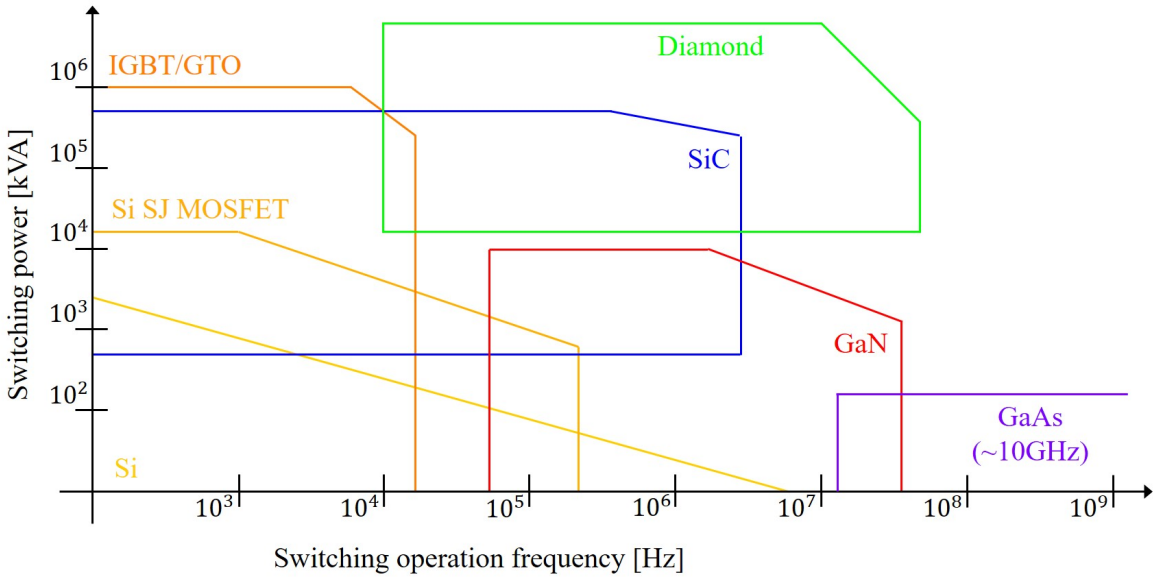


Figure 1.1 Major territories of power semiconductor devices.

1.2 Problems in realizing high power density SiC power conversion system

Passive components such as inductor and capacitor dominate the size and weight of power conversion systems. High frequency switching operation using high speed switching with SiC unipolar power devices allows to use the less inductance and capacitance in power conversion systems. High di/dt and dv/dt in fast switching, however, induce large switching surge voltage and current with the parasitic components in the circuit. This leads to failure operation or high frequency electromagnetic interference (EMI) noise problem of power conversion systems. References [32] and [33] analyzed self turn-on phenomena induced by the high switching speed. Modeling and visualization of noise source and path have been conducted to achieve electromagnetic compatibility (EMC) design [34] [35]. Modularization of power semiconductor devices and miniaturization of power conversion systems are one way of reducing parasitic components. Designing power module structure is effective to reduce parasitic components [36]-[39]. Reference [40] reported the design method of the parasitic inductance and capacitance in laminated busbars, which connects power module to power conversion system. On the other hand, miniaturization increases heat dissipation per unit area/volume and thermal interference effect among components in the module and/or circuit. These problems make thermal management difficult and concern about long-term reliability in actual operation. Therefore, thermal design is a key factor for miniaturization of power conversion systems to maximize SiC power semiconductor device capability.

Thermal design of power module aims at spreading and transferring heat dissipated in the power semiconductor device. Heat spreading and transferring mainly depends on the structure and material property of power module constitutions. The conventional static thermal resistance model evaluates the temperature difference between junction to case of power modules in steady-state operation. However, a transient thermal network model represented by thermal resistance and thermal capacitance is needed to estimate the time response of junction temperature (T_{J}) in over or fault current condition [41]-[53]. References [46] and [47] assessed the dynamic thermal coupling effect for multi-chip power module packages. References [48]-[52] identified a transient ther-

mal network model in the frequency domain using Fourier series expansion. Frequency domain modeling is also conducted for several thermal circuit models in reference [53]. Static test method [54] is the standard method for identifying the transient thermal network model of power module packages. This method estimates T_{J} by the temperature dependency in $I - V$ characteristics of power semiconductor devices in power modules.

Reference [54] performs some numerical calculations such as deconvolution calculation to identify the transient thermal network model from the time response of T_{J} in cooling operation from thermal equilibrium in self heated condition. The precise numerical calculation procedure to identify the transient thermal network model is not clearly addressed in [54]. And the conventional model identification algorithm has difficulty in eliminating the influence of noise in the measured signal. An additional filtering or another signal processing algorithm is necessary in order to achieve higher noise reduction capability for identifying the accurate transient thermal network model from the estimated time response of T_{J}.

Other problem is that SiC MOSFET has difficulty of the gate threshold voltage shift due to the carrier traps in the level of gate oxide or interface [55]. The static gate threshold voltage shift has been improved, but the dynamic gate threshold voltage shift, for example negative bias temperature instability (NBTI) problem [56] [57], still remains great concern. The latter causes an error in T_{J} estimation of SiC MOSFETs using its temperature dependency of $I - V$ characteristics [58]. This error makes it difficult to identify the transient thermal network model of power module packages with SiC MOSFETs. Thus new evaluation method for SiC power semiconductor device is necessary.

1.3 Purpose and outline of this thesis

This thesis is concerned with developing thermal design evaluation methods of SiC power modules to realize a high power density SiC power conversion system. This research focuses on an algorithm to accurately identify the transient thermal network model of power module packages, and a thermal characterization method for SiC MOS-

FETs without the influence of the dynamic gate threshold voltage shift. This research also evaluates the thermal design of power module substrates for SiC power modules using the developed transient thermal network model identification method.

Chapter 2 treats the structure and property of SiC power semiconductor devices and power modules. The electrical characteristics and its temperature dependency of SiC SBD and SiC MOSFET are derived from solid state physics. Constitutions and its function of power module packages are also explained in this chapter. And the developed SiC power module with a multi-layered ceramic substrate in this study is shown.

Chapter 3 develops an algorithm for identifying the transient thermal network model of SiC power modules using weighted discrete Fourier transformation and noise filtering in frequency domain. The influence of quantization error and noise in the measured signal is evaluated for the simulated time response of T_{J} with a given transient thermal network model. The accuracy of the identified transient thermal network model for a discrete power device and a power module package is experimentally evaluated.

Chapter 4 proposes an accurate T_{J} estimation procedure for SiC MOSFETs without the dynamic gate threshold voltage shift, which advances the conventional static test method. The estimated time response of T_{J} using the proposed procedure is validated with temperature sense diode embedded in SiC MOSFET. And this chapter also evaluates the estimated time response of T_{J} for the developed SiC MOSFET with built-in SBD, whose $I_{\mathrm{d}} - V_{\mathrm{sd}}$ characteristic does not depend on V_{gs}.

Chapter 5 evaluates the thermal design of SiC power module substrates for varieties of power module constitutions using the developed transient thermal network model. This chapter performs the parametric study of transient thermal characteristics for power module constitution with a single chip module, and obtains the significant parameters to improve transient thermal characteristics of power module. The obtained measured results are validated using the numerical simulation based on finite volume method (FVM).

And chapter 6 summarizes this thesis and suggests industrial impacts and topics for future research work.

Chapter 2

SiC power device and its module packages

2.1 Introduction

A power module consists of packaged plural power devices. Thus, electrical characteristics and its temperature dependency of power device are very important for analyzing electrical and thermal behavior of power conversion systems. Moreover, power module structure and packaging technology critically affect parasitic components and thermal characteristics of SiC power modules. Section 2.2 explains the structure of some typical SiC power devices and derives its electrical characteristics including temperature dependency from device structure. Section 2.3 explains typical structures and materials of the conventional and next generation power modules. And section 2.3 introduces the developed multi-layered ceramic substrate, and evaluates its electrical characteristics.

2.2 SiC power device

SiC is a IV-IV compounded material with unique physical properties. The strong chemical bonding between Si and C atoms gives thermal, chemical and mechanical stability. SiC is the best known example as polytypism such as 3C-, 4H- and 6H-SiC crystal structure and their physical properties are different. In the field of power electronics, 4H-SiC is the most popular material. This is because a high quality 4H-SiC

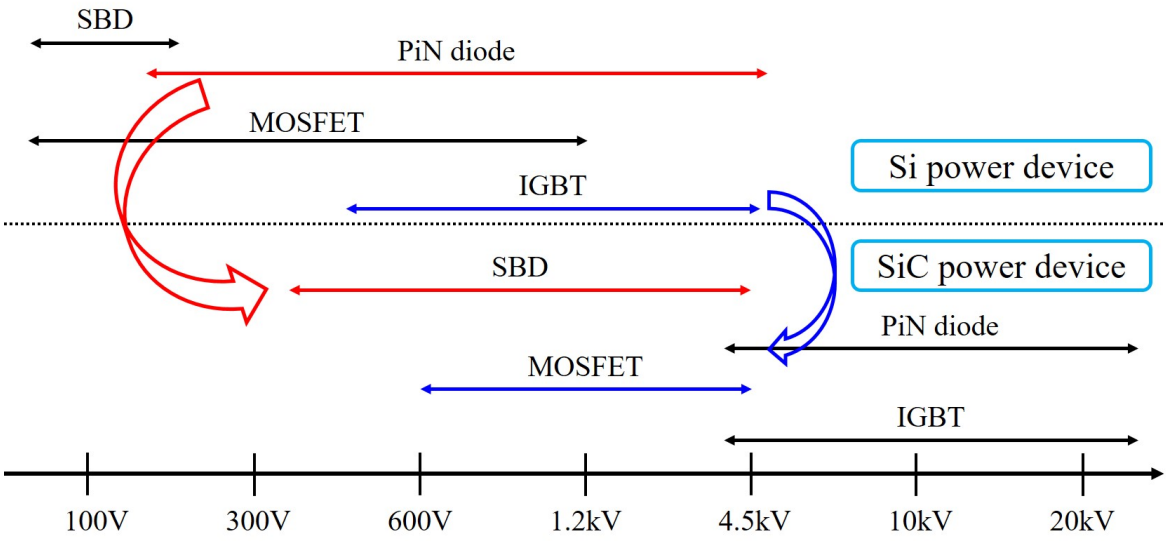


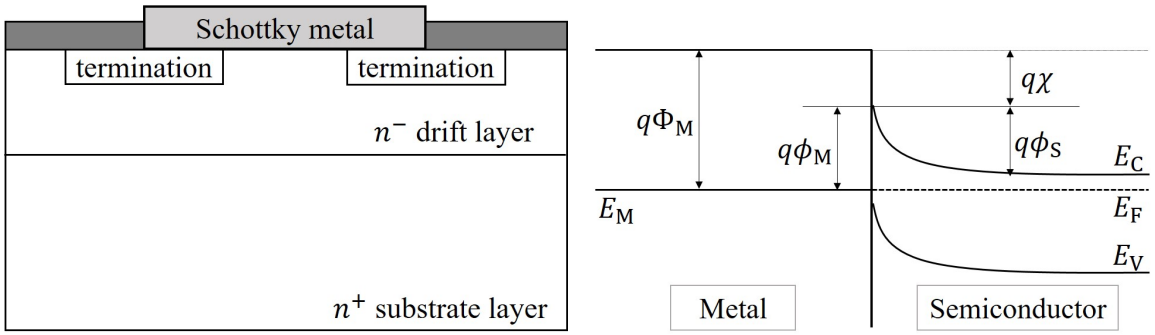
Figure 2.1 Major territories of Si and SiC power semiconductor devices.

crystal had been obtained by epitaxial growth [24]. Moreover, 4H-SiC has the most high electron mobility compared to other polytypes.

Fig. 2.1 shows the major territories of Si and SiC power devices. In the conventional Si power device, bipolar power device such as PiN diode or insulated gate bipolar transistor (IGBT) is often used in several hundreds to thousands voltage application. Bipolar power device achieves high breakdown voltage and low on-state resistance by conductivity modulation effect. On the other hand, it is difficult to obtain high switching speed because the time to sweep minority carrier needs in the turn-off transient. The critical breakdown voltage of SiC is about ten times higher than that of Si, thus it enables to achieve high breakdown voltage of power device by unipolar power device such as Schottky barrier diode (SBD) and metal-oxide semiconductor field effect transistor (MOSFET). This section explains the structure and electrical characteristics of SBD and MOSFET in detail.

2.2.1 SiC SBD

Fig. 2.2(a) is the typical cross-sectional structure of SBD. SBD is a rectifier device that utilizes Schottky junction by contacting semiconductor and metal such as titanium and nickel [59]. Barrier height of Schottky junction is designed by the different junction



(a) Cross-sectional structure. (b) Energy band diagram.

Figure 2.2 Typical cross-sectional structure and energy band diagram of SBD.

metal and surface processing. Lightly-doped (n^-) drift layer on heavily-doped (n^+) substrate layer plays an important role in blocking the reverse voltage as power device, which is derived from Poisson equation. Fig. 2.2(b) illustrates the energy band diagram of SBD. Here, Φ is the work function and "M" and "S" denote metal and semiconductor, respectively. The work function is the energy obtained by subtracting the vacuum level from Fermi level. The electron affinity χ is the energy obtained by subtracting the vacuum level from the conductor level. Φ and χ are the potential, thus it is necessary to multiply the elementary charge q.

When the forward bias voltage applies to Schottky junction, the electron density at the junction n_e is obtained by the following equation:

$$n_e = N_c \exp\left(-\frac{E_c - E_F}{k_B T}\right) = N_c \exp\left[-\frac{q\phi_M - qV}{k_B T}\right], \tag{2.1}$$

where N_c is the number of electron per unit area at the conduction band, k_B is the Boltzmann constant, and T is the absolute temperature. V is the voltage applied to the device and defined as the forward voltage from metal to semiconductor.

The electron current density from semiconductor to metal J_S is assumed to be proportional to the electron density, and the following equation is given by

$$J_S = \alpha \exp\left[-\frac{q\phi_M - qV}{k_B T}\right] \left(= \alpha \exp\left(-\frac{q\phi_M}{k_B T}\right) \exp\left(\frac{qV}{k_B T}\right)\right). \tag{2.2}$$

Here, α is a function of temperature as $\alpha = AT^2$, and A is the effective Richardson constant. Eq. (2.2) reveals that J_S increases as the forward bias voltage increases.

The electron current density from metal to semiconductor J_M is balanced to J_S when a voltage is not applied. Then substituting $V = 0$ into Eq. (2.2), we obtain the

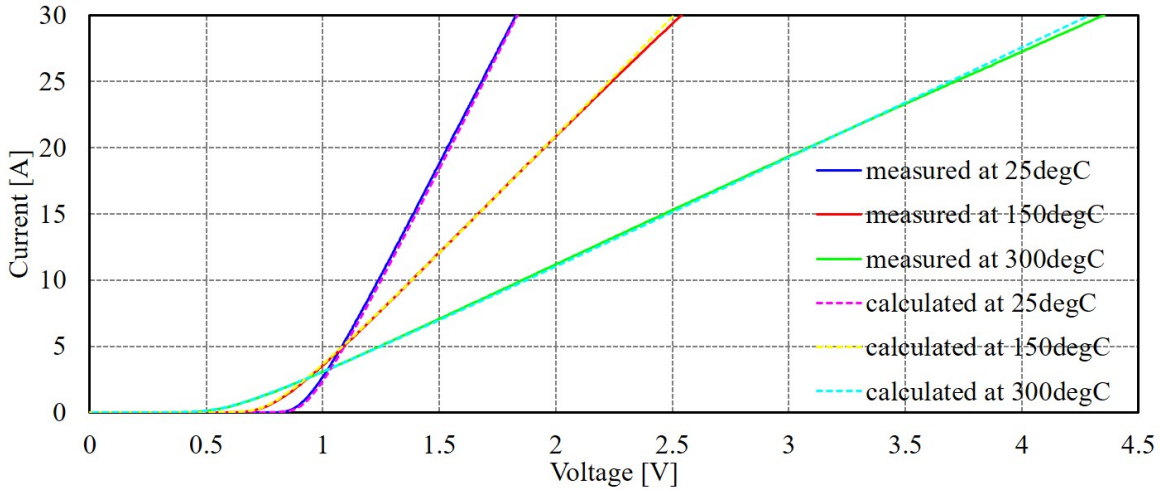


Figure 2.3 Temperature dependency of $I-V$ characteristic for C4D20120A.

following equation:

$$J_{\mathrm{M}} = \alpha \exp\left(-\frac{q\phi_{\mathrm{M}}}{k_{\mathrm{B}}T}\right). \tag{2.3}$$

Therefore, the net electron current density J is given as follow:

$$J = J_{\mathrm{S}} - J_{\mathrm{M}} = \alpha \exp\left(-\frac{q\phi_{\mathrm{M}}}{k_{\mathrm{B}}T}\right)\left[\exp\left(\frac{qV}{k_{\mathrm{B}}T}\right) - 1\right]. \tag{2.4}$$

We assume that the actual voltage decreases by the voltage drop V_0 of the on-state resistance R_{Td} in Eq (2.4). The forward current of diode I, which is derived by multiplying the current density J and the cross-sectional area of current flow path S, is obtained by the following equations:

$$I = I_0\left[\exp\left(\frac{qV_0}{nk_{\mathrm{B}}T}\right) - 1\right], \tag{2.5}$$

$$I_0 = AT^2 \exp\left(-\frac{q\phi_{\mathrm{M}}}{k_{\mathrm{B}}T}\right), \tag{2.6}$$

$$V_0 = V - R_{\mathrm{Td}}I. \tag{2.7}$$

Here, I_0 is the saturation current, and n is the ideal factor. Generally, n is 1 for SBD which dominates the drift current, and n is 2 for PiN diode which dominates recombination current.

Fig. 2.3 is the temperature dependency of $I-V$ characteristic for SiC SBD C4D20120A (1200 V/20 A, CREE). Here, "measured" is the measured $I-V$ characteristic at each temperature, and "calculated" is calculated using Eq. (2.5) and Table 2.1 extracted

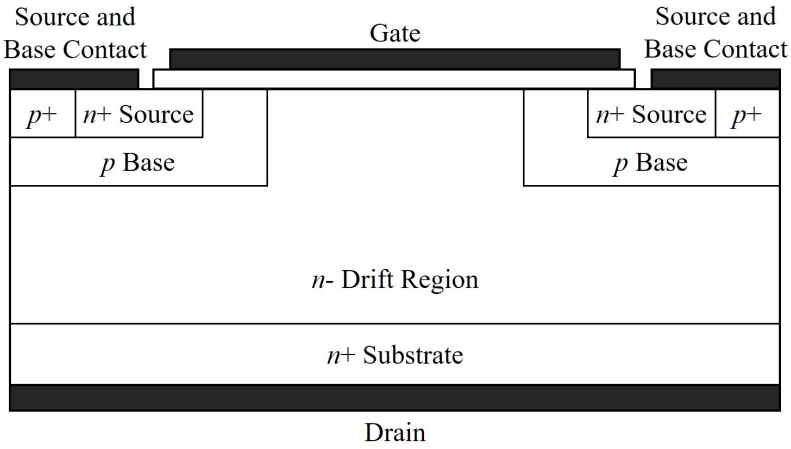
Table 2.1 Obtained each parameter of studied SiC SBD

T [°C]	n	I_0 [A]	R_{Td} [mΩ]
25	1.042	2.313×10^{-15}	27.75
50	1.025	4.786×10^{-14}	31.23
75	1.020	9.167×10^{-13}	35.66
100	1.016	1.240×10^{-11}	40.89
125	1.018	1.316×10^{-10}	46.92
150	1.004	8.980×10^{-10}	54.26
175	1.006	5.969×10^{-9}	62.25
200	1.013	3.492×10^{-8}	71.31
225	0.997	1.447×10^{-7}	81.88
250	1.004	6.260×10^{-7}	92.96
275	0.971	1.962×10^{-6}	105.51
300	0.974	6.510×10^{-6}	118.14

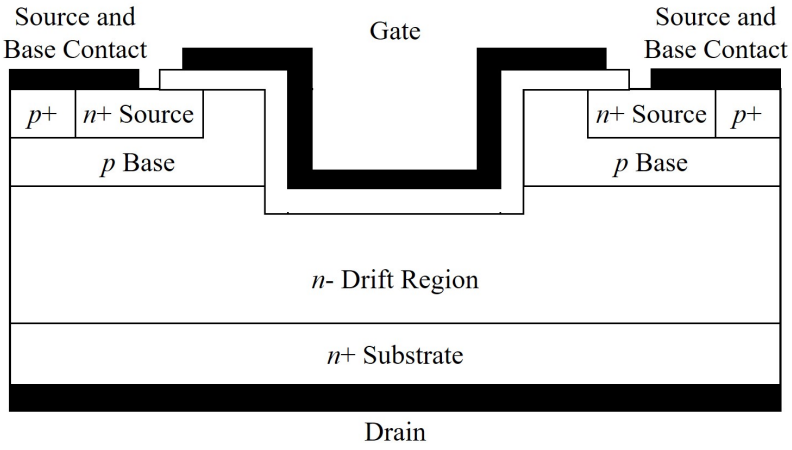
by the measured data. Fig. 2.3 shows that the knee voltage of SiC SBD decreases as the junction temperature increases. This is the feature of semiconductor that carrier excites as the junction temperature increases. In the high current region, the gradient of $I-V$ characteristic becomes small. This is because lattice vibration at Schottky metal becomes active as the junction temperature increases, and this leads to increase the on-state resistance of SiC SBD. The calculated $I-V$ characteristic of studied SiC SBD coincides with the measured result. The obtained Richardson constant A is 9.25 $\times10^{-2}$ and the work function ϕ_{M} is 1.10. From Table 2.1, ideal factor n is almost 1.

2.2.2 SiC MOSFET

MOSFET is a semiconductor device which is widely used for switching and amplifying electric signals. MOSFET can switch on/off operation, and this enables to change voltage/current amplitude and/or frequency in power electronics. Generally, "power MOSFET" indicates the vertical structure whose drain current flows vertically in the structure. By contrast, the lateral structure, whose drain current flows horizontally thorough the inversion layer under the gate oxide, is often used for integrated circuit



(a) Planer gate structure.



(b) Trench gate structure.

Figure 2.4 Cross-sectional structure of typical n-type power MOSFET.

(IC) or large scale integration (LSI).

Fig. 2.4 is the cross-sectional structure of a typical n-type vertical power MOSFET. Fig. 2.4(a) is a planer gate double implanted MOSFET (DiMOSFET), which is derived from the similar structure of Si power device. Fig. 2.4(b) is a trench gate U-shaped MOSFET (UMOSFET). In general, n^- drift region of vertical power MOSFET is formed on a thick, richly-doped n^+ substrate, and current flows vertically through the drift region. Trench gate SiC MOSFET is attractive for reducing the specific on-resistance resulting from a small cell pitch and high channel mobility on the trench sidewall [60]. Another reason is that the electron mobility on the vertical and lateral

direction is different in the c-axis of 4H-SiC crystal[*1]. Gate terminal of MOSFET is formed by thermally oxidized polysilicon insulation layer and metal electrode.

This section briefly shows some important equations to understand electrical characteristics of MOSFET. They are covered in many semiconductor textbooks in detail, thus the reader refers to the literature for the detailed derivations.

The voltage across gate oxide V_{OX} has the relationship to the total charge par unit area at the oxide/semiconductor interface Q_{S}.

$$V_{\mathrm{OX}} = E_{\mathrm{OX}} t_{\mathrm{OX}} = \frac{Q_{\mathrm{S}}}{\varepsilon_{\mathrm{OX}}} t_{\mathrm{OX}} = \frac{Q_{\mathrm{S}}}{C_{\mathrm{OX}}}, \tag{2.8}$$

where t_{OX}, $\varepsilon_{\mathrm{OX}}$ and C_{OX} are the thickness, relative dielectric constant and capacitance par unit area of the gate oxide, respectively. When the inversion layer occurs at the oxide/semiconductor interface, its surface potential ψ_{S} is two times higher than the bulk potential ψ_{B}.

$$\psi_{\mathrm{S}} = 2\psi_{\mathrm{B}}. \tag{2.9}$$

The bulk potential ψ_{B} is the potential of the depletion layer, and ψ_{B} has a function of the impurity concentration in semiconductor.

$$\psi_{\mathrm{B}} = \left(\frac{E_{\mathrm{i}} - E_{\mathrm{FS}}}{q} \right) = \frac{k_{\mathrm{B}} T}{q} \ln \left(\frac{p_0}{n_{\mathrm{i}}} \right) = \frac{k_{\mathrm{B}} T}{q} \ln \left(\frac{N_{\mathrm{A}}}{n_{\mathrm{i}}} \right). \tag{2.10}$$

Here, E_{i} is the intrinsic Fermi energy, E_{FS} is the flatband energy, and n_{i} is the intrinsic carrier concentration. p_0 is the hole concentration, and this is equal to impurity concentration N_{A} in silicon. Thus, the threshold voltage of MOSFET V_{TH} is given as the following equation:

$$V_{\mathrm{TH}} = \frac{Q_{\mathrm{S}}}{C_{\mathrm{OX}}} + \psi_{\mathrm{S}} = \frac{Q_{\mathrm{S}}}{C_{\mathrm{OX}}} + 2\psi_{\mathrm{B}}. \tag{2.11}$$

The total charge par unit area at the oxide/semiconductor interface in weak inversion is given as follow:

$$Q_{\mathrm{S}} = \sqrt{2\varepsilon_{\mathrm{S}} q p_{\mathrm{p0}} \psi_{\mathrm{S}}} = \sqrt{4\varepsilon_{\mathrm{S}} q N_{\mathrm{A}} \psi_{\mathrm{B}}}. \tag{2.12}$$

[*1] Vertical:1020cm^2/V/s, lateral:1200cm^2/V/s [25]

Here, ε_{S} is the relative dielectric constant of semiconductor, and n_{p0} is the electron concentration in the depletion region of semiconductor at the chemical equilibrium condition. Eq. (2.11) is rewritten as follow using Eq. (2.12):

$$V_{\mathrm{TH}} = \frac{\sqrt{4\varepsilon_{\mathrm{S}} q N_{\mathrm{A}} \psi_{\mathrm{B}}}}{C_{\mathrm{OX}}} + 2\psi_{\mathrm{B}}. \tag{2.13}$$

And Eq. (2.13) can be rewritten as follow using Eq. (2.10):

$$V_{\mathrm{TH}} = \frac{\sqrt{4\varepsilon_{\mathrm{S}} k_{\mathrm{B}} T N_{\mathrm{A}} \ln(N_{\mathrm{A}}/n_{\mathrm{i}})}}{C_{\mathrm{OX}}} + \frac{2k_{\mathrm{B}}T}{q} \ln\left(\frac{N_{\mathrm{A}}}{n_{\mathrm{i}}}\right). \tag{2.14}$$

The first term of Eq. (2.14) dominates the threshold voltage of MOSFET. V_{TH} is also expressed as the following equation by rewriting the capacitance at the gate oxide and neglecting the second term in Eq. (2.14).

$$V_{\mathrm{TH}} = \frac{t_{\mathrm{OX}}}{\varepsilon_{\mathrm{OX}}} \sqrt{4\varepsilon_{\mathrm{S}} q N_{\mathrm{A}} \psi_{\mathrm{B}}} \tag{2.15}$$

$$= \frac{t_{\mathrm{OX}}}{\varepsilon_{\mathrm{OX}}} \sqrt{4\varepsilon_{\mathrm{S}} k_{\mathrm{B}} T N_{\mathrm{A}} \ln\left(\frac{N_{\mathrm{A}}}{n_{\mathrm{i}}}\right)}. \tag{2.16}$$

Eq. (2.16) shows that the threshold voltage of MOSFET is proportional to the square of the gate oxide thickness and doping concentration.

Differentiating Eq. (2.13) by T and we obtain the following equation:

$$\frac{dV_{\mathrm{TH}}}{dT} = \frac{d\psi_{\mathrm{B}}}{dT} \left[\frac{1}{C_{\mathrm{OX}}} \sqrt{\frac{\varepsilon_{\mathrm{S}} q N_{\mathrm{A}}}{\psi_{\mathrm{B}}}} + 2\right]. \tag{2.17}$$

Here, $d\psi_{\mathrm{B}}/dT$ is approximated as follow [61]:

$$\frac{d\psi_{\mathrm{B}}}{dT} \approx \frac{1}{T} \left[\frac{E_{\mathrm{g}}(T=0)}{2q} - |\psi_{\mathrm{B}}(T)|\right]. \tag{2.18}$$

Eqs. (2.17) and (2.18) show that the threshold voltage of MOSFET decreases as the junction temperature increases if $|\psi_{\mathrm{B}}(T)| > E_{\mathrm{g}}(T=0)/2q$.

Next, we consider current-voltage relationship of MOSFET. The channel current I_{D} is given as follow:

$$I_{\mathrm{D}} = \left(\frac{W}{L}\right) C_{\mathrm{OX}} \mu_{\mathrm{n}} \left[\left(V_{\mathrm{G}} - V_{\mathrm{FB}} - 2\psi_{\mathrm{B}} - \frac{V_{\mathrm{D}}}{2}\right) V_{\mathrm{D}} - \left(\frac{2}{3}\right) \frac{\sqrt{2\varepsilon_{\mathrm{S}} q N_{\mathrm{A}}} [(V_{\mathrm{D}} + 2\psi_{\mathrm{B}})^{3/2} - (2\psi_{\mathrm{B}})^{3/2}]}{C_{\mathrm{OX}}}\right]. \tag{2.19}$$

Eq. (2.19) shows that channel current increases as the increase of drain and gate voltage. This region is called as the linear operating region of MOSFET, and channel current is also called as drift current. Eq. (2.19) is simply rewritten as follow with assuming N_{A} is small:

$$I_{\mathrm{D}} = \left(\frac{W}{L}\right) C_{\mathrm{OX}} \mu_{\mathrm{n}} \left(V_{\mathrm{G}} - V_{\mathrm{TH}} - \frac{V_{\mathrm{D}}}{2}\right) V_{\mathrm{D}}. \tag{2.20}$$

In actual MOSFET, the drain current is limited by a saturated carrier velocity over the saturated drain voltage V_{Dsat}. We consider the condition of $dI_{\mathrm{D}}/dV_{\mathrm{D}} = 0$.

(i) $V_{\mathrm{D}} \ll 2\psi_{\mathrm{B}}$

$$V_{\mathrm{D}} = V_{\mathrm{Dsat}} = V_{\mathrm{G}} - V_{\mathrm{TH}}, \tag{2.21}$$

(ii) $V_{\mathrm{D}} \gg 2\psi_{\mathrm{B}}$

$$\begin{aligned} V_{\mathrm{D}} &= V_{\mathrm{Dsat}} \\ &= V_{\mathrm{G}} - V_{\mathrm{FB}} - 2\psi_{\mathrm{B}} + \frac{K^2}{2} - \left(\frac{K}{2}\right) \sqrt{K^2 + 4(V_{\mathrm{G}} - V_{\mathrm{FB}} - 2\psi_{\mathrm{B}})}. \end{aligned} \tag{2.22}$$

Here, $K = \frac{\sqrt{2\varepsilon_{\mathrm{S}} q N_{\mathrm{A}}}}{C_{\mathrm{OX}}}$. Thus, I_{Dsat} is obtained as the following equation under $V_{\mathrm{D}} > V_{\mathrm{Dsat}}$:

(i) $V_{\mathrm{D}} \ll 2\psi_{\mathrm{B}}$

$$I_{\mathrm{D}} = \left(\frac{W}{2L}\right) C_{\mathrm{OX}} \mu_{\mathrm{n}} (V_{\mathrm{G}} - V_{\mathrm{TH}})^2, \tag{2.23}$$

(ii) $V_{\mathrm{D}} \gg 2\psi_{\mathrm{B}}$

$$I_{\mathrm{D}} = \left(\frac{W}{L}\right) C_{\mathrm{OX}} \mu_{\mathrm{n}} \left[V_{\mathrm{G}} - V_{\mathrm{FB}} - 2\psi_{\mathrm{B}} - \left(\frac{2}{3}\right) \frac{\sqrt{2\varepsilon_{\mathrm{S}} q N_{\mathrm{A}}}}{C_{\mathrm{OX}}} - \frac{V_{\mathrm{Dsat}}}{2}\right] V_{\mathrm{Dsat}}. \tag{2.24}$$

After the drain current saturated, the inversion layer narrows near the drain, and eventually pinches off. When this occurs, Eq. (2.19) is no longer valid. The drain voltage that causes the pinch-off can be found by setting the charge in the inversion layer at the drain to zero. This region is called as the saturated region.

In practical, $I-V$ characteristics of MOSFET at the linear and saturated region are given as the following equations:

$$I_{\mathrm{D}} = \alpha\left(V_{\mathrm{G}} - V_{\mathrm{TH}} - \frac{V_1}{2}\right)V_1 \text{ for } V_{\mathrm{D}} < V_{\mathrm{G}} - V_{\mathrm{TH}}, \tag{2.25}$$

$$I_{\mathrm{D}} = \frac{\alpha}{2}(V_{\mathrm{G}} - V_{\mathrm{TH}})^2(1+\lambda_{\mathrm{c}}V_{\mathrm{D}}) \text{ for } V_{\mathrm{D}} > V_{\mathrm{G}} - V_{\mathrm{TH}}, \tag{2.26}$$

$$V_1 = V_{\mathrm{D}} - R_{\mathrm{Tm}}I_{\mathrm{D}}, \tag{2.27}$$

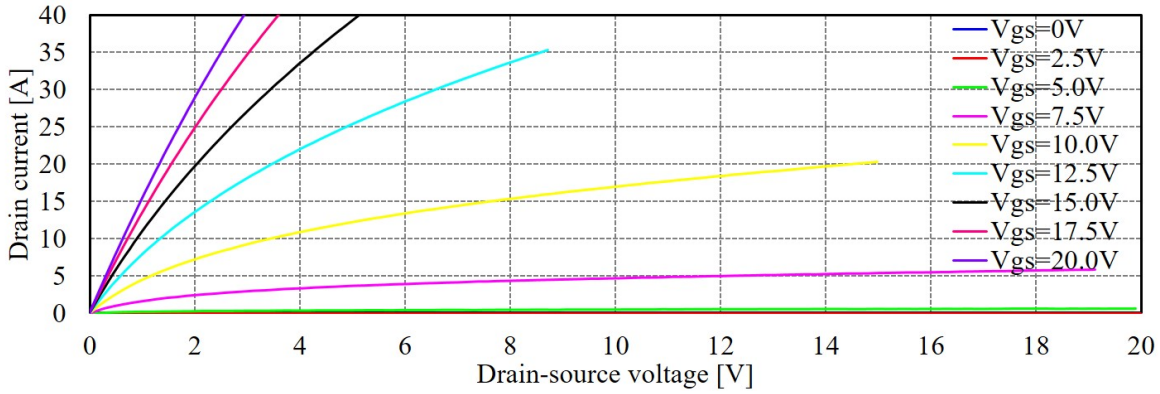
$$\alpha = \left(\frac{W}{L}\right)C_{\mathrm{OX}}\mu_{\mathrm{n}}. \tag{2.28}$$

Fig. 2.5 is the temperature dependency of $I-V$ characteristics for SiC MOSFET CMF20120D (1200 V/40 A, CREE). Figs. 2.5(a) and 2.5(b) are $I_{\mathrm{d}}-V_{\mathrm{ds}}$ characteristics at room temperature and $T = 300°\mathrm{C}$, respectively. For a relatively large gate voltage, the gradient of $I-V$ carves becomes small as the junction temperature increases. This is because the on-state resistance becomes large as shown in Fig. 2.5(c). And for a relatively small gate voltage over the gate threshold voltage, the saturation current becomes larger for the same gate voltage. This is because the gate threshold voltage becomes lower as the junction temperature increases. Fig. 2.5(c) shows that the gate threshold voltage becomes low as the junction temperature increases, which coincides with Eqs. (2.17) and (2.18).

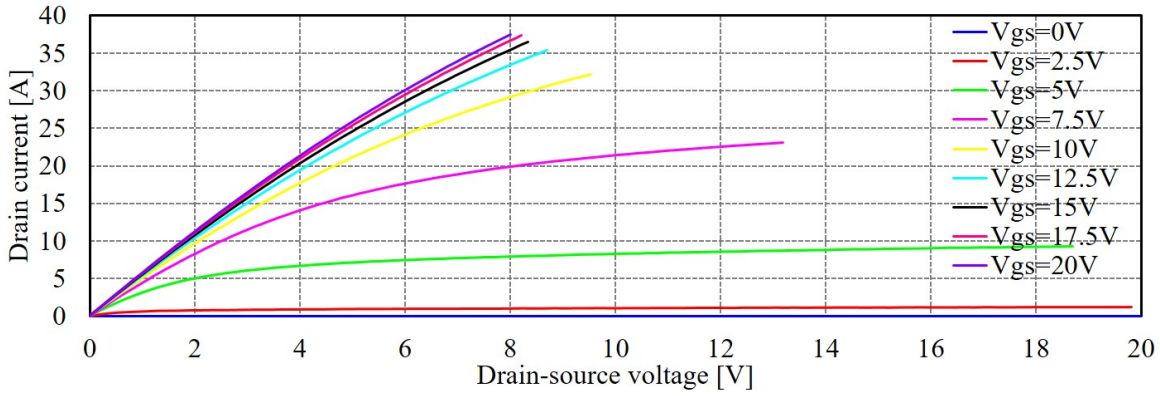
2.2.3 SWITCH-MOS

Knee voltage of body diode in SiC MOSFETs is relatively large due to its wide bandgap, which results in the large conduction losses in reverse conduction through body diode. In addition, the current conduction in body diode induces the bipolar degradation due to the recombination of injected minority carriers [62]. This causes the increase of the on-state resistance of SiC MOSFET.

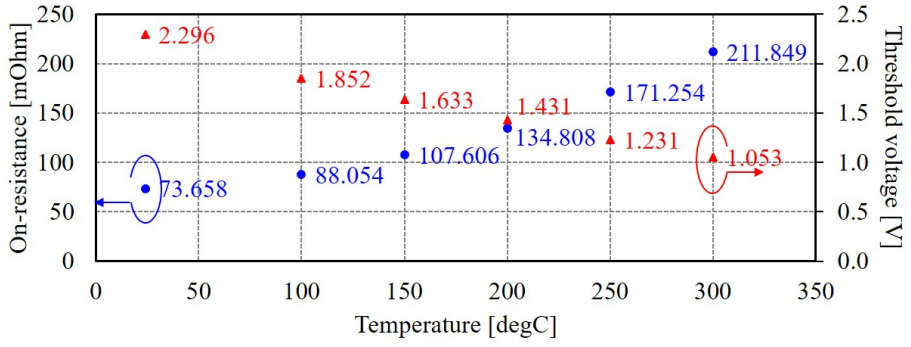
Fig. 2.6 shows the typical device structure of the developed SiC MOSFET with built-in SBD [63] [64]. This is named as SBD-Wall-Integrated TrenCH MOSFET (SWITCH-MOS). While the planer gate SiC MOSFET with built-in SBD was reported in the same time [65], SWITCH-MOS is designed based on the trench gate SiC UMOSFET [66]. SWITCH-MOS is designed to have the reverse current flow through built-in SBD rather than through pn body diode by controlling the electric field around



(a) $I_{\mathrm{d}} - V_{\mathrm{ds}}$ characteristics（$T = 24°\mathrm{C}$）.



(b) $I_{\mathrm{d}} - V_{\mathrm{ds}}$ characteristics（$T = 300°\mathrm{C}$）.



(c) Temperature dependency of V_{TH} and R_{on}.

Figure 2.5 Temperature dependency of $I - V$ characteristics for SiC MOSFET.

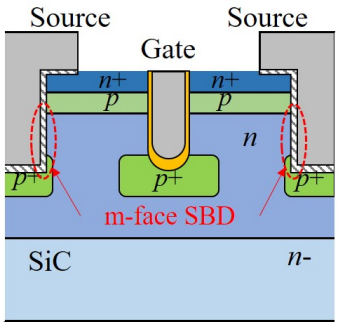


Figure 2.6 Cross-sectional structure of SWITCH-MOS.

the p^+ layer of bottom gate trench. This results in suppressing conduction losses and the bipolar degradation, and reducing the area in the package for the external free wheeling diode.

2.2.4 Temperature sensitive electrical parameter of SiC power device

Thermal management with monitoring the junction temperature of power device (T_J) is one of the most important interest in the safety and reliable operation of power conversion systems. There are some methods to the estimate T_J of power modules.

1. Thermocouple

   This method applies Seebeck effect, which is the thermoelectric force caused by different temperature between 2 different metal wire. Thermocouple has fast response time for the temperature change, but it needs to attach directly on measuring objects. And this also has the large error in the estimated temperature about ± 2°C.

2. Thermometer or Thermal image viewer

   This method measures the temperature based on the black body radiation. Thermal image viewer also can show the temperature distribution on the measuring object by color variation. Though this method does not need to directly attach on measuring objects, the response time is not good.

3. Electrical Test Method (ETM) [67]

   This method utilizes the temperature dependency in $I-V$ characteristics of power device itself. Temperature dependency of the knee voltage for power diodes and the gate threshold voltage for IGBTs or MOSFETs are used for estimating T_{J}. This method enables to use power devices as not only the heat source but also the temperature sensor. While this method enables to obtain the fast time response of T_{J}, it is necessary to be care about the electrical noise of measuring system.

This study focuses on ETM method to utilizes the fast time response for estimating T_{J} of SiC power device. For a fixed measurement current I_{M}, the terminal voltage is almost linearly proportional to T_{J}. This is called as temperature sensitive electrical parameter (TSEP) or K factor. Here, I_{M} is small enough to neglect the self heating effect on power device.

First of all, we derive K factor of power diode, especially of SBD. Eq. (2.5) can be rewritten as the following equation for I_{M}, which is very small to neglect the on-state resistance.

$$I_{\mathrm{M}} = I_0 \left[\exp\left(\frac{qV_{\mathrm{J}}(T)}{nk_{\mathrm{B}}T} \right) - 1 \right], \tag{2.29}$$

where $V_{\mathrm{J}}(T)$ is the junction voltage of power device and as a function of temperature T. Assuming that the temperature dependency of I_0 can be neglect, Eq. (2.29) is rewritten as follow:

$$\begin{aligned} \log\left(\frac{I_{\mathrm{M}}}{I_0} - 1 \right) &= \frac{qV_{\mathrm{J}}(T)}{nk_{\mathrm{B}}T}, \\ \Leftrightarrow V_{\mathrm{J}}(T) &= \frac{nk_{\mathrm{B}}T}{q} \left(\frac{I_{\mathrm{M}}}{I_0} - 1 \right). \end{aligned} \tag{2.30}$$

Differentiating Eq. (2.30) by T, we can obtain K factor for diode.

$$\frac{1}{K_{\mathrm{diode}}} = \frac{dV_{\mathrm{J}}(T)}{dT} = \frac{nk_{\mathrm{B}}}{q} \left(\frac{I_{\mathrm{M}}}{I_0} - 1 \right). \tag{2.31}$$

We can also derive K factor of MOSFET as the following procedure. Assuming the GD short condition ($V_{\mathrm{ds}} = V_{\mathrm{gs}}$), I and $V_{\mathrm{ds}} = V_{\mathrm{gs}}$ are replaced by I_{M} and $V_{\mathrm{ds}} = V_{\mathrm{gs}} = V_{\mathrm{J}}(T)$ as a function of T, respectively. And then,

$$V_{\mathrm{J}}(T)^2 - 2V_{\mathrm{TH}}V_{\mathrm{J}}(T) - \frac{2LI_{\mathrm{M}}}{W\varepsilon_{\mathrm{S}}C_{\mathrm{OX}}} = 0. \tag{2.32}$$

Solving Eq. (2.32) and we obtain the following equation:

$$V_{\mathrm{J}}(T) = V_{\mathrm{TH}} \pm \sqrt{V_{\mathrm{TH}}^2 + \frac{2LI_{\mathrm{M}}}{W\varepsilon_{\mathrm{S}}C_{\mathrm{OX}}}}. \tag{2.33}$$

For a forward bias condition, $V_{\mathrm{J}}(T)$ is larger than 0. Thus,

$$V_{\mathrm{J}}(T) = V_{\mathrm{TH}} + \sqrt{V_{\mathrm{TH}}^2 + \frac{2LI_{\mathrm{M}}}{W\varepsilon_{\mathrm{S}}C_{\mathrm{OX}}}}. \tag{2.34}$$

Differentiating Eq. (2.34) by T with Eq. (2.15) and we obtain the following equation.

$$\begin{aligned}
\frac{dV_{\mathrm{J}}(T)}{dT} &= \frac{dV_{\mathrm{TH}}}{dT} + \frac{V_{\mathrm{TH}}\dfrac{dV_{\mathrm{TH}}}{dT}}{\sqrt{V_{\mathrm{TH}}^2 + \dfrac{2LI_{\mathrm{M}}}{W\varepsilon_{\mathrm{S}}C_{\mathrm{OX}}}}} \\
&= \frac{dV_{\mathrm{TH}}}{dT}\left(1 + \frac{V_{\mathrm{TH}}}{\sqrt{V_{\mathrm{TH}}^2 + \dfrac{2LI_{\mathrm{M}}}{W\varepsilon_{\mathrm{S}}C_{\mathrm{OX}}}}}\right).
\end{aligned} \tag{2.35}$$

Eq. (2.35) can be rewritten as follow using Eq. (2.32):

$$\begin{aligned}
\frac{dV_{\mathrm{J}}(T)}{dT} &= \frac{dV_{\mathrm{TH}}}{dT}\left(1 + \frac{V_{\mathrm{TH}}}{\sqrt{V_{\mathrm{TH}}^2 - 2V_{\mathrm{TH}} + V_{\mathrm{J}}(T)^2}}\right) \\
&= \frac{dV_{\mathrm{TH}}}{dT}\left(1 + \frac{V_{\mathrm{TH}}}{|V_{\mathrm{TH}} - V_{\mathrm{J}}(T)|}\right) \\
&= \frac{dV_{\mathrm{TH}}}{dT}\left(1 + \frac{1}{\left|\dfrac{V_{\mathrm{J}}(T)}{V_{\mathrm{TH}}} - 1\right|}\right).
\end{aligned} \tag{2.36}$$

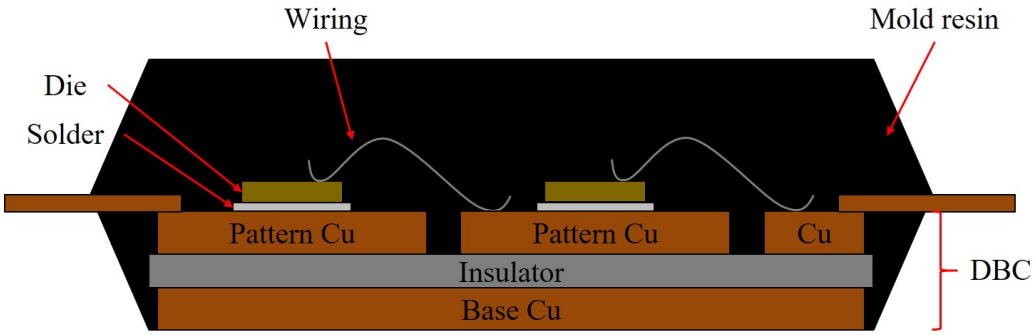
And then,

$$\frac{1}{K_{\mathrm{MOSFET}}} = \frac{dV_{\mathrm{J}}(T)}{dT} = \frac{1}{T}\left[\frac{E_{\mathrm{g}}(T=0)}{2q} - |\psi_{\mathrm{B}}(T)|\right]\left(1 + \frac{1}{\left|\dfrac{V_{\mathrm{J}}(T)}{V_{\mathrm{TH}}} - 1\right|}\right). \tag{2.37}$$

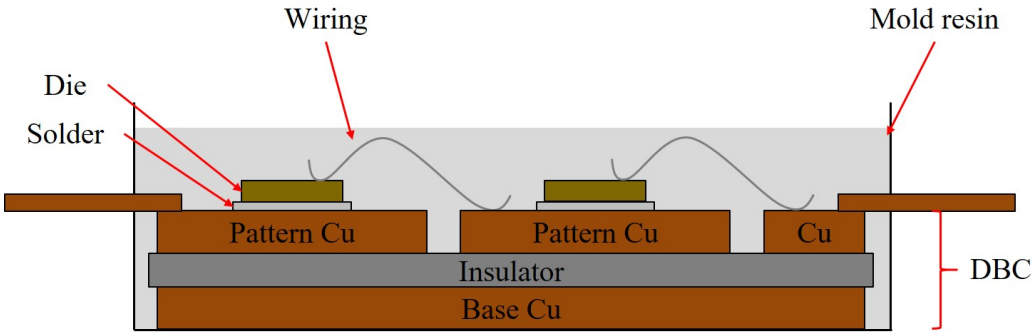
Eq. (2.37) shows that it is possible to estimate T_{J} of MOSFET using K factor.

2.3 SiC power module

A power module packages plural switching devices such as MOSFET or IGBT and/or free wheeling diode (FWD). Modularization enables to obtain the high breakdown and



(a) Transfer mold type.



(b) Case type.

Figure 2.7 Typical structures of power module.

large current capacity by connecting power devices in series and parallel. Actually, most power module connects two or more power devices in parallel on the module in order to realize high current capacity, although the rated voltage is determined by least breakdown voltage among parallel connected devices, and series connection is rarely seen. Another advantage of modularization is to miniaturize power conversion systems. Integrating and implementing devices in the module package reduces the area to implement components in power conversion systems. Moreover this enables to reduce parasitic components in the circuit, which results in improving electrical behavior of power conversion systems such as switching surge voltage. This section summarizes typical structures and materials of recent power module packages.

2.3.1 Typical power module constitution

Fig. 2.7 illustrates typical structures of power module, which are almost same structure. Fig. 2.7(a) is a transfer mold encapsulated power module and molded by thermal resin. Fig. 2.7(b) is a case type power module and covered with protective resin such as Si gel.

Bare die of power device is attached on the module substrate using solder material and forms die attach. Die attach plays an important role in flowing both the large current and the heat generated in junction of power device. Due to RoHS, Pb free solder such as Sn/Ag/Cu (SAC) is generally used as die attach material. However, Pb free solder has difficulty in terms of reliability for high temperature application because its melting point is lower than the conventional Pb solder [68] [69]. This concerns about long-term reliability at the harsh environment using SiC power devices over 300°C. Sintered die attach using nano particle metal such as Ag or Cu attracts attention to achieve the low electrical and thermal resistance for high density power module. A variety of sintered die attach materials have been reported [70]-[72]. Reference [73] developed 3.3 kV/1000 A SiC power module with sintered Cu die attach.

Metal wire bonding forms a electrical connection between power device and module as shown in Fig. 2.8 by ball bonding or wedge bonding. Al or Cu wire, whose diameter is 50 to 500 μm are often used to flow large current. Ribbon bonding technology attracts attention for using interconnections instead of multiple bonding wires. Ribbon bonding increases current capability of ribbons, and also carries the heat generated in junction of power device [74] [75].

Insulation layer plays an important role in making the electrical insulation between power device and heatsink and transferring heat from power device to heat sink. This is required to obtain the high insulation resistance and high thermal conductivity at the high temperature condition. Table 2.2 shows physical properties of typical ceramic material. Here, λ is the thermal conductivity, c is the specific heat, ρ is the density, σ_{MAX} is the 3-points bending strength, CTE is the coefficients of thermal expansion, and ε_{r} is the relative dielectric constant. Aluminium oxide (Al_2O_3) is used for direct bonding copper (DBC) substrate as insulation layer for a long time. Active metal brazing (AMB) technology with active metal enables to joint copper and silicon nitride

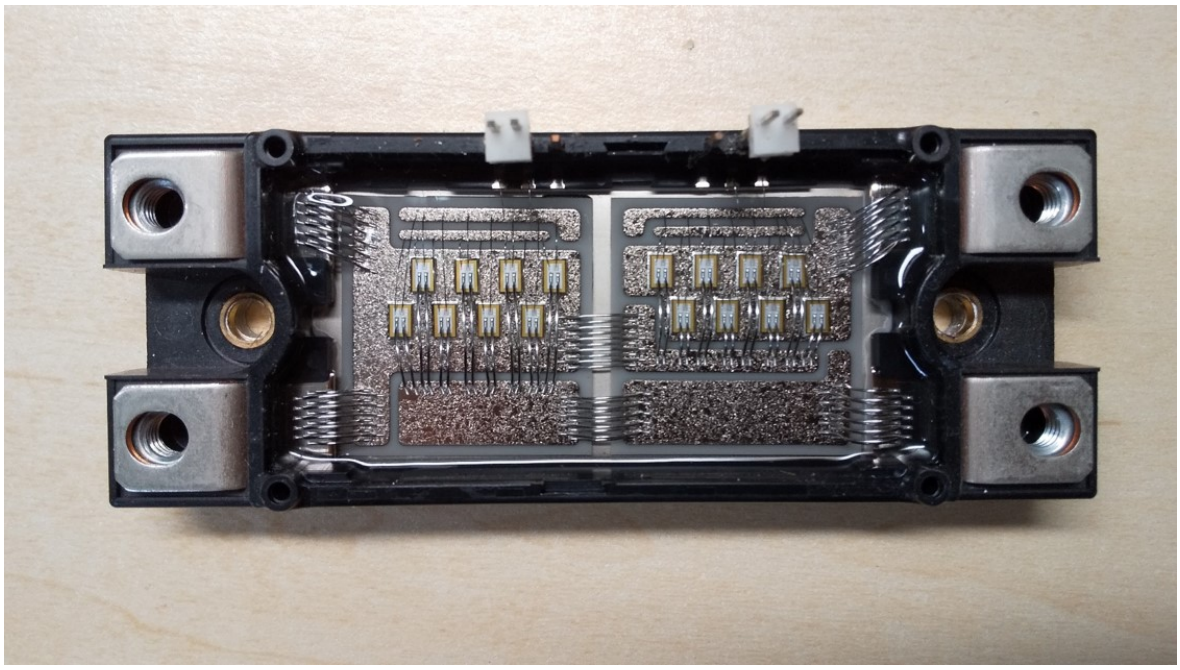


Figure 2.8 Example of case type power module and bonding wire (BSM180D12P2C101, ROHM).

Table 2.2 Physical properties of typical ceramic material

Material	λ [W/m/K]	c [J/g/K]	ρ [g/cm^3]	σ_{MAX} [MPa]	CTE [ppm/K]	ε_{r}
Al_2O_3	36	0.779	3.9	400	7.2	9.9
Si_3N_4(SN-490)	85	0.69	3.2	820	2.3	9.5
Si_3N_4(SN-460)	58	0.63	3.5	790	2.7	9.6
AlN	150	0.71	3.4	310	4.6	8.6

(Si_3N_4).

Fig. 2.9 shows a new power module structure for double sided cooling particularly developed for automotive applications [76] [77]. This structure solders both backside and top side of power device on the heat spreader without wire bonding. This structure enables to not only flow the large current but also transfer the heat dissipated in junction at both direction of power device and reduce the total thermal resistance, which differs from the conventional direct lead bonding (DLB) structure [78].

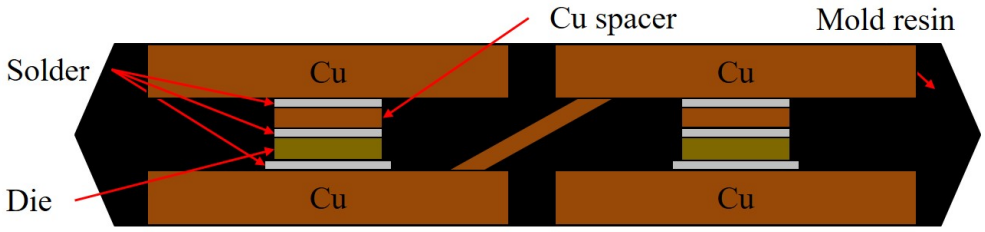


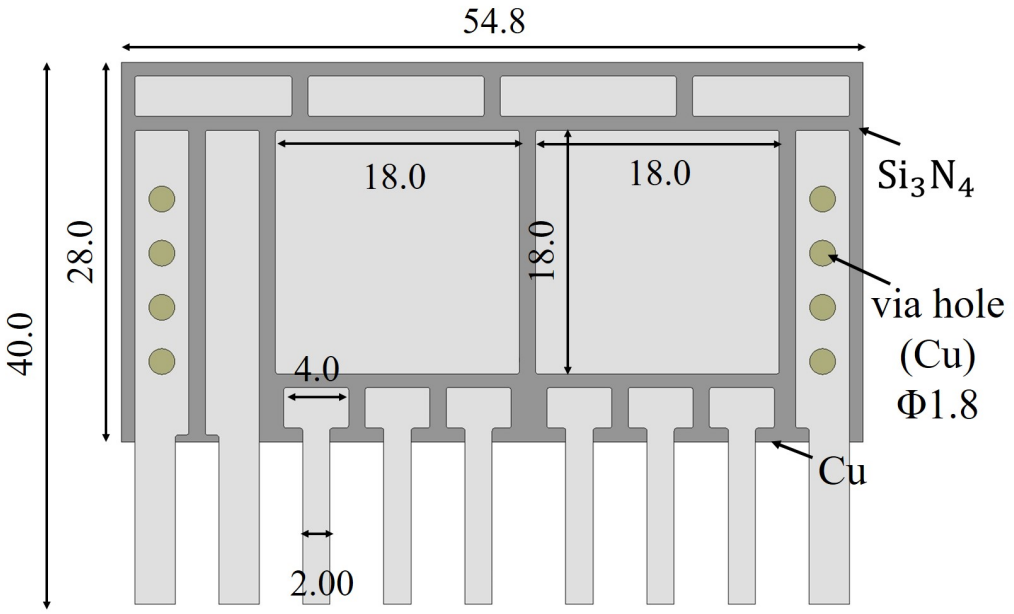
Figure 2.9 Power module with double sided cooling.

2.3.2 Developed multi-layered ceramic substrate for power module

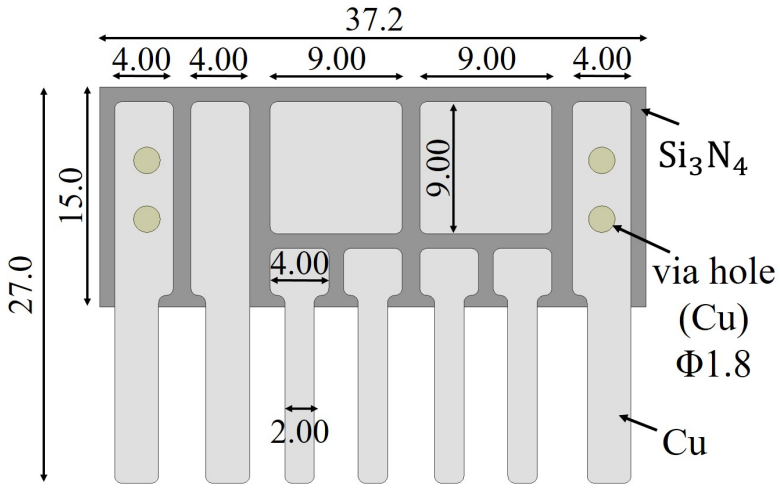
The developed multi-layered ceramic substrate for SiC power module in this study is illustrated in Fig. 2.10. The dimension of module substrate A and B are different to mount various types of chip size, parallelization and wiring connection layout. The insulation layer is composed of Si_3N_4 with 320μm. The Cu plate is brazed with active metal as the conduction layer on the both side of insulation layer. Two double side substrate is stacked to constitute multi-layered substrate. Pattern and middle layer conductor are electrically connected at terminal M and N through two ϕ1.8mm vias with Cu cores to flow the large current.

Fig. 2.11 shows the typical topology of buck converter. Here, the dashed line indicates power module. The parasitic inductance in power conversion system L_{PCB} and in power module L_{PM} induces switching surge voltage with high current switching transient (di/dt). Though C snubber near power module is often used for the switching surge voltage suppression, but this still remains the parasitic inductance of power module itself. The developed multi-layered ceramic substrate enables to directly attach the snubber capacitor on the substrate across DC bus for eliminating the parasitic inductance of wiring between half-bridge and smoothing DC capacitor. This results in suppressing switching surge voltage with high speed switching using unipolar SiC power device.

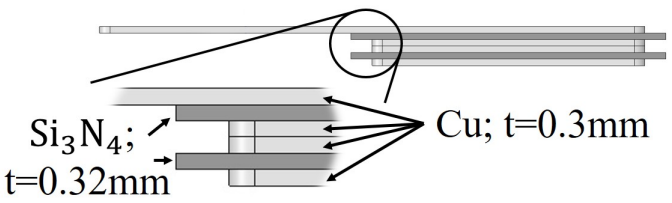
Fig. 2.12 is a example of SiC power module using the developed multi-layered ceramic substrate. SiC MOSFET CPM2-1200-0080B (1200 V/40 A, 3.1 mm/3.36 mm/180 μm, CREE) is attached with 120 μm Sn/Ag/Cu solder (SMIC) on pattern



(a) Module substrate A.



(b) Module substrate B.



(c) Cross-sectional structure.

Figure 2.10 Developed multi-layered ceramic substrate.

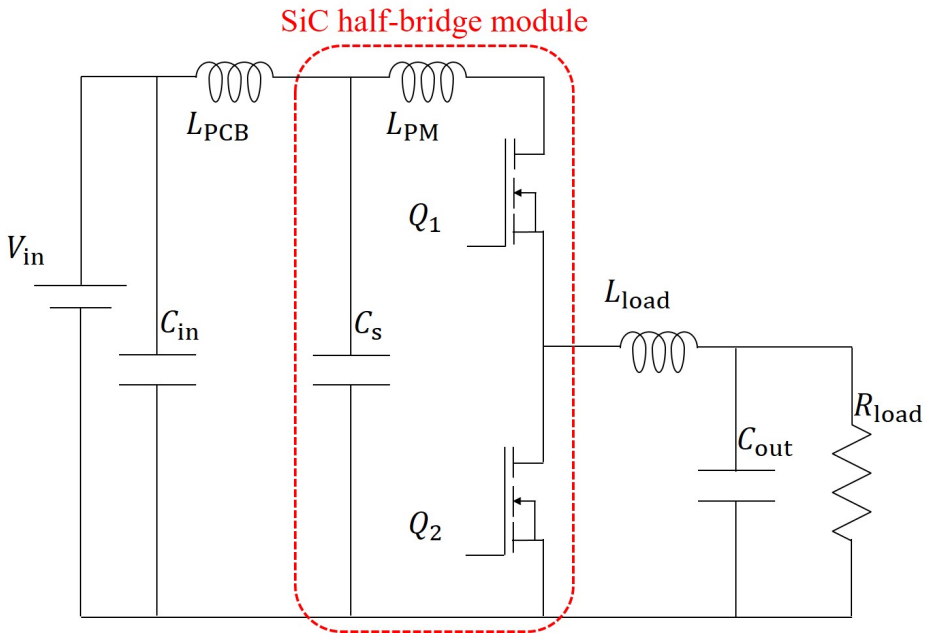
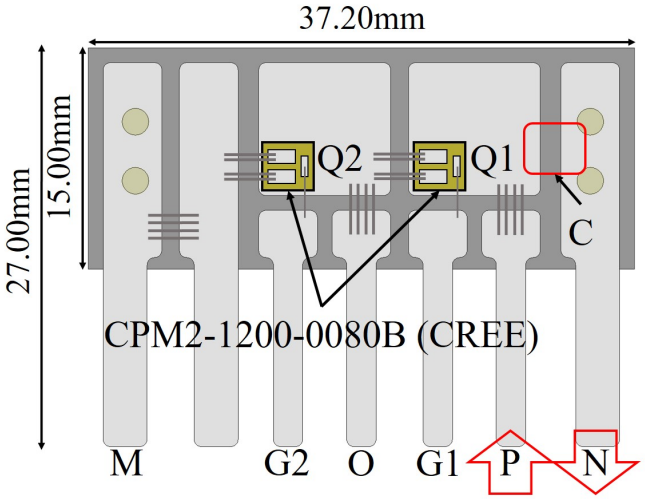


Figure 2.11 Typical buck converter topology using power module.

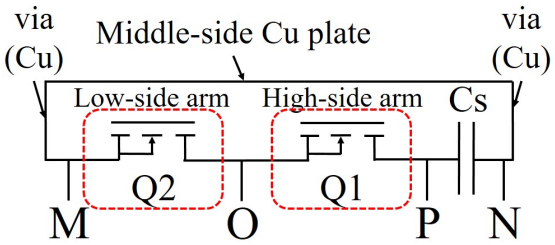
Cu for both arm. Multi-layered ceramic capacitor (MLCC) GRM43DR73A473KW01 (1 kV, 0.047 μF, Murata) is attached directly on the module substrate across DC bus between half-bridge and smoothing DC capacitor. Fig. 2.13 is the frequency characteristics of impedance for terminal P to N. Here, this is experimentally obtained by impedance analyzer 4294A (Agilent Techonolgy). The parasitic inductance without and with MLCC of the developed SiC power module obtained from Fig. 2.13 is 4.51nH and 3.38nH, respectively.

2.4 Summary

This chapter treated fundamentals of SiC power devices and power modules. Electrical characteristics and its temperature dependency of SBD and MOSFET were derived in section 2.2. The knee voltage of SBD and the gate threshold voltage of MOSFET became small as T_J of power device increases, which would be used for T_J estimation as K factor. Section 2.3 described typical power module constitutions. Recent and next generation structures and materials of power module were shown in section 2.3.1. The developed multi-layered ceramic substrate in this study was shown in 2.3.2. This



(a) Circuit topology.



(b) Equivalent circuit of developed module.

Figure 2.12 Developed SiC power module using multi-layered ceramic substrate.

structure enables to reduce the parasitic inductance with snubber capacitor, which results in suppressing switching surge voltage of SiC power module with high speed switching.

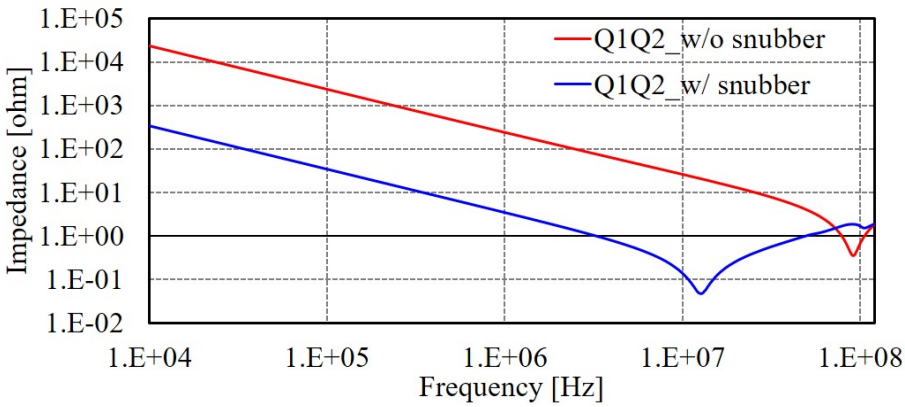


Figure 2.13 Frequency characteristics of impedance for terminal P to N.

Chapter 3

Transient thermal network model identification for power module packages

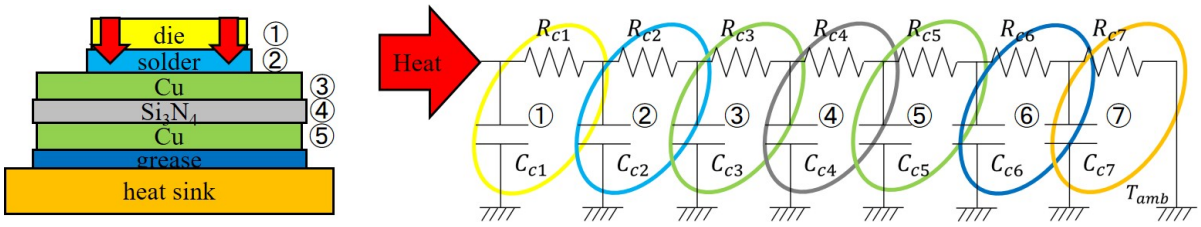
3.1 Introduction

Transient thermal characterization of power modules plays an important role in designing power conversion systems for miniaturization. The transient thermal network model of power module packages is identified by deconvolution calculation for the time response of junction temperature (T_{J}) in power semiconductor devices, which is obtained by static test method. This chapter develops a signal processing algorithm using weighted discrete Fourier transformation and noise filtering in frequency domain for nonuniform time step data in the converted logarithmic time domain to apply deconvolution calculation. The developed algorithm suppresses the influence of noise superimposed on the measured signal and enables the accurate identification of transient thermal network model.

3.2 Transient thermal network model of power module packages

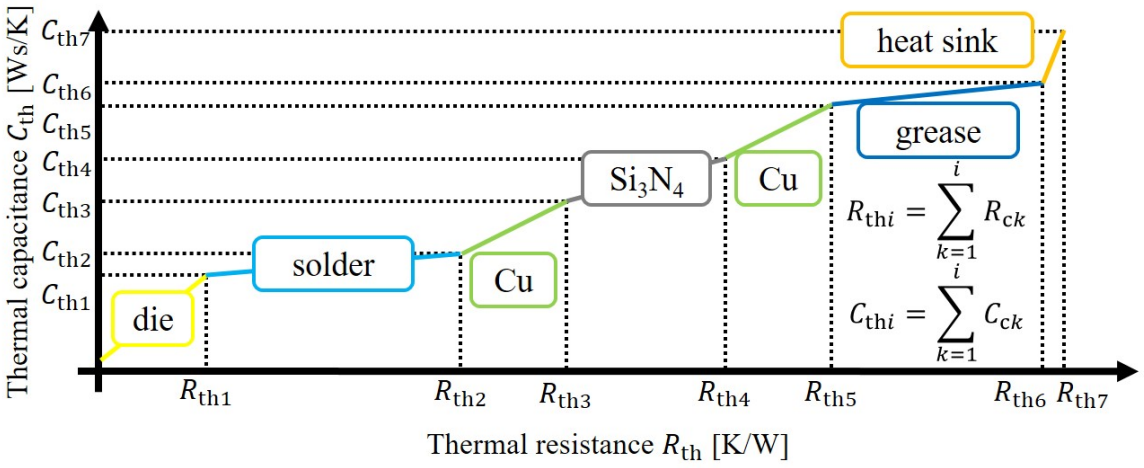
This section summarizes the theory and the measurement setup of static test method. For more details on the method, the reader refers the standard text [54] and related references.

3.2.1 Structure function related to transient thermal networks



(a) Power module package.

(b) Cauer thermal network.

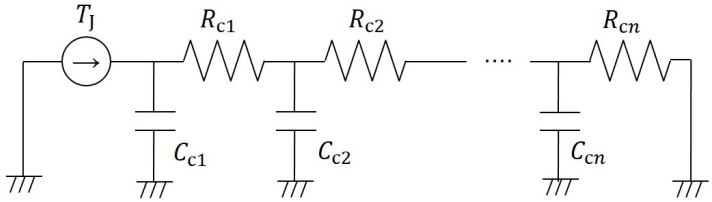


(c) Structure function.

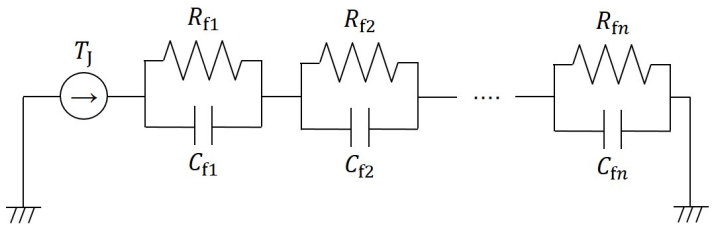
Figure 3.1 Structure function related to actual power module package.

The typical structure of a power module package with active metal bonding (AMB) substrate is illustrated in Fig. 3.1(a). The heat dissipated in junction of power device approximately flows to heat sink through each layer of power module package in one direction. The thermal equivalent circuit is modeled by the cascade connected pairs

of thermal resistance and thermal capacitance as Cauer thermal network illustrated in Fig. 3.1(b), by assuming that each layer of the power module package is uniform and heat spreading in the horizontal axis is integrated. Here, the electrical potential and current in electrical circuit correspond to the junction temperature and heat flow in thermal circuit, respectively. The Protonotarious-Wing function [79], or structure function [80], represents the cumulative thermal capacitance as a function of the cumulative thermal resistance as illustrated in Fig. 3.1(c). In other words, structure function related to Cauer thermal network represents transient thermal behavior of respective components in the power module.



(a) Cauer thermal network.



(b) Foster thermal network.

Figure 3.2 Transient thermal network models.

Generally, the thermal impedance of an nth order Cauer thermal network $Z_{\mathrm{cauer}}(s)$ in Laplace (s-)domain is given by the following equation with the parameters in Fig. 3.2(a):

$$Z_{\mathrm{cauer}}(s) = \cfrac{1}{sC_{c1} + \cfrac{1}{R_{c1} + \cfrac{1}{sC_{c2} + \cfrac{1}{R_{c2} + \cfrac{1}{\ddots + \cfrac{1}{sC_{cn} + \cfrac{1}{R_{cn}}}}}}}}. \tag{3.1}$$

Although Cauer thermal network corresponds to the actual physical parameter and

structure of power module packages, but the parameter extraction directly from the measured time response of T_{J} is difficult. We therefore consider the numerical equivalent transient thermal network model illustrated in Fig. 3.2(b). This network is known as Foster thermal network, and its parameters do not have physical correspondence to the model structure. The thermal impedance of an nth order Foster thermal network $Z_{\mathrm{foster}}(s)$ in s-domain is given by the summation of fractional impedances with the parameters in Fig. 3.2(b):

$$Z_{\mathrm{foster}}(s) = \frac{R_{\mathrm{f1}}}{1 + sR_{\mathrm{f1}}C_{\mathrm{f1}}} + \frac{R_{\mathrm{f2}}}{1 + sR_{\mathrm{f2}}C_{\mathrm{f2}}} + \cdots + \frac{R_{\mathrm{f}n}}{1 + sR_{\mathrm{f}n}C_{\mathrm{f}n}} = \sum_{i=1}^{n} \frac{R_{\mathrm{f}i}}{1 + sR_{\mathrm{f}i}C_{\mathrm{f}i}}. \quad (3.2)$$

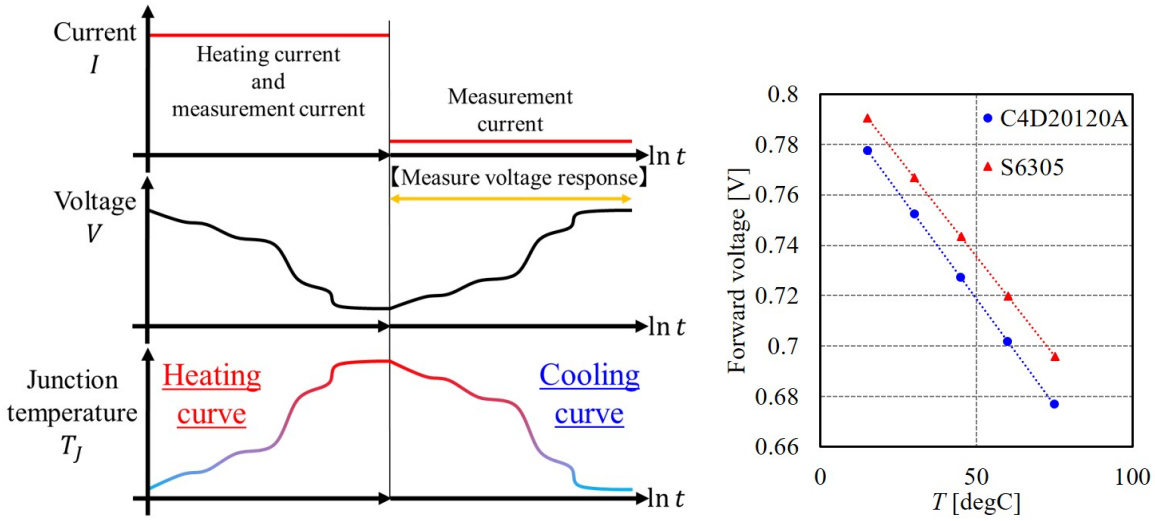
By converting Eq. (3.2) from s-domain to time domain, the time response of junction temperature $T_{\mathrm{J}}(t)$ for ΔP_{H} power dissipation is calculated by the following equation:

$$T_{\mathrm{J}}(t) = \Delta P_{\mathrm{H}} \sum_{i=1}^{n} R_{\mathrm{f}i}[1 - \exp(-t/\tau_{\mathrm{f}i})], \quad (3.3)$$

where $\tau_{\mathrm{f}i} = R_{\mathrm{f}i}C_{\mathrm{f}i}$ is the thermal time constant. This equation means that the time response of T_{J}, which is obtained experimentally from power devices in power modules, is represented by the summation of exponential functions. Moreover, the desired Cauer thermal network is obtained from Foster thermal network by numerical equivalent transformation.

3.2.2 Foster thermal network model identification by deconvolution

The time response of T_{J} is experimentally obtained using static test method. The measurement procedure is summarized as follows, and illustrated in Fig. 3.3(a). First, a device under test (DUT) is attached on the temperature-controlled coldplate. A large current, which is sufficient to achieve self-heating, is forced to flow through a DUT until it reaches thermal equilibrium condition. The heating current then shunts off and the time response of T_{J} in cooling operation is measured. T_{J} is obtained from the measured voltage drop to a small constant current, whose self-heating effect is negligible, and the temperature dependency in $I - V$ characteristics of power semiconductor devices. The measured time response of junction voltage (V_{J}) is converted to the time response of



(a) Measurement response of static test method.

(b) K factor.

Figure 3.3 Static test method.

T_J using K factor. Fig. 3.3(b) shows the example of K factor for SiC Schottky barrier diode (SBD) C4D20120A (1200 V/20 A, CREE, TO-220 package) and S6305 (1200 V/50 A, ROHM, mounted on ceramic substrate).

Cauer thermal network model is identified from the measured time response of T_J using the procedure listed in Table 3.1. In this chapter, this procedure is referred as the conventional algorithm, which is implemented in the analysis software T3SterMaster (MentorGraphics). Eq. (3.3) is rewritten as the transfer function $a(t)$ for the unit power step input:

$$a(t) = \frac{T_\mathrm{J}(t)}{\Delta P_\mathrm{H}} = \sum_{i=1}^{n} R_{\mathrm{f}i}[1 - \exp(-t/\tau_{\mathrm{f}i})], \tag{3.4}$$

where $a(t)$ is transformed to $a(z)$ by introducing the logarithmic time scale $z = \ln t$, and $\zeta = \ln \tau$. Thermal time constant spectrum or TCS, $R(z)$, is given as the following equation with the deconvolution integral $\otimes^{-1}$:

$$R(z) = \frac{d}{dz} a(z) \otimes^{-1} w(z), \tag{3.5}$$

where $w(z) = \exp(z - \exp(z))$ is the given weight function. The obtained Foster thermal network model from TCS by deconvolution can be transformed to Cauer thermal network model by Foster-Cauer transformation.

Table 3.1 The conventional algorithm for identifying transient thermal network model

Step	Domain	Procedure
1	Time (t)	Measure the time response of V_{J} in the cooling operation
2	Time (t)	Convert $V_{\mathrm{J}}(t)$ to $T_{\mathrm{J}}(t)$ using K factor and divide it by the input power ΔP_{H}
3	Time (t)	$T_{\mathrm{J}}(0)$ estimation by extrapolating [81]
4	Time (t)	Convert $a(t)$ from the linear time domain to the logarithmic time domain
5	Time (t)	Remove the noise with moving average filter and resample
6	Time (z)	Differentiate $a(z)$ with z to obtain $da(z)/dz$
7	Time (z)	Calculate $w_{\mathrm{z}}(z)$
8	Frequency	FFT of $da(z)/dz$ and $w_{\mathrm{z}}(z)$
9	Frequency	Deconvolution calculation
10	Time (z)	Obtain TCS by IFFT using the filter function with Fermi-Dirac function [54]
11	Time (z)	Determine Foster thermal network model from TCS
12	Time (z)	Determine Cauer thermal network model by Foster-Cauer transformation

3.3 Signal processing algorithm in logarithmic time domain

Table 3.2 shows the signal processing algorithm developed in this study to identify Cauer thermal network model, and the difference in procedure from Table 3.1 is specified by bold number. The conventional algorithm eliminates noise in the measured signal using a moving average filter in the linear time domain. However, the moving average filter cannot fully eliminate the measurement noise, and the residual noise is emphasized in numerical differentiation of $a(z)$, which degrades the accuracy of the identified transient thermal network model. The developed algorithm adopts weighted discrete Fourier transformation and noise filtering in logarithmic frequency domain to suppress the influence of measurement noise. The details of each calculation is discussed in this chapter.

Table 3.2 The developed algorithm for identifying transient thermal network model

Step	Domain	Procedure
1	Time (t)	Measure the time response of V_{J} in the cooling operation
2	Time (t)	Convert $V_{\mathrm{J}}(t)$ to $T_{\mathrm{J}}(t)$ using K factor and divide it by the input power ΔP_{H}
3	Time (t)	$T_{\mathrm{J}}(0)$ estimation by extrapolating [81]
4	Time (t)	Convert $a(t)$ from the linear time domain to the logarithmic time domain
5	Time (z)	Differentiate $a(z)$ with z to obtain $da(z)/dz$
6	Frequency	Weighted DFT of $da(z)/dz$
7	Frequency	Noise reduction with Fermi-Dirac function
8	Time (z)	IDFT for the filtered frequency response
9	Time (z)	Bayesian deconvolution to obtain TCS
10	Time (z)	Determine Foster thermal network model from TCS
11	Time (z)	Determine Cauer thermal network model by Foster-Cauer transformation

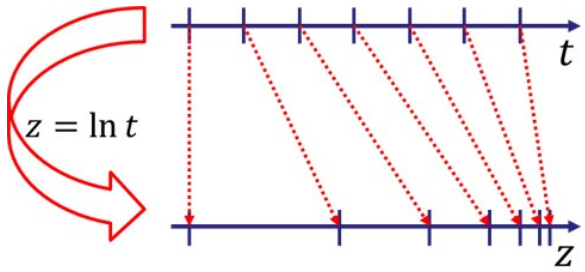


Figure 3.4 Transformation of sampling point from the uniform time step in linear time domain to logarithmic time domain.

3.3.1 Transformation of time domain from linear to logarithmic

The phenomenon of heat transfer progresses exponentially in time, and the transient thermal network model identification is processed in the logarithmic time domain as shown in Table 3.1 and 3.2. The measurement of V_{J} time response is sampled with uniform time step Δt in the linear time domain, and thus the converted data to the logarithmic time domain has nonuniform time step as illustrated in Fig. 3.4. This time step in the logarithmic time domain becomes small as time progresses. This leads to the excess samples in the logarithmic time domain and increases the computational time in identifying the transient thermal network model. Decimation in the logarithmic time

domain is required to reduce the number of data in the identification process. This paper decimates the measured data in the linear time domain by halving sampling frequency, when the following condition is satisfied:

$$\frac{|z_{i+1} - z_i|}{z_1 - z_0} \leq \frac{1}{2Z}, \tag{3.6}$$

where z_i for $0 \leq i \leq N_{\text{lin}} - 1$ is the discretized logarithmic time converted from the linear time t_i. Z is a coefficient determined by users, and $z_0 > 0$ is the first time point of measurement. For example, the sampling frequency is halved to 500 kHz, 250 kHz, 125 kHz, ..., for the initial sampling frequency of 1 MHz, which reduces the number of data for identification to N ($N < N_{\text{lin}}$). Z is determined in terms of time resolution based on the time constant of interest. For example, 100000 numbers of 1 sec data by 100 kHz sampling reduces 1500 after decimation in Z=100. The calculation time of the developed algorithm without and with decimation is 1344.21 sec and 1.13 sec, respectively for Core i7-8700K and DDR4-32GB memory system.

Though the conventional algorithm also adopts this method, but the decimated measured time response of T_{J} is filtered by the moving average filter, and then re-sampled to the uniform logarithmic time step. The noise elimination with the moving average filter to the decimated data is ineffective, and thus this filtering method in the conventional algorithm seems to occur the large residual noise.

3.3.2 Noise reduction using weighted discrete Fourier transformation

Fourier transformation of a given function $x(z)$, and its inverse Fourier transformation are given by the following equations:

$$X(\Phi) = \int_{-\infty}^{\infty} x(z) e^{-j2\pi\Phi z} dz, \tag{3.7}$$

$$x(z) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(\Phi) e^{j2\pi\Phi z} d\Phi. \tag{3.8}$$

Here, $j^2 = -1$. It should be noted that Φ denotes the logarithmic frequency, which corresponds with logarithmic time domain z. We assume that $x(z)$ is the periodic function for $z = a$ to $z = b$, and discretizes in the nonuniform time step for the total

number of data N. In this time, the fundamental frequency Φ_0 and Nyquist frequency Φ_c in the logarithmic frequency domain are given as follows:

$$\Phi_0 = \frac{1}{\Delta z_{\max}}, \tag{3.9}$$

$$\Phi_c = \frac{1}{2\Delta z_{\max}}. \tag{3.10}$$

Here, $\Delta z_{\max} = \max\{z_{i+1} - z_i\}$ for $0 \leq i \leq N-1$ after decimation. Eq. (3.8) is discretized as follows with $\Phi_k = k\Phi_0$:

$$X(\Phi_k) = \int_a^b x(z) e^{-j2\pi \left(\frac{k}{z_{N-1} - z_0} \right) z} \mathrm{d}z. \tag{3.11}$$

Then, $X(\Phi_k)$ is rewritten by adopting the trapezoidal formula for Eq. (3.11):

$$X(\Phi_k) \simeq \sum_{n=0}^{N-2} \left(x_{n+1} e^{-j2\pi \frac{k}{z_{N-1} - z_0}(z_{n+1} - z_0)} + x_n e^{-j2\pi \frac{k}{z_{N-1} - z_0}(z_n - z_0)} \right) \frac{(z_{n+1} - z_n)}{2}. \tag{3.12}$$

Eq. (3.12) is taken as weighted discrete Fourier transformation. In order to suppress the influence of noise in the measured signal, a low-pass filter is adopted in the frequency domain. In practice, Fermi-Dirac function F_{fd} [54] is used as the low-pass filter.

$$F_{\mathrm{fd}}(\Phi_k) = \left[\exp\left(\frac{|\Phi_k| - \Phi_0}{\sigma} \right) \right]^{-1}. \tag{3.13}$$

The shape of Fermi-Dirac function is determined by two parameters: the bandwidth Φ_0 and the edge steepness σ. The parameter is adjusted for the best compromise between the resolution and noise enhancement. $\Phi_0 = 0.45$ and $\sigma = 0.05$ are good values as given in [54].

Inverse discrete Fourier transformation (IDFT) is processed to the noise eliminated signal for deconvolution calculation in the logarithmic time domain. The nonuniform time step of the measured signal in the logarithmic time domain is transformed to the uniform time step by IDFT, i.e. the resynthesised signal is resampled. The conventional algorithm sets the output data to become 20 point samples per octave.

3.3.3 Bayesian deconvolution

Practical deconvolution algorithms have been applied for the transient thermal characterization of power module packages, such as Bayesian deconvolution [82] [83] and Fourier domain inverse filtering [84]. This paper performs Bayesian deconvolution for the low-pass filtered signal in logarithmic time domain.

$$R_i^{(m+1)} = R_i^{(m)} \sum_k \frac{w_{ki} \left(\left. \frac{da}{dz} \right|_i \right)}{\sum_j w_{kj} R_i^{(m)}}, \tag{3.14}$$

where R_i is the discretized TCS, $R_i^{(m)}$ is the estimated R_i after m iterations, and $w_{ki} = \exp(z_k - z_i - \exp(z_k - z_i))$. Convolution and correlation sums in Eq. (3.14) have to be recalculated for each iteration step. The iteration number m is estimated to be sufficient to the order of 1000 in [82].

3.4 Improvement of accuracy for the identified transient thermal network model using the developed algorithm

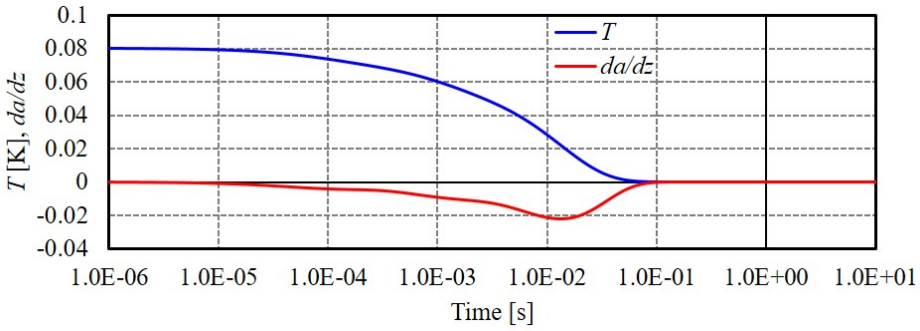


Figure 3.5 Ideal time response of T_J.

The developed algorithm is validated using an ideal time response of T_J shown in Fig. 3.5. This time response is numerically calculated from Eq. (3.3) for Foster thermal network model parameters, which is obtained by Cauer-Foster transformation for

Table 3.3 Cauer thermal network model parameters

n	R_{ci}	C_{ci}	τ_{ci}
1	0.01	0.01	0.0001
2	0.02	0.05	0.001
3	0.05	0.20	0.01

the parameters listed in Table 3.3. The evaluation is processed for a 1 MHz sampling frequency, and a decimation coefficient $Z = 100$. The developed algorithm is programmed with C including GNU Multiple Precision Arithmetic Library (GMP).

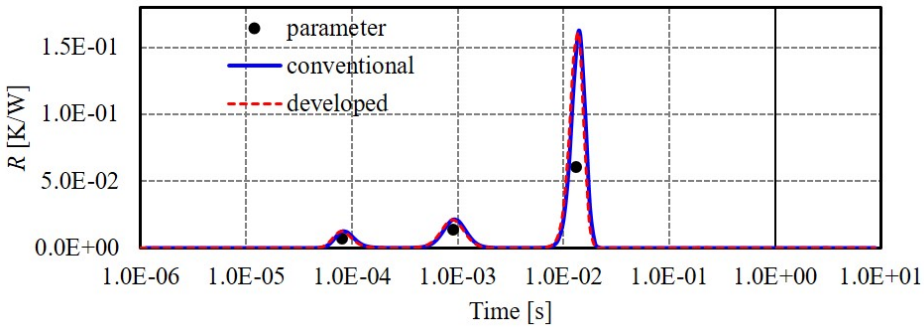


Figure 3.6 TCS calculated from Fig. 3.5.

The TCSs of $da(z)/dz$ in Fig. 3.5 are shown in Fig. 3.6. The number of Bayesian iteration m is 1000. The developed algorithm adopts Φ_0=0.45 and σ=0.05, while it is not disclosed for T3SterMaster. The blue solid and the red dotted lines in Fig. 3.6 are calculated by T3SterMaster and the developed algorithm, respectively. The black dot denotes the given Foster thermal network model parameter in Table 3.3. The TCS calculated using the conventional and the developed algorithm coincides with the given time constant.

3.4.1 Quantization error

The sampling frequency and the bit length of A/D converter (ADC) in the discretization and the quantization of the measured data affect resolution and accuracy of the calculated transient thermal network model. Generally, signal-to-noise ratio (SNR) of the quantization error to an ideal sinusoidal wave for full-scale input N_{bit} bit ADC is

given as follow [85] [86]:

$$SNR[\mathrm{dB}] = 6.02N_{\mathrm{bit}} + 1.76. \tag{3.15}$$

From Eq. (3.15), for example, the SNR of a 12bit ADC is 74dB. Over sampling is the general method for suppressing the quantization error for the same bit length ADC [85]-[88]. The improved SNR for oversampled signal ratio (OSR) is redefined after low-pass filtering and decimation as given by Eq. (3.16) [85].

$$SNR[\mathrm{dB}] = 6.02N_{\mathrm{bit}} + 1.76 + 10\log_{10}(OSR). \tag{3.16}$$

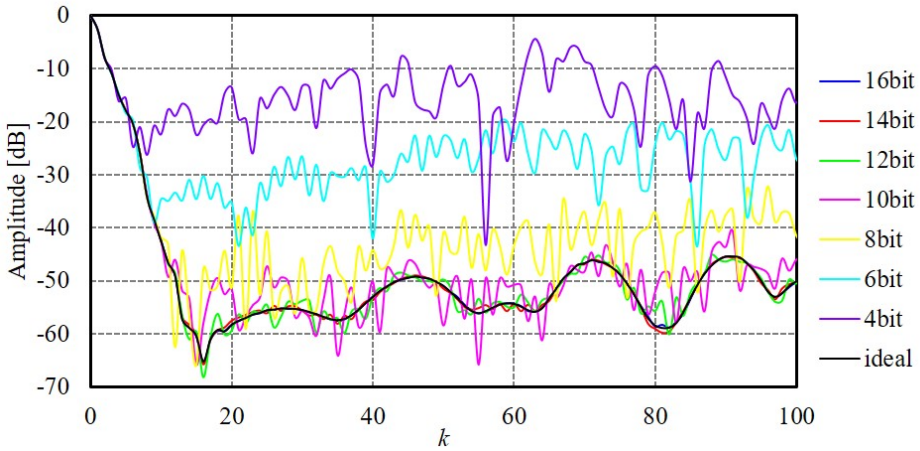
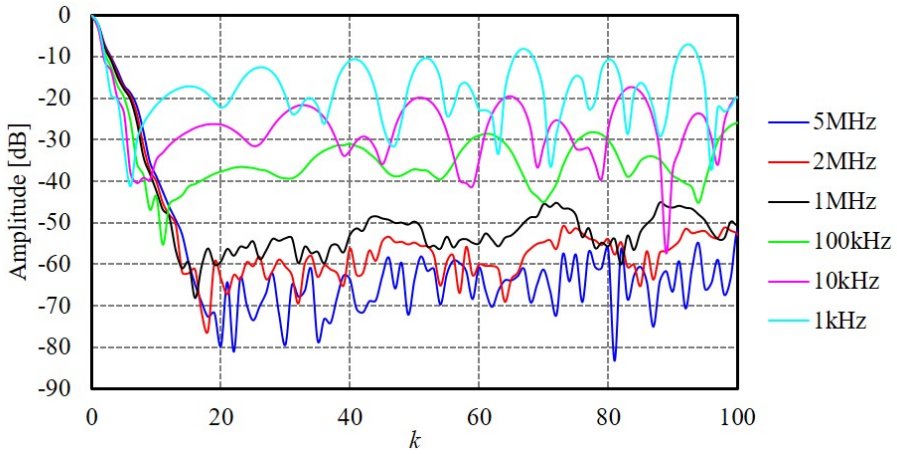


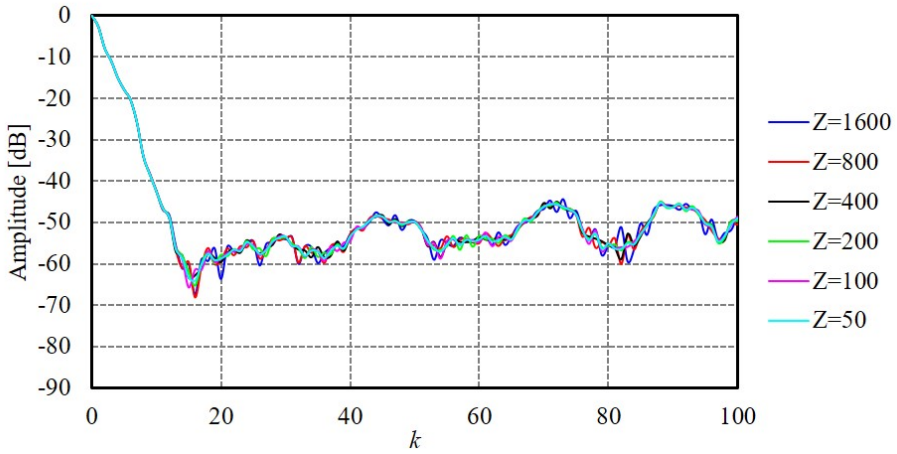
Figure 3.7 Power spectra of the $da(z)/dz$ for the bit length of ADC (1MHz, Z =100).

The power spectra of $da(z)/dz$ in Fig. 3.5 is shown in Fig. 3.7. Here, k is the order to the fundamental frequency, and the amplitude is normalized for $k = 0$. The bit length of ADC for full-scale input is given as the parameter for evaluating the influence of the quantization error, which appears as the difference in amplitude of power spectrum. This result shows that the longer bit length gives the lower floor noise level, and the amplitude of power spectrum coincides with the result calculated from Eq. (3.16). The power spectra larger than 10 bit are in agreement with its ideal spectra in full-scale input ADC. In actual measurement environment, the effective bit length of ADC for the input signal should be considered because this result assumes the full-scale input.

The power spectrum of $da(z)/dz$ in Fig. 3.5 is calculated as shown in Fig. 3.8. Sampling frequency and decimation coefficient Z are given as the parameters for 12bit full-scale input ADC in Fig. 3.8(a) and 3.8(b), respectively. Fig. 3.8(a) shows that



(a) Sampling frequency (12bit, Z=100).



(b) Decimation coefficient (12bit, 1MHz).

Figure 3.8 Power spectrum of $da(z)/dz$ for the OSR (12bit).

the higher sampling frequency gives the lower floor noise level by suppressing the quantization error due to oversampling, which coincides with the value calculated by Eq. (3.16). It is noted that the number of the measured data becomes large for high sampling frequency. Fig. 3.8(b) reveals that Z does not influence on the power spectrum of $da(z)/dz$, and Z can be chosen as small as possible unless the resolution of TCS after decimation does not degrade.

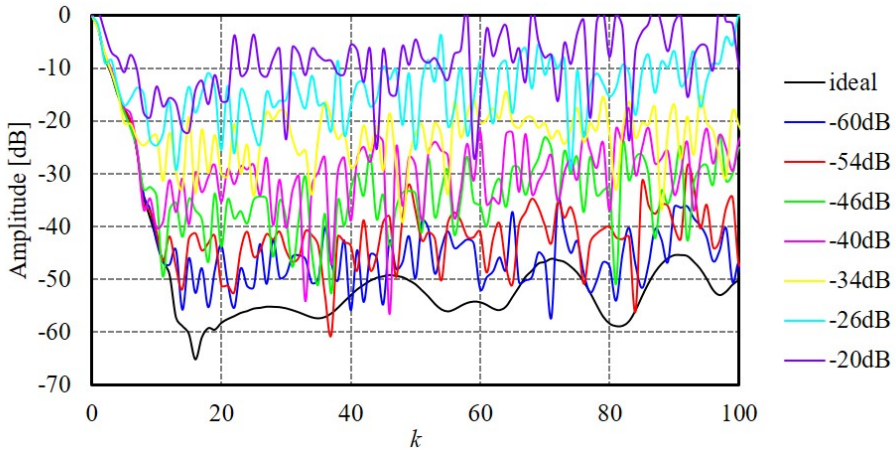


Figure 3.9 Power spectrum of $da(z)/dz$ for white noise (1MHz, Z=100).

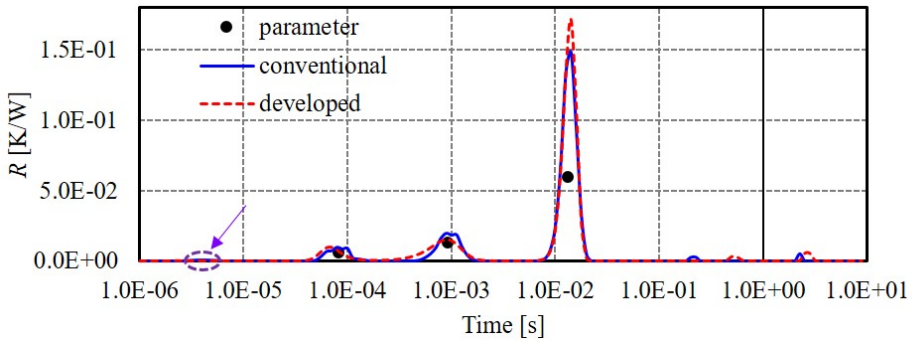
3.4.2 Evaluation of robustness for the noise superimposed on the ideal signal

Fig. 3.9 is the power spectra of $da(z)/dz$ with white noise superimposed on the ideal signal in Fig. 3.5. The quantization is not considered in this section. The amplitude of noise superimposed on the ideal signal is the parameter referred to as SNR for evaluating the effect of noise elimination using the developed algorithm. The amplitude of white noise clearly increases the floor noise level in the power spectrum of $da(z)/dz$ as shown in Fig. 3.9.

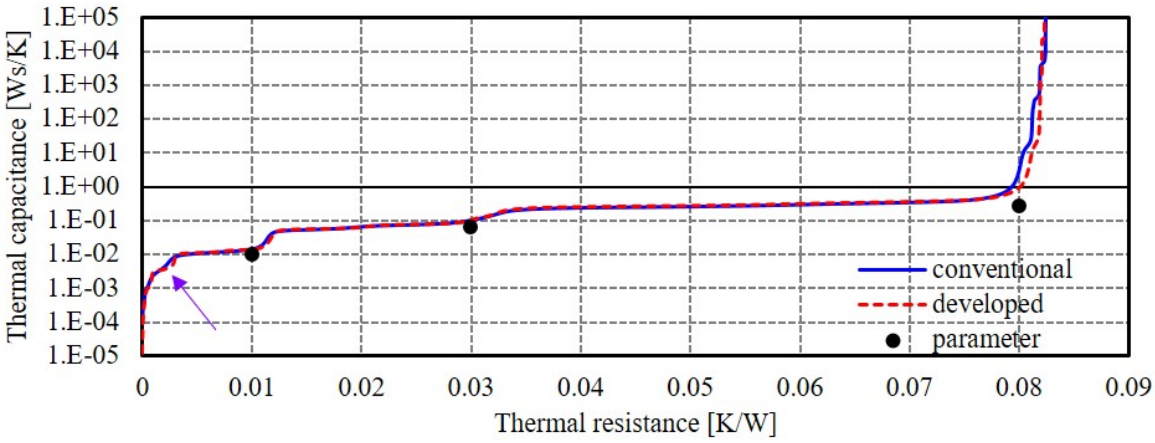
Table 3.4 RMS error for $da(z)/dz$

SNR	developed	conventional
-60dB	5.02×10^{-5}	2.24×10^{-4}
-46dB	2.40×10^{-4}	5.93×10^{-4}
-40dB	3.39×10^{-4}	1.08×10^{-3}
-26dB	8.02×10^{-3}	1.01×10^{-2}

The obtained TCS of $da(z)/dz$ with 40dB white noise superposition and its structure function is shown in Fig. 3.10. The conventional algorithm gives unintended peaks on TCS in the small time constant as indicated by arrows in Fig. 3.10(a), which is not in the given model parameter and makes the step shape of structure function obscure. The residual noise at large time constant appears as the undesired peak for both algorithm.



(a) TCS.



(b) Structure function.

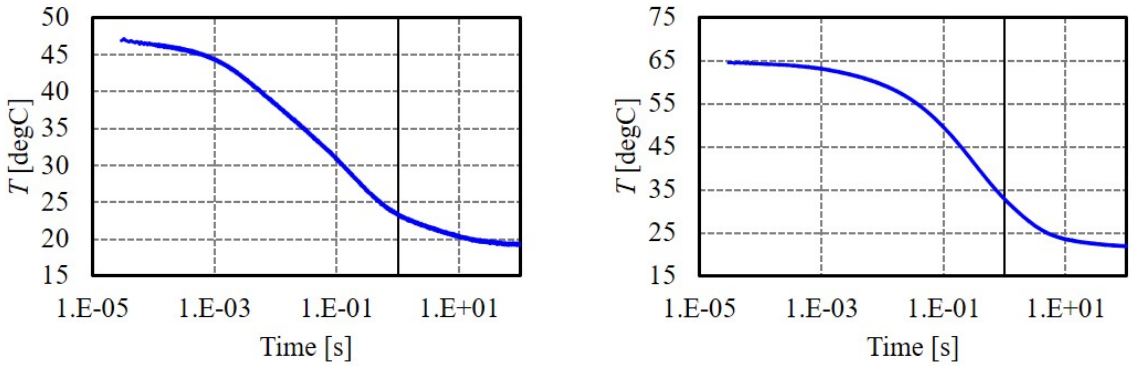
Figure 3.10 TCS of $da(z)/dz$ for SNR=-40dB and the structure function (1MHz, Z =100).

The amplitude of the intended peak calculated by the developed algorithm is higher than that calculated by the conventional algorithm. This enables to clearly extract the transient thermal network model parameters from structure function. The structure function calculated by the conventional and the developed algorithm in Fig. 3.10(b) coincides with the given model parameter in Table 3.3.

Table 3.4 shows the root mean square (RMS) error of $da(z)/dz$ from the ideal $da(z)/dz$ for each algorithm. The developed algorithm can suppress the influence of white noise, and improve the accuracy of obtained TCS and identified transient thermal network model.

3.4.3 Experimental validation for discrete power device and power module package

The transient thermal network model of discrete power device and power module package is experimentally identified with the conventional and the developed algorithm. Studied discrete power device package does not have insulation and bottom copper layer shown in Fig. 3.1(a). AMB substrate has high critical electric field and high thermal conductivity, and is often used for high density power modules. The studied power module package with SiC SBD S6305 is attached on SiN power module substrate shown in Fig. 3.1(a) by Pb free solder and Al wired with ϕ 300 μm.

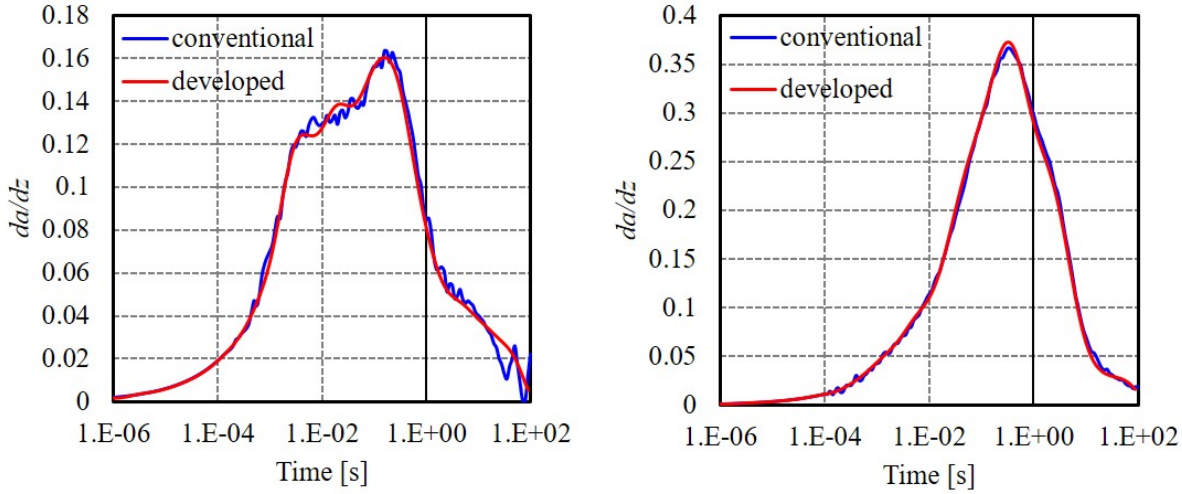


(a) Discrete package (C4D20120A). (b) Studied power module (S6305).

Figure 3.11 The time response of estimated T_{J}.

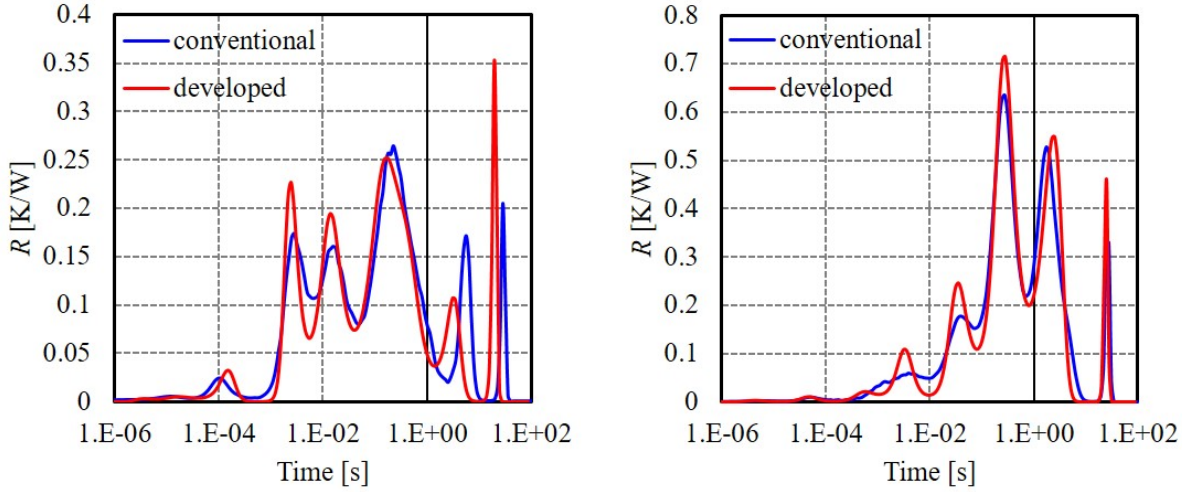
The time response of estimated T_{J} for discrete SiC SBD C4D20120A (TO-247) and the studied power module is experimentally obtained by static test method using T3Ster (MentorGraphics) with 12bit ADC at 1 MHz sampling frequency as shown in Fig. 3.11. The time response of measured V_{J} for Fig. 3.11(a) in cooling operation is obtained to a small 10 mA constant current after self heated thermal equilibrium condition with a 15 A heating current. And Fig. 3.11(b) is obtained to a small 100 mA constant current after self heated thermal equilibrium condition with a 20 A heating current. T_{J} in Fig. 3.11 is estimated using the K factor in Fig. 3.3(b). These packages are attached on a 20°C coldplate with 10 cN/m screw torque.

Fig. 3.12 and 3.13 show the calculated $da(z)/dz$ for the filtered measured signal to Fig. 3.11 and TCS with 1000 Bayesian iteration, respectively. The developed algorithm



(a) Discrete package (C4D20120A). (b) Studied power module (S6305).

Figure 3.12 The time response of $da(z)/dz$.



(a) Discrete package (C4D20120A). (b) Studied power module (S6305).

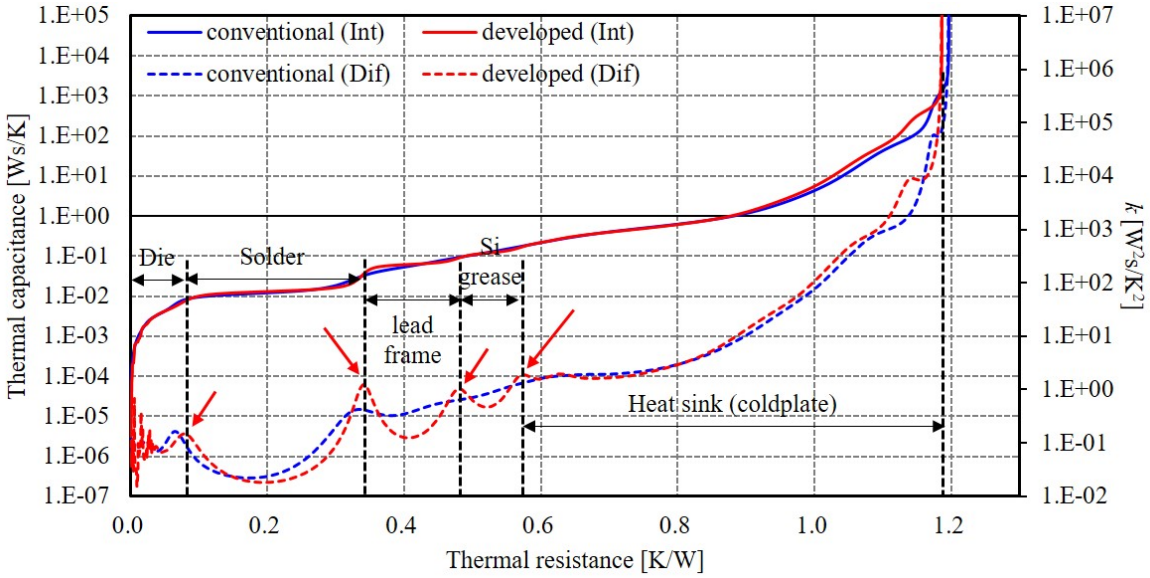
Figure 3.13 TCS.

eliminates the measurement noise as shown in Fig. 3.12. The specific peak of TCS corresponding to its package is emphasized as shown in Fig. 3.13.

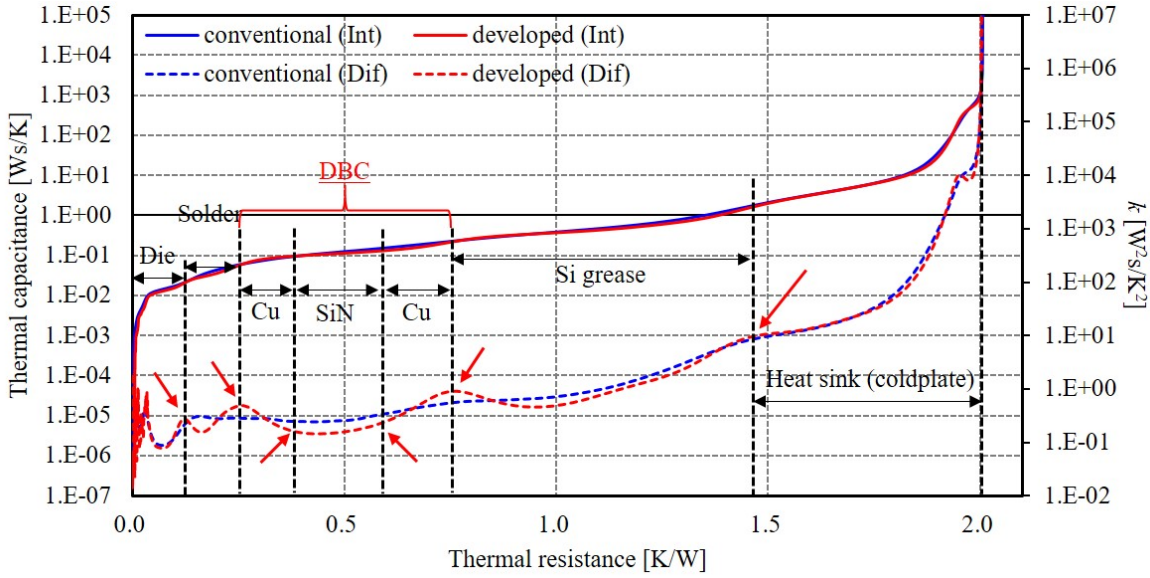
The structure function obtained from Fig. 3.13 is shown in Fig. 3.14. "Int" and "Dif" denote the integral and differential structure function, given as solid and dashed line, respectively. The inflection point of differential structure function for the developed algorithm is clear compared to the conventional algorithm indicated by red arrows in Fig. 3.14. The layer structure of tested discrete power device and module package is identified as the structure function shown in Fig. 3.14. In general, it is difficult to clearly separate layers for low thermal resistance multi-layered structure e.g. AMB. The developed algorithm enables to identify AMB structure and obtain thermal resistance and capacitance of each layer. These results show that the developed algorithm enables the accurate extraction of transient thermal network model of power module packages.

3.5 Summary

This chapter developed the signal processing algorithm to identify the accurate transient thermal network model for power module packages. Measurement noise was eliminated in the logarithmic frequency domain after weighted discrete Fourier transformation. And this chapter evaluated the influence of quantization error and noise in the measured data using the developed algorithm. The high sampling frequency of ADC could suppress the influence of quantization error. Low-pass filtering in frequency domain using the developed algorithm eliminated the influence of measurement noise compared to the conventional algorithm. The transient thermal network models obtained by the developed algorithm for TO-247 discrete power device package and AMB substrate of power module package were easily extracted from the structure function. The developed signal processing algorithm enables to distinguish the boundaries of multi-layered substrate for power module in the structure function, and improved the accuracy of the identified transient thermal network model.



(a) Discrete package (C4D20120A).



(b) Studied power module (S6305).

Figure 3.14 Structure function.

Chapter 4

Dynamic junction temperature estimation method for SiC MOSFET

4.1 Introduction

The transient thermal resistance measurement standard using static test method utilizes the temperature dependency in $I-V$ characteristics of power devices to estimate the junction temperature (T_{J}). SiC MOSFET has still concern about the dynamic gate threshold voltage shift due to the trap in the oxide/semiconductor interface, which violates the estimated time response of T_{J}. This chapter proposes an accurate transient T_{J} estimation procedure for SiC MOSFETs with advancing the static test method, and validates the estimated temperature with temperature sense diode (TSD) embedded in SiC MOSFET. In addition, section 4.3 evaluates the time response of T_{J} for the developed SWITCH-MOS without the proposed measurement method.

4.2 Evaluation of modified junction temperature estimation method for SiC MOSFET

4.2.1 Dynamic thermal characterization setup for MOSFET

The standardized static test method measures T_J in cooling operation from thermal equilibrium condition of self heating. Thermal sensitive electrical parameter of MOSFET is used for in-situ measurement of T_J. This section evaluates the influence of the dynamic gate threshold voltage shift of SiC MOSFET on transient T_J estimation for the following 4 mode characterization setup. Mode 1, 2 and 3 are subjected to the conventional static test method. Mode 4 is the proposed method, which expands Mode 2.

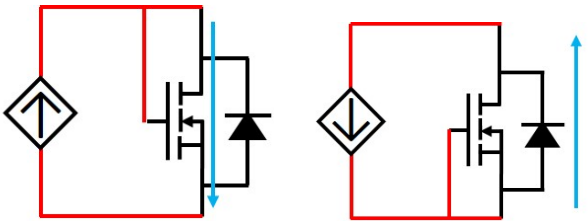
Mode 1: MOS-diode mode: Fig. 4.1(a).
Shunt gate and drain terminal ($V_{gs} = V_{ds}$).

Mode 2: Body-diode mode (GS-short): Fig. 4.1(b).
Shunt gate and source terminal ($V_{gs} = 0$).

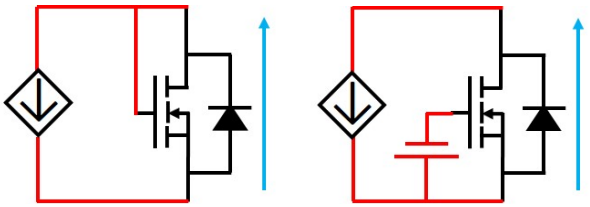
Mode 3: Body-diode mode (GD-short): Fig. 4.1(c).
Shunt gate and drain terminal ($V_{gs} = V_{ds}$).

Mode 4: Body-diode mode (with negative bias V_{gs} application): Fig. 4.1(d).
A constant negative bias voltage is applied across gate and source terminal (V_{gs}) by external voltage supply.

The both large current for self heating and small current for measurement flows in the direction of arrows in the Fig. 4.1. Mode 1 estimates T_J from the measured gate threshold voltage with flowing a constant small forward current. Mode 2, 3 and 4 estimate T_J from the measured knee voltage of body diode with flowing a constant small reverse current through body diode. The measurement current is set small enough to neglect self heating effect.

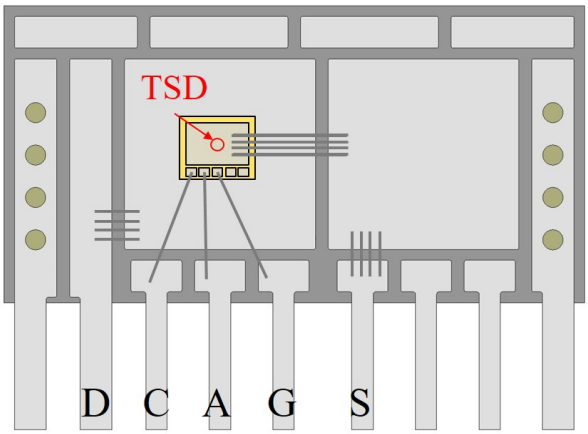


(a) Mode 1. (b) Mode 2.

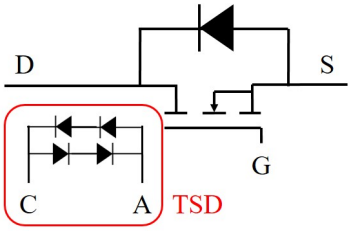


(c) Mode 3. (d) Mode 4.

Figure 4.1 Thermal characterization setup of MOSFET.



(a) Studied module configuration.



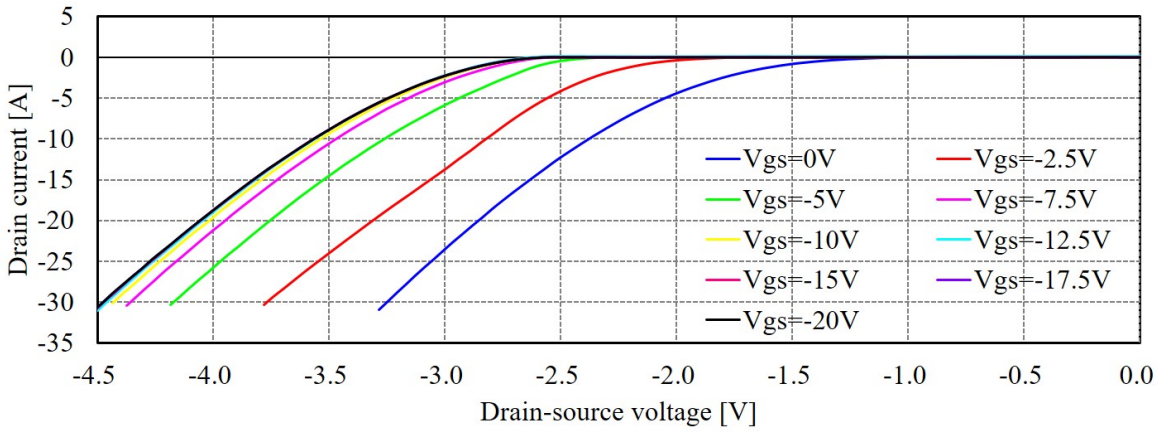
(b) Equivalent circuit of SiC MOSFET with TSD.

Figure 4.2 Studied SiC MOSFET.

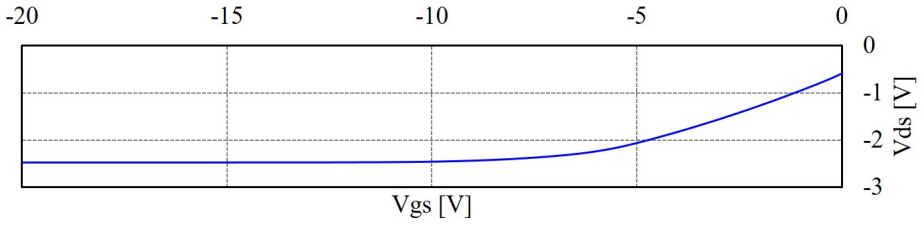
4.2.2 Studied power module

Fig. 4.2 illustrates the overview of studied SiC MOSFET module. TSD is embedded in the top of SiC MOSFET to estimate device temperature. G, D and S denote gate, drain and source terminal of SiC MOSFET, respectively. A and C denote anode and cathode terminal of TSD, respectively. This SiC MOSFET die is attached on the developed multi-layered ceramic substrate A as shown in Fig. 2.10.

$I-V$ characteristics of body diode in studied SiC MOSFET at room temperature is shown in Fig. 4.3. $I_{\mathrm{d}}-V_{\mathrm{sd}}$ characteristics does not change when the gate bias voltage V_{gs} is lower than -12.5 V, because current path through body diode is fixed for a large negative gate bias voltage. -18 V bias voltage is applied in Mode 4 by battery as isolated voltage supply.



(a) I_{d}-V_{sd} characteristics.



(b) V_{ds}-V_{gs} characteristics for a fixed 5mA current.

Figure 4.3 $I-V$ characteristics of studied SiC MOSFET at room temperature.

The voltage across drain and source terminal of MOSFET for each measurement mode and TSD for a fixed small current (5 mA) to the temperature are shown in Fig. 4.4 and Table 4.1.

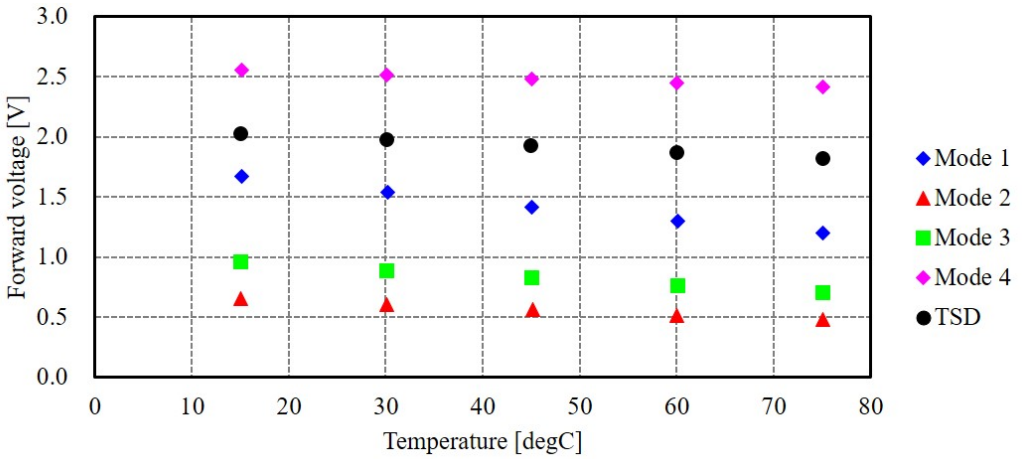


Figure 4.4 K factor.

Table 4.1 K factor for each mode and device

Mode	K factor [mV/K]
1	-7.933
2	-3.004
3	-4.202
4	-2.286
5	-3.449

4.2.3 Evaluation of estimated time response of junction temperature with TSD

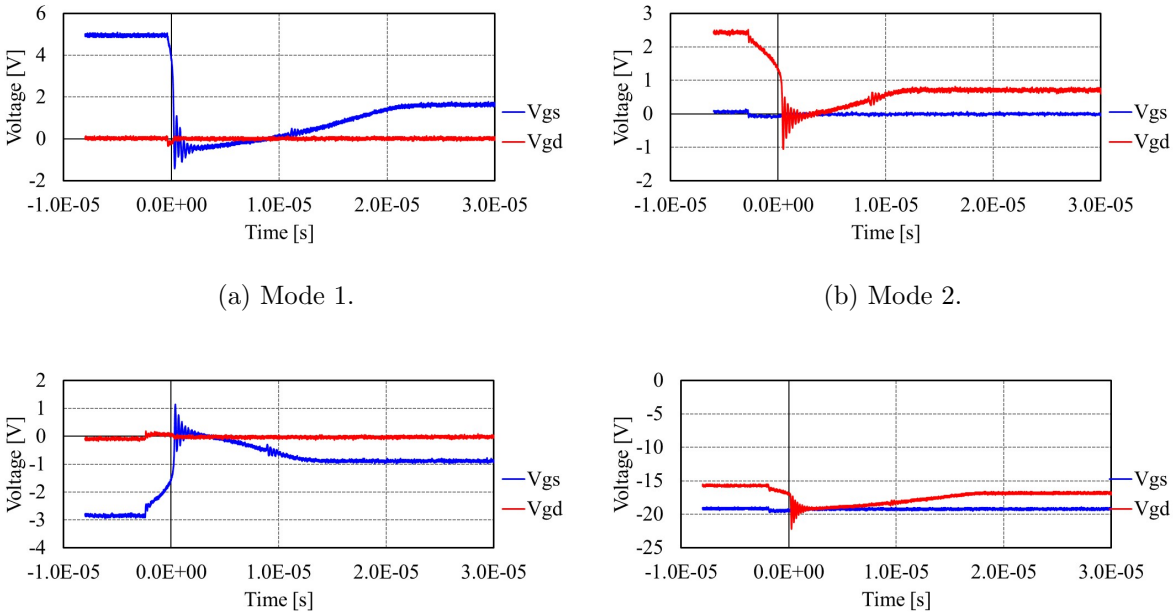
Fig. 4.5 shows V_{gs} and V_{gd} time response in switching transient from heating to cooling for each measurement mode. Here, this is experimentally obtained by oscilloscope DPO4104B (Tektronix) with differential voltage probes. The estimated time response of T_J for each measurement mode in cooling operation of SiC MOSFET after 300 sec heating is shown as semi-log plot in Fig. 4.6. Time response of voltage for a small constant current measured as T_J with T3Ster (MentorGraphics). The estimated temperature with MOSFET and TSD are given as solid and dashed line, respectively. Measurement current is 5mA, and heating power P_{in} is shown in Fig. 4.6.

Fig. 4.6(a) shows the estimated time response of T_J for MOSFET in Mode 1, which does not correspond with that for TSD in the entire measurement period. Moreover, the

initial rise of estimated T_{J} in cooling operation is observed. This temperature response is inconsistent with physical phenomenon, and can be attributed to the influence of the dynamic gate threshold voltage shift in SiC MOSFET by large V_{gs} change for switching a large heating drain current to a small measurement current as shown in Fig. 4.5(a) [55]. The temperature difference converges in a several days. Mode 1 does not give the accurate time response estimation of T_{J} for SiC MOSFET.

Figs. 4.6(b) and 4.6(c) show the estimated time response of T_{J} in Mode 2 and 3. These modes also show the initial rise of estimated T_{J}. The gate bias voltage from heating to cooling operation is shown in Figs. 4.5(b) and 4.5(c), and this induces the dynamic gate threshold voltage shift. The estimated T_{J} does not coincide with T_{J} for TSD in the measurement time scale. In Mode 2 and 3, the negative gate bias voltage applied by voltage drop with heating and measurement drain current is insufficient to fix $I - V$ characteristics of body diode in Fig. 4.3.

Fig. 4.6(d) shows the estimated time response of T_{J} in Mode 4. The influence of the dynamic gate threshold voltage shift is not observed for the monotonic temperature fall. Fig. 4.5(d) shows V_{gs} and V_{gd} response in switching transient. The influence of the gate threshold voltage shift does not occur. Because V_{gs} and V_{gd} kept lower than -12.5 V in the entire time scale, where $I - V$ characteristics of body diode is fixed. The estimated time response of T_{J} for MOSFET is almost consistent with the estimated time response of T_{J} for TSD. TSD temperature does not completely correspond with T_{J} of SiC MOSFET during fast transient for several msec. TSD embedded in MOSFET is not located in the same position of PN junction of body diode in MOSFET. TSD temperature is consistent with T_{J} of MOSFET in thermal equilibrium condition for start and end of cooling operation and expected to be close to the "true" T_{J} of MOSFET during transient condition. The gate bias voltage in Mode 4 is large enough to fix $I - V$ characteristics of body diode in Fig. 4.3, and the proposed method is useful in estimating T_{J} for SiC MOSFET.



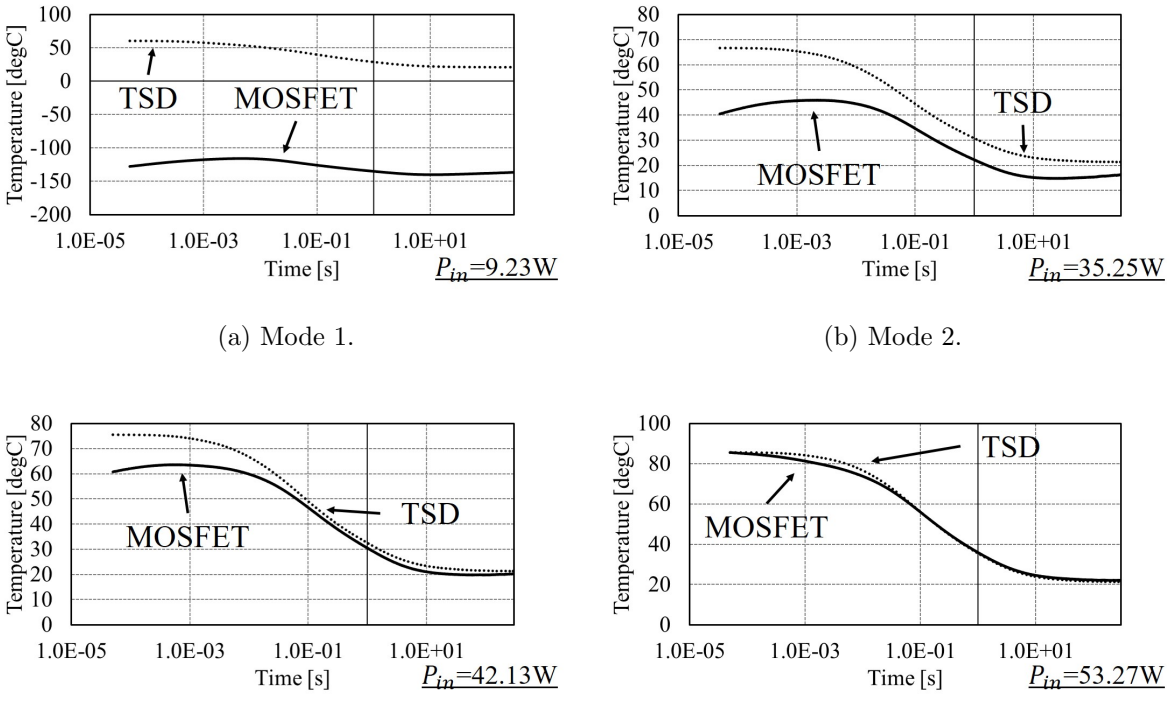
(a) Mode 1.

(b) Mode 2.

(c) Mode 3.

(d) Mode 4.

Figure 4.5 V_{gs} and V_{gd} waveform in switching heating to cooling operation.



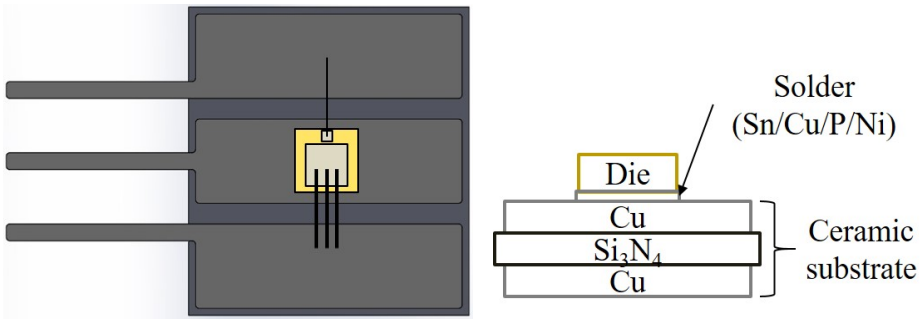
(a) Mode 1.

(b) Mode 2.

(c) Mode 3.

(d) Mode 4.

Figure 4.6 Temperature response of MOSFET and TSD for each measurement mode.



(a) Placement of studied module. (b) Cross section.

Figure 4.7 Studied power module.

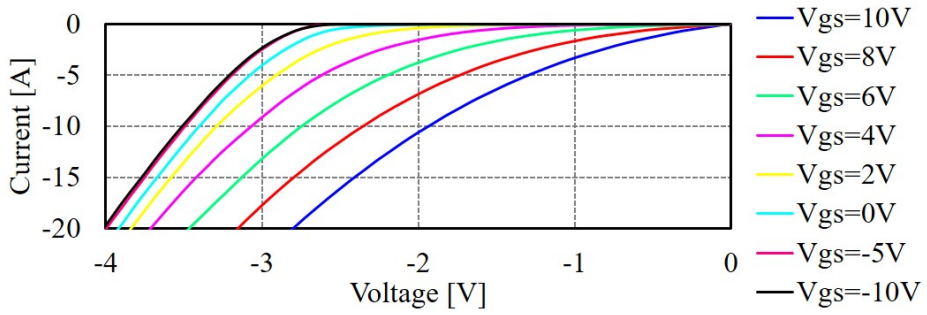
4.3 Junction temperature estimation for SWITCH-MOS

4.3.1 Studied SWITCH-MOS and measurement setup

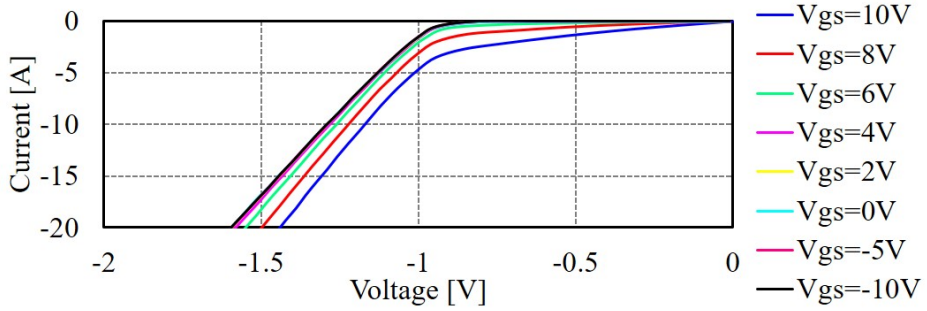
Three types of SiC MOSFET modules are evaluated in this section: Module A) the conventional trench gate SiC MOSFET, Module B) the conventional trench gate SiC MOSFET and external SBD, and Module C) SWITCH-MOS. The rated gate voltage of the conventional SiC MOSFET used for Module A and B is +20 V/−3 V, and that of SWITCH-MOS is +20 V/−5 V. The overview of each studied module is shown in Fig. 4.7. In Module B, the external free wheeling SBD is located on next to the center MOSFET.

Fig. 4.8 shows $I_d - V_{sd}$ characteristic of each studied module for reverse conduction at room temperature. The knee voltage of body diode in the conventional SiC MOSFET (Module A) changes with V_{gs}. $I_d - V_{sd}$ characteristic of Module A does not change when $V_{gs} < -5$ V, because current path through body diode is fixed for a large negative gate bias voltage. The knee voltage of reverse conduction in the conventional SiC MOSFET with SBD (Module B) V_{ds}=−0.9 V does not change for V_{gs} <2 V. Most of the reverse current flow through external SBD, and partially through body diode of SiC MOSFET. The knee voltage of SWITCH-MOS (Module C) V_{ds}=−1.2 V does not change for V_{gs} <6 V. Almost all reverse current in SWITCH-MOS flow through built-in SBD and is not affected by the applied V_{gs} when channel is not formulated.

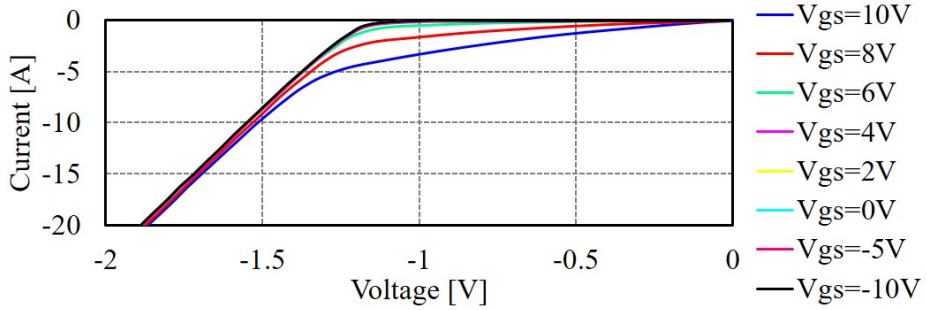
Dynamic thermal resistance measurement setup for MOSFET is already explained



(a) Module A.



(b) Module B.



(c) Module C.

Figure 4.8 I_{d}-V_{sd} characteristic of each studied modules for reverse conduction at room temperature.

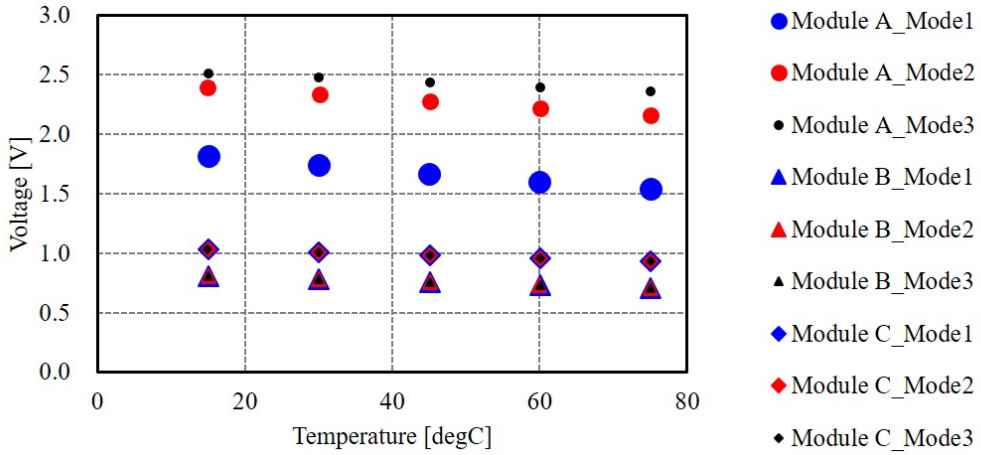
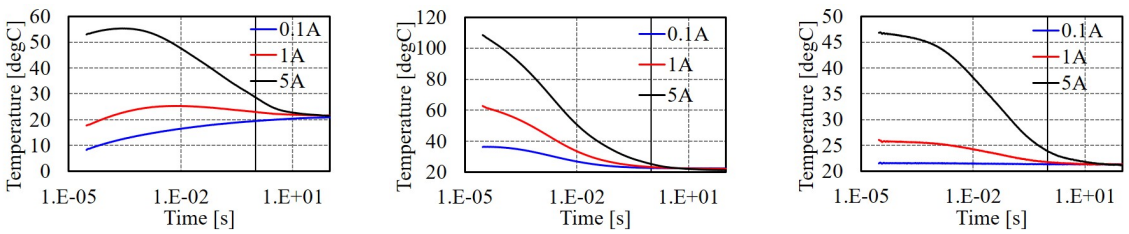


Figure 4.9 K factor.

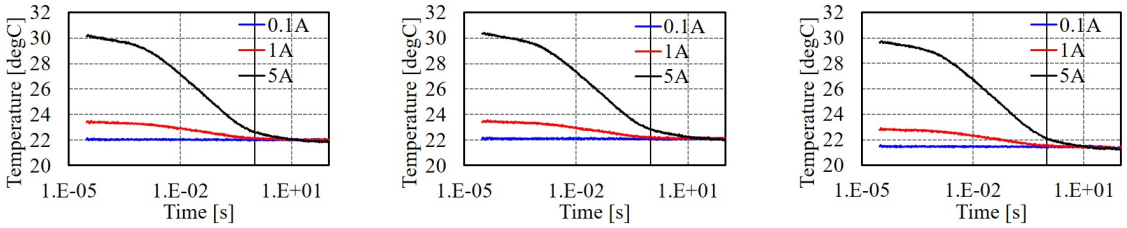
in section 4.2.1. Forward conduction characteristic does not change regardless of built-in SBD, and the dynamic gate threshold voltage shift occurs even for SWITCH-MOS in T_J estimation with the gate threshold voltage. Therefore, this chapter evaluates the influence of the dynamic gate threshold voltage shift of each SiC MOSFET on transient T_J measurement for Mode 2 to 4 with knee voltage of body diode/built-in SBD. −9 V bias voltage is applied in Mode 4 by battery as isolated voltage supply. Fig. 4.9 shows K factor of each studied module for a fixed 5 mA measurement current. K factor of Module B and C coincide in each measurement mode, and overlapped in the figure. This is because $I_\mathrm{d} - V_\mathrm{sd}$ characteristic does not depend on V_gs <0 V.

4.3.2 Comparative evaluation of estimated time response of junction temperature



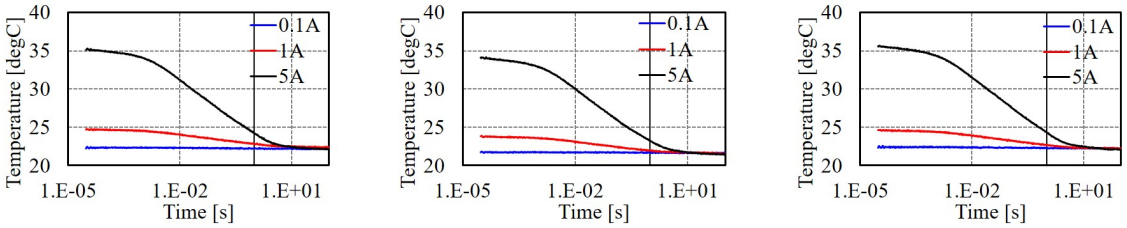
(a) Mode 2. (b) Mode 3. (c) Mode 4.

Figure 4.10 Time response of estimated T_J for Module A.



(a) Mode 2. (b) Mode 3. (c) Mode 4.

Figure 4.11 Time response of estimated T_J for Module B.



(a) Mode 2. (b) Mode 3. (c) Mode 4.

Figure 4.12 Time response of estimated T_J for Module C.

Figs. 4.10 to 4.12 show the estimated time response of T_J for Module A to C, respectively for measurement Mode 2 to 4. The heating current shown in the legend is used as the parameter for thermal equilibrium temperature. Fig. 4.13 is photograph and thermal images of each module at thermal equilibrium condition for a 5 A heating current. The red part of the image is high temperature point, which is the place where the power device is heated.

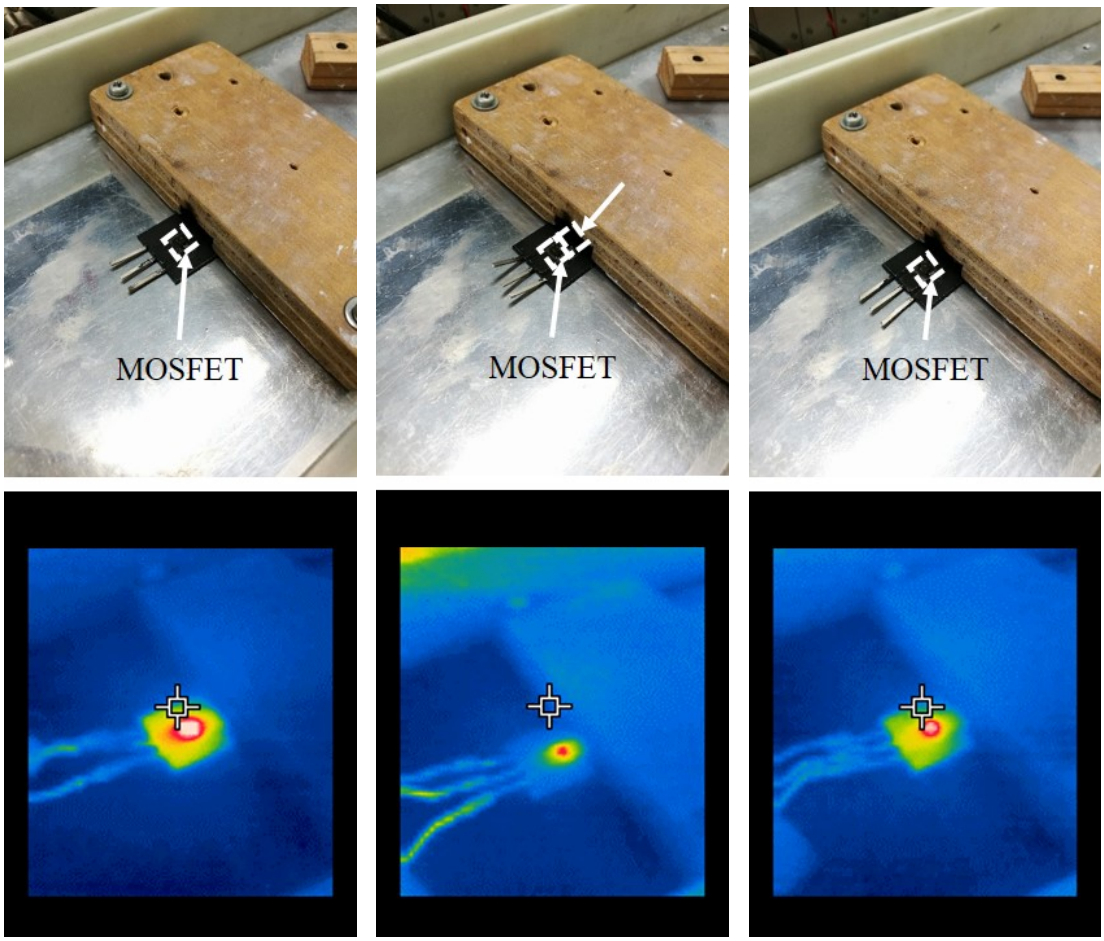
The initial elevation of the estimated T_J in Fig. 4.10(a) is observed for all heating current on Module A. This is inconsistent with the physical phenomenon, and can be attributed to the influence of the dynamic gate threshold voltage shift in SiC MOSFET. The voltage across gate-source changes with switching from a large heating drain current to a small measurement current. Though the initial temperature elevation is not observed in Fig. 4.10(b), but it seems that the estimated temperature rise due to the dynamic gate threshold voltage shift is smaller than the temperature fall due to cooling in power device. The negative gate bias voltage obscures the dynamic threshold voltage shift in T_J estimation for the trench gate SiC MOSFET shown in Fig. 4.10(c).

The monotonic decrease of the estimated T_J is observed irrespective of heating current as shown in Figs. 4.11 and 4.12. This result shows that the dynamic gate

threshold voltage shift does not influence on the estimated time response of T_{J} in Module B and C. But Module B does not characterize SiC MOSFET itself, because the reverse current flows through external free wheeling SBD, not through the body diode of SiC MOSFET. The heating area in Fig. 4.13(b) is next to center compared to others, where the external free wheeling SBD is mounted. The developed SWITCH-MOS (Module C), which embeds SBD in the trench gate SiC MOSFET, can estimate the accurate time response of T_{J} due to the reverse current flowing through built-in SBD on SiC MOSFET. This structure enables to evaluate transient thermal characteristics of SiC MOSFET in power modules.

4.4 Summary

This chapter proposed the T_{J} estimation method for SiC MOSFET in transient thermal characterization with expanding the static test method. The error of estimated temperature with the gate threshold voltage and knee voltage of body diode in SiC MOSFET for the conventional method was evaluated with the temperature from embedded TSD. The dynamic gate threshold voltage shift of SiC MOSFET violates T_{J} estimation. The proposed negative gate bias voltage application estimated the accurate time response of T_{J} for SiC MOSFET. This enabled to extract transient thermal resistance of power module with SiC MOSFET. And the time response of T_{J} for the developed trench gate SiC MOSFET with built-in SBD (SWITCH-MOS) was also estimated. $I_{\mathrm{d}} - V_{\mathrm{sd}}$ characteristic of SWITCH-MOS in the reverse conduction did not depend on V_{gs} because the reverse current flows through built-in SBD. As the result, an accurate time response of T_{J} can be estimated for SWITCH-MOS without clamping negative bias V_{gs}.



(a) Module A. (b) Module B. (c) Module C.

Figure 4.13 Thermal image at thermal equilibrium condition.

Chapter 5

Thermal design evaluation of SiC power module substrate

5.1 Introduction

Thermal management of SiC power modules is important for the reliable and safe operation of power conversion systems. As mentioned in previous chapters, heat spreading and transferring mainly depend on the structure and material property of power module constitutions. This chapter evaluates the thermal design of power module substrates with a single chip for a variety of structure and material constitutions using the transient thermal network model. In addition, finite volume method (FVM) simulation is performed to evaluate the validity of obtained transient thermal characteristics. Section 5.2 briefly explains the procedure of numerical simulation with FVM and defines typical simulation model for characterizing transient thermal network model of power module packages. Section 5.3 experimentally evaluates transient thermal characteristics of power module substrate for different die size, die attach material, and thickness of each structure for basic active metal bonding (AMB) structure. Transient thermal characteristics of the developed multi-layered ceramic substrate using the developed transient thermal network model identification algorithm is evaluated in section 5.4.

5.2 Numerical modeling for transient thermal characterization of power module package

Power module design requires an accurate model to coincide with the actual electrical and thermal behavior of power modules. Numerical simulation is a major tool for analyzing and designing electrical, thermal, and mechanical characteristics of power modules, which enables to provide high precision analysis for these characteristics [89] [90]. In the following chapter, finite volume method (FVM) with FloEFD (Mentor-Graphics) is performed to validate transient thermal characteristics of the experimental result.

We assume the following variables in Cartesian coordinate system (x, y, z) with time t to thermal fluid dynamics.

- u, v, w: Velocity for the direction x, y, z
- p: Pressure
- T: Temperature of fluid and/or solid

For these variables, we define the following governing equations of fluid dynamics.

- Velocity: momentum conservation at each direction
- Pressure: equation of continuity $\simeq$ mass conservation equation
- Temperature: heat equation

Next, we define analysis mesh named as control volume to solve these differential equations. Each control volume, which is discretizing the objected model by finite rectangular cell, conserves the solved value of each equation. For example, temperature T in a cell can be calculated with 6 cell around a objected cell T_i ($i = 1, 2, ..., 6$) and the temperature at old time step T_0.

$$T = \frac{C_0T_0 + C_1T_1 + C_2T_2 + C_3T_3 + C_4T_4 + C_5T_5 + C_6T_6 + S}{C_0 + C_1 + C_2 + C_3 + C_4 + C_5 + C_6}. \tag{5.1}$$

Here, C is a constant which related to the status next to a objected cell, and S is a constant related to the boundary condition. In practical, these calculation repeat for each cell in each time step.

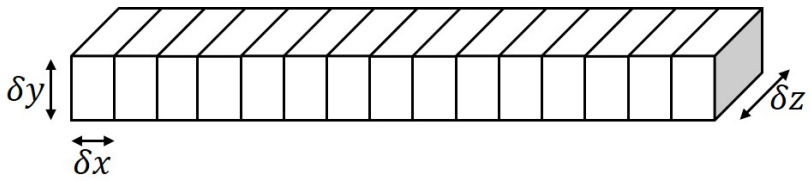


Figure 5.1 Uniform one-dimensional unsteady fluid path to the direction x.

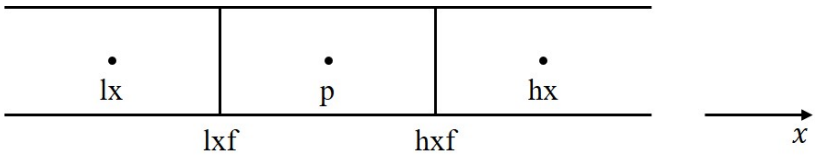


Figure 5.2 Terms of each cell index.

5.2.1 Finite volume equation

To simplify the problem, we consider the one-dimensional cell at unsteady state to the direction x. Then, differential type finite volume equations are given as follows:

$$\frac{\partial \rho}{\partial t} + \frac{\partial (\rho u)}{\partial x} = 0, \tag{5.2}$$

$$\frac{\partial \rho C_{\mathrm{p}} T}{\partial t} + \frac{\partial (\rho u C_{\mathrm{p}} T)}{\partial x} - \frac{\partial}{\partial x}\left(\lambda \frac{\partial T}{\partial x}\right) = S. \tag{5.3}$$

Here, ρ is the density of fluid, and index "p" denotes the objected control volume at current time step as illustrated in Fig. 5.2. Eq. (5.2) and (5.3) are the continuity and temperature equation, respectively. Finite volume equation is finally given as follow by integrating each equation at each cell. Here, cell volume at the objected control volume is $V_{\mathrm{p}} = \delta x \delta y \delta z$ and boundary area at x direction: $A_x = \delta y \delta z$.

Integrating Eq. (5.2) gives the following equations:

$$\iiint \frac{\partial \rho}{\partial t} dx dy dz = \left(\frac{\rho_{\mathrm{p}} - \rho_{\mathrm{t}}}{\partial t}\right) \delta x \delta y \delta z = \left(\frac{\rho_p - \rho_{\mathrm{t}}}{\delta t}\right) V_{\mathrm{p}}, \tag{5.4}$$

$$\begin{aligned} \iiint \frac{\partial (\rho u)}{\partial x} dx dy dz &= \iint [(\rho u)_{\mathrm{hxf}} - (\rho u)_{\mathrm{lxf}}] dy dz \\ &= (\rho u)_{\mathrm{hxf}} \delta y \delta z - (\rho u)_{\mathrm{lxf}} \delta y \delta z = (\rho u)_{\mathrm{hxf}} A_x - (\rho u)_{\mathrm{lxf}} A_x. \end{aligned} \tag{5.5}$$

Here, index "t" of Eq. (5.4) denotes the previous time step. And index "hxf" and "lxf" of Eq. (5.5) are boundary as illustrated in Fig. 5.2. Eqs. (5.4) and (5.5) give mass flow rate and net fluid flow at the objected control volume, respectively. Finally we obtain

$$\left(\frac{\rho_{\mathrm{p}}-\rho_{\mathrm{t}}}{\delta t}\right)V_{\mathrm{p}}+(\rho u)_{\mathrm{hxf}}A_x-(\rho u)_{\mathrm{lxf}}A_x=0. \tag{5.6}$$

Especially in steady state and uniform material, 1st left term of Eq. (5.6) is zero and thus net fluid is zero.

Integrating Eq. (5.3) yields the following equations about temperature:

- Unsteady term: increase rate of heat capacitance at the objected control volume

$$\iiint\frac{\partial(\rho C_{\mathrm{p}}T)}{\partial t}dxdydz=\left(\frac{(\rho C_{\mathrm{p}}T)_{\mathrm{p}}-(\rho C_{\mathrm{p}}T)_{\mathrm{t}}}{\partial t}\right)V_{\mathrm{p}}. \tag{5.7}$$

- Convection term: net heat convection

$$\begin{aligned}\iiint\frac{\partial(\rho u C_{\mathrm{p}}T)}{\partial x}dxdydz &= \iint[(\rho u C_{\mathrm{p}}T)_{\mathrm{hxf}}-(\rho u C_{\mathrm{p}}T)_{\mathrm{lxf}}]dydz,\\ &= [(\rho u C_{\mathrm{p}}T)_{\mathrm{hxf}}A_x-(\rho u C_{\mathrm{p}}T)_{\mathrm{lxf}}A_x], \qquad (5.8)\\ &= [\rho_{\mathrm{p}}C_{\mathrm{p}}u_{\mathrm{hxf}}T_{\mathrm{p}}A_x-\rho_{\mathrm{lx}}C_{\mathrm{p}}u_{\mathrm{lxf}}T_{\mathrm{lx}}A_x]. \qquad (5.9)\\ (\because u\geq 0 &\rightarrow T_{\mathrm{hxf}}=T_{\mathrm{p}},T_{\mathrm{lxf}}=T_{\mathrm{lx}},\rho_{\mathrm{hxf}}=\rho_{\mathrm{p}},\rho_{\mathrm{lxf}}=\rho_{\mathrm{lx}})\end{aligned}$$

- Heat conduction term: net heat conduction

$$\begin{aligned}\iiint\frac{-\partial}{\partial x}\lambda\left(\frac{\partial T}{\partial x}\right)dxdydz &= -\iint\left[\lambda\left(\frac{\partial T}{\partial y}\right)_{\mathrm{hxf}}-\lambda\left(\frac{\partial T}{\partial y}\right)_{\mathrm{lxf}}\right]dydz,\\ &= -\left[\lambda\left(\frac{T_{\mathrm{hx}}-T_{\mathrm{p}}}{\delta x}\right)-\lambda\left(\frac{T_{\mathrm{p}}-T_{\mathrm{lx}}}{\delta x}\right)\right]A_x \qquad (5.10)\end{aligned}$$

- Heat source term: net heat transfer

$$\iiint Sdxdydz = S_pV_{\mathrm{p}}. \tag{5.11}$$

And then, we obtain

$$\begin{aligned}T_{\mathrm{p}}\left[\frac{\rho_{\mathrm{p}}C_{\mathrm{p}}V_{\mathrm{p}}}{\delta t}+\rho_{\mathrm{p}}C_{\mathrm{p}}u_{\mathrm{hxf}}A_x+\frac{\lambda A_x}{\delta x}\right] &- \left[\frac{\rho_{\mathrm{p}}C_{\mathrm{p}}V_{\mathrm{p}}T_{\mathrm{t}}}{\delta t}+\left(\rho_{\mathrm{lx}}C_{\mathrm{p}}u_{\mathrm{lxf}}A_x+\frac{\lambda A_x}{\delta x}T_{\mathrm{lx}}\right)+\frac{\lambda A_x}{\delta x}T_{\mathrm{hx}}\right]\\ &= S, \qquad (5.12)\\ \Leftrightarrow a_{\mathrm{p}}T_{\mathrm{p}} &= a_{\mathrm{t}}T_{\mathrm{t}}+a_{\mathrm{lx}}T_{\mathrm{lx}}+a_{\mathrm{hx}}T_{\mathrm{hx}}+S. \qquad (5.13)\end{aligned}$$

5.2.2 Simulation model

Fig. 5.3 shows the simplified cross-sectional structure of Schottky barrier diode (SBD) and the example of actual SiC SBD bare die. This simplified model consists of Al electrode, drift layer and substrate as shown in Fig. 5.3(a). In general, bare die has guard ring to make the electrical field distribution in power device uniform, and to prevent breakdown by the electrical field concentration. Thus the effective area is in the guard ring as shown in Fig. 5.3(b). Electrode thickness t_{ele} is 5 μm to 10 μm, and drift layer thickness t_{drift} is 10 μm to 20 μm. Assuming that the heat is generated in Schottky junction and drift layer in uniform, the size of heating volume called "active area" is 2.5 mm×2.5 mm×20 μm for 3 mm×3 mm device.

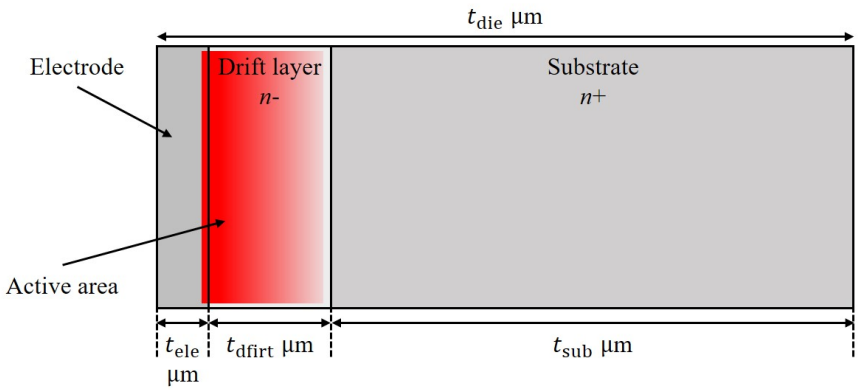
The typical CAD model to simulate transient thermal characteristics for a SiC power module with active metal bonding (AMB) structure is shown in Fig. 5.4. Active area is located into die and dissipated heat is set in uniform. Table 5.1 shows the physical properties of each material in model at room temperature. SiC has thermal isotropic in thermal conductivity at *c*-axis [91] [92]. Temperature dependency of the specific heat and thermal conductivity are shown in Fig. 5.5.

5.3 Parametric study of transient thermal characteristics for SiC power module

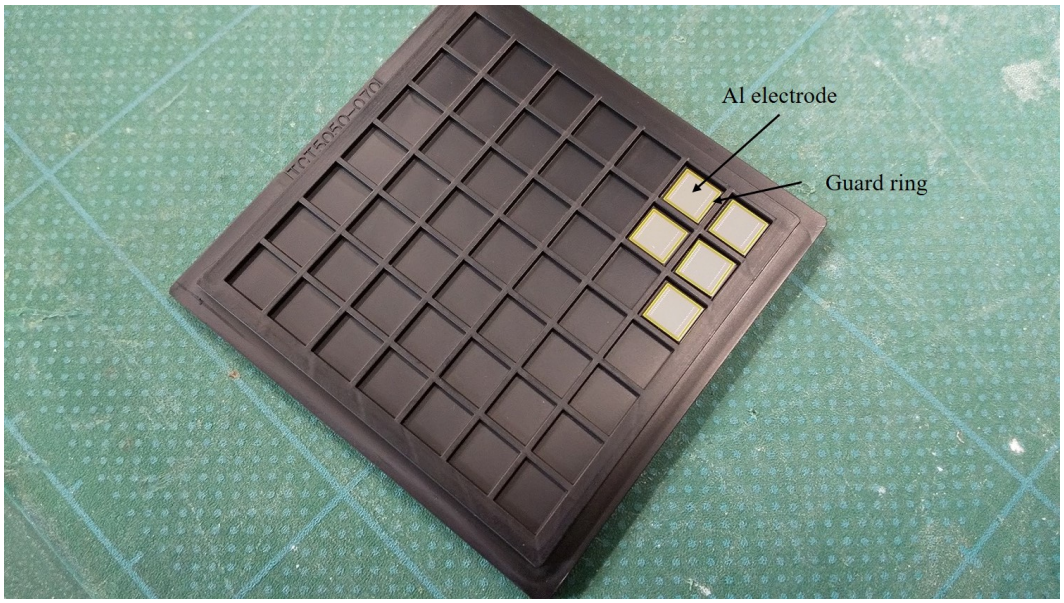
5.3.1 Studied power module constitution

Fig. 5.6 is the basic structure of AMB substrate for power module studied in this section. SiC SBD is mounted on the center of AMB substrate as a heat source to evaluate transient thermal characteristics of power module substrate. ϕ200 μm Al wires as Anode and Kelvin sense. Die and baseplate are attached to AMB substrate with 50 μm AuGe solder in same reflow process. AMB substrate and baseplate are Au plated.

This section focuses on the following structural features of AMB substrate: die thickness t_{die}, die dimension d_{die}, die attach material, Cu thickness t_{Cu}, and baseplate material. Table 5.2 lists each combination of AMB substrate constitution. SiC SBD



(a) Cross-section structure of SBD for thermal modeling.



(b) Actual SBD bare die (S6305).

Figure 5.3 Basic specification of studied power module.

Table 5.1 Physical properties of typical materials at room temperature

Material	λ [W/m/K]	c [J/g/K]	ρ [g/cm^3]
SiC //(0001)	495	680	3240
SiC $\perp$(0001)	296	680	3240
AuGe	42	151	14700
Sn/Ag/Cu	55	231	7400
Sintered Cu	180	-	-
Sintered Ag	200	-	-
Sn/Cu/Ni/P	58	240	7300
Cu	401	384	8960
Al	237	902	2689
SUS304	16.7	590	7930
Si grease	0.84	800	2340

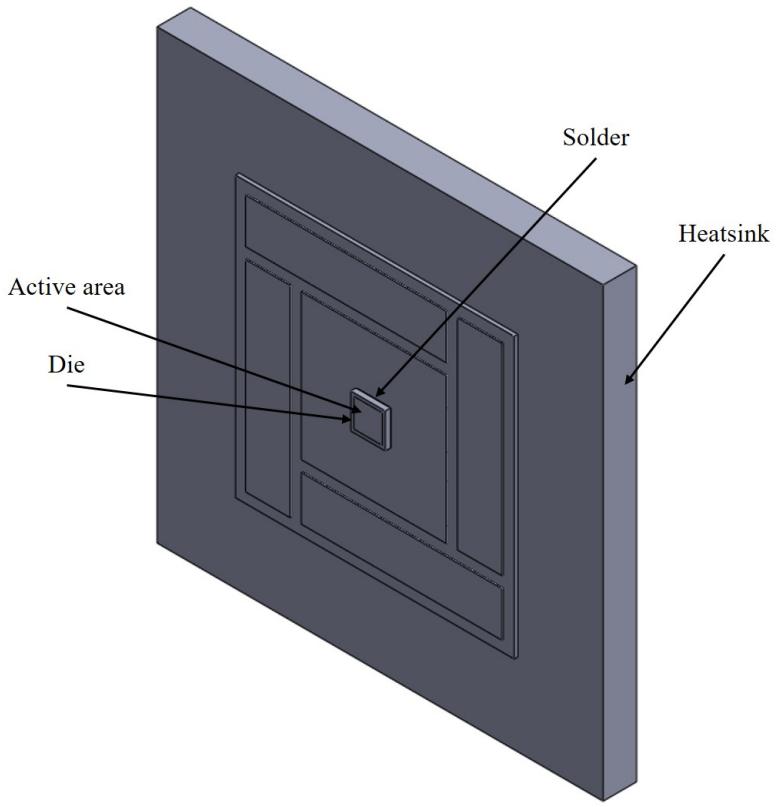


Figure 5.4 Typical simulation model for transient thermal characterization.

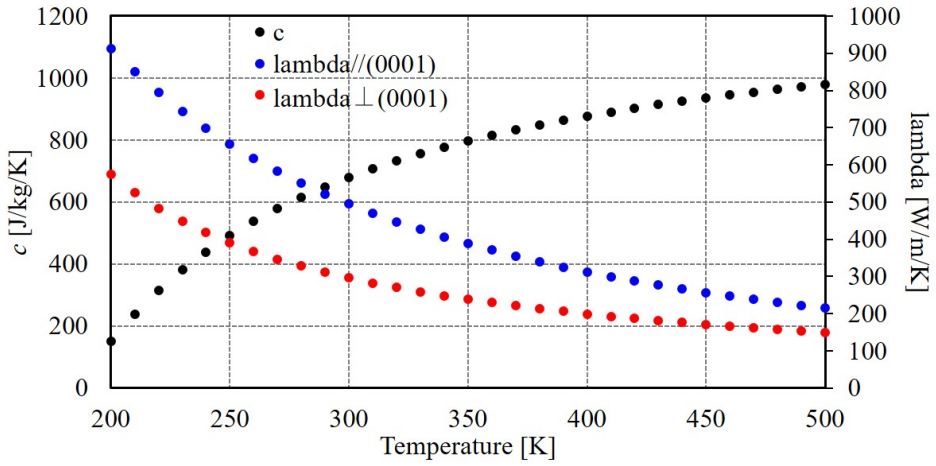
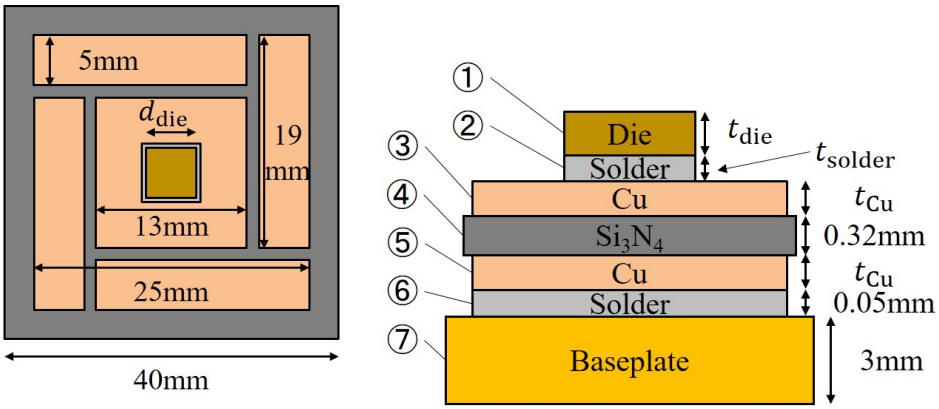
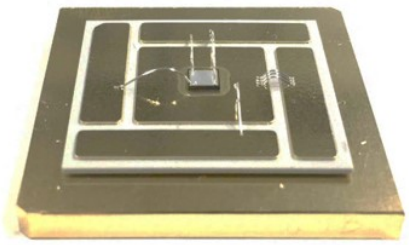


Figure 5.5 Temperature dependency of specific heat and thermal conductivity for SiC.



(a) Configuration.

(b) Cross-sectional structure.



(c) Photograph.

Figure 5.6 Basic specification of studied power module.

CPW4-1200-S020B (1200 V/20 A, 3.08 mm/3.08 mm/380 μm, CREE) is used as the heat source for reference sample. Pattern and base Cu thickness is same to take into account for thermal stress in actual fabrication and use. Actual die attach thickness t_{solder} is measured using laser interferometer after soldered, and also listed in Table 5.2. Sample #1 is used as the reference material in this section, and variables are emphasized by red color in Table 5.2.

Typical K factors of studied power modules on each SiC SBD for a fixed 100mA measurement current are shown in Fig. 5.7. The slope of K factors are -1.556 mV/K, -1.422 mV/K and -1.536 mV/K for 3/3/0.38, 3/3/0.20 and 5/5/0.36, respectively.

Fig. 5.8 illustrates the identification procedure of transient thermal network model parameter from the obtained structure function. The thermal resistance of die is obtained from zero to 1st peak of differential structure function. The thermal resistance of die attach is obtained from 1st peak to 2nd peak of differential structure function. Because structure function is plotted as semi-log plot, the thermal resistance of AMB structure and baseplate can be exponentially approximated as follow:

$$y_1 = a_1 e^{b_1 x}, \tag{5.14}$$

$$y_2 = a_2 e^{b_2 x}. \tag{5.15}$$

Here a_1, a_2, b_1, and b_2 are coefficients. The thermal resistance of AMB with base attach is obtained from 2nd peak to cross-point of y_1 and y_2 X_{p}. The junction to case thermal resistance will be separated by thermal dual interface (TDI) method [54], thus thermal resistance of baseplate is obtained from X_{p} to TDI split.

5.3.2 Experimental evaluation of transient thermal network model

Fig. 5.9 shows that the thermal resistance of each layer for studied power modules, which is distinguished based on Fig. 5.8. Figs. 5.10 to 5.14 are the structure functions experimentally obtained by static test method using T3Ster (MentorGraphics). The reference sample #1 is given as the blue line in each figure. “Int” and “Dif” denotes the integral and differential structure function, given as solid and dashed line, respectively.

Table 5.2 Physical properties of WBG and conventional semiconductor materials

No.	t_{die} [mm]	d_{die} [mm]	Die attach	t_{Cu} [mm]	Baseplate	t_{solder} [μm]
#1	3 × 3	380	AuGe	0.1	Al	47
#2	3 × 3	200	AuGe	0.1	Al	47
#3	3 × 3	380	Sn/Ag/Cu	0.1	Al	47
#4	3 × 3	380	Cu sintering	0.1	Al	47
#5	3 × 3	380	Ag sintering	0.1	Al	47
#6	3 × 3	380	AuGe	0.2	Al	25
#7	3 × 3	380	AuGe	0.3	Al	37
#8	3 × 3	380	AuGe	0.1	Cu	33
#9	3 × 3	380	AuGe	0.1	SUS	45
#10	5 × 5	360	AuGe	0.1	Al	44
#11	5 × 5	360	AuGe	0.2	Al	39
#12	5 × 5	360	AuGe	0.3	Al	38

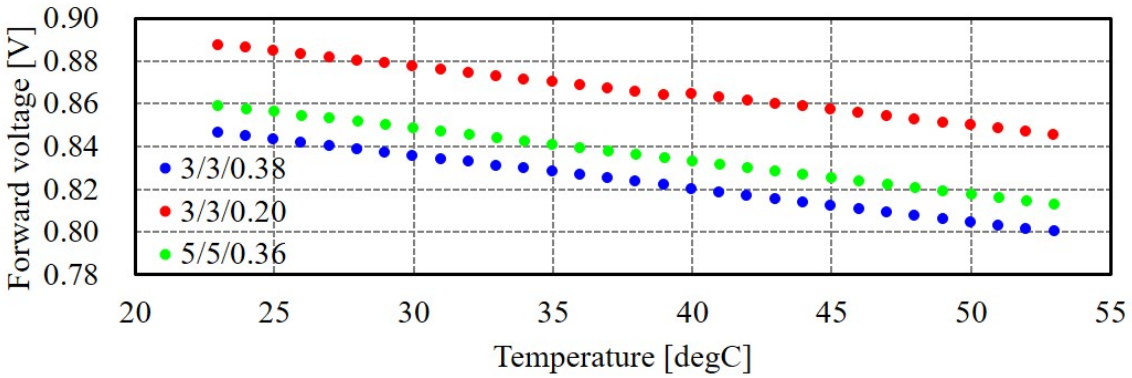


Figure 5.7 K factors of studied power module.

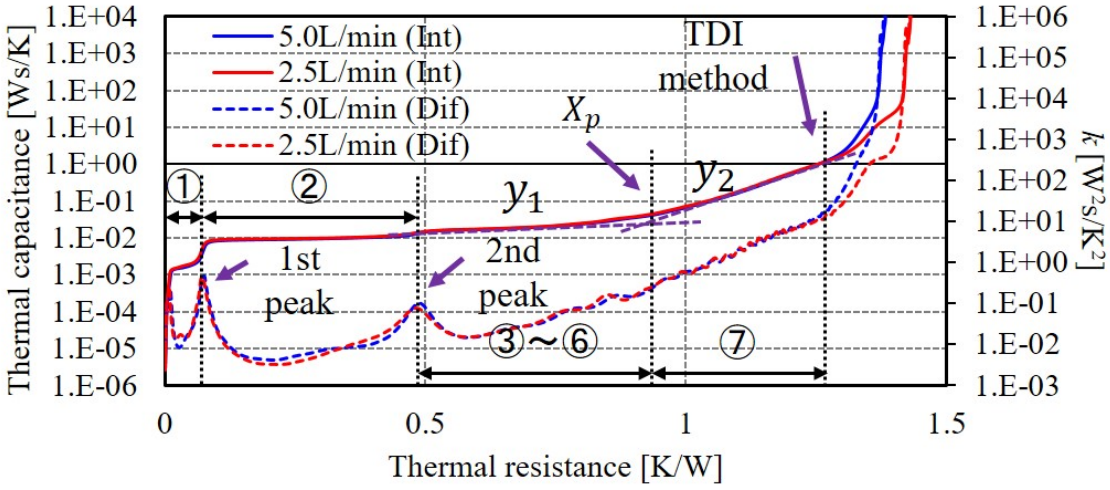


Figure 5.8 Identification procedure of transient thermal network model in this section.

The time response of T_J is obtained for 100 sec cooling transient after thermal equilibrium condition with the heating current 10 A. Fig. 5.15 is computed tomography (CT) images of die attach for each studied power module, which is obtained from back side of baseplate. Here, magenta square shows die size and green value means the ratio of void in the die attach layer. It is noted that CT images of #8 and #9 are not available because X-ray is not transmissive to the thick Cu and SUS baseplate.

The structure functions of sample #1 and #2 are shown in Fig. 5.10. The die thickness t_{die} is used as the parameter. The thermal resistance of die in #1 is smaller than #2, and the thermal capacitance of die in #1 is larger than that in #2. Though the thicker die gives the larger thermal resistance, but the measured result does not coincide with this assumption. This is because heating area of power device lies inside the guard ring, and heat spreading area becomes large as far from active area. This indicates that the die thickness t_{die} should be designed to lower the thermal resistance.

Fig. 5.11 shows the structure functions of sample #1, #3, #4, and #5. The die attach material is used as the parameter, whose thermal conductivity is shown in Ta-

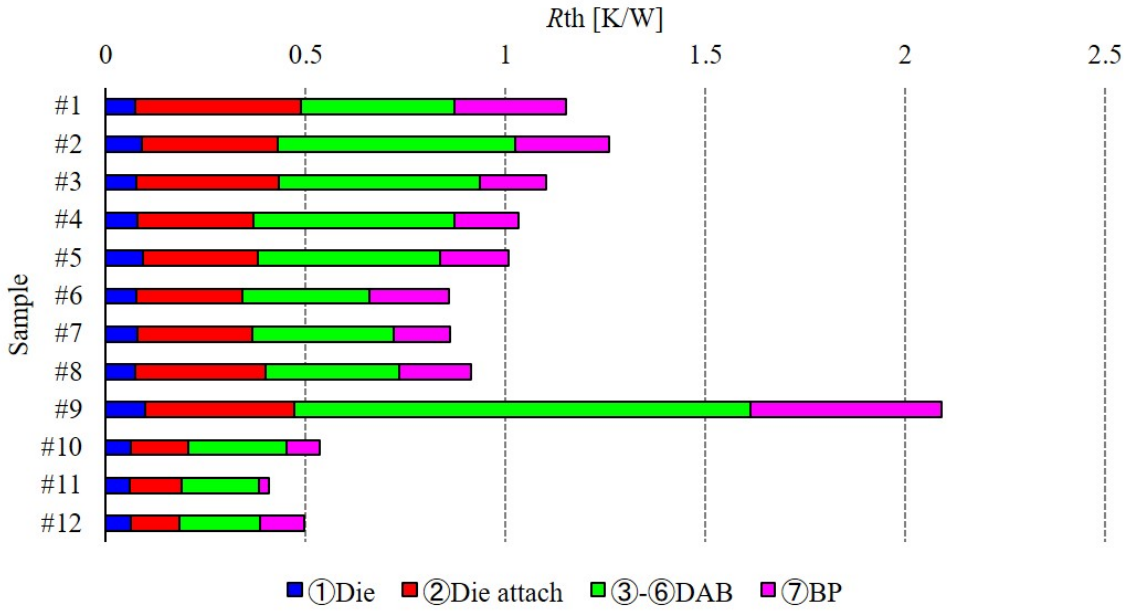


Figure 5.9 Thermal resistance of each layer for studied power module.

ble. 5.2. The thermal resistance of die attach $R_{\text{die attach}}$ is listed in Table 5.3. The higher thermal conductivity leads to the lower thermal resistance of die attach. However, the ratio of thermal resistance does not coincide with thermal conductivity, especially for sintered die attach. There is a few ratio of void for #4 and #5 as shown in Figs. 5.15(d) and 5.15(e). The thermal conductivity of sintered material listed in Table 5.2 shows the typical value in catalog, and its detail physical properties after sintered are not described. It is necessary to observe cross-sectional observation of die attach layer.

Table 5.3 Physical properties of WBG and conventional semiconductor materials

No.	$R_{\text{die attach}}$ [K/W]
#1	0.4128
#3	0.3558
#4	0.2887
#5	0.2870

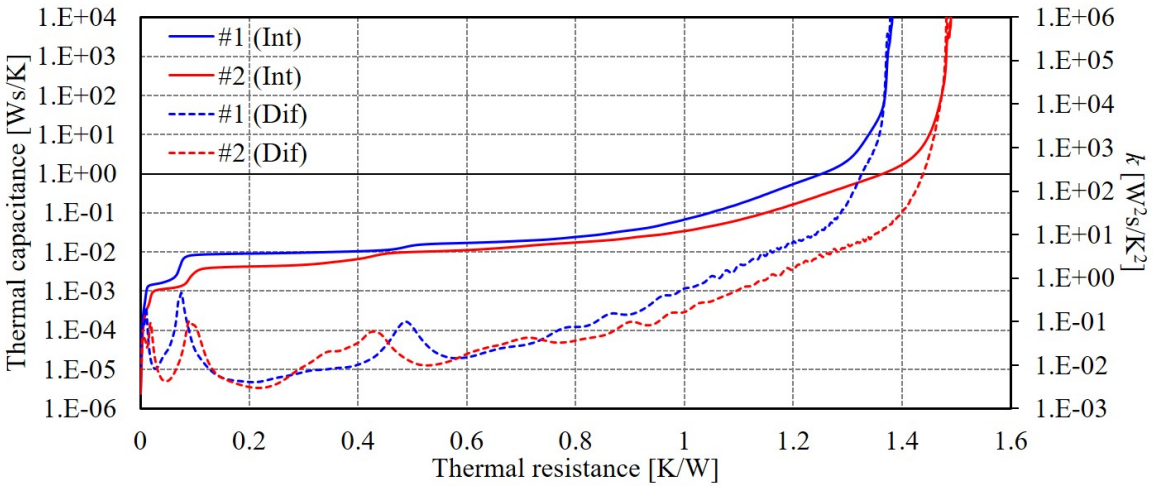


Figure 5.10 Structure function of sample #1 and #2.

Fig. 5.12 shows the structure function of sample #1, #6, and #7. The Cu thickness t_{Cu} is used as the parameter. Though the thermal resistance becomes larger as the thickness t is larger, but the thicker Cu thickness t_{Cu} induces the smaller thermal resistance. The thicker Cu layer spreads heat horizontally, which results in expanding heat spreading area and lower the thermal resistance. It is noted that the thermal resistance of #6 and #7 is almost same. The thickness of solder layer in #7 is 12 μm thicker than that of #6, and this increases the total thermal resistance of studied power module. Moreover, #7 has large void in die attach as shown in Fig. 5.15, which results in the larger thermal resistance.

Fig. 5.13 shows the structure function of sample #1, #8, and #9. The baseplate material, which differs thermal conductivity, is used as the parameter. Total thermal resistance of each module becomes small as the thermal conductivity is large. The thermal resistances of baseplate 0.279K/W, 0.178K/W, and 0.479K/W for Al, Cu and SUS baseplate are almost agreement with thermal conductivity of each material in Table 5.1. This result shows that baseplate material is the critical parameter in designing transient thermal characteristics of power module for practical use. It is

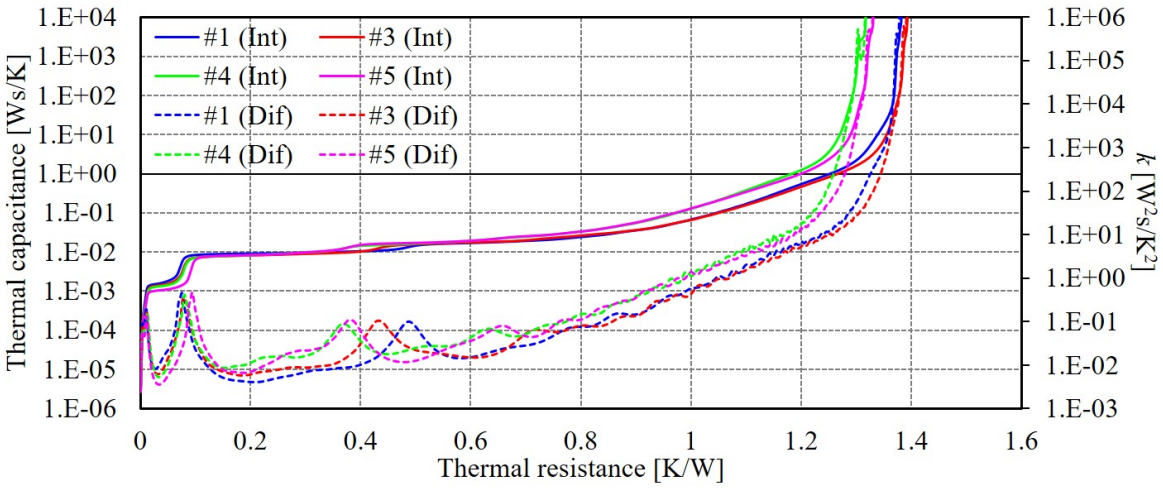


Figure 5.11 Structure function of sample #1, #3, #4, and #5.

noted that Cu baseplate has the larger thermal conductivity and larger density than Al, which prevents to reduce weight of power conversion system.

Fig. 5.14 shows the structure function of sample #1, #10, #11, and #12. The die dimension d_{die} and Cu thickness t_{Cu} are used as the parameters. Chip dimension drastically reduces total thermal resistance as shown in #1 and #10 of Fig. 5.14. When die dimension changes from 3 mm×3 mm to 5 mm×5 mm, heat spreading area becomes about 2.5 times higher, which results in lower thermal resistance of power module. And the thicker Cu thickness t_{Cu} also leads to the lower thermal resistance of power module. This results coincide with the result for 3 mm×3 mm power device.

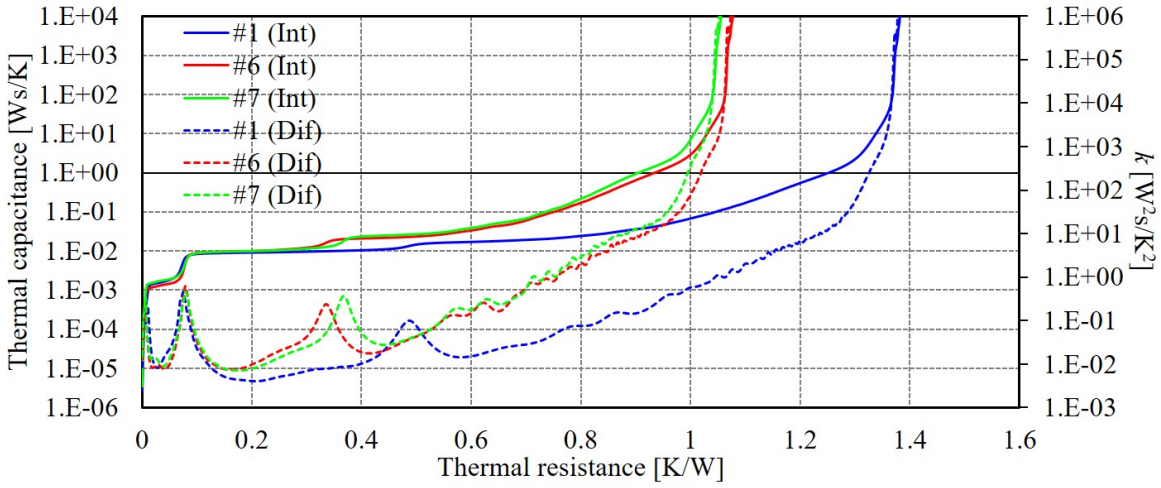


Figure 5.12 Structure function of sample #1, #6, and #7.

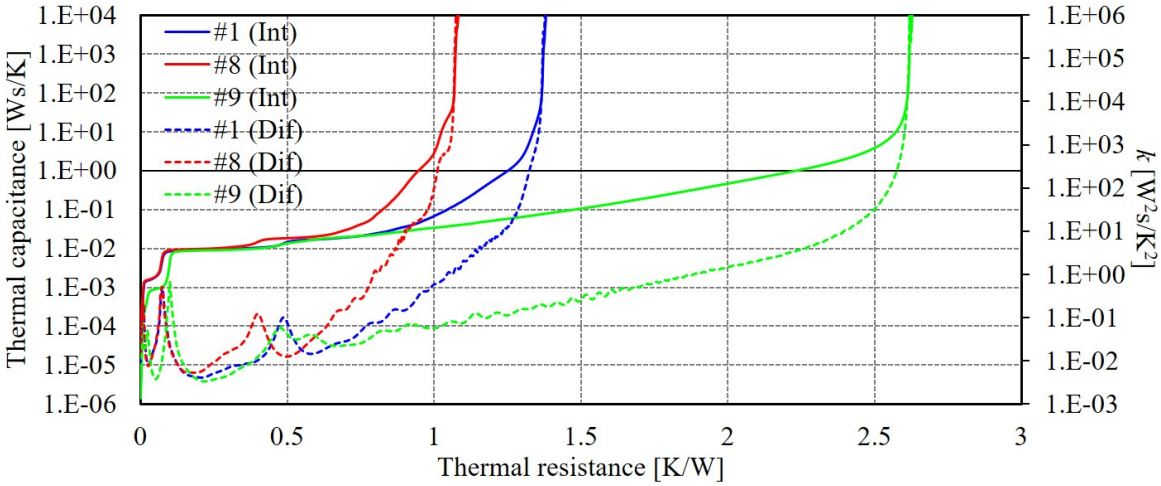


Figure 5.13 Structure function of sample #1, #8, and #9.

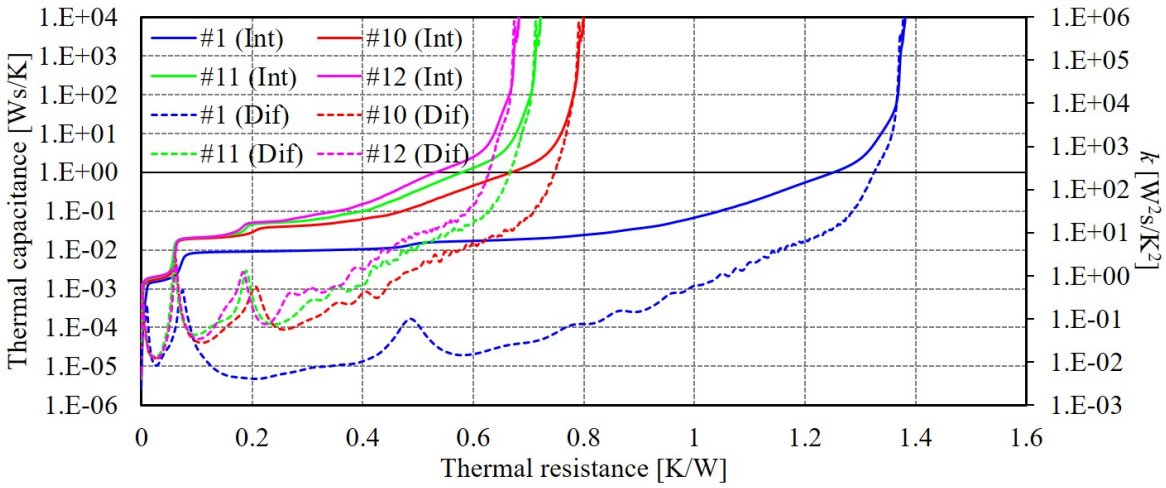
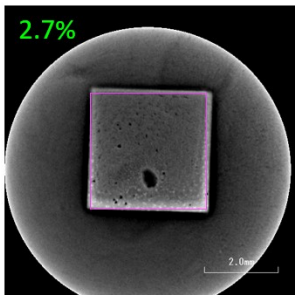
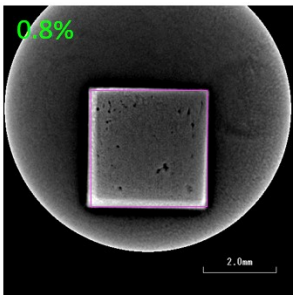


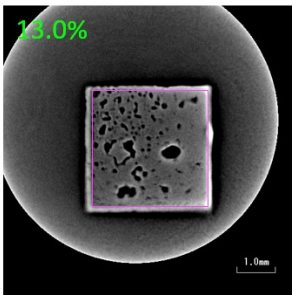
Figure 5.14 Structure function of sample #1, #10, #11, and #12.



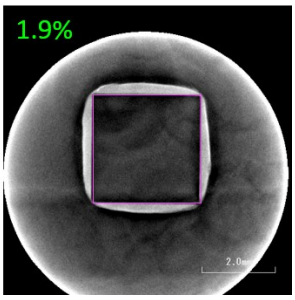
(a) #1.



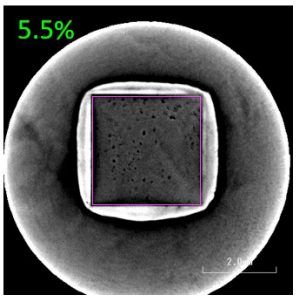
(b) #2.



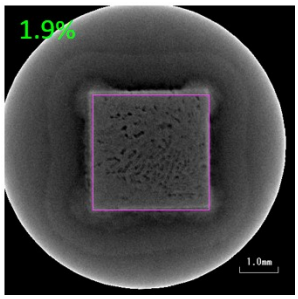
(c) #3.



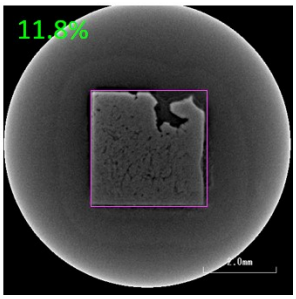
(d) #4.



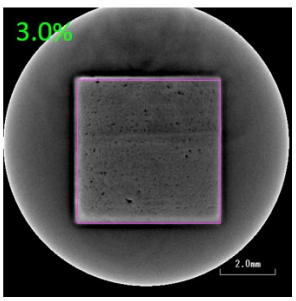
(e) #5.



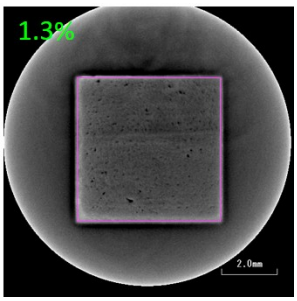
(f) #6.



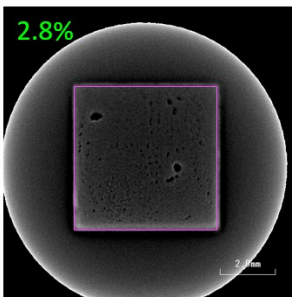
(g) #7.



(h) #10.



(i) #11.



(j) #12.

Figure 5.15 CT image of die attach for studied power module.

5.4 Thermal design evaluation of the developed multi-layered ceramic substrate

5.4.1 Specification of studied power module constitution

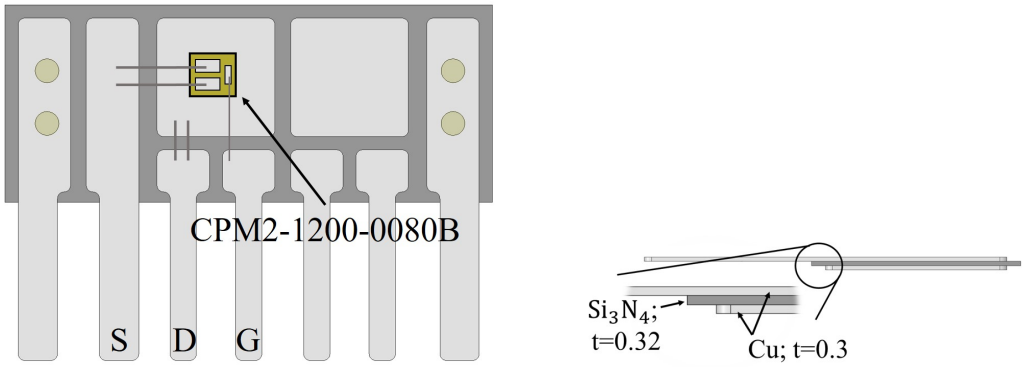
The studied module substrate and device placement is illustrated in Fig. 5.16. The basic configuration of developed power module is already shown in section 2.3. SiC MOSFET CPM2-1200-0080B (1200V/36A, 3.1 mm/3.36 mm/180 μm, CREE) is attached on the center of substrate as a heat source. Bare die is attached with 120 μm solder Sn/Ag/Cu (SMIC) and wired with ϕ300 μm Al bonding wire.

This study evaluates three types of power module substrate. Sample A has one insulation layer (Type-1 in Fig. 5.16(b)) with high thermal conductive material (85 W/m/K in Table 2.2). Sample B is Type-1 with low thermal conductive material (58 W/m/K in Table 2.2). Sample C has two insulation layers (Type-2 in Fig. 2.10(c)) with low thermal conductive material. The physical properties of substrate materials are listed as Table 2.2 and Table 5.1.

5.4.2 Experimental results

The structure functions of the developed power module substrate are obtained by the developed algorithm as shown in Fig. 5.17. The time response of T_{J} for each sample is experimentally obtained by the static method using T3Ster. Here, Mode 4 in section 4.2 is used as measurement setup with -9 V bias voltage by battery as isolated voltage supply. Sample A, B and C are given as blue, red and green line, respectively. "Int" and "Dif" denotes the integral and differential structure function, given as solid and dashed line, respectively. The time response of T_{J} is obtained for 100 sec cooling transient after thermal equilibrium condition with the heating current 5 A. The obtained junction-to-case thermal resistances $R_{\theta \mathrm{JC}}$ by TDI method are 1.226 K/W, 1.307 K/W and 1.035 K/W, respectively for Sample A, B and C.

Sample A and B differ with their heat conductivity of (Si_3N_4) insulation layer. The thermal resistance of insulation layers are identified with the bifurcation point in the structure function in Fig. 5.17, and they are 0.140K/W and 0.167K/W, respectively for



(a) Configuration. (b) Cross-sectional structure.

Figure 5.16 Basic specification of studied power module.

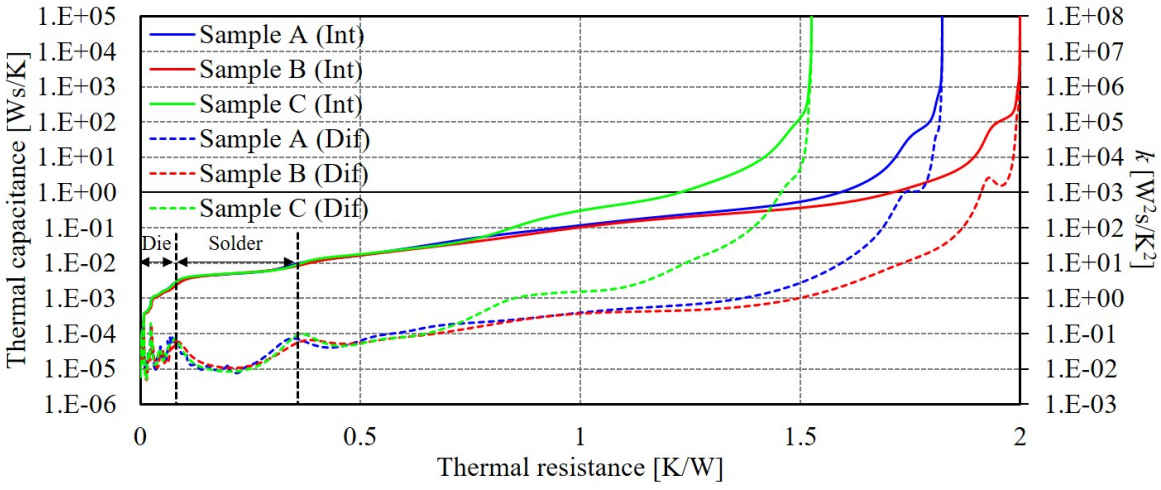


Figure 5.17 Obtained structure function of each sample.

Sample A and B. The higher thermal conductivity leads to the lower thermal resistance of power module. But the ratio of thermal resistance in insulation layer of Sample A to B does not coincide with the ratio of heat conductivity of ceramics. This stems from the difference in die attach with voids in it.

Though Sample C has thicker insulation layer in total, but the junction-to-case thermal resistance of Sample C is smaller than B by 0.272K/W. The thermal capacitance of Sample C is double compared to Sample B at x=0.9 K/W, which results from the middle thick Cu layer of Sample C. Expanding heat spreading area at middle Cu layer stems from this lower thermal resistance. This result also coincides with section 5.3. It is noted that the thicker Cu layer enables to reduce the thermal resistance, but increase the weight of power module.

5.4.3 Simulation results

The example of the simulation model with FloEFD for Sample C is illustrated in Fig. 5.18. This model consists of die, die attach, multi-layered ceramic substrate, grease and heatsink. Boundary condition is set on the backside of heatsink as the convection condition with ambient temperature T_{amb} =20°C. 20 W is set for each simulation model of active area, whose size is 2.6 mm×2.4 mm×20 μm.

Figs. 5.19 to 5.21 show the structure functions obtained from the measured and simulated time response of T_{J}. The obtained structure functions from the simulation results coincide with the measured result. The temperature distribution of each studied power module is shown in Fig. 5.22. The black arrows indicate the heat flux vector. Fig. 5.22 show that middle Cu layer of Sample C spreads the heat horizontally and this results in the lower thermal resistance by expanding heat spreading area. These results indicate that numerical simulation can be used to design transient thermal characteristics of power module.

5.5 Summary

This section evaluated the thermal design of power modules with an AMB substrate for various types of power module constitutions using the transient thermal network

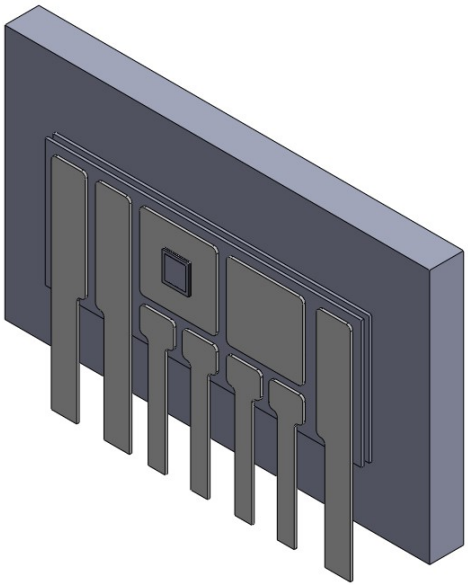


Figure 5.18 Thermal simulation model for Sample C.

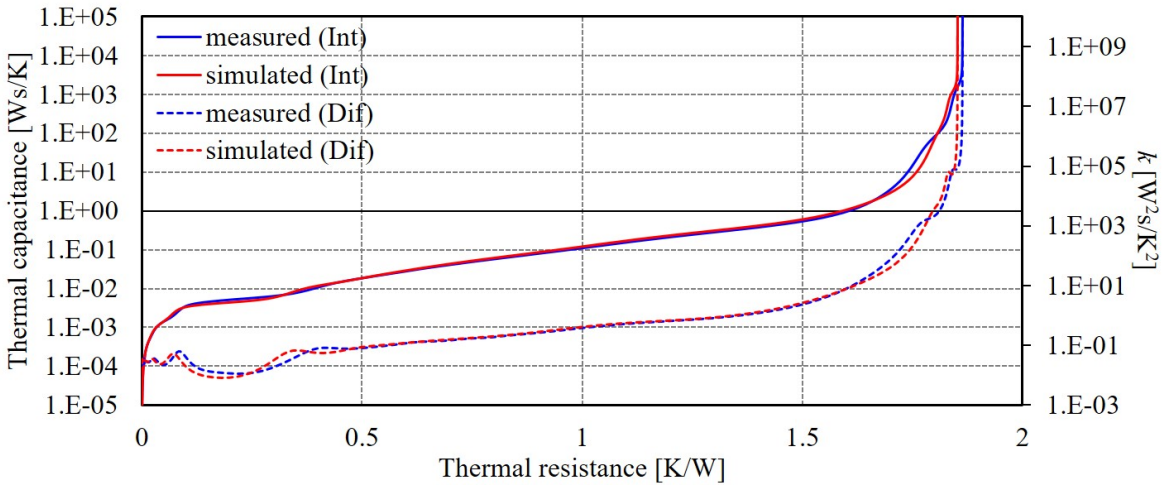


Figure 5.19 Measured and simulated structure function of Sample A.

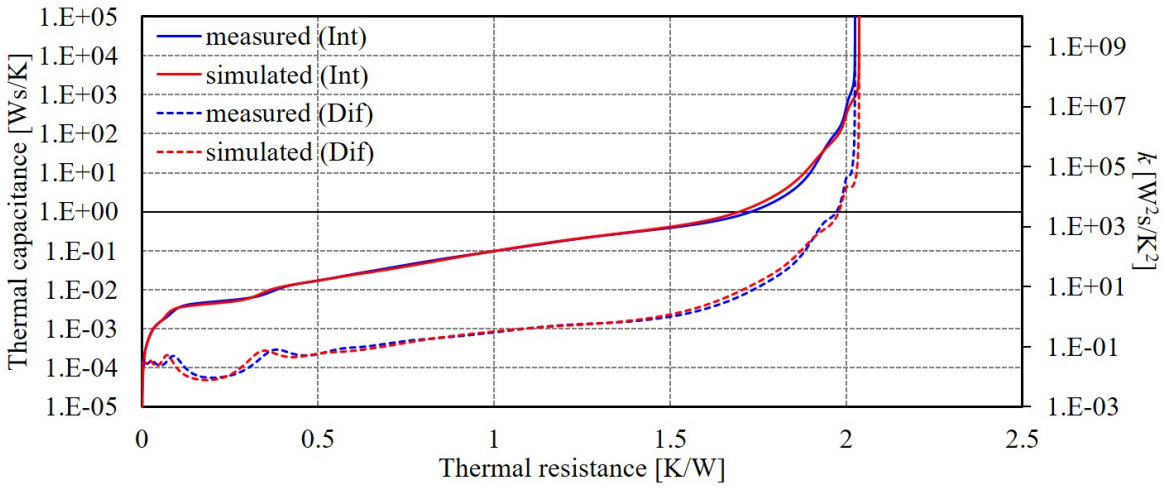


Figure 5.20 Measured and simulated structure function of Sample B.

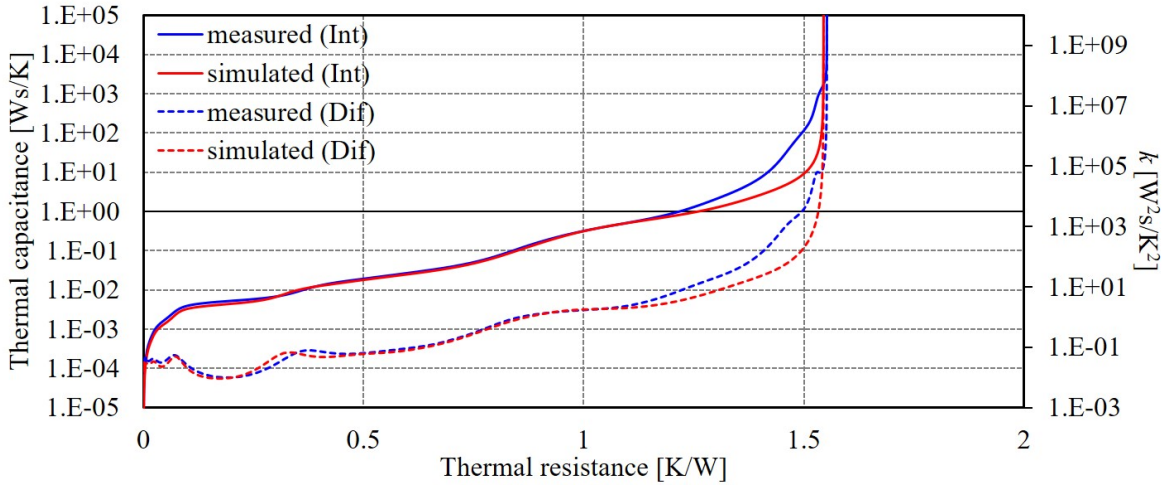
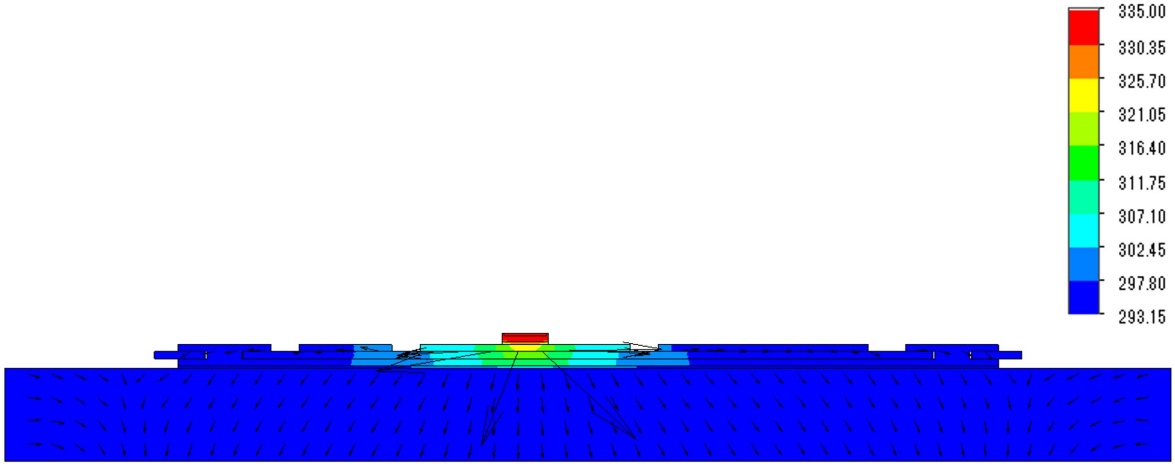
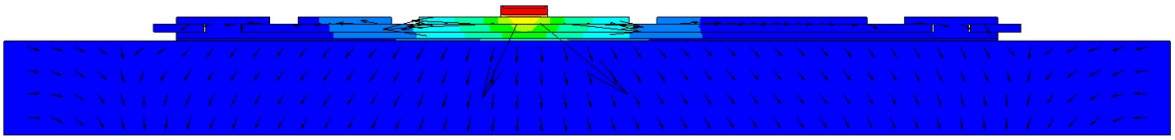


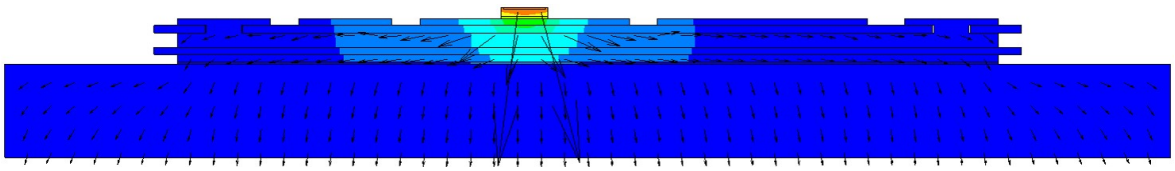
Figure 5.21 Measured and simulated structure function of Sample C.



(a) Sample A.



(b) Sample B.



(c) Sample C.

Figure 5.22 Simulated temperature distribution.

model. Numerical simulation with FVM was introduced to validate the measured transient thermal network model. Parametric study of transient thermal characteristics for power module constitutions revealed the critical factor to improve transient thermal characteristics of power module packages. The larger thermal conductivity of packaging material and die size led to the lower thermal resistance of power modules. In addition, the thicker Cu layer of AMB substrate spread heat from junction in horizontal axis, which lowered thermal resistance of power module. Though the developed multi-layered ceramic substrate had double insulation layer, but the middle Cu layer enabled to reduce the thermal resistance by expanding heat conduction area, which is also revealed by the simulation result of FVM.

Chapter 6

Conclusions

6.1 Conclusions

This paper devoted to studies on thermal design evaluation methods of SiC power module. This section generalizes the obtained results in this thesis.

First of all, fundamentals of SiC power devices and modules were described. The author derived temperature sensitive electrical parameter (K factor) of SiC power device from the temperature dependency in knee voltage of SBD and gate threshold voltage of MOSFET for a fixed small current. This could be used for the junction temperature estimation in order to identify the transient thermal network model of power modules. Moreover, recent and next generation structures and materials of power module packages were described. It was also shown that the developed multi-layered ceramic substrate in this study enabled to reduce the parasitic inductance with snubber capacitor, which resulted in suppressing switching surge voltage of SiC power module accomplished with high speed switching.

An advanced signal processing algorithm to identify the accurate transient thermal network model for power module packages was developed. This algorithm eliminated measurement noise in the logarithmic frequency domain after weighted discrete Fourier transformation. The high sampling frequency of ADC could suppress the influence of quantization error. A low-pass filtering in frequency domain using the developed algorithm eliminated the influence of measurement noise compared to the conventional algorithm. The transient thermal network models obtained by the developed algorithm

for a TO-247 discrete power device package and an AMB substrate of power module package were easily extracted from the structure function. The developed signal processing algorithm enabled to distinguish the boundaries of multi-layered substrate for power module in the structure function, and to improve the accuracy of the identified transient thermal network model.

A junction temperature estimation method for SiC MOSFETs in the transient thermal characterization with expanding the static test method was proposed. The proposed negative gate bias voltage application estimated the accurate time response of T_{J} for SiC MOSFETs without the dynamic gate threshold voltage shift, which was validated by the embedded temperature sense diode on SiC MOSFET. And the time response of T_{J} for the developed SWITCH-MOS was also evaluated to estimate T_{J} dynamically. $I_{\mathrm{d}} - V_{\mathrm{sd}}$ characteristic of SWITCH-MOS in the reverse conduction does not depend on V_{gs} because the reverse current flows through built-in SBD. As the result, an accurate time response of T_{J} could be estimated for SWITCH-MOS without clamping negative bias V_{gs}. These methods and structures enabled to evaluate and design a high density power module using SiC power devices.

The thermal design of power module packages for various types of power module constitutions was evaluated using the developed transient thermal network model identification algorithm. The numerical simulation with finite volume method was introduced to validate the measured transient thermal network model. The obtained transient thermal network model for various types of power module constitutions was evaluated to design power module packages. These experimental results revealed the significant parameters to improve transient thermal characteristics. Moreover, the developed multi-layered ceramic substrate enabled to reduce not only the parasitic inductance but also the thermal resistance by spreading heat in horizontal.

This thesis focused on thermal design evaluation methods for designing transient thermal characteristics of SiC power modules in order to maximize the high density power conversion system capability with SiC power devices. The developed algorithm enables to accurately identify the transient thermal network model of power module packages. And the proposed thermal characterization method for SiC power MOSFETs can obtain the accurate time response of T_{J} eliminating the influence of dynamic gate

threshold voltage shift. These achievements would enable to design not only electrical behavior but also thermal behavior of SiC power modules.

6.2 Industrial impacts

The conventional transient thermal characterization of power module packages with static test method used in this thesis is standardized by Joint Electron Device Engineering Council (JEDEC) in United States. In general, the transient thermal network model identification from the obtained time response of T_J utilizes the analysis software T3SterMaster (MentorGraphics), which requires high cost. Though the free software TDIM-Master supported by JEDEC also can identify the transient thermal network model of power module packages, but this software limits the number of input and output data, which makes difficult to obtain the high accuracy of the identified transient thermal network model. The developed free and higher accuracy identification algorithm in this thesis would accelerate the development of high density power conversion systems with SiC power modules.

A SiC power module is expected to achieve the longer-term reliability and to operate at the harsh environment over 200°C using SiC power device capability compared with the conventional Si power device. The conventional power module package materials such as solder, module substrate and molding resin does not consider to operate at such the higher temperature environment. Thus packaging technology as well as power device itself plays an important role in SiC power module under the harsh environment. The developed identification algorithm enables to evaluate the developed package materials by own company with low cost. As a result, many companies easily enter the development competition of power module package materials, which improves the performance of power modules. This also leads to cost down to fabricate SiC power modules.

6.3 Future outlooks

This research mainly focused on thermal design for SiC power modules. Though the conventional transient thermal network model assumes that the heat path from junction to heatsink approximately flows in one direction, but a next generation power module package flows heat in two or more directions. It is necessary to develop the improved or new transient thermal network model and its identification method in order to obtain the high accurate model.

Moreover, electro-thermal co-design is important to maximize SiC power device capability and to achieve high power density power conversion systems. The key to simultaneously design electrical and thermal characteristics will be a multi-objective optimization method of power modules such as non-dominated sorting genetic algorithm (NSGA) or multi-objective particle swam optimization (MOPSO). The developed transient thermal network model identification method for SiC power modules in this thesis enables to evaluate and design thermal characteristics of SiC power modules, which results in the multi-objective design of high density power module.

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[Awards]

1. 2017 Academic Plaza Award (Shuhei Fukunaga, Tsuyoshi Funaki, 2017).
2. Joint Technical Meeting on Electron Device and Semiconductor Power Converter 2017 Best Student Paper Award (2017).
3. IEE Japan Excellent Presentation Award from Industry Applications Society (2017).
4. Joint Technical Meeting on Electron Device and Semiconductor Power Converter 2018 Best Student Paper Award (2018).