A Study on Equivalent Circuit Modeling of Wiring Inductance in SiC Power Module for Predicting Conducted EMI of Power Converter

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***Abstract*— Silicon Carbide (SiC) power semiconductor devices achieve low switching losses with fast switching operation and miniaturized power conversion circuit. SiC power module for high voltage and large current is subject to large di/dt and dv/dt in switching transient. Large di/dt induces surge voltage and ringing oscillation by interacting with circuit parasitic inductance and capacitance. These are fatal factors for electromagnetic interference (EMI) of the circuit. This report studies modeling of parasitic inductance in SiC power module based on three-dimensional (3-D) electromagnetic analysis to realize low EMI design for power conversion circuit. The developed Partial Equivalent Element Circuit (PEEC) model of SiC power module is applied to circuit analysis. The simulated time response of voltage/current in switching operation and frequency spectrum of the conducted EMI for the tested converter agree with the measurement result well.**

Keywords—SiC Poewer Module, PEEC method, parasitic inductance, conducted EMI

I. INTRODUCTION

Silicon Carbide (SiC) power semiconductor devices enable fast switching operation of high voltage and large current. Fast switching leads low switching losses and miniaturization of passive components in a high-power converter [1], [2]. SiC power module with parallel connected MOSFET realizes large current operation. However, large di/dt induces surge voltage by interacting with the circuit parasitic inductance. Resonant current also flows the circuit parasitic inductance and output capacitance (C_{oss}) of SiC MOSFET or DC-link capacitor in switching operations. This leads to ringing oscillation voltage and current in switching transient response of SiC MOSFET. As a result, electromagnetic interference (EMI) issues become more difficult.

There has been increasing interest in predicting and suppressing EMI of SiC-based power conversion circuit to suffice the electromagnetic compatibility (EMC) regulations (e.g., CISPR and FCC). Many papers and technical reports mention that it is important to identify parasitic inductance around the power devices in the circuit [3-6]. The authors have evaluated parasitic inductance of interconnect wiring and visualized high-frequency noise current distribution in 2-D structure SiC half-bridge power module [7].

Most of the wiring layouts of power module have a 2-D structure on direct bonded copper (DBC) substrate. We study effective parasitic inductance in power module which have 3-D wiring structure. Partial equivalent element circuit (PEEC) method is known to be useful as a means to identify parasitic parameter or mutual electromagnetic (EM) coupling such as PCB wiring and EMI filter components [8-10]. The PEEC method is suitable for circuit analysis and it allows to analyze in both time-domain and frequency-domain. In Section II, we modeled electrical characteristics of SiC power module with 3-D wiring structure by PEEC method. The developed PEEC model is validated by comparing the measured results and electromagnetic analysis results based on Finite Element Method (FEM). In Section III, the developed PEEC model is applied to the circuit analysis. The tested circuit is DC-DC buck converter using SiC power module. The transient response of the power module in switching operation is obtained by the circuit analysis, and it is compared with the measured time response. In Section IV, frequency spectrum of the conducted EMI is obtained by the circuit analysis, and they are compared with measurement to validate the studied model.

II. THE DEVELOPED SIC POWER MODULE WITH 3-D WIRING STRUCTURE AND EMBEDDED DC-LINK CAPACITOR

A. Circuit topology and static characteristic of the developed SiC power module

Fig. 1 shows (a) internal wiring structure, (b) cross-sectional structure, and (c) circuit diagram of SiC half-bridge power module. One arm in the power module has paralleled four 1200 V-40 mΩ SiC MOSFET dies on DBC substrate. The wiring inductance in the studied power module can be reduced by utilizing the magnetic flux cancellation as explained in Fig.1(b) .

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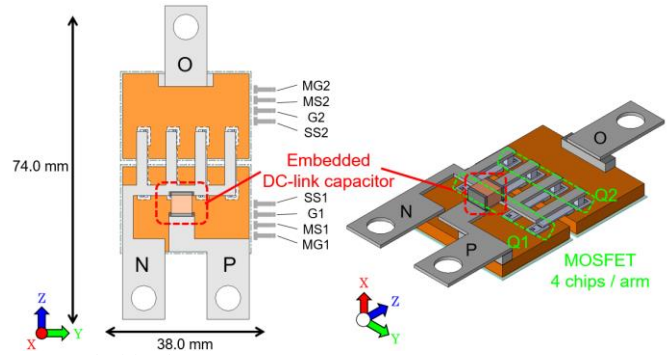
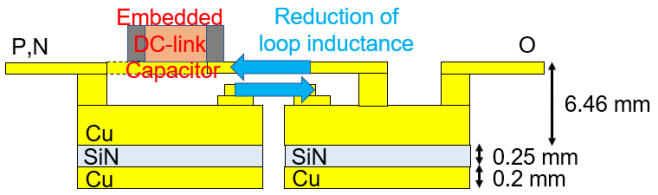
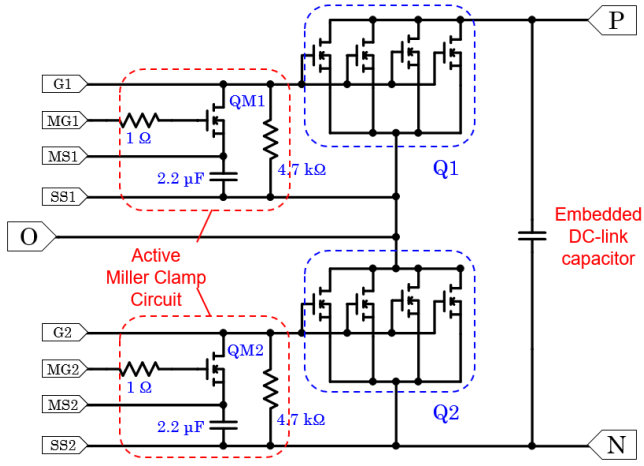


a) Internal wiring layout

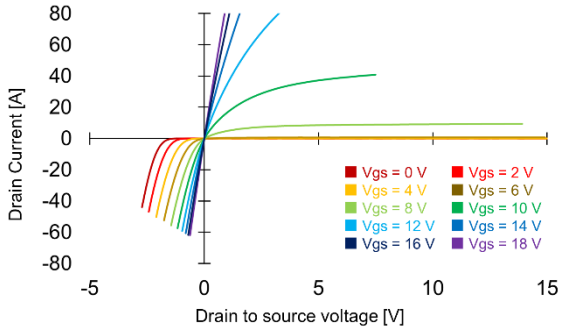


b) Cross-sectional structure

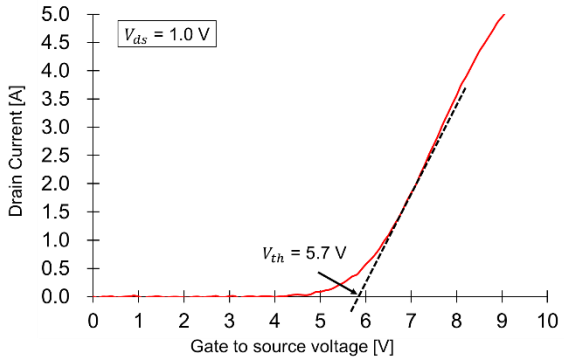


c) Circuit diagram

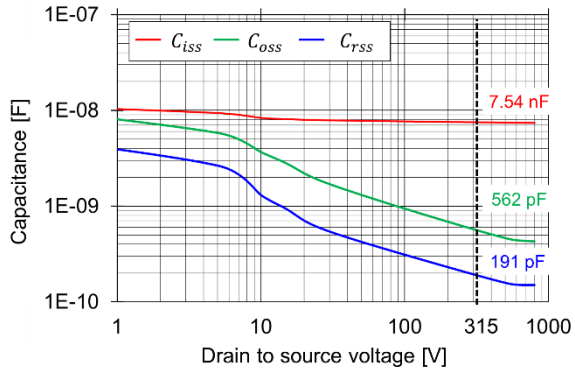
Fig. 1. The tested SiC half-bridge power module



a) $I_d - V_{ds}$ characteristics



b) $I_d - V_{gs}$ characteristics



c) $C_{iss}, C_{oss}, C_{rss} - V_{ds}$ characteristics

Fig. 2. Static characteristics of SiC power module

Fig. 2 shows the static I-V characteristics and DC bias voltage dependency of terminal capacitance (C-V characteristics) of low-side Q2 in SiC power module. These characteristics were measured by curve tracer (Keysight, B1505A) at room temperature. The on-resistance R_{on} is identified as 12 mΩ at $I_d = 80$ A from I_d-V_{ds} characteristics for V_{gs} =18 V as shown in Fig. 2 (a). The threshold gate voltage is identified as V_{th}= 5.7 V from I_d-V_{gs} characteristics for V_{ds} =1 V as shown in Fig. 2 (b). $C_{iss} = 7.54$ nF , $C_{oss} = 562$ pF, and $C_{rss} = 191$ pF at $V_{ds} = 315$ V are obtained from C-V characteristics in Fig. 2 (c). There is no noticeable difference in these characteristics between both Q1 and Q2.

B. *Development of PEEC model for interconnects of the SiC power module*

3-D solid conductor is divided into a bundle and sequence of straight segments for the PEEC method. The charge density distribution or the current density distribution is uniform in each segment. The electric field $\boldsymbol{E^{inc}}$ on a segment is given as follows (1), where σ is the conductivity of the conductor, $\boldsymbol{J}(x,y,z,t)$ is a current density, $\boldsymbol{A}(x,y,z,t)$ is a vector potential and $\Phi(x,y,z,t)$ is a scalar potential [11].

$$\boldsymbol{E^{inc}}(x,y,z,t) = \frac{\boldsymbol{J}(x,y,z,t)}{\sigma} + \frac{\partial \boldsymbol{A}(x,y,z,t)}{\partial t} + \nabla\Phi(x,y,z,t) \quad (1)$$

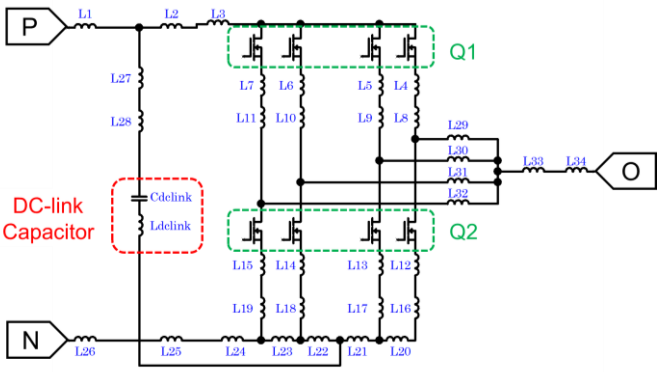


Fig. 3. Studied equivalent circuit model of based on PEEC method

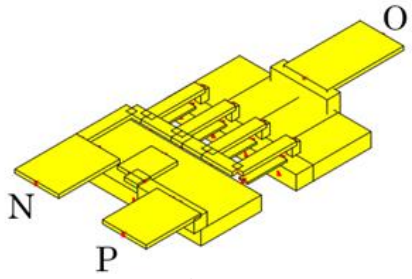


Fig. 4. Conductor placement of PEEC

The second term is an inductive component, and the partial inductance L_{sgm} is obtained by (2). Here, a_k and a_m denote the cross areas of the segment k and m. μ is permeability of the segment. $d\boldsymbol{l_k}$ and $d\boldsymbol{l_m}$ are vectors of different elements, and b_k, c_k, b_m, c_m denote the start point and the end point of the segment. r_{km} is distance between elements $d\boldsymbol{l_m}\,da_m$ and $d\boldsymbol{l_k}\,da_k$. $k = m$ gives partial self-inductance, and $k \neq m$ gives partial mutual inductance.

$$L_{sgm} = \frac{1}{a_k a_m}\frac{\mu}{4\pi}\int_{b_k}^{c_k}\int_{b_m}^{c_m}\int_{a_k}\int_{a_m}\frac{1}{r_{km}}d\boldsymbol{l_k}\cdot d\boldsymbol{l_m}da_k da_m \quad (2)$$

The current distribution in bundled conductor for high frequency range is non-uniform due to skin effect. Therefore, the cross-section of each segment should be divided into a filament [12]. The thickness h_{fil} of filament near the surface of conductor is needed to be less than half the skin depth δ given by (3). The skin depth δ is 6.6 µm for $f = 100$ MHz, $\sigma = 5.8 \times 10^7$ S/m, and $\mu = \mu_0 = 4\pi \times 10^{-7}$ H/m. The segment thickness h_{fil} was also determined less than 3.3 µm.

$$\delta = \frac{1}{\sqrt{\pi f \sigma \mu}} \quad (3)$$

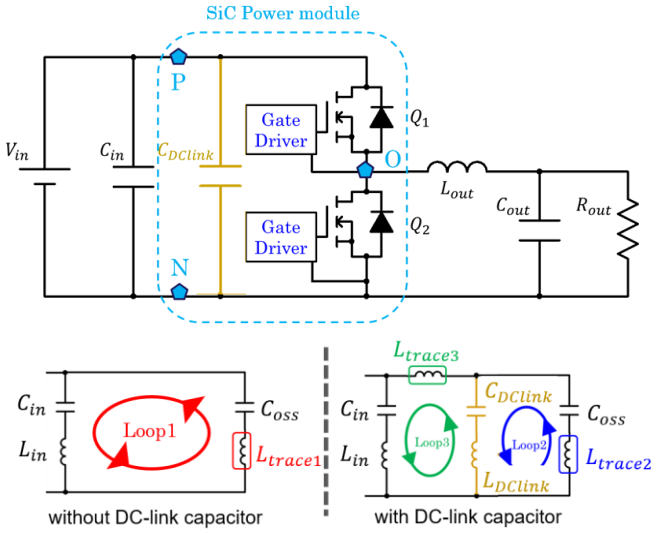


Fig. 5. Oscillation current loop in DC-DC buck converter

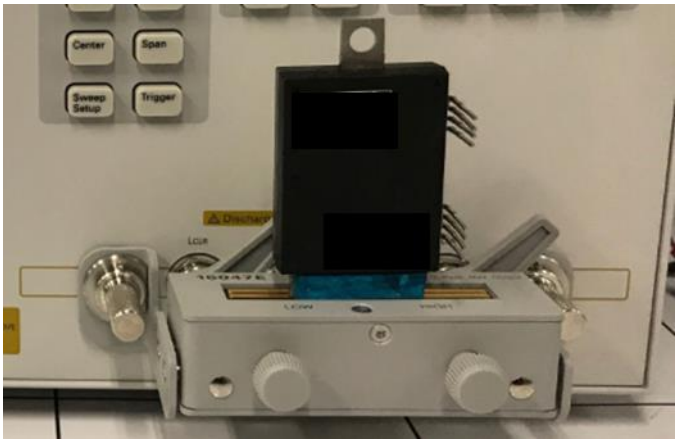


Fig. 6. Impedance measurement of SiC power module

This report studies parasitic inductance of 3-D structure wiring for the tested SiC power module with embedded DC-link capacitor. Fig. 3 shows the developed PEEC model of tested SiC power module. Fig. 4 depicts the conductor placement of tested SiC power module. Fig. 5 shows parasitic inductance L_{trace1}, L_{trace2}, and L_{trace3} related to ringing oscillation. They are L_{trace1} via P-Q1-Q2-N path, L_{trace2} via DC-link capacitor - FET path, and L_{trace3} via P-DC-link capacitor - N path. These values are calculated for PEEC model.

The self-inductance of L_{trace1}, L_{trace2}, and L_{trace3} calculated for PEEC model are 15.4 nH, 5.2 nH, and 19.1 nH, respectively. L_{trace1} and L_{trace2} including the mutual EM coupling inductance are different from the ones of not including the mutual EM coupling by 3 nH in TABLE I. This indicates that the magnetic flux cancellation shown in Fig. 1 (b) is effective for lowering parasitic inductance. In this power module, an effective loop inductance can be reduced by about 50% with incorporating a DC-link capacitor in the SiC power module even though the loop include the ESL (below 2.0 nH) in it.

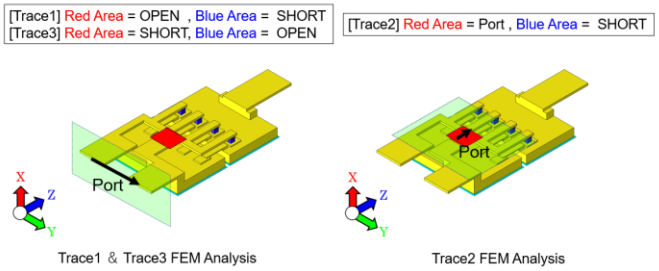


Fig. 7. Electromagnetic analysis by FEM

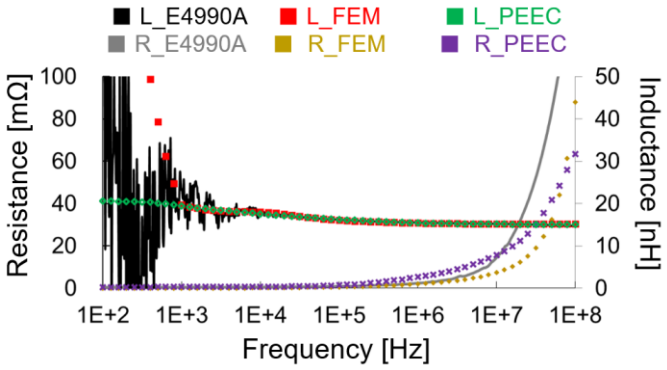


Fig. 8. Frequency characteristic of resistance and inductance in Trace1

TABLE I.
Measurement and simulation results of
partial inductance in SiC power module

	L_{trace1} [nH]	L_{trace2} [nH]	L_{trace3} [nH]
Measurement	15.5	---	---
FEM	15.4	4.2	17.8
PEEC (self inductance only)	19.8	8.4	19.2
PEEC (mutual coupling include)	15.4	5.2	19.1

L_{trace1} was identified from the frequency characteristics of impedance measured by impedance analyzer (Keysight E4990A) in Fig. 6, for the power module whose Q1 and Q2 are shorted. L_{trace2} and L_{trace3} could not be measured directly. These self-inductance are also calculated by FEM (EMPro, Keysight) as shown in Fig. 7. TABLE I shows measurement and calculation results of these self-inductance. The frequency characteristics of resistance and inductance in Trace1 is shown in Fig. 8. It was confirmed that the value calculated by the PEEC method matched well with the measurement and the FEM results.

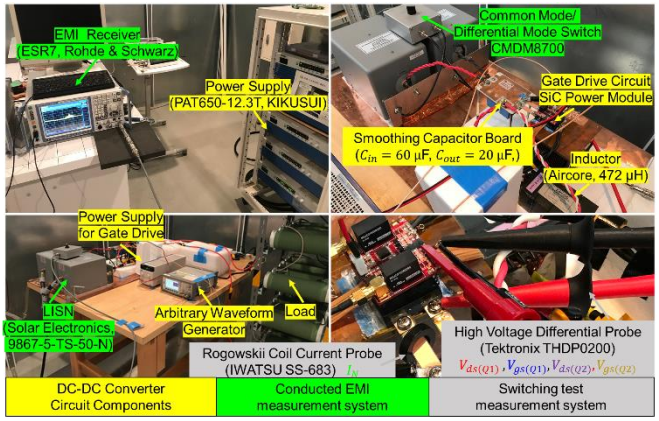


Fig. 9. Measurement system for switching test and conducted EMI

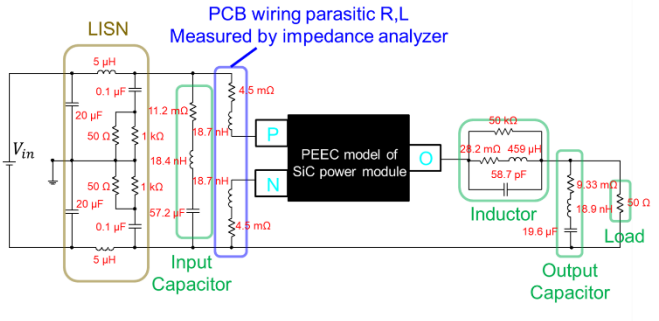


Fig. 10. Circuit analysis diagram for DC-DC buck converter

III. Circuit Analysis of Transient Response in Switching Operation for DC-DC Buck Converter

A. *Operating Condition of DC-DC Buck Converter*

Fig.9 shows measurement setup for capturing switching transient response of the tested SiC power module in the DC-DC buck converter (Fig. 5). The tested conditions are as follows; input DC voltage V_{in} = 315 V, output DC voltage V_{out} = 150 V, resistive load R_{out} = 50 Ω, duty ratio 0.4762, and switching frequency f_{sw} = 50 kHz. PCB wiring inductance is 37.4 nH, ESL of input capacitor is 18.4 nH. From Fig.1 (b), the parasitic capacitance resulting from the insulating layer (SiN) in the tested SiC power module is obtained by (4). Here, S is parallel plates of area, d is separation distance and ε is the dielectric permittivity. The capacitance for the insulating layer (SiN) is 180 pF.

$$C = \varepsilon \frac{S}{d} \tag{4}$$

The developed PEEC model is applied to the circuit analysis in Fig.10. The applied PEEC model incorporated the device model of SiC MOSFET [13]. Keysight Advanced Design System software was used as the circuit simulation.

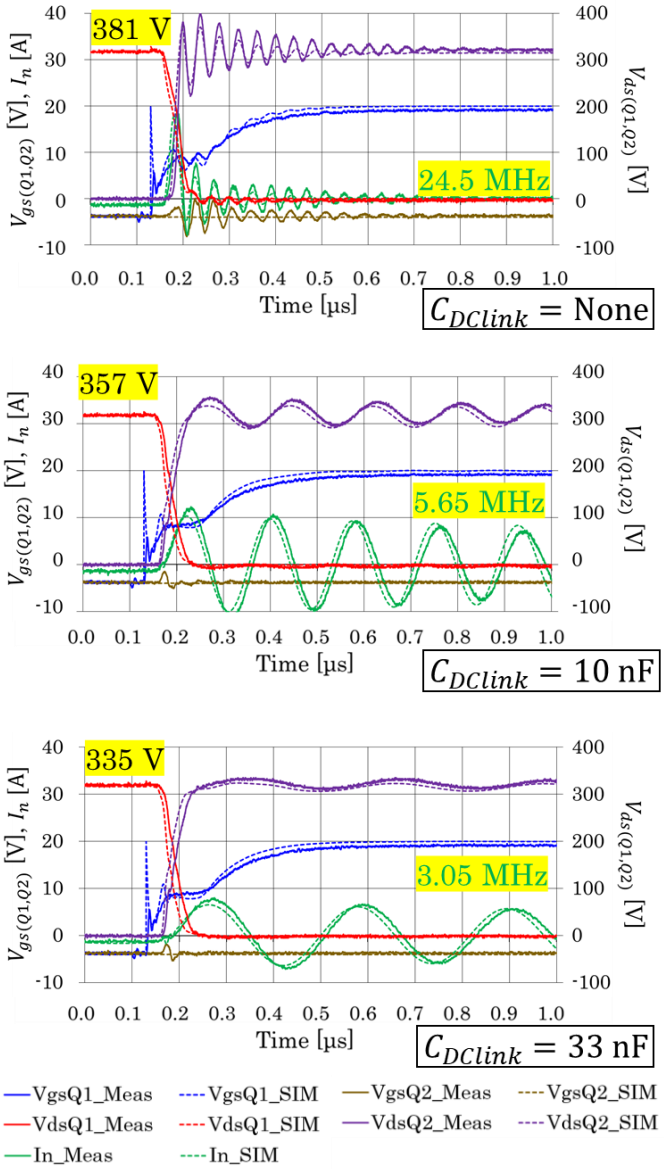


Fig. 11. Switching characteristics of the SiC power module

B. *Circuit Analysis of Transient Response in Switching Operation*

As shown in Fig. 9, the voltages V_{gs} , V_{ds} of Q1, Q2 and the current I_N through the module N terminal were measured. The transient response for Q2 turn-off operation is evaluated in this section. Fig. 11 shows measurement and simulated results of time response of voltage and current in the tested SiC power module. The simulation results agree with the measurement results. The surge voltage is reduced 24 V for $C_{DClink} = 10$ nF, and is reduced 46 V for $C_{DClink} = 33$ nF, respectively. The resonant frequency for Loop1 is identified as 24.5 MHz in Fig.5. The resonant frequency for Loop3 is 3.05 MHz or 5.65 MHz. The damping of ringing oscillation for Loop2 is less than Loop1. The resonance frequency for Loop2 is expected to be 80 MHz for C_{oss} of SiC MOSFET and the inductance of Loop2, but it is too attenuated to be visible.

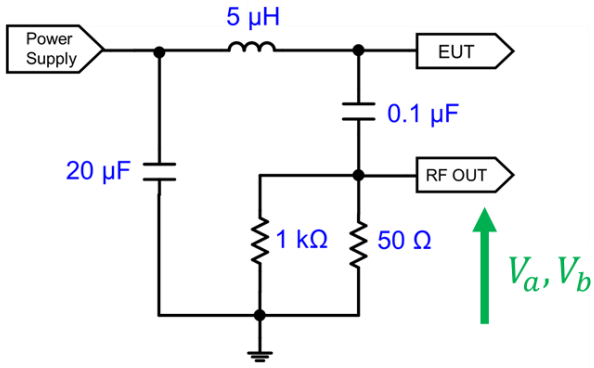


Fig. 12. Circuit configuration of LISN

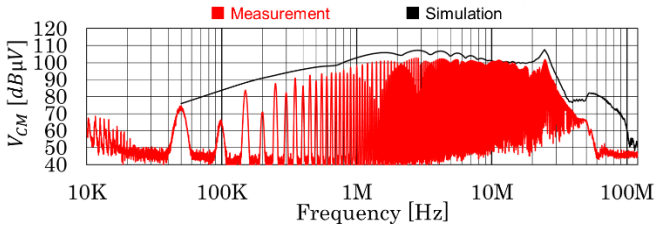


Fig. 13. Measurement and simulated results of common mode conducted EMI

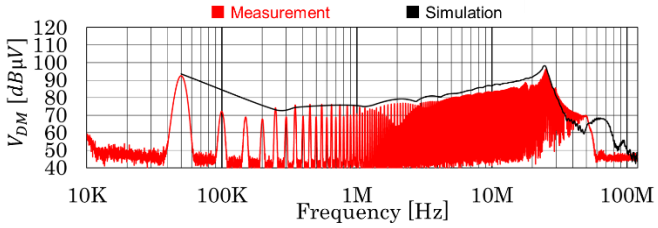


Fig. 14. Measurement and simulated results of differential mode conducted EMI

IV. Conducted EMI Modeling

The DC power supply lines of DC-DC buck converter are connected two Line Impedance Stabilization Networks (LISNs) as shown in Fig.12. LISN is used to measure the power supply line to ground voltage V_a and V_b. Conducted EMI is classified into Differential Mode (DM) and Common Mode (CM) by the difference of the propagation mode. The line to ground voltage V_a and V_b are decomposed into common and differential mode as (5). V_{CM} and V_{DM} are measured by using CM/DM switch (Schwarzbeck, CMDM8700).

$$V_{DM} = \frac{1}{2}(V_a - V_b),\ V_{CM} = \frac{1}{2}(V_a + V_b) \quad (5)$$

Fig.9 shows measurement setup of conducted EMI for the tested DC-DC converter without embbeded DC-link capacitor. Then, frequency spectrum of conducted EMI measured by the EMI test receiver (ROHDE & SCHWARZ, ESR7) with the V-type LISN (Solar Electronics, 9867-5-TS-50-N) in the shielded room. Fig.13 and Fig.14 show frequency spectrum of common

mode (CM) and differential mode (DM) conducted EMI. The both frequency spectrum has peaks at odd integer multiples of the switching frequency and at the ringing frequency. The superiority of CM or DM conducted EMI changes with the frequency. At switching frequency (50 kHz), DM conducted EMI is 93 dBμV, while CM conducted EMI is 75 dBμV. In MHz band, DM conducted EMI is from 70 to 80 dBμV, while CM conducted EMI is almost 100 dBμV.

The frequency spectrums were calculated by the circuit analysis with the developed PEEC model. The calculated results corresponds with the measurement within 5 dB in the wide frequency range in both mode. However, there is 20 dB difference around 100 MHz. The measurement system length (above 1 m) is not negligible compared with the 1/4 wavelength of the target signal at the frequency of 100 MHz (75 cm). For this reason, the noise level between the measurement and the calculation is mismatched.

V. Conclusion

This paper developed the PEEC model of SiC power module with 3-D wiring structure. The parasitic inductance via P-Q1-Q2 -N path calculated from the PEEC model corresponds well with the measured result. The calculated results of transient response in switching operation and conducted EMI using PEEC model also coinsides, this approach makes it possible to characterize conducted EMI of power conversion circuit with SiC power module and is applicable to the EMC design of the high-power converter. The accuracy of conducted EMI prediction will be further improved, in the future research, and it will be studied on conducted EMI reduction design method using the PEEC model.

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