An Experimental Study on Terrestrial Radiation-Induced Single Event Upsets in Planar and FinFET SRAMs

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Publications

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3. **T. Kato**, T. Yamazaki, N. Saito, and H. Matsuyama, "Neutron-induced multiple-cell upsets in 20 nm bulk SRAM: angular sensitivity and impact of multi-well potential perturbation," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 7, pp. 1381–1389, Jul. 2019.

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2. K. Kobayashi, J. Furuta, H. Maruoka, M. Hifumi, S. Kumashiro, **T. Kato**, and S. Kohri, "A 16 nm FinFET radiation-hardened flip-flop, bistable cross-coupled dual-modular-redundancy FF for terrestrial and outer-space highly-reliable systems," in *Proc. IEEE Int. Reliab. Phys. Symp. (IRPS)*, 2017, pp. SE-2.1–SE-2.3.

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5. **T. Kato**, R. Akano, T. Uemura, Y. Watanabe, and H. Matsuyama, "Neutron shielding effect of stacked servers and its impact on reduction of soft error rate," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3408–3415, Dec. 2014.

6. T. Uemura, **T. Kato**, R. Tanabe, H. Iwata, J. Ariyoshi, H. Matsuyama, and M. Hashimoto, "Exploring well-configurations for minimizing single event latchup," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3282–3289, Dec. 2014.

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10. T. Uemura, **T. Kato**, H. Matsuyama, and M. Hashimoto, "Soft-error in SRAM at ultra-low voltage and impact of secondary proton in terrestrial environment," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4232–4237, Dec. 2013.

11. T. Uemura, **T. Kato**, and H. Matsuyama, "Impact of parasitic bipolar action and soft-error trend in bulk CMOS at terrestrial environment," in *Proc. IEEE Int. Reliab. Phys. Symp. (IRPS)*, 2013, pp. 6C.4.1–6C.4.6.

12. **T. Kato**, T. Uemura, H. Mori, Y. Ikeda, K. Suzuki, S. Satoh, and H. Matsuyama, "Impact of parasitic bipolar effect on single-event upset in p-type metal-oxide-semiconductor field effect transistor with embedded SiGe," *Jpn. J. Appl. Phys.*, vol. 52, no. 4S, pp. 04CC15-1–04CC15-5, Mar. 2013.

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16. T. Uemura, **T. Kato**, H. Matsuyama, K. Takahisa, M. Fukuda, and K. Hatanaka, "Investigation of multi cell upset in sequential logic and validity of redundancy technique," in *Proc. IEEE Int. On-Line Testing Symp. (IOLTS)*, 2011, pp. 7–12.

Abstract

In the terrestrial environment, all semiconductor devices are continuously exposed to terrestrial radiations originating from cosmic-rays and natural radioisotopes. A problem is that the terrestrial radiations deposit charge on the semiconductor devices through ionization and can cause transient errors, so-called soft errors.

The growing integration of semiconductor devices, such as system-on-a-chips, has increased the susceptibility to the terrestrial radiations and has made the soft error problem more challenging. At the same time, the soft error phenomena have become complex due to the aggressive scaling of transistors. Among the semiconductor devices, static random access memories (SRAMs) are one of the most susceptible devices to the terrestrial radiations. This is because the SRAM devices have been highly integrated, and because the size and voltage scaling of SRAM cells has drastically decreased the amount of stored charge. Therefore, the appropriate understanding of the terrestrial radiation-induced soft errors in the SRAM devices is necessary to cope with soft error issues in advanced semiconductor devices.

This thesis focuses on single-event upsets (SEUs) and multiple-cell upsets (MCUs) induced by the terrestrial radiations in advanced SRAMs, with the aim of understanding the impact of the technology advancement on the SEU and MCU responses. For the advanced SRAMs, this thesis deals with both planar and fin-shaped field-effect transistor (FinFET) technologies. For the terrestrial radiations, the major sources of the SEUs have been considered to be high-energy neutrons, thermal neutrons, and alpha particles. In addition to these particles, negative and positive muons have recently received great attention as potential sources of the SEUs. This thesis covers all these particles. The SEU and MCU responses of the planar and FinFET SRAMs are extensively studied by a variety of experimental methods. In particular, particle irradiation testing is performed for all the above particles. Moreover, an emerging laser irradiation technique is utilized to explore the underlying mechanism.

The studies in this thesis address the effects of size scaling, critical charge reduction, and transistor geometry change, which are the key factors in the technology advancement of SRAMs. The studies begin with the exploration of MCU mechanisms complicated by the size scaling. Single-pulse laser irradiations unveil a novel mechanism, named multi-well coupled potential unbalancing. The size scaling also affects the angular sensitivity of high-energy neutron-induced SEUs and MCUs. High-energy neutron irradiations at several incidence angles reveal the significant angular dependence of SEU and MCU responses in 20-nm planar SRAMs. This angular sensitivity is also studied in 12-nm FinFET SRAMs. The comparative analyses between the planar and FinFET SRAMs demonstrate the difference in the angular sensitivities due to the transistor geometry change. The final study investigates muon-induced SEUs and MCUs, which can be significant due to the critical charge reduction. The unique SEU and MCU characteristics are clarified in the 20-nm planar SRAMs through negative and positive muon irradiations with comparison to

other terrestrial radiations.

This thesis provides interesting and insightful findings through the studies based on various irradiation experiments and deepens the understanding of the terrestrial radiation-induced SEUs in advanced SRAMs. The findings are meaningful not only for understanding SEU phenomena, but also for developing effective mitigation techniques. On the basis of the obtained findings, some suggestions are offered for SEU mitigation. Therefore, the results yielded in this thesis will be helpful for resolving soft error problems and for achieving radiation tolerance in current and future semiconductor devices.

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2D	Two-**D**imensional
3D	Three-**D**imensional
3DAP	**3D A**tom **P**robe
ATE	**A**utomated **T**est **E**quipment
BL	**B**it **L**ine
BPSG	**B**oro**P**hospho**S**ilicate **G**lass
BTI	**B**ias **T**emperature **I**nstability
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CMP	**C**hemical-**M**echanical **P**olishing
CS	**C**ross **S**ection
DRAM	**D**ynamic **R**andom **A**ccess **M**emory
DUT	**D**vice **U**nder **T**est
ECC	**E**rror **C**orrection **C**ode
EXPACS	**EX**cel-based **P**rogram for calculating **A**tmospheric **C**osmic-ray **S**pectrum
FBM	**F**ail **B**it **M**ap
FET	**F**ield **E**ffect **T**ransistor
FF	**F**lip-**F**lop
FinFET	**F**in-shaped **F**ield-**E**ffect **T**ransistor
FIT	**F**ailure **I**n **T**ime
FPGA	**F**ield-**P**rogrammable **G**ate **A**rray
HCI	**H**ot **C**arrier **I**njection
HWNIF	**H**eavy **W**ater **N**eutron **I**rradiation **F**acility
HyENEXSS	**Hy**per **EN**vironment for **EX**ploration of **S**emiconductor **S**imulation
IoT	**I**nternet **o**f **T**hings
IR	**I**nfra**R**ed
JANIS	**JA**va-based **N**uclear **I**nformation **S**oftware
JENDL	**J**apanese **E**valuated **N**uclear **D**ata **L**ibrary
J-PARC	**J**apan **P**roton **A**ccelerator **R**esearch **C**omplex
KUR	**K**yoto **U**niversity Research **R**eactor
LA	**L**ow **A**lpha
LET	**L**inear **E**nergy **T**ransfer
MBU	**M**ultiple-**B**it **U**pset
MCBI	**M**ulti-**C**oupled **B**ipolar **I**nteraction
MCU	**M**ultiple-**C**ell **U**pset

MOS	**M**etal-**O**xide-**S**emiconductor
MTBF	**M**ean **T**ime **B**etween **F**ailure
MUSE	**MU**on **S**cience **E**stablishment
MWCPU	**M**ulti-**W**ell **C**oupled **P**otential **U**nbalancing
NA	**N**umeric **A**perture
nMOS	**n**-type **MOS**
PBE	**P**arasitic **B**ipolar **E**ffect
PE	**P**ulse **E**nergy
PHITS	**P**article and **H**eavy **I**on **T**ransport code **S**ystem
PHYSERD	**P**HITS-**HY**ENEXSS integrated code **S**ystem for **E**ffects of **R**adiation on **D**evices
pMOS	**p**-type **MOS**
PW	**P**ulse **W**idth
RCNP	**R**esearch **C**enter for **N**uclear **P**hysics
SBU	**S**ingle **B**it **U**pset
SEB	**S**ingle-**E**vent **B**urnout
SECDED	**S**ingle-bit **E**rror **C**orrection **D**ouble-bit **E**rror **D**etection
SEE	**S**ingle-**E**vent **E**ffect
SEFI	**S**ingle-**E**vent **F**unctional **I**nterupt
SEGR	**S**ingle-**E**vent **G**ate **R**upture
SEL	**S**ingle-**E**vent **L**atchup
SER	**S**oft **E**rror **R**ate
SEU	**S**ingle-**E**vent **U**pset
SoC	**S**ystem-**o**n-a-**C**hip
SRAM	**S**tatic **R**andom **A**ccess **M**emory
SRIM	**S**topping and **R**ange of **I**ons in **M**atter
SULA	**S**uper **U**ltra-**L**ow **A**lpha
TDDB	**T**ime-**D**ependent **D**ielectric **B**reakdown
TPA	**T**wo-**P**hoton **A**bsorption
ULA	**U**ltra-**L**ow **A**lpha
WCSI	**W**ell-**C**ollapse **S**ource-**I**njection
WL	**W**ord **L**ine

Chapter 1

Introduction

1.1 Soft Errors in Semiconductor Devices

Today, electronic systems are highly dependent on semiconductor devices, such as microcontrollers and system-on-a-chips (SoCs), not only for their performance, but also for their dependability. The semiconductor devices have been evolved to meet the growing demand for more sophisticated systems, such as telecommunication infrastructures and Internet of Things (IoT) platforms. The key factor of this evolution has been the scaling of transistors, but, the scaling is approaching its physical limitation for planar field effect transistors (FETs). To overcome this limitation, three-dimensional (3D) structures have been adopted for the transistors in recent years. In advanced complementary metal-oxide-semiconductor (CMOS) technologies, fin-shaped field-effect transistors (FinFETs) are the most common 3D transistors. As illustrated in Fig. 1.1, the triple gate structure of the FinFETs suppresses short channel effects and provides better electrical characteristics compared to the planar FETs. Meanwhile, the reliability assurance of the semiconductor devices is becoming more challenging with the scaling and geometry change of the transistors. It is therefore essential to address reliability problems in the advanced semiconductor devices to ensure the dependability of current and future electronic systems.

Soft errors induced by radiation are one of the major problems that threaten the reliability of the semiconductor devices. The soft errors are transient errors with no permanent damage on the devices, in contrast to hard errors, such as hot carrier injection (HCI), bias temperature instability (BTI), and time-dependent dielectric breakdown (TDDB). Thanks to this nondestructive nature, malfunctions caused by the soft errors can be recovered by power cycling or resetting of the devices, whereas that caused by the hard errors cannot. However, the soft errors significantly degrade the dependability of mission critical systems, where the power cycling and resetting are not always possible. An important point here is that the mission critical systems are becoming widespread and ubiquitous in contemporary society. One example for such systems is automated driving systems, in which failures in the system can result in serious accidents and hence transient errors in the semiconductor devices should be completely suppressed. Another example is networking systems, which are essential to provide internet services and require continuous operation without

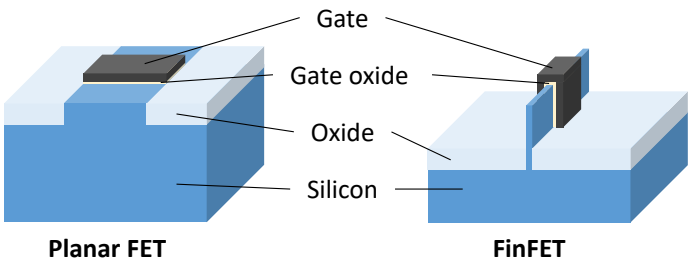

FIGURE 1.1: Schematic structures of planar FET and FinFET.

any interruptions. Thus, the soft error problem can undermine the safety and well-being of the society.

In modern semiconductor devices, the soft errors are caused by terrestrial radiation, such as secondary cosmic-rays and alpha particles. Here, charge deposition induced by such ionizing radiation is the origin of the soft errors. Historically, the soft errors were considered as a problem in space applications, where the semiconductor devices are exposed to hazardous space radiation, such as primary cosmic rays and solar flares. The first report on the soft errors was satellite anomalies caused by unexpected triggering of flip-flops (FFs) in 1975 [1]. After that, in 1978, the soft errors in terrestrial applications were reported for the first time in dynamic random access memories (DRAMs), where the radiation source was alpha particles emitted from radioisotopes in package materials [2]. In 1993 and 1994, it was evidenced that the soft errors in static random access memories (SRAMs) and DRAMs are caused by atmospheric neutrons, which are a part of the secondary cosmic-rays [3], [4]. Since then, the soft errors have become one of the major challenges with increased integration of semiconductor devices used in terrestrial applications. As a result, considerable efforts have been devoted to understand and mitigate the terrestrial radiation-induced soft errors [5]–[9].

An important concern for the soft errors is an increased susceptibility to the terrestrial radiation in advanced semiconductor devices. This is due to the aggressive scaling of CMOS technologies in terms of physical size and supply voltage. The smaller size and lower voltage result in the decreased amount of charge necessary for representing logic states, “0” and “1”, in semiconductor circuits. This leads to the increased vulnerability to electric noises induced by ionizing radiation. In other words, for the scaled devices, unexpected alterations in the logic states are more likely to be caused by the terrestrial radiation. In addition to this scaling, as described above, the FinFETs have been introduced in advanced CMOS technologies. Since the geometry of the FinFETs is significantly different from that of the conventional planar FETs, the responses to the terrestrial radiation are expected to be different from each other. Therefore, it is necessary to investigate and understand the impact of the terrestrial radiation on the advanced planar and FinFET devices.

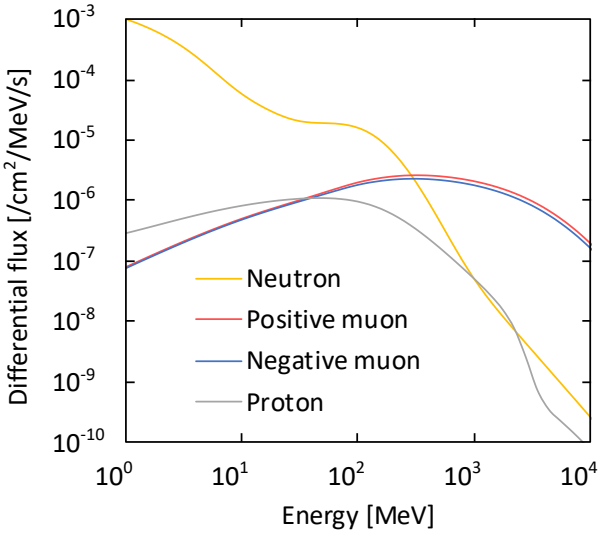

FIGURE 1.2: Energy spectra of neutrons, muons, and protons at sea level, New York City obtained from EXPACS [12].

1.2 Terrestrial Radiation

In the terrestrial environment, secondary cosmic-rays and alpha particles from natural radioisotopes are the main radiation sources of the soft errors [7]. The secondary cosmic-rays are constantly produced in the atmosphere by primary cosmic-rays. On the other hand, the natural radioisotopes are inherently present in the materials of the semiconductor devices. Basically, the soft errors caused by the radioisotopes can be reduced by employing materials with low radioisotope content, whereas that caused by the secondary cosmic-rays cannot be suppressed by changing the materials. Therefore, the secondary cosmic-rays are a primary concern for the terrestrial soft errors in recent semiconductor devices [10].

The secondary cosmic-rays originate from interactions between primary cosmic-rays and the Earth's atmosphere. The primary cosmic-rays are predominantly composed of protons ($\sim$ 90%), the energy of which ranges from 10 MeV to 10^{20} eV [11]. When this high-energy protons strike the atmosphere, some of the protons interact with atmospheric atoms, and cascades of various particles are invoked [10]. The particles produced through the cascades are the so-called secondary cosmic-rays. At sea level, the secondary cosmic-rays consist mainly of neutrons, protons, muons, electrons, and photons [1]. Among these particles, the electrons and the photons cannot cause the soft errors. The energy spectra and integral fluxes of the neutrons, the protons and the muons at sea level are shown in Fig. 1.2 and Table 1.1, respectively, where the data are based on Excel-based Program for calculating Atmospheric Cosmic-ray Spectrum (EXPACS) [12]. The muons are the most abundant particles at sea level. The next most abundant particles are the neutrons. At the present time, the neutrons are considered as a major contributor to the terrestrial soft errors [10].

[1] The particles reaching the ground are often called terrestrial cosmic-rays.

TABLE 1.1: Integral fluxes above 1 MeV for neutron, muon, and proton at sea level, New York City estimated from Fig. 1.2.

Particle	**Flux [/cm^2/h]**
Neutron	21
Proton	1.3
Positive muon	37
Negative muon	31

TABLE 1.2: Alpha particle emissivities of device materials [18].

Material	**Emissivity [/cm^2/kh]**
30 μm thick Cu metal	< 0.3
20 μm thick AlCu metal	< 0.3
Mold compound	$< 24 - < 0.5$
Flip chip underfill	$< 4 - < 0.7$
Pb-based solders	$< 7.2 \times 10^3 - < 0.9$

Importantly, on the other hand, there is an increasing concern that the muons can be a source of the soft errors in advanced semiconductor devices [13], [14].

The alpha particles originate from the decay of natural radioisotopes in the device materials, such as packages and metal layers. In most cases, the package materials, such as mold resin and solders, are the primary source. In these materials, radioisotopes are naturally present and emit the alpha particles. The emissivity of the alpha particles depends on the abundance of radioisotopes, and hence it varies depending on the materials [15]–[17]. The typical emissivities of the device materials are given in [18], and are presented in Table. 1.2. In the materials used in manufacturing processes, there are several classes with respect to the alpha particle emissivity: low alpha (LA), ultra-low alpha (ULA), and super ultra-low alpha (SULA). The emissivities for the LA, ULA, and SULA classes are generally $2 - 20$ /cm^2/kh, < 2 /cm^2/kh, and < 1 /cm^2/kh, respectively. Obviously, by replacing the device materials with, for example, the SULA materials, the soft errors induced by the alpha particles can be suppressed. However, the alpha particle-induced soft errors are still a concern because such replacement may not be allowed due to the increased cost of products.

As described above, the neutrons, the muons, and the alpha particles are major concerns for the terrestrial soft errors in advanced semiconductor devices. In the following subsections, basic characteristics of these particles are described to discuss their impacts on the soft errors in this thesis.

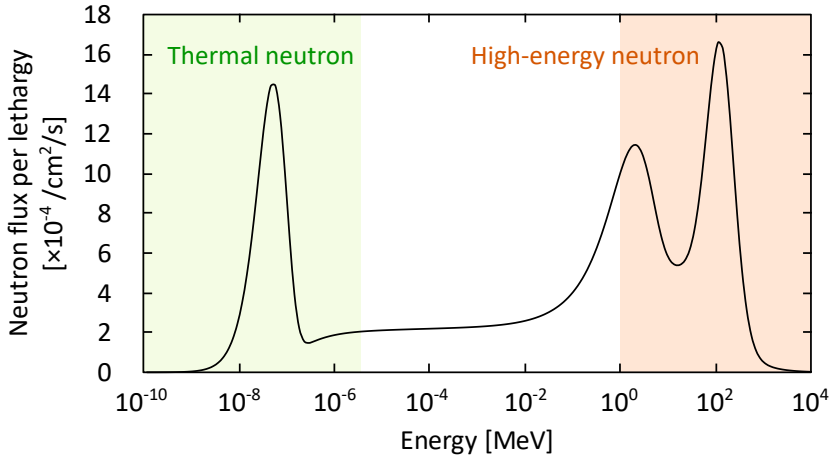

FIGURE 1.3: Energy spectrum of atmospheric neutrons at sea level, New York City obtained from EXPACS [12]. The vertical axis corresponds to (Energy) × (Differential flux).

1.2.1 Neutrons

The energy spectrum of the terrestrial neutrons ranges from thermal energy to high-energy. In Fig. 1.2, only the high-energy region (> 1 MeV) is shown. The full energy spectrum of the terrestrial neutrons is presented in Fig.1.3. In addition to the high-energy region, the spectrum has a considerable portion around 0.025 eV, i.e., thermal energy. Generally, neutrons with energies around 0.025 eV and above 1 MeV are called thermal neutrons and high-energy neutrons, respectively. In this spectrum at New York City, the fluxes of the thermal and high-energy neutrons are 10 /cm^2/h and 21 /cm^2/h, respectively. Importantly, the neutron energy spectrum varies with altitude, geomagnetic location, solar activity, and surrounding materials, and hence the flux also varies. For example, the flux of the high-energy neutrons at Tokyo is 12 /cm^2/h, which is smaller than that at New York City [12]. In the evaluation of the soft errors, the integral flux above 10 MeV at sea level, New York City is often used as the reference flux of the high-energy neutrons, where the value is 13 /cm^2/h [18]. For the thermal neutrons, the commonly used reference flux is 6.5 /cm^2/h, which corresponds to the integral flux below 0.4 eV at sea level, New York City [18].

The high-energy neutrons induce the soft errors through interactions with the materials of the semiconductor devices. The neutrons do not directly deposit charge to the devices because they are electrically neutral particles. The charge deposition is induced by secondary ions produced through spallation reactions and recoil reactions in the semiconductor devices. For silicon-based devices, the most important ones are the reactions between the high-energy neutrons and Si atoms, in which various secondary ions are produced: for example,

$$^{28}\mathrm{Si} + \mathrm{n}_{\text{high-energy}} \rightarrow {}^{24}\mathrm{Na} + \alpha + \mathrm{p}. \tag{1.1}$$

Fig. 1.4 presents the secondary ions produced by the high-energy neutrons with

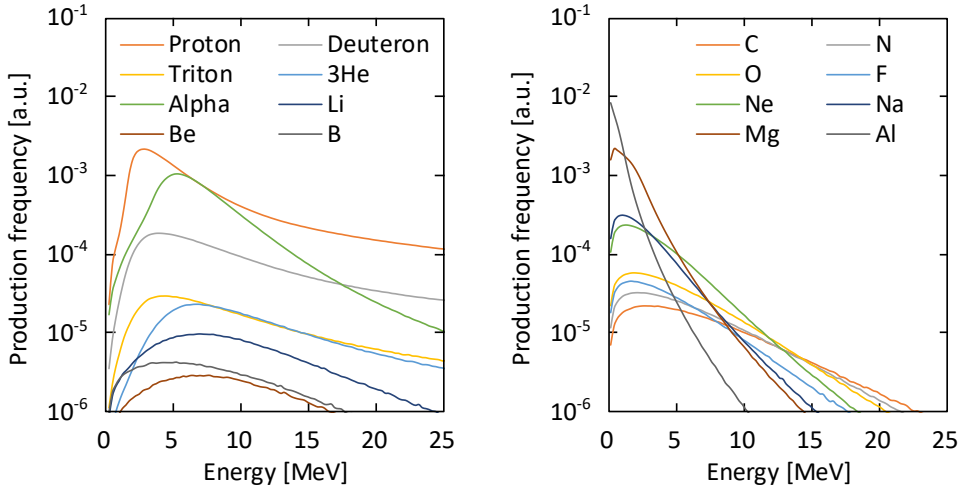

FIGURE 1.4: Secondary ions produced by terrestrial high-energy neutrons as a function of energy calculated using PHITS [19].

the terrestrial energy spectrum, which are calculated using Particle and Heavy Ion Transport code System (PHITS) [19]. The produced ions range from light elements to heavy elements, where protons are the most abundant element. These secondary ions travel inside the devices and deposit charge along their tracks by ionization. The amount of the charge deposition is often expressed by linear energy transfers (LETs). The LET is defined as the amount of energy loss per unit length. In Fig. 1.5(a), the LETs in silicon for protons, alpha particles, lithium ions, sodium ions, and aluminum ions are shown as a function of the energy, where the calculation is conducted using Stopping and Range of Ions in Matter (SRIM) [20]. The LET depends on the atomic number and energy of ions, as seen in Fig. 1.5(a). Basically, heavier ions have higher LETs and hence can induce larger charge deposition to the semiconductor devices. On the other hand, the ranges of the heavier ions are shorter than those for lighter ions, as shown in Fig. 1.5(b). An interesting feature of the ion energy loss is that the LET reaches its maximum at a certain energy specific to each ion. This LET maximum is called a Bragg peak. The energy at the Bragg peak decreases with the decrease in the atomic number, as observed in Fig. 1.5(a).

The variety of the secondary ions produced through the interactions between the high-energy neutrons and the device materials results in the broad distribution of the LET. Fig. 1.6 presents a calculation result of the total track length of secondary ions produced in silicon by the high-energy neutrons as a function of their LETs. In this figure, the total track length reflects the number and range of the secondary ions. In other words, the larger number and longer range of the secondary ions with a certain LET results in the longer track length at the LET. As confirmed in Fig. 1.6, the total track length in silicon decreases with increased LET. This means that charge deposition by low-LET ions occurs more frequently than high-LET ions. According to this distribution, the maximum LET is $\sim$ 14 MeV cm^2/mg. It is worthwhile to note that, in addition to the secondary ions produced through interactions

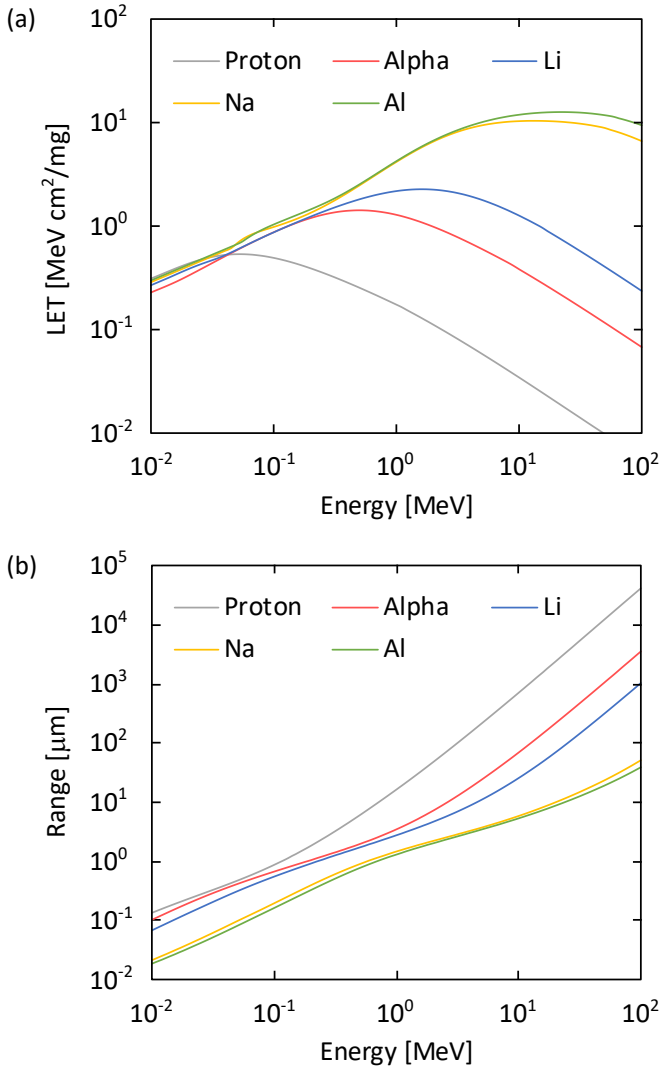

FIGURE 1.5: (a) LETs and (b) ranges in silicon for protons, alpha particles, lithium ions, sodium ions, and aluminum ions as a function of energy calculated by SRIM [20].

with silicon, those produced through interactions with high-Z materials are also important. This is because the semiconductor devices consist not only of silicon but also of high-Z elements, such as copper, tungsten, and cobalt. The interactions between these high-Z elements and the high-energy neutrons can produce secondary ions with higher-LET than 14 MeV cm^2/mg, leading to larger charge deposition. It is thus necessary to consider the device structure including both silicon and metals for correctly understanding the impact of the high energy neutrons.

Another noteworthy feature of the high-energy neutrons is the anisotropic angular distribution of flux in the terrestrial environment. The angular distribution is expressed as $\cos^n \theta$, where θ denotes the zenith angle. In this expression, the reasonable value of the exponent n has been reported as 3 at sea level [21]. This means that the large portion of the high-energy neutrons is directed downward at sea level.

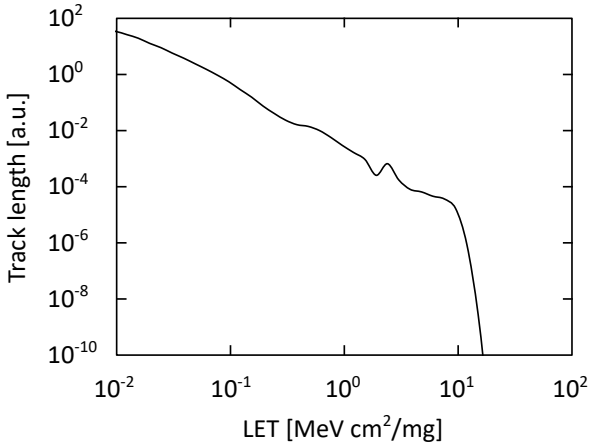

FIGURE 1.6: Total track length of secondary ions produced in silicon by terrestrial high-energy neutrons as a function of their LETs calculated using PHITS [19]. The total track length reflects the number and range of the secondary ions with each LET.

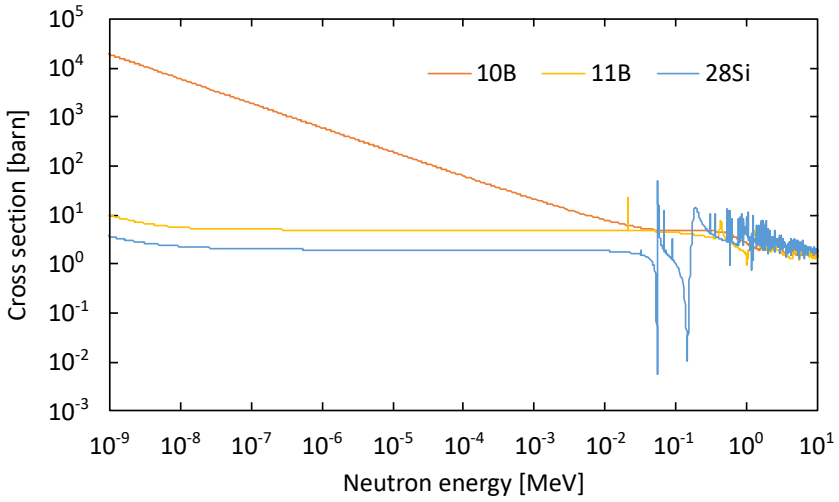

FIGURE 1.7: Cross sections of neutron-induced nuclear reactions for ^{28}Si, ^{10}B, and ^{11}B atoms as a function of energy obtained from JENDL 4.0 [23] using JANIS [24].

This anisotropic angular distribution can impact on charge deposition in the semiconductor devices because the emission angle of the secondary ions depends on the incident direction of the high-energy neutrons. It is known that the secondary ions produced through spallation reactions tend to be emitted forward, i.e., to the same direction of neutron incidence [22]. These features awaken a concern that the mounting direction of the semiconductor devices may affect the susceptibility to the high-energy neutrons in the terrestrial environment. Therefore, the angular sensitivity of the high-energy neutron-induced soft errors is one of the fundamental issues in terrestrial devices.

For the thermal neutrons, the soft errors are induced by interactions with ^{10}B atoms, and hence the sensitivity to the thermal neutrons depends on the abundance of the ^{10}B atoms in the semiconductor devices. There are two isotopes in natural

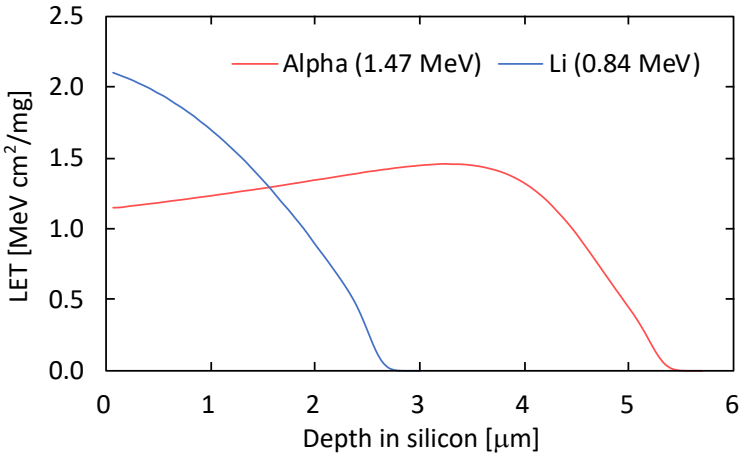

FIGURE 1.8: LETs in silicon for an alpha particle of 1.47 MeV and a lithium ion of 0.84 MeV as a function of depth calculated by SRIM [20].

boron: ^{11}B (80%) and ^{10}B (20%). One of the reasons why only the ^{10}B atom is considered is its large cross section (CS) of nuclear reaction for the thermal neutron. Here, the nuclear reaction CS is defined as the effective area where a target atom can interact with a neutron. In other words, the large CS means the high probability of nuclear reaction. The nuclear reaction CSs for the ^{10}B and ^{11}B atoms are compared in Fig. 1.7, where the CS for ^{28}Si atoms is also shown. The CS for the ^{10}B atoms at around 0.025 eV is $\sim 10^4$ barn [2], which is larger than that for the ^{11}B and ^{28}Si atoms by more than three orders of magnitude. Another reason is the production of secondary ions by the fission of the ^{10}B atoms in neutron capture reaction. When a ^{10}B atom captures a thermal neutron, a lithium ion, an alpha particle, and a photon (gamma-ray) are emitted:

$$^{10}\mathrm{B} + \mathrm{n}_{\mathrm{thermal}} \rightarrow {}^{7}\mathrm{Li}\ (0.84\ \mathrm{MeV}) + \alpha\ (1.47\ \mathrm{MeV}) + \gamma\ (0.48\ \mathrm{MeV}), \tag{1.2}$$

where no photon is emitted in 6% of the reactions [25]. On the other hand, when a ^{11}B atom captures a thermal neutron, only a photon is emitted. In the capture reaction of the ^{10}B atoms, these secondary ions can cause the soft errors through their ionization. The LETs of these ions are shown in Fig. 1.8 as a function of depth in silicon, where the maximum LET is ~ 2 MeV cm^2/mg. It is worthwhile to point out that the maximum LET induced by the thermal neutrons is considerably lower than that induced by the high-energy neutrons, which ~ 14 MeV cm^2/mg. [see Fig. 1.6]. Furthermore, the emission direction of the secondary ions is different between the thermal neutrons and the high-energy neutrons. The secondary ions produced in the neutron capture reaction of the ^{10}B atoms are emitted isotropically, whereas those produced in the spallation reactions induced by the high-energy neutrons are emitted forward, as described above.

[2] 1 barn equals to 10^{-24}cm^2.

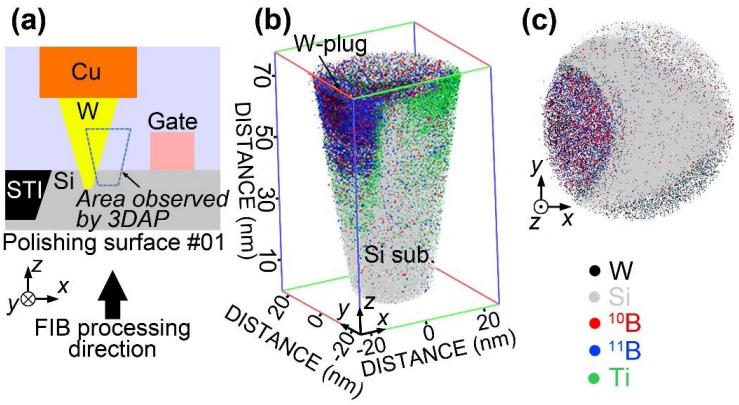

FIGURE 1.9: 3DAP analysis of ^{10}B atoms in a tungsten plug (reconstructed from [26]). (a) Schematic diagram of the device area used in 3DAP observation. (b) Reconstructed 3D image. (c) Projected image of the reconstructed 3D image along the z-direction.

In recent semiconductor devices, the ^{10}B atoms are introduced at the layer of tungsten plugs that serve as contacts between the transistors and the first metal layer. In past devices, the origin of the ^{10}B atoms was borophosphosilicate glass (BPSG), which was used as a dielectric layer above transistors [27]. For semiconductor devices using the BPSG, the thermal neutrons were considered as a primary source of the terrestrial soft errors [28]. As chemical-mechanical polishing (CMP) was introduced, the BPSG was removed from the device structure, and hence the thermal neutron-induced soft errors were completely suppressed. However, recent manufacturing processes have employed diborane (B_2H_6) gass instead of silane (SiH_4) gass to improve the performance of the tungsten plugs. The ^{10}B atoms are present in this diborane gass and remain around the tungsten plug layer of the devices [29]. For example, as shown in Fig. 1.9, the presence of the ^{10}B atoms was confirmed at the position of the tungsten plug by 3D atom probe (3DAP) analyses [26]. As a result, the thermal neutron-induced soft errors have reemerged as an issue of the terrestrial soft errors.

1.2.2 Muons

The atmospheric muons consist of negative and positive muons and are the most abundant particle in the secondary cosmic-rays. From the energy spectra shown in Fig. 1.2, the total integral flux above 1 MeV for the negative and positive muons is 68 /cm^2/h, which is more than three times higher than that for the high-energy neutrons [see Table 1.1]. As seen in Fig. 1.2, a large portion of the negative and positive muons are in the energy range above 100 MeV. The above difference in the integral flux between the muons and the high-energy neutrons mainly reflects the flux difference above 100 MeV. This high abundance of the muons is one of the reasons why the muons are concerned in terrestrial soft errors.

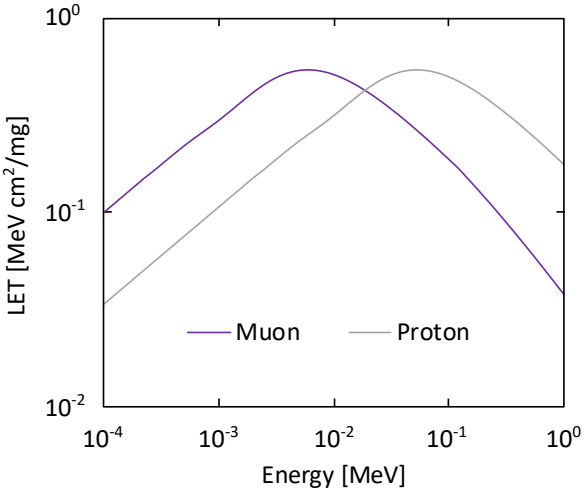

FIGURE 1.10: LETs in silicon for muons and protons as a function of energy calculated by SRIM [20].

Unlike the neutrons, the muons are charged particles and hence can directly deposit charge to the semiconductor devices by ionization. Here, both the negative and positive muons (μ^- and μ^+) are unstable particles with the mean lifetime of 2.2 μs and decay into three particles:

$$\begin{aligned} \mu^- &\rightarrow e^- + \bar{\nu}_e + \nu_\mu \\ \mu^+ &\rightarrow e^+ + \nu_e + \bar{\nu}_\mu, \end{aligned} \tag{1.3}$$

where e^- and e^+ are electron and positron, ν_e and $\bar{\nu}_e$ are electron neutrino and electron antineutrino, ν_μ and $\bar{\nu}_\mu$ are muon neutrino and muon antineutrino, respectively. Although the decayed electrons and positrons are also charged particles, their impact on the soft errors is negligible because their LETs are very low. Fig. 1.10 presents the LETs in silicon for muons and protons as function of the energy. It should be noted that the LETs of the negative and positive muons are almost identical [30]. The LET of the muons is similar to that of the protons, where the maximum LET is $\sim$ 0.5 MeV cm^2/mg. The discrepancy in the Bragg peak energy is due to the mass difference between the muons and the protons, where the mass of the muons is about one ninth of the mass of the protons [31]. As described above, the proton is one of the secondary ions produced by the high-energy neutrons, and its LET is lower than the other secondary ions [see Fig. 1.5(a)]. This means that the LET of the muons is relatively low compared to the LETs of the secondary ions produced by the high-energy and thermal neutrons. The key point here is that, with the scaling of transistors, the semiconductor devices have become more vulnerable to small charge deposition, i.e., low-LET particles. For this reason, there have been increasing concerns about the muon-induced soft errors in advanced semiconductor devices.

In addition to the direct ionization of the muons, the negative muons can produce secondary ions through muon capture reactions, whereas the positive muons

TABLE 1.3: Energy of alpha particles emitted from radioisotopes in the decay chain of thorium [33].

Radioisotope	Half life	Energy [MeV]
^{232}Th	1.41×10^{10} y	4.013
^{228}Th	1.91 y	5.423
^{224}Ra	3.66 d	5.685
^{220}Rn	55.6 s	6.288
^{216}Po	0.15 s	6.778
^{212}Po	0.296 μs	8.784

cannot. When the negative muons stop in silicon, 66% of them are captured by silicon nucleus, and the remaining 34% decay as expressed in Eq. (1.3) [32]. In this capture reactions, similarly to the high-energy neutron-induced spallation reactions, various secondary ions are produced: for example,

$$^{28}\mathrm{Si} + \mu^- \rightarrow {}^{24}\mathrm{Na} + \alpha. \tag{1.4}$$

The resulting secondary ions have higher-LETs than the negative muons and hence can deposit a large amount of charge to the semiconductor devices. An important difference between the muon capture reactions and the neutron-induced spallation reactions is the difference in the emission direction of the secondary ions. In the case of the neutron-induced spallation reactions, the secondary ions are emitted forward. In the case of the muon capture reactions, on the other hand, the secondary ions are emitted isotropically, as is the case of thermal neutron capture reactions of ^{10}B atoms. This difference could lead to different impacts on the soft errors. Therefore, to properly characterize the negative muon-induced soft errors, it is essential to consider the muon capture reactions and the isotropic emission of the secondary ions.

1.2.3 Alpha Particles

The alpha particles are emitted from radioisotopes naturally present in the device materials (mainly packages), as already explained above. The radioisotopes of the primary concern for the soft errors are uranium and thorium and their decay products. For the decay chain of thorium, the radioisotopes emitting the alpha particles and the energy of the emitted alpha particles are listed in Table. 1.3 [33]. There are six radioisotopes emitting the alpha particles, the energy of which is in the range between 4 MeV and 9 MeV.

The emitted alpha particles can travel in the semiconductor devices and deposit charge through ionization. The LETs in silicon for the alpha particles with energies from 4.0 MeV to 8.5 MeV are presented in Fig. 1.11 as a function of depth in silicon. The maximum LET is $\sim$ 1.5 MeV cm^2/mg at the Bragg peaks. A noteworthy feature is the long range of the alpha particle. As confirmed in Fig. 1.11, the range of the

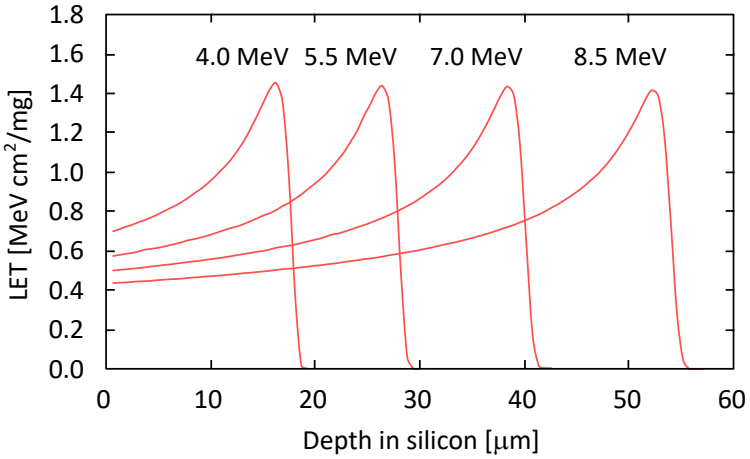

FIGURE 1.11: LET in silicon for alpha particles with energies from 4.0 MeV to 8.5 MeV as a function of depth calculated by SRIM [20].

alpha particle with 5.5 MeV is 29 μm in silicon, which is larger than the scale of the semiconductor device structure, e.g. the thickness of metal layers. This means that the alpha particles emitted in the region of packages can pass through the metal layers of the devices and can reach the region of transistors. This is the reason why the radioisotopes in the packages are of concern in the terrestrial soft errors.

1.3 Single-Event Upsets in SRAMs

SRAMs are fundamental memory elements in semiconductor devices because of their high-speed operations. In recent CMOS technologies, SRAM devices are the most susceptible to the terrestrial radiation-induced soft errors [34]. One of the reasons for this is that the size of SRAM cells is considerably small compared to other types of circuit cells, such as latches and FFs. The SRAM cell size has been aggressively scaled down and reaches less than 0.1 μm^2 in advanced CMOS technologies [35]. As already mentioned, this size scaling leads to increased vulnerability to radiation-induced charge deposition. Another reason is that, in modern semiconductor devices, such as SoCs, the amount of embedded SRAMs is rapidly growing, and hence the soft errors in the SRAMs can be dominant compared to those in latches, FFs, and combinational logic [34]. Therefore, the impact of the terrestrial radiation on the SRAM devices is of primary concern in the terrestrial soft errors.

1.3.1 SRAM Circuit

In the SRAM cell, the data value is represented as the voltage levels of two internal nodes of the SRAM circuit. The standard SRAM circuit consists of six transistors: four n-type MOS (nMOS) transistors and two p-type MOS (pMOS) transistors. The schematic circuit and physical layout of the SRAM cell are illustrated in Fig. 1.12. As seen in this illustration, two inverters are connected in a cross-coupled fashion,

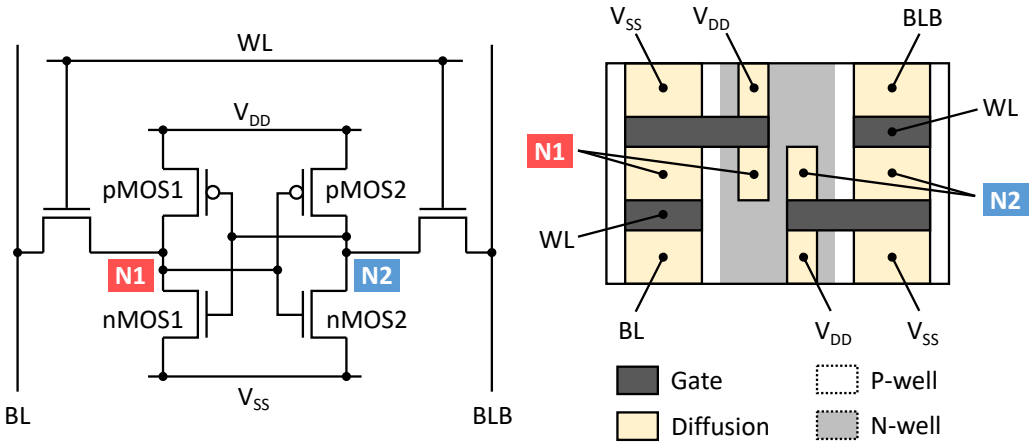

FIGURE 1.12: SRAM circuit (left) and schematic cell layout (right).

making a latch circuit. At the same time, two nMOS transistors serve as transfer gates between bit lines (BLs) and the two internal nodes of this latch circuit. In Fig. 1.12, the BLs are denoted as BL and BLB, and the internal nodes are denoted as N1 and N2. The states of the transfer gates are controlled by a word line (WL), which is connected to the gates of these nMOS transistors. In write and read operations of the SRAM cell, the WL is set to high (V_{DD}) so as to open the transfer gates. Once the transfer gates are opened, the voltage levels of the two internal nodes, N1 and N2, can be altered or read via the BLs. There are two stable sates of the internal nodes, which represent the data values: "0" and "1." Specifically, if one pair of voltage levels (N1, N2) = (high (V_{DD}), low (V_{SS})) is defines as the value "1," another pair (N1, N2) = (low (V_{SS}), high (V_{DD})) is the value "0." Since the standard SRAM circuit is a symmetric circuit and the physical layout is symmetric as well, the states of "0" and "1" are topologically identical. Therefore, the noise margins for these two states are essentially the same.

The key point is that the difference in the voltage level of the internal node corresponds to the different amount of charge stored in the node. The amount of charge stored in the high (V_{DD}) node can be expressed as $C_{node} \times V_{DD}$, where C_{node} denotes the capacitance of the internal node. The capacitance C_{node} comprises the gate capacitances of the transistors and various parasitic capacitances inherent in the SRAM cell. Hence, the size scaling of the transistors and the SRAM cell decreases C_{node}, resulting in the reduced amount of charge stored in the node. Similarly, the scaling of the supply voltage V_{DD} also reduces the amount of stored charge. For these reasons, the amount of charge to represent the data value of the SRAM cell decreases with the scaling of CMOS technologies. This apparently leads to the increased vulnerability of the SRAM cells to radiation-induced charge deposition.

1.3.2 Single-Event Upset

The most common type of soft errors in the SRAM devices is single-event upsets (SEUs), in which data values stored in one or more SRAM cells are flipped by a single particle strike. When a particle strike deposits charge on an SRAM cell, some charge is collected in the internal nodes. This charge collection can induce a noise current in the SRAM circuit. If the charge collection is significant and the resulting noise current exceeds the noise margin of the SRAM circuit, the internal nodes undergo transition from the current state to another stable state: for example, (N1, N2) = (high, low) $\rightarrow$ (N1, N2) = (low, high) in the circuit presented in Fig. 1.12. As a result, a wrong data value is stored in the SRAM cell. Since this state transition is a reversible phenomenon with no permanent damage, the wrong data value can be corrected by rewriting the SRAM cell. Therefore, the SEUs are soft errors.

In the physical layout of the SRAM cell, the drain diffusion area of the nMOS transistor in the high node is generally the most sensitive to the particle-induced charge deposition [5]. Basically, the SEUs can occur when transient currents are induced in the off-state transistors of the SRAM circuit. In this sense, both the nMOS transistor in the high node and the pMOS transistor in the low node are sensitive to the charge deposition for the SEU occurrence. On the other hand, there is the difference in the size and driving power between the nMOS and pMOS transistors. In most cases, the size of the nMOS transistor is designed to be larger than that of the pMOS transistor to maximize the performance of the SRAM cell [36]. In this case, the charge collection in the nMOS transistor is more efficient than that in the pMOS transistor because the transient current is generated by charge collection at the drain diffusion and the drain area increases with the size of transistors. At the same time, the driving power is stronger for the nMOS transistors than for the pMOS transistors. Hence, the low node is more resilient to the transient current than the high node because the low level (V_{SS}) is kept by the nMOS transistors. For these reasons, the nMOS transistor in the high node is the dominant contributor to the SEU occurrence. As an example, Fig. 1.13 presents a simulation result comparing the contributions of the nMOS and pMOS transistors to the SEU occurrence in a 28-nm bulk planar SRAM [37]. As confirmed in this result, the contribution of the nMOS transistor is dominant, more than 90% in this case. The significant contribution of nMOS transistors was also demonstrated in FFs [38].

One of the important parameters indicating the SEU susceptibility of an SRAM circuit is a critical charge, which is denoted as Q_{crit}. The critical charge is the minimum amount of collected charge required for the SEU occurrence. Hence, the SEU susceptibility increases with the decreased critical charge. In the first order approximation, the critical charge equals to the amount of charge stored in the internal node of the SRAM cell: $Q_{crit} \sim C_{node} \times V_{DD}$. Therefore, the increased SEU susceptibility due to the scaling of the supply voltage and the SRAM cell size can be interpreted as the lowering of the critical charge. It should be noted that the critical charge is different between the high and low nodes of the SRAM circuit. As explained above,

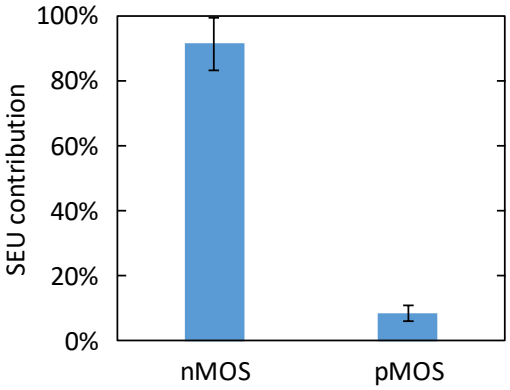

FIGURE 1.13: Simulated SEU contribution of nMOS and pMOS transistors in a 28-nm bulk planar SRAM (reconstructed from [37]).

the high node is typically more vulnerable to transient currents than the low node. This difference leads to the lower critical charge for the high node than for the low node.

1.3.3 Classification

The SEUs are a subset of single-event effects (SEEs) and can be divided into several types of error events. The SEEs include both soft errors and hard errors and are defined as any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system resulting from a single energetic particle strike [18]. Although the major type of soft errors in the SRAM devices is the SEUs, it is worthwhile to describe the classification of the SEEs including phenomena other than the SEUs.

The classification of the SEEs is explained in Fig. 1.14. There are six types of phenomena in the SEEs: SEU, single-event transient (SET), single-event functional interrupt (SEFI), single-event latchup (SEL), single-event gate rupture (SEGR), single-event burnout (SEB). Among these phenomena, the SEGR and the SEB are problems mostly in power devices and are categorized as hard errors with permanent damage on the devices. The SEL is a latchup triggered by a single particle strike, where parasitic thyristors inherent in CMOS structures turn on and high-current flow is induced in semiconductor devices. When the level and duration of the current flow is enough for causing permanent damage on the devices, the SEL is considered as hard errors. Otherwise, the SEL is considered as soft errors because the high-current state can be recovered by power cycling. The SET and the SEFI cause transient errors without permanent damage on the devices and hence categorized as soft errors, as is the case of the SEU. The SET indicates a transient noise in semiconductor circuits induced by a single particle strike. It can said that the SEU is induced by the SET in SRAM circuits. The SEFI also can be considered to be induced by the SET. In the soft errors of the SRAM devices, the SEFI corresponds to transient malfunctions of peripheral circuits, such as address decoders and sense amplifiers. The impact of the

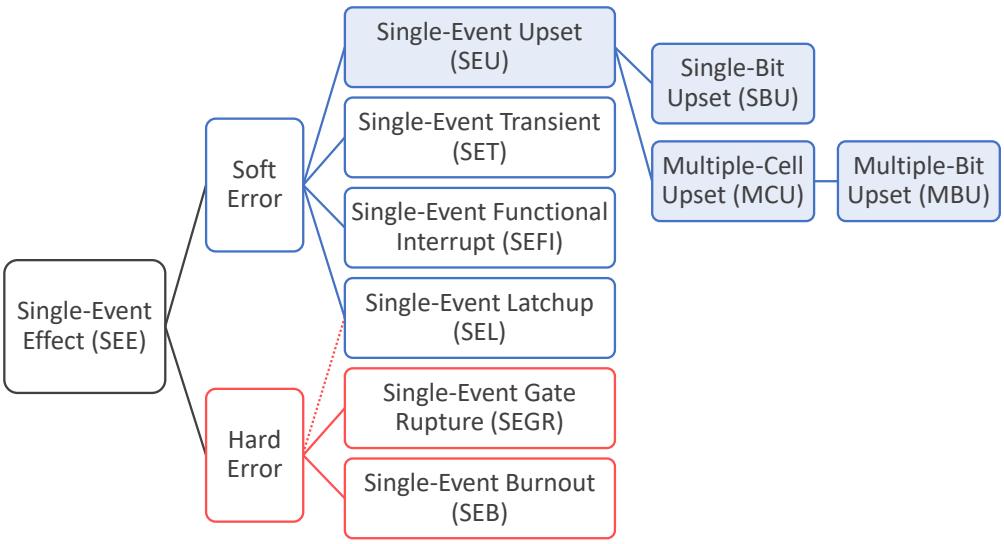

FIGURE 1.14: SEE classification. This thesis focuses on SEUs.

peripheral circuits is generally less significant compared to that of the SRAM cells because the area of the peripheral circuits is smaller than that of the SRAM cell arrays. Hence, this thesis focuses on the soft errors in the SRAM cells, and emphasis is given to the SEUs.

The SEUs consist of single-bit upsets (SBUs) and multiple-cell upsets (MCUs), where the MCUs include multiple-bit upsets (MBUs). The SEU events are divided into these categories according to the condition of fail bits induced in the SRAM devices. The SBU events are error events where a single fail bit is induced by a single particle strike. The MCU events are error events where multiple fail bit are simultaneously induced by a single particle strike. The MBU events are a particular case of the MCU events, where multiple fail bits are induced in the same logical word. Among these categories, the MBUs are the most critical events from the reliability point of view. This is because the MBU events cannot be corrected by standard error correction codes (ECCs), where single-bit error correction double-bit error detection (SECDED) is commonly used. To suppress such uncorrectable errors, bit-interleaving methods are often employed, where same logical words are assigned to physically distant BLs. However, the effectiveness of this method can degrade when the physical locations of fail bits in an MCU event spread over multiple BLs. Therefore, the investigation of the MCU and MBU responses to the terrestrial radiation is particularly important for evaluating the efficiency of SEU mitigation techniques using the ECCs and bit-interleaving.

1.3.4 SEU CS and SEU Rate

The SEU susceptibility of the SRAM devices is generally expressed by SEU CSs and SEU rates, where the SEU rates are often referred as soft error rates (SERs). The SEU CSs are commonly given in the units of cm^2/bit or cm^2/Mbit. The SEU rates

are commonly given in the units of FIT/Mbit or FIT/device. Here, FIT is failure in time (FIT) and is defined as the average number of failures in one billion (10^9) hours of device operation. It is worthwhile to note that the FIT can be converted to mean time between failure (MTBF), which is the average time of device operation between failures. From the definition of the FIT, the MTBF corresponding to 1 FIT is 10^9 hours.

The SEU CS is an intrinsic parameter representing the area sensitive to a single particle strike in the SRAM cell, where the larger SEU CS means the higher SEU susceptibility of the SRAM cell. Since, as explained above, the sensitive region in the cell layout mainly corresponds to the drain diffusion area of the nMOS transistors, the SEU CS typically increases with the size of the nMOS transistors. In addition to this layout dependence, the SEU CS depends on various factors involved in the SEU occurrence, such as particle type, critical charge, charge deposition, and charge collection. In other words, the SEU CS is the *effective* area influenced by SEU mechanisms. For example, when comparing high-energy neutrons and alpha particles, the SEU CS for the alpha particles is significantly higher than that for the high-energy neutrons by several orders of magnitude. This difference stems from the difference in the probability of the interactions with the device materials. In the case of the alpha particles, charge deposition is induced by the direct ionization. In the case of the high-energy neutrons, on the other hand, charge deposition is induced by secondary ions produced through nuclear reactions, where the occurrence probability of the nuclear reactions is quite low [3]. This results in the low probability of the charge deposition induced by a high-energy neutron strike, and hence the SEU CS is extremely low compared to the alpha particles.

The SEU rate, or the SER, is a practical metric representing the frequency of the SEU occurrence and is calculated as

$$\text{SEU rate} = \sigma_{\text{SEU}} \times \phi, \tag{1.5}$$

where σ_{SEU} and ϕ denote an SEU CS and a particle flux of interest, respectively. As expressed in this equation, the SEU rate increases with the increased particle flux. This means that the SEU rate is affected by radiation environment where the SRAM devices are used. Hence, to calculate the SEU rate, it is essential to specify the particle flux in the radiation environment of interest. For the terrestrial radiation, there are some reference fluxes commonly used in the evaluation of the SEU rates. In the case of the high-energy neutron, the reference flux is 13 /cm^2/h, which is the integral flux above 10 MeV for a reference energy spectrum [18]. The reference energy spectrum corresponds to the spectrum at sea level, New York City for mid-level solar activity. In the case of the thermal neutron, the reference flux is 6.5 /cm^2/h, which is the integral flux below 0.4 eV for the same conditions as the reference energy spectrum [18]. In the case of the alpha particle, the flux of 0.001 /cm^2/h is widely used as

[3] For a neutron of 10 MeV, the mean free pass in silicon is approximately 10 cm. This roughly corresponds to one nuclear reaction per ten thousand (10^4) neutrons for a 10 μm thick silicon target.

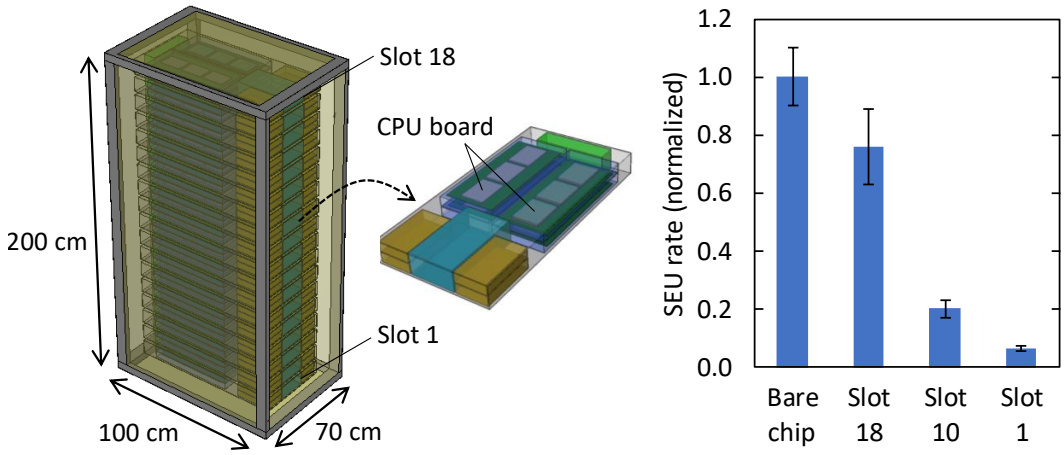

FIGURE 1.15: Simulated SEU rate reduction for terrestrial high energy neutrons due to the shielding effect of a server structure (reconstructed from [39]). The left figure depicts the model of the server structure. The right figure shows SEU rates for the slots 1, 10, and 18 normalized by that for the bare chip without the server structure.

the reference value. This flux corresponds to the alpha particle emissivity of SULA class materials.

The fluxes of the high-energy and thermal neutrons vary depending on surroundings, such as buildings and chassis enclosing the SRAM devices. The neutron flux can be attenuated through the scattering and absorption by the surrounding materials, i.e., shielding. As a result, the shielding effects have a considerable impact on the SEU rate [39], [40]. Fig. 1.15 presents a simulation result demonstrating the reduced SEU rate for the high-energy neutron due to the shielding effect of a server structure [39]. In this simulation, the SEU rate of 28-nm planar SRAMs in each slot is estimated using PHits-HYenexss integrated code System for Effects of Radiation on Devices (PHYSERD) with circuit simulation [41]. Since the high-energy neutrons are largely directed downward in the terrestrial environment, the lower slots benefit from the shielding effect, and hence the SEU rates for the lower slots are considerably reduced. As confirmed in Fig. 1.15, the SEU rate of the slot 1 is less than one tenth that without the server structure. It should be noted here that, in most cases, the benefit from the shielding effect is small because surrounding materials are not as heavy as the server structure.

1.3.5 Technology Dependence

The susceptibility to SEUs of the SRAM devices strongly depends on CMOS technologies, in terms of manufacturing processes, design parameters, and operation conditions. For the manufacturing processes, transistor geometries and impurity doping profiles affect charge deposition and charge collection induced by the terrestrial radiation. In addition, device materials also affect the radiation sensitivity. Specifically, as already described, the thermal neutron sensitivity is determined by

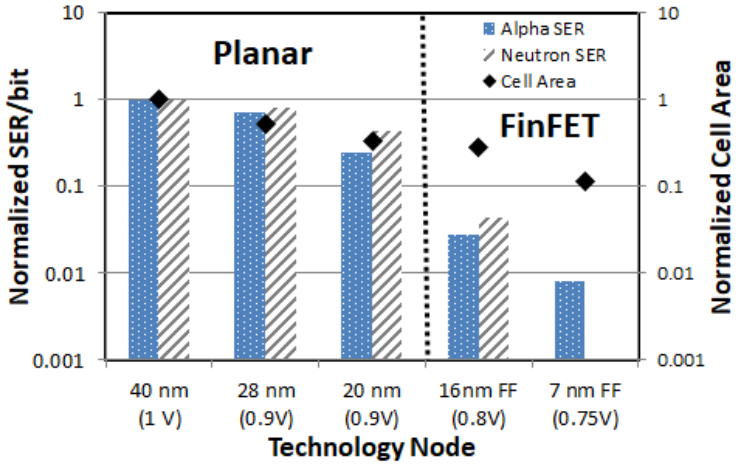

FIGURE 1.16: Technology trend of alpha particle- and high-energy neuton-induced SERs for SRAMs from a 40-nm planar to a 7-nm FinFET technologies [42]. The normalized area of the SRAM cells is also shown in the right vertical axis. ©[2018] IEEE.

the amount of ^{10}B atoms in the materials. For the design parameters, the size of the transistors and the physical layout of the SRAM cell affect the tolerance against transient noises caused by ionizing radiation. This is because the noise margin of the SRAM circuit is determined by the driving strength of the transistors and the overall capacitance of the SRAM cell. This noise margin corresponds to the critical charge from the aspect of the SEUs. As mentioned above, the size scaling of the SRAM cells decreases the critical charge and hence reduces the tolerance to the radiation-induced noises. Importantly, at the same time, this size scaling could lead to decreased radiation sensitivity. This is because, typically, the smaller size of the SRAM cell corresponds to the smaller drain diffusion area of the nMOS transistors, i.e., the smaller sensitive region in the cell layout. As a result, the SEU CS can decrease with the size scaling. In other words, there is the competing effects of the size scaling on the SEU susceptibility. As for the operation conditions, the power supply voltage of the SRAM devices is a primary factor affecting the SEU susceptibility. As explained above, the reduced supply voltage results in the decreased critical charge and hence leads to the increased SEU susceptibility.

In modern SRAM devices, the SEU CS, as well as the SEU rate and the SER, tends to decrease with the scaling of CMOS technologies [42]. This means that the impact of the shrinkage of the sensitive region is more significant than the impact of the reduction of the critical charge. It should be mentioned that this is not the case for the thermal neutron-induced SEU because its CS significantly depends on the amount of ^{10}B atoms in the device materials, which is different in each manufacturing process [43], [44]. Fig. 1.16 presents the technology trend of SERs for the high-energy neutrons and the alpha particles in SRAMs from a 40-nm planar to a 7-nm FinFET technologies [42]. The relative difference in the SRAM cell size (area) is also shown in this figure. This data clearly demonstrates the decreasing trend of the SERs with

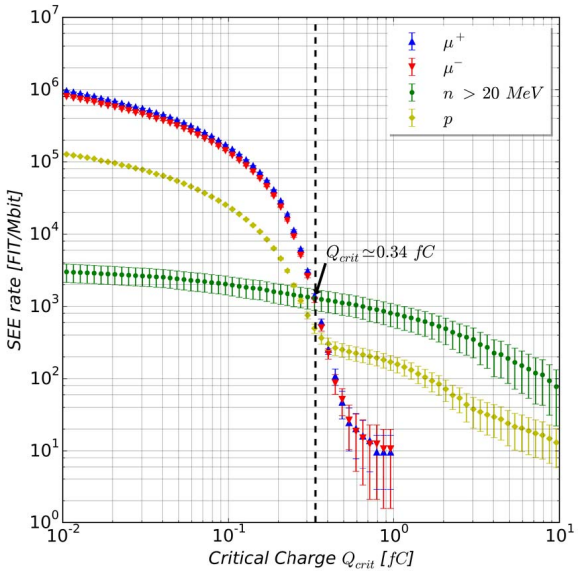

FIGURE 1.17: Simulated SER for terrestrial radiation particles as a function of critical charge [14]. ©[2017] IEEE.

the shrinkage of the SRAM cell size. Furthermore, the drastic SER reduction is found in the transition from a 20-nm planar to a 16-nm FinFET technologies. This is due to the geometry change of the transistors from planar to fin structures [45]. This geometry change leads to reduced charge deposition in the silicon region for the FinFETs because the silicon volume is smaller for the FinFETs than for the planar FETs [see Fig. 1.1]. Since the SEUs are caused by charge deposition in the silicon region of the transistors, the reduced charge deposition for the FinFETs results in the reduced SER in the FinFET technologies. Nevertheless, the SEUs are still a concern even in the FinFET technologies because the growing integration of SRAM devices can result in the higher SER at system level.

On the other hand, for the muon-induced SEUs, the scaling of CMOS technologies potentially increases the SEU rate of the SRAM devices. This is because the decreased critical charge results in the increased vulnerability to low-LET particles, such as the muons, and the muons are the most abundant particle in the secondary cosmic-rays. As already mentioned, the terrestrial radiation includes negative and positive muons. For the positive muons, the technology trend of the SER was experimentally demonstrated for SRAMs from a 65-nm planar to a 14-nm FinFET technologies, where the SER increases with the scaling of planar technologies and reduced with the transition from planar to FinFET technologies [46], [47]. For the negative muons, in contrast, only a few CMOS technologies were experimentally investigated, where the most scaled device is 28-nm planar SRAMs [48]–[50]. As shown in Fig. 1.17, simulation results indicate that both the positive and negative muons can be a primary source of the terrestrial radiation-induces SEUs in SRAM devices with low critical charges, i.e., highly scaled SRAM devices [14]. Furthermore, for the negative muons, recent experiments evidenced that muon capture reactions have significant impact of the negative muon-induced SEUs, where the SEU CS for the

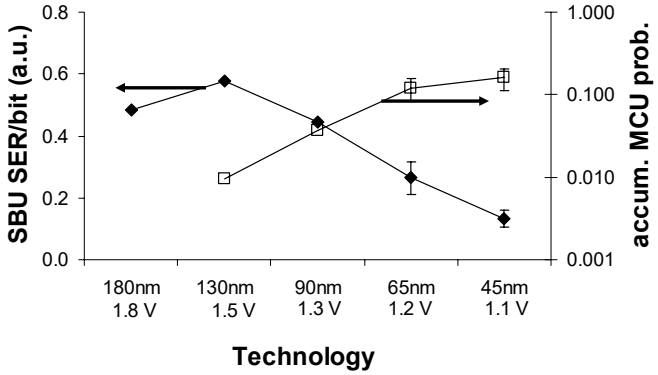

FIGURE 1.18: Neutron-induced SBU SER and MCU probability for SRAMs from a 180-nm to a 45-nm planar technologies [51]. ©[2008] IEEE.

negative muons is considerably higher than that for the positive muons [48]–[50]. Therefore, it is of importance to experimentally explore the negative muon-induced SEUs in more advanced SRAM devices.

Another important point to consider in advanced CMOS technologies is the increased susceptibility to MCUs. In a simple picture, MCU events are caused by charge deposition in multiple SRAM cells. Since the base material of the devices does not change with the technology scaling and is silicon, the range of charge deposition induced by an ionizing particle is independent of CMOS technologies. In this case, the size scaling of the SRAM cells can result in the higher probability of charge deposition in multiple SRAM cells, leading to increased occurrence of MCU events. Fig. 1.18 presents experimental results demonstrating the increasing trend of the MCU probability for SRAMs from a 180-nm to a 45-nm planar technologies [51]. Similarly, the size scaling can lead to increased occurrence of MBU events [52]. As described above, the MBU events degrade the efficiency of SEU mitigation techniques. Hence, it is necessary to investigate the characteristics of terrestrial radiation-induced MCUs and MBUs in advanced SRAM devices.

1.3.6 MCU Mechanisms

As the SRAM cells and the constituting transistors scale down, MCU mechanisms are becoming more and more complex, where the details of charge deposition and collection need to be considered. As already mentioned, the origin of the SEUs, as well as of the MCUs, is charge deposition on the SRAM devices by ionizing particles. This charge deposition is completely determined by the ionizing interaction between the particle and the device materials. The amount of the deposited charge increases with the LET of the particle. Here, the charge deposition corresponds to the generation of electron-hole pairs. In silicon, an electron-hole pair is generated by the energy deposition of 3.6 eV [53]. After this electron-hole pair generation, some electrons or holes need to be collected by the transistors for SEU occurrence. When this charge collection occurs in multiple SRAM cells, i.e., multiple transistors, the MCU

events can take place. The key point is that the charge collection is determined not only by the condition of the charge deposition but also by the transient responses of the transistors. Therefore, the physical range where the deposited charge is collected depends on both the initial distribution of the deposited charge and the complicated behaviors of the electrons and the holes in the transistors.

Focusing on the charge deposition, the large range of electron-hole pair generation obviously leads to the charge collection in multiple SRAM cells, i.e., MCU events. The total amount and spacial distribution of the generated electron-hole pairs depend on the LET and track of ionizing particles. In the situation where a high-LET particle travels along SRAM cell arrays, the pair generation can cover the multiple SRAM cells, and hence the MCU occurrence is highly probable. In other words, the susceptibility to the MCUs of the SRAM devices is a function of the particle type, energy, and track direction. When considering that the terrestrial radiation includes high-energy neutrons, thermal neutrons, negative muons, positive muons, and alpha particles, the particle dependence of the MCU susceptibility should be studied to understand the impact of the terrestrial radiation on the MCUs. Furthermore, in the case of the high-energy neutrons, the relative angle between the incidence direction of the neutrons and the device orientation is one of the factors determining the MCU susceptibility. This is due to the forward emission of the secondary ions produced by the high-energy neutrons, which results in different track directions in the cell arrays for different incidence angles of the neutrons. Importantly, the scaling of the SRAM cells can make this angular effect more significant because the number of the cells within the track length of the secondary ion increases with the reduced cell size. It is thus necessary to investigate the angular dependence of the high-energy neutron-induced MCUs in advanced SRAM devices.

Next, the charge collection is discussed. The mechanisms causing the MCU events can be divided into three types: charge deposition on multiple cells, charge sharing, and parasitic bipolar effects (PBEs) [4] [54]. The charge deposition on multiple cells corresponds to the case where the track of a single particle covers several SRAM cells, resulting in charge collections in those SRAM cells. In this case, multiple fail bits occur along the particle track. In the case of the charge sharing, generated electrons and holes spread over multiple SRAM cells, and hence charge collection can occur in several neighboring cells even when the particle track does not cover those cells [55]. The PBEs are very different from these mechanisms.

Fig. 1.19 explains the phenomenon of the PBEs in nMOS transistors of SRAM cells, where a 2×2 SRAM array and its cross-sectional view along the dotted line A–D are illustrated in the upper and lower parts, respectively. As depicted in the cross-sectional view, parasitic npn bipolar transistors are inherently present in the nMOS transistors, where the source, p-well, and drain regions serve as the emitter, base, and collector of the npn bipolar transistor, respectively. When an ionizing

[4] The PBE is also known as parasitic bipolar action (PBA).

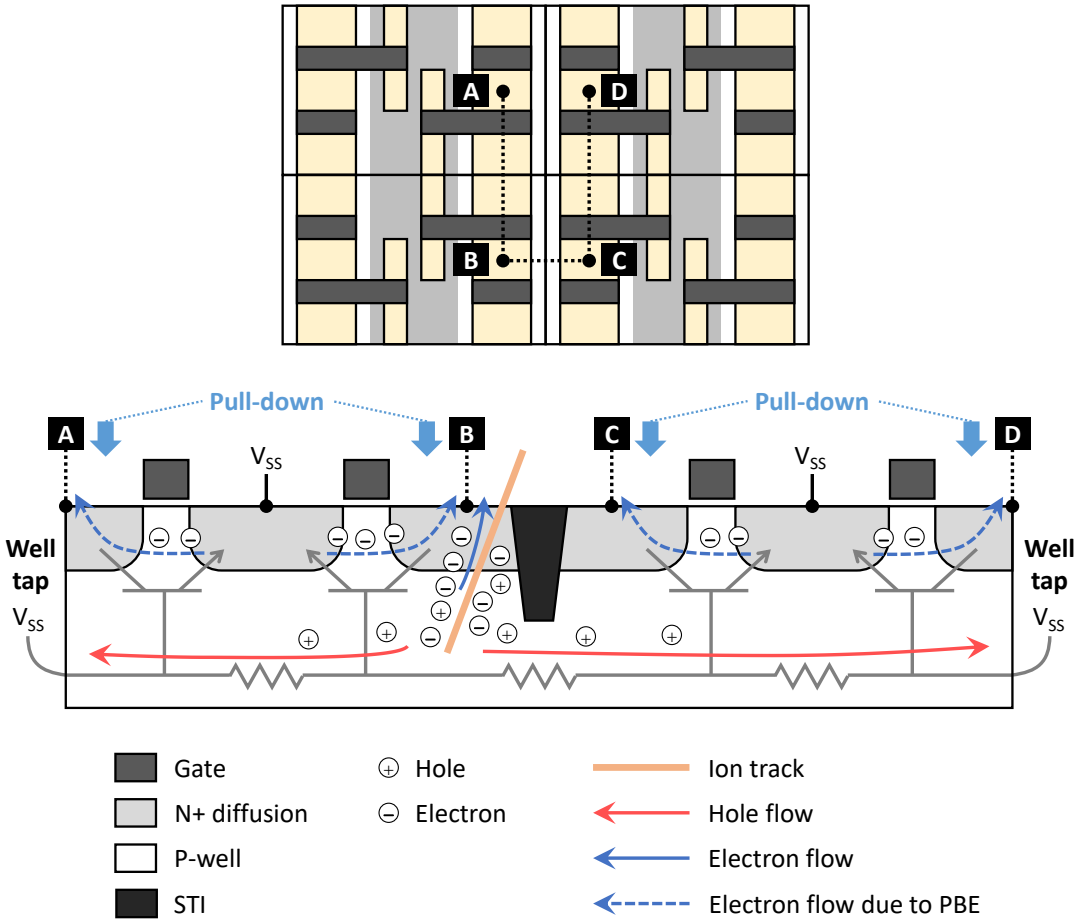

FIGURE 1.19: Conceptual illustration of PBEs in SRAM cells. The upper figure depicts a 2×2 array of the SRAM cells shown in Fig. 1.12. The lower figure corresponds to the cross-sectional view of the SRAM array along the dotted line from A to D, which includes four nMOS transistors. Parasitic npn bipolar transistors are depicted in each nMOS transistor, where the bipolar transistors are connected through p-well resistances. Hole and electron flows induced by an ion strike (orange line) are represented by the red and blue arrows, respectively. The dotted blue arrows represent the electron flows due to PBEs in the nMOS transistors. Due to these electron flows, the nodes A–D are pulled down to low (V_{SS}) regardless of the gate voltage, as denoted by the light blue arrows.

particle strikes the nMOS transistor (in Fig. 1.19, the node labeled as B), electron-hole pairs are generated along the ion track (orange line). The electrons are typically collected by the drain of the nMOS transistor. The remaining holes and their flows to well taps elevate the p-well potential. Due to this potential rise, the parasitic npn bipolar transistors can transiently turn on, and hence electrons can flow from the source to the drain even though the gate is low. This behavior corresponds to the charge collection in the PBEs. As a result, the voltage level of the drain is pulled to that of the source, i.e., low (V_{SS}) regardless of the gate voltage.

The key point here is that the PBEs are triggered by the well potential perturbation. Since tha SRAM cells share the wells with the neighboring cells, the well

potential perturbation can cause the PBEs in multiple cells of the same well simultaneously, resulting in the MCU event. In the case of Fig. 1.19, due to the potential rise of the p-well, the PBEs are induced in the four nMOS transistors that share the p-well. In this case, the nodes A–D can be simultaneously pulled to low (V_{SS}), and hence the four SRAM cells potentially become fail bits, i.e., the MCU event. Another important point is that the PBEs are more active at higher supply voltage because the current gain of the bipolar transistors increases with the voltage.

With the scaling of the transistors, the contribution of the PBEs have become significant, leading to the complicated processes of MCU occurrence. As explained above, the PBE is based on the action of the parasitic bipolar transistor. Since the base width of the bipolar transistor corresponds to the gate length, the scaling of the transistor size results in the decreased base width. This increases the performance of the parasitic bipolar transistor, and hence the PBE becomes more powerful. Due to the increased contribution of the PBEs, novel MCU mechanisms have emerged, such as multi-coupled bipolar interaction (MCBI) and well-collapse source-injection (WCSI) [54], [56]. Therefore, the impact of the PBEs on the MCUs needs to be explored in advanced SRAM devices.

1.4 Challenges in Terrestrial Radiation-Induced SEUs

The continuous advancement of the SRAM devices poses new challenges in the terrestrial radiation-induced SEUs, due to factors of size scaling, critical charge reduction, and geometry changes of transistors. These factors have a considerable impact on SEU mechanisms and hence differentiate the SEU response of advanced SRAM devices from that of conventional ones. This would lead to difficulties in understanding and evaluating the SEU characteristics on the basis of existing knowledge, although the SEUs in the SRAM devices are of great concern for modern semiconductor devices in the terrestrial environment. Therefore, it is necessary to clarify the impact of these factors on the mechanisms and the resulting characteristics of SEUs for the terrestrial radiation, i.e., high-energy neutrons, thermal neutrons, negative muons, positive muons, and alpha particles.

The size scaling leads to increased MCU susceptibility and complicated MCU mechanisms of the SRAM devices. Due to the shrinkage of SRAM cells, charge deposition induced by a single particle strike can cover multiple cells. In addition, the miniaturization of transistors increases the contribution of PBEs for charge collection in multiple cells. These conditions imply that a large number of cells are simultaneously affected by the PBEs in scaled SRAM devices, which will make the MCU mechanism more complicated than the known ones, such as MCBI and WCSI [54], [56]. Furthermore, in the case of the high-energy neutrons, the size scaling would impact on the sensitivity of the MCU characteristics to the angle of neutron incidence. This is because scaled SRAM cells are more sensitive to the configuration of secondary ion tracks and because the track configuration varies depending on the

incidence angle due to the forward emission of the secondary ions. This angular sensitivity has been demonstrated to be considerable in 90-nm and 65-nm planar SRAMs [57]–[59]. However, there is a lack of studies investigating this in further scaled SRAMs. Therefore, it is essential to study the MCU responses of advanced SRAM devices with the consideration of both the PBEs in multiple cells and the effect of the incidence angle of the high-energy neutrons.

The critical charge reduction increases the vulnerability of the SRAM devices to charge deposition induced by low-LET particles, such as the muons. Since, as explained earlier, the negative and positive muons are the most abundant particles in the terrestrial environment, the muons potentially become a significant source of SEUs for advanced SRAM devices with low critical charge. However, the mechanisms and characteristics of the muon-induced SEUs have not been well established. As mentioned earlier, previous experiments have investigated the positive muon-induced SEUs in several SRAMs from a 65-nm planar to a 14-nm FinFET technologies [46], [47]. On the other hand, the negative muon-induced SEUs have been investigated only in 65-nm and 28-nm planar SRAMs [48]–[50]. At the same time, for the negative muons, it is important to consider muon capture reactions, which are absent for the positive muons. This is because the capture reactions can induce considerable MCUs through the production of secondary ions with LETs higher than the negative muon itself [49], [50]. This raises a concern about the impact of the negative muons on MCUs in more scaled SRAM devices. Therefore, the investigation of the muon-induced SEUs, particularly for the negative muons, is required to understand the impact of atmospheric muons in current and future semiconductor devices.

The geometry change of transistors arises from the introduction of FinFETs in recent CMOS technologies and has a significant impact on the SEU response of the SRAM devices. It has been demonstrated that SEU susceptibility for FinFET SRAMs is drastically reduced compared with conventional planar SRAMs. This is due to the smaller silicon volume of transistor region for the FinFETs than that for the planar FETs, which results in the reduction of charge collection for the FinFET SRAMs. In addition to this volume shrinkage, the geometry of the FinFETs is very anisotropic due to their narrow fin width. Typically, the fin width is less than 10 nm, whereas the fin height is several tens of nanometers [35]. As mentioned above, the secondary ions produced by the high-energy neutrons are emitted forward, i.e., anisotropic emission, whereas the ions produced by the thermal neutrons are emitted isotropically. For these reasons, there is a possibility that the relative angle between the fin direction and the incidence direction of the high-energy neutrons affects the SEU characteristics in the FinFET SRAMs. However, there have been no studies investigating this angular effect in the FinFET SRAMs. Therefore, the angular dependence of the high-energy neutron-induced SEUs should be explored for the FinFET SRAMs.

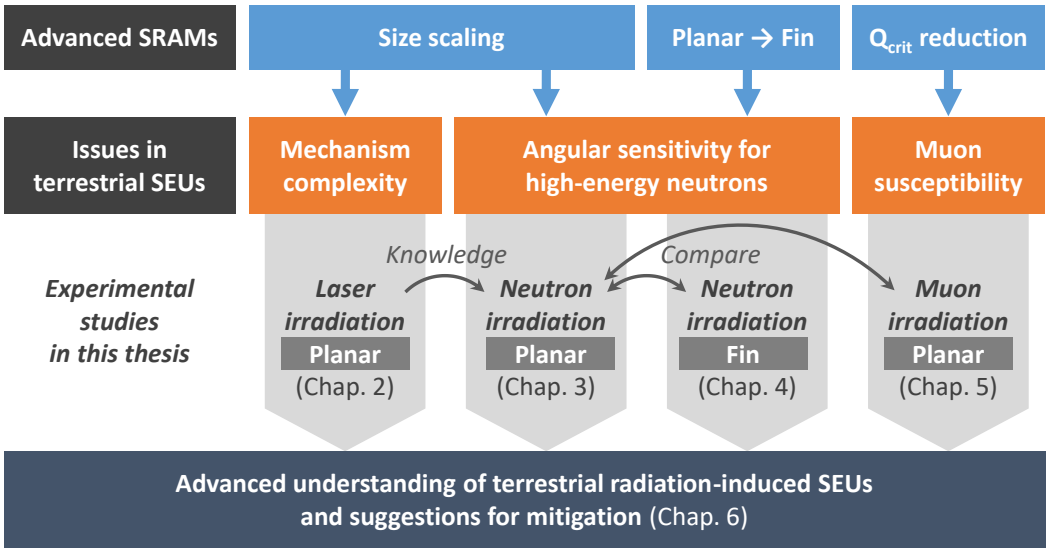

FIGURE 1.20: Overview of this thesis.

1.5 Objective and Overview of This Thesis

The general objective of this thesis is to advance the understanding of the impact of the terrestrial radiation on SEUs in advanced planar and FinFET SRAMs, which help develop and improve soft error mitigation techniques for resilient system designs. As stated above, these SRAMs are facing new challenges that have not been adequately addressed, and therefore studies are needed to properly understand the terrestrial radiation-induced SEUs in modern SRAM devices.

In particular, from the considerations in the previous section, this thesis focuses on the following key issues: MCU mechanisms in scaled SRAMs, negative and positive muon-induced SEUs, and the angular sensitivity of high-energy neutron-induced SEUs. In this thesis, these issues are studied through various experiments on 20-nm bulk planar SRAMs and 12-nm bulk FinFET SRAMs. The technology generations of these two SRAMs are close, but these transistor structures are different. Therefore, these SRAMs are suitable for investigating the impact of transistor geometry change. The experiments include high-energy neutron, thermal neutron, alpha particle, and muon irradiations, which cover all the terrestrial radiations. Furthermore, a laser irradiation technique is employed to investigate the MCU mechanisms. The overview of the studies in this thesis is illustrated in Fig.1.20.

In Chap. 2, the MCU mechanism is explored through laser irradiation experiments on the 20-nm bulk planar SRAMs. A single-pulse two-photon absorption (TPA) method is utilized to simulate charge deposition by an ionizing particle on the multiple SRAM cells. The MCU responses of the 20-nm planar SRAMs are investigated with varying focal positions, pulse energies (PEs), supply voltages, and data patterns written in the SRAM cells. The results show an anomalous dependence of fail bit patterns on the data patterns stored in the SRAM cells. By analyzing the physical topology of the observed fail bit patterns, the strong impact of PBEs in

multiple p-wells is indicated. From the experimental results, a novel MCU mechanism based on the unbalanced PBEs among the p-wells is identified and named as multi-well coupled potential unbalancing (MWCPU).

In Chap. 3, the angular dependence of high-energy neutron-induced SEUs and MCUs is investigated for the 20-nm bulk planar SRAMs by high-energy neutron irradiation experiments. The irradiation experiments are performed at several angles of neutron incidence. The statistical evaluation of SEU, MCU, and MBU rates reveals that, although the SEU rate decreases with increasing angle of incidence, the MBU rate increases at grazing incidence. From this result, it is suggested that the efficiency of ECCs can deteriorate depending on the orientation of SRAM devices in the terrestrial environment. Furthermore, the thorough analyses of the MCU characteristics demonstrate that the forward emission of secondary ions, the rectangular geometry of the SRAM cells, and the PBEs are key factors in determining the angular sensitivity of the MCU response. Especially, the contribution of the MWCPU mechanism, which is identified with laser irradiations, in Chap. 2, is confirmed with the high-energy neutron irradiations from particular fail bit patterns that have gap structures.

In Chap. 4, the differences in the angular dependence of high-energy neutron-induced SEUs and MCUs between planar and FinFET SRAMs are explored. High-energy neutron irradiation experiments are performed on the 12-nm bulk FinFET SRAMs at several angles of neutron incidence. SEU, MCU, and MBU rates are statistically evaluated and are compared with those for the 20-nm bulk planar SRAMs that are investigated in Chap. 3. This comparative investigation demonstrates that the angular sensitivity of the MCU response is different between the 12-nm FinFET SRAMs and the 20-nm bulk planar SRAMs. This discrepancy is speculated to be due to the different contribution of PBEs, where the PBE is less significant in the 12-nm FinFET SRAMs than in the 20-nm planar SRAMs. In addition, it is suggested that the PBE contribution is different at different incidence angles in the 12-nm FinFET SRAMs.

In Chap. 5, the negative and positive muon-induced SEUs are investigated by muon irradiation experiments on the 20-nm bulk planar SRAMs. SEU, MCU, and MBU CSs are evaluated with varying muon energies, supply voltages, and data patterns. The comparison of the CSs between the negative and positive muons demonstrates the significant contribution of muon capture reactions for the negative muon-induced SEUs. Furthermore, the differences in the SEU and MCU responses between the muons and the other terrestrial radiation sources are explored, where the CSs for high-energy neutrons, thermal neutrons, and alpha particles are also evaluated by irradiation experiments. The experimental results show the clear difference in the voltage dependence of the CSs among the particles. Through the comparative analyses of these CSs, it is revealed that the unique nature of the muon capture reactions differentiates the MCU characteristics for the negative muon from that for the high-energy neutrons and the thermal neutrons.

Finally, Chap. 6 reviews the studies in this thesis and summarizes their contributions to the understanding of the terrestrial radiation-induced SEUs in advanced SRAM devices. Furthermore, on the basis of the obtained understanding, some suggestions for mitigation strategies are made.

Chapter 2

Novel MCU Mechanism in Scaled SRAMs

This chapter studies the impact of size scaling on MCU mechanisms by performing laser irradiation experiments in 20-nm bulk planar SRAMs. A single-pulse TPA system is utilized to simulate charge deposition on multiple SRAM cells. [1] MCUs induced by the laser irradiation are thoroughly analyzed in terms of the number and spatial distribution of fail bits. The analyses reveal unique topologies of fail bit patterns and their strong dependence on data patterns written in the SRAM cells. These results indicate that PBEs in multiple p-wells are the phenomena underlying the unique topologies. From these results, a novel MCU mechanism based on the imbalance of the PBEs is identified and named multi-well coupled potential unbalancing (MWCPU). Furthermore, the dominance of the MWCPU mechanism is examined through multiple-pulse laser irradiation experiments.

2.1 Introduction

The susceptibility of SRAM devices to MCUs has increased with technology scaling [51], [52], [61]. As mentioned in Sec. 1.3.3, the MCUs are one of the serious problems in SRAM devices because the MCU events containing multiple fail bits in the same logical word, i.e., MBU events, cannot be corrected by simple ECCs. Many mitigation techniques for the MCUs have been proposed in terms of process engineering, layout designing, and bias conditioning [62]–[66]. Here, the efficiency of the mitigation techniques depends on MCU characteristics. Since the MCU characteristics are affected by underlying mechanisms, it is meaningful to investigate MCU mechanisms in scaled SRAM devices for understanding the MCU characteristics and for selecting appropriate mitigation techniques.

The size scaling of SRAM cells has resulted in complicated MCU mechanisms, as described in Sec. 1.3.6. In particular, PBEs have played a significant role in MCU occurrence as the size of transistors has shrunk [5]. Since the PBEs are activated by well potential perturbation and SRAM cells share wells in bulk CMOS technologies, multiple SRAM cells in the same well can be simultaneously affected by the PBEs.

[1] This chapter is based on [60].

Osada *et al.* [63] demonstrated that the PBEs in nMOS transistors cause MCU events, where the PBEs are triggered by prolonged potential rise in p-wells. Ibe *et al.* [54] demonstrated that the PBEs with the action of parasitic thyristors, which they call MCBI, induce MCU events with particular fail bit patterns. Black *et al.* [56] demonstrated that the PBEs in pMOS transistors are induced through hole injection from the pMOS sources to the n-well, which they call WCSI, and that the resulting fail bit pattern depends on the relative location of the pMOS sources to an ion strike.

At the same time, the detailed spatial distribution of charge deposition has become more important with the scaling of SRAM cells. One of the factors affecting the charge distribution is the angle of ion incidence to the SRAM array. In the scaled SRAM cells, the grazing incidence easily results in charge deposition on multiple cells. Another factor is the radial distribution of charge deposition around an ion track. It has been reported that this radial distribution affects the occurrence of MCU events [67]–[69]. The range of the radial distribution has been investigated using a penumbra model [70]. According to this model, the radial range of charge deposition can exceed 100 nm. This means that, in advanced SRAM devices, one ion can induce charge deposition on multiple cells even when the ion strikes normal to the cell array. Hence, it is essential to consider multiple-cell charge deposition to understand MCU mechanisms in scaled SRAM devices.

Although the spatial distribution of charge deposition has a considerable impact on MCU occurrence, it is difficult to identify its contribution by conventional particle irradiation testing. This is due to the lack of control of the particle incidence position in SRAM devices. In recent years, TPA laser testing has been adopted for the investigation of SEEs in SRAM devices [71], [72]. The TPA laser testing is capable of controlling both the 3D position and amount of charge deposition. Moreover, since the typical size of the laser spot is $\sim$1 μm, the TPA-induced charge deposition can cover multiple SRAM cells. The TPA laser is therefore particularly suitable for exploring the effect of spatial charge distribution on MCU mechanisms.

This study investigates the impact of multiple-cell charge deposition on MCUs in 20-nm bulk planar SRAMs. Single-pulse laser irradiation experiments are performed using a TPA laser system. The SEU and MCU responses of the SRAMs are characterized by controlling the laser parameters and the SRAM operation conditions. The analyses of fail bit maps (FBMs) clearly demonstrate that fail bit patterns have unique topologies that depend on data patterns written in the SRAM. On the basis of the observed unique topologies, the effect of well potential perturbation is discussed. Finally, a novel MCU mechanism is distinguished and its validity is examined by multiple-pulse laser irradiation experiments.

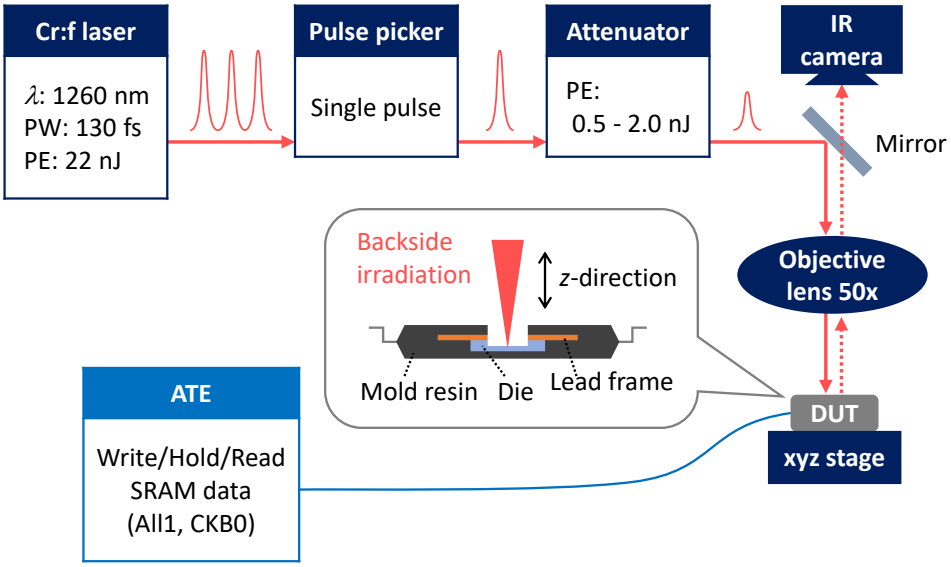

FIGURE 2.1: TPA-based soft error simulation system with ATE [73]. A single laser pulse is focused on the backside of the DUT. The backside of the DUT is opened for the laser injection.

2.2 Experimental Setup

2.2.1 TPA Laser Irradiation

Laser irradiation was performed using the TPA-based soft error simulation system [73]. In this system, an automated test equipment (ATE) was utilized to operate a device under test (DUT). The setup of the system is explained in Fig. 2.1. The wavelength (λ), pulse width (PW), and PE of the Cr:forsterite laser are 1260 nm, 130 fs, and 22 nJ (max), respectively. A pulse picker was employed for a single-pulse irradiation to avoid the accumulative effect of multiple pulses. The PE was adjusted through an attenuator. The laser pulse was focused on the DUT by a 50$\times$ microscope objective lens. The minimum spot size, according to Rayleigh's criterion, is computed to be 1.8 μm. The PEs presented in the following are the energies after passing through the objective lens, where the transmission factor of the lens is taken into account. An infrared (IR) camera was attached to confirm the position of the laser spot and the layout pattern of the DUT. The focal position inside the DUT is controlled by utilizing an xyz-stage.

2.2.2 Tested Device and Operation

The test vehicle was an SRAM chip fabricated in a 20-nm bulk planar technology. The package type was a standard plastic quad flat package. The backside of the package was opened for backside irradiation as depicted in Fig. 2.1. Then, the silicon substrate of the die was mechanically thinned and polished to a thickness of approximately 80 μm by using a dimple grinder. A 12 Kbit SRAM block in the SRAM chip was used for the laser irradiation. The layout pattern of this SRAM block was

imaged with the IR-camera. On the basis of this image, the xy-position of the xyz-stage was adjusted to meet the laser spot to around the center of the SRAM block. The xy-position was fixed in each irradiation test.

The SRAM operation consisted of write, hold, and read cycles in this order. After data were written in all the SRAM cells, the DUT was irradiated by a single laser pulse in the subsequent hold cycle. The number and locations of fail bits induced by the irradiation were then obtained in the read cycle. All tests were carried out in a static mode with no read operation during the hold cycles. Two types of data patterns were employed: All1 and CKB0. In the case of the All1 pattern, a logical "1" was written in all the bits. In the case of the CKB0 pattern, logical "0" and "1" were arranged in a checkerboard fashion, where "0" was written in the first bit.

2.3 Results and Discussion

2.3.1 Focal Position Dependence of SEU Susceptibility

The SEU susceptibility to the laser irradiation was investigated by performing single-pulse laser irradiations at various z-positions of the focal point. The laser irradiation was conducted at three PEs: 0.33, 0.52, and 0.98 nJ. In Fig. 2.2, the number of fail bits induced by the single laser pulse is plotted for the three PEs as a function of the focal position in z-direction, where the z-direction is normal to the die surface [see Fig. 2.1]. As seen in this figure, the single laser pulse induced a number of fail bits simultaneously, i.e., an MCU. The z-coordinate denotes the depth position of the focal point inside the die, which was estimated considering the refractive index of silicon. The z-coordinate origin ($z = 0$) was set to around the position of the interface between the silicon substrate and the metal layers, which was determined by analyzing IR images obtained throughout the measurements. In the z-axis, the positive and negative directions are toward the metal layers and the backside of the silicon substrate, respectively.

It was clearly observed that the number of fail bits and the z-range of SEU occurrence increase with increased PE, and that the number of fail bits exhibited a maximum near $z = 0$. These results probably reflect the nature of TPA-induced charge deposition. When a laser pulse is focused on the silicon substrate, electron-hole pairs are generated by TPA around the focal point of the laser, where the radial range of the pair generation is the largest at the focal point [74]. At the same time, the number of electron-hole pairs increases with the number of incident photons, i.e., the PE of the laser pulse. Thus, the number of SRAM cells covered by the TPA-induced charge deposition becomes larger when the focal point is near the SRAM cell array and when the PE is high. Here, the increased number of SRAM cells covered by the charge deposition obviously results in the increased number of fail bits. Therefore, from Fig. 2.2, it can be deduced that the focal point meets the position of the SRAM cell array at around $z = 0$. This view is consistent with the layer structure of the

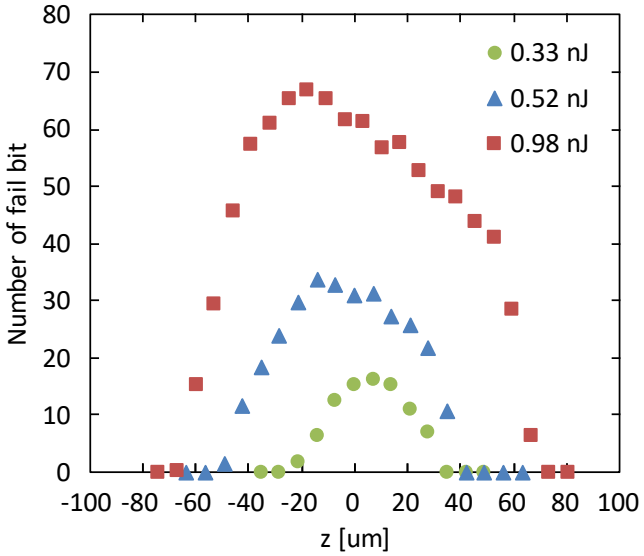

FIGURE 2.2: Number of fail bits as a function of the focal position in z-direction. Green circle, blue triangle, and red square symbols are for the PEs of 0.33, 0.52, and 0.98 nJ, respectively. The number of fail bits is the average value over three measurements. The origin of the z-axis ($z = 0$) corresponds to the interface between the silicon substrate and the metal layers, where the positive direction is toward the metal layers. The data pattern and supply voltage are CKB0 and 0.7 V, respectively.

SRAM chip because the SRAM cell array is located at the top of the silicon substrate, i.e., at the vicinity of $z = 0$.

The z-range of SEU occurrence was approximately 120 μm for the PE of 0.98 nJ, as confirmed in Fig. 2.2. This range was larger than the charge generation range reported in a previous work, where the range of the initial charge structure was estimated to be $\sim$ 14 μm by using a Si PIN photodiode [73]. One possible reason for this discrepancy is the difference in the numeric aperture (NA) of the objective lens. The NA of the objective lens used in this experiment is smaller than that used in [73]. It is known that a smaller NA results in a longer focal depth. This can lead to the elongated distribution of charge generation along the incidence direction, i.e., the z-direction. Another possible reason is the effect of charge collection. The SEU occurrence observed in this experiment is a consequence of complicated charge collection processes including diffusion of electrons and holes. On the other hand, the charge generation range estimated in [73] was the initial range before the diffusion starts. Since the charge distribution spreads due to the diffusion, the range of SEU occurrence can be larger than the charge generation range.

It is interesting that the profile of the focal position dependence was asymmetric at the PEs of 0.52 and 0.98 nJ, as seen in Fig. 2.2. In particular, the peak positions for these PEs shifted toward the negative z-direction, compared to that for 0.33 nJ. Here, the negative z-direction corresponds to the direction toward the back side of the silicon substrate. A possible reason for this asymmetric profile is the cutoff of

charge generation due to the metal layers. Since TPA-induced charge generation occurs around the focal point inside the silicon substrate, the distribution of the charge generation can be cut off by the metal layers when the focal point is located near the metal layers. This charge generation cutoff probably becomes larger as the focal position moves toward the metal layers. Hence, the total amount of generated charge can be decreased as the focal position shifts to the positive z-direction in Fig. 2.2. Since the decreased amount of charge can lead to the reduced number of fail bits, the number of fail bits in the positive (right) side of the profile can be smaller than that in the negative (left) side of the profile. Moreover, the charge generation cutoff is possibly more significant at higher PEs because of the broader distribution of charge generation. These considerations are consistent with the observed asymmetry.

Although the observed asymmetric profile of the focal position dependence can be explained by the charge generation cutoff by the metal layers, there are two possible factors that affect the profile. One is the distortion of laser wavefront due to reflection on the metal layers, as indicated in a previous work on TPA-induced SEL [72]. Another is the intrinsic asymmetry in TPA-induced charge generation, where charge collection experiments and numerical simulation demonstrated that the distribution of the charge generation is asymmetric along its axial direction [75], [76]. Further studies are needed to understand the observed asymmetry in the focal position dependence. Nevertheless, this asymmetry does not play a role in the following discussion because the focal position is fixed.

2.3.2 Effects of Supply Voltage and Data Pattern on TPA-induced MCUs

The effects of the supply voltage and data pattern on TPA-induced MCUs were investigated in terms of the number and range of fail bits as a function of the supply voltage, as presented in Fig. 2.3 and 2.5. In these figures, the results for All1 and CKB0 patterns are represents by circle and square symbols, respectively. These investigations were conducted by single-pulse laser irradiations with a fixed focal position.

The number of fail bits decreased with increasing the supply voltage in both the All1 and CKB0 patterns, as seen in Fig. 2.3. This decreasing trend can be explained by the critical charge. As explained in Sec. 1.3.2, the critical charge increases with increasing the supply voltage, and hence SEU occurrence requires larger charge deposition at higher supply voltages. Fig. 2.4 illustrates the conceptual relationship between the critical charge and the range of fail bits for a given distribution of TPA-induced charge deposition. In this figure, two cases of the critical charge are considered: Q_c and Q_c', where $Q_c > Q_c'$. According to the typical radial distribution of TPA-induced charge generation, the amount of generated charge decreases with increasing distance from the center of the laser spot [74]. In this case, the higher critical charge (Q_c) results in the reduced range of fail bits, as depicted in Fig. 2.4. Hence, the number of fail bits decreased at higher critical charge, i.e., at higher supply voltage, as observed in Fig. 2.3.

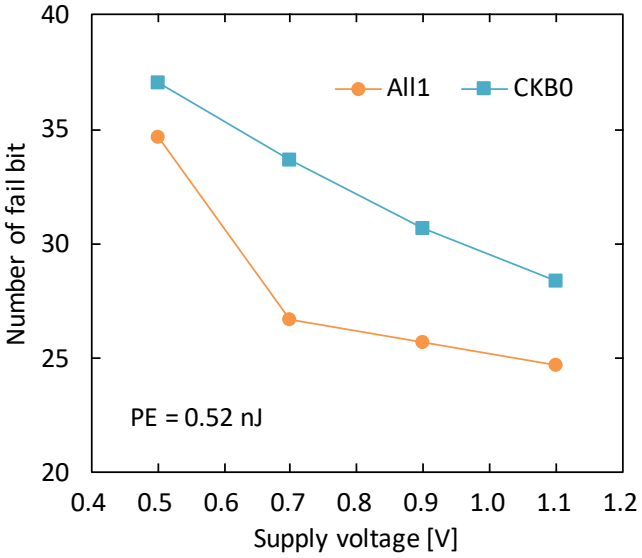

FIGURE 2.3: Supply voltage dependence of the number of fail bits for All0 and CKB0 patterns. Circle and square symbols correspond to the All1 and CKB0 patterns, respectively. The PE is 0.52 nJ. The number of fail bits is the average value over three measurements.

The range of fail bits exhibited a decreasing trend in the supply voltage dependence, as shown in Fig. 2.5. Here, the BL and WL ranges of fail bits are presented for the All1 and CKB0 patterns. This decreasing trend is consistent with the speculation of Fig. 2.4. An important observation was the difference between the BL and WL ranges, where the BL range was larger than the WL range, as seen in Fig. 2.5. This difference is probably due to the geometry of the SRAM cells. The SRAM cells are of rectangular shape, where the long and short sides are parallel to the WL and BL directions. Since the spatial distribution of TPA-induced charge deposition is essentially identical in the WL and BL directions, the number of the SRAM cells covered by the charge deposition is larger in the BL direction and is smaller in the WL direction.

A noteworthy finding was that the number and range of fail bits were larger for the CKB0 pattern than for the All1 pattern, as observed in Fig. 2.3 and 2.5. This cannot be explained by the critical charge and the distribution of charge generation because these are independent of the data patterns. To explore the difference between the All1 and CKB0 patterns, the spatial distribution of fail bits were analyzed by drawing FBMs. Fig. 2.6 presents the FBMs for the All1 and CKB0 patterns obtained at PEs from 0.33 to 1.30 nJ. In each FBM, small rectangular cells represent SRAM cells, where the blue and red cells correspond to pass and fail bits, respectively. As denoted in this figure, the vertical and horizontal directions are parallel to the WL and BL directions, respectively.

The FBMs shown in Fig. 2.6 clearly demonstrated that the number and range of fail bits increased with increasing PE for both the All1 and CKB0 patterns. Here, the PE increases from top to bottom in Fig. 2.6. This result corresponds to the PE

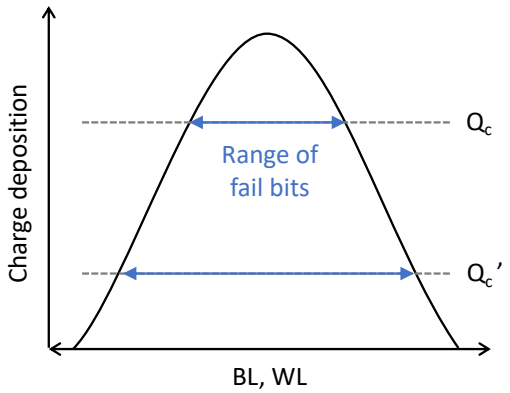

FIGURE 2.4: Conceptual illustration of the relationship between the critical charge and the WL or BL range of fail bits for a given distribution of TPA-induced charge deposition. The ranges of fail bits for two cases of critical charge (Q_c and Q_c') are depicted by blues arrows, where $Q_c > Q_c'$.

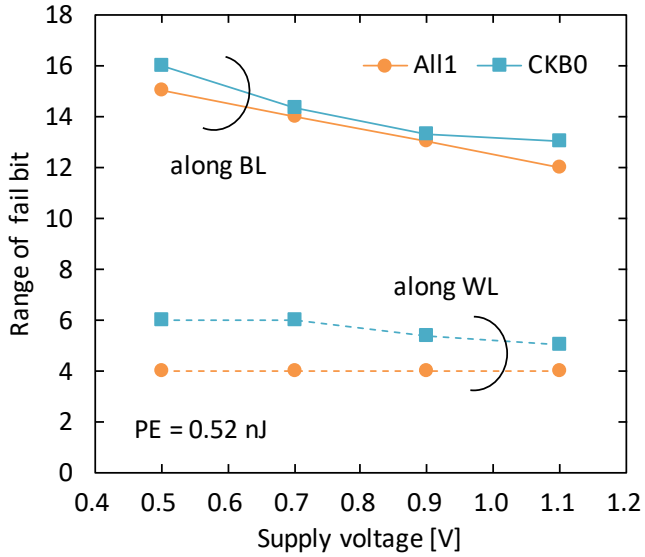

FIGURE 2.5: WL and BL ranges of fail bits as a function of supply voltage for All0 and CKB0 patterns. Solid and broken lines correspond to the WL and BL ranges, respectively. Circle and square symbols correspond to the All1 and CKB0 patterns, respectively. The PE is 0.52 nJ. The range of fail bits is the average value over three measurements.

dependence shown in Fig. 2.2, where the number of fail bits increased with increasing PE. These FBM analyses confirmed that the distribution of TPA-induced charge generation becomes broader as the PE increases, and that the multiple SRAM cells are covered by the charge distribution. In addition, it was also observed that the WL range of fail bits is smaller than the BL range of ones. For example, in the FBM of the All1 pattern at the PE of 0.52 nJ, the WL and BL ranges are 4 and 15, respectively. This range difference corresponds to the results shown in Fig. 2.5.

More important, the FBMs revealed unique topologies in fail bit patterns, as seen in Fig. 2.6. Here, the topology was different between the All1 and CKB0 patterns. In the case of the All1 pattern, the fail bits were continuous in the BL direction and

were discontinuous in the WL direction. In the case of the CKB0 pattern, on the other hand, the fail bits were discontinuous in the BL direction and were arranged in stripe-like patterns, where the BL position of the fail bits tended to be different between the right and left regions of the fail bit patterns. A key observation was that these topological differences result in the differences in the number and range of fail bits between the All1 and CKB0 patterns even at the same PE. This is the reason why the number and range of fail bits were different between the All1 and CKB0 patterns in Fig. 2.3 and 2.5, where the number and range were larger for the CKB0 pattern than for the All1 pattern.

These topologies of fail bit patterns have not been reported so far. To explore the underlying mechanism for these unique topologies and the difference between the All1 and CKB0 patterns, the next section focuses the fail bit patterns marked in bold in Fig. 2.6 (FBMs of the All1 pattern at 0.52 nJ and of the CKB0 pattern at 0.39 nJ).

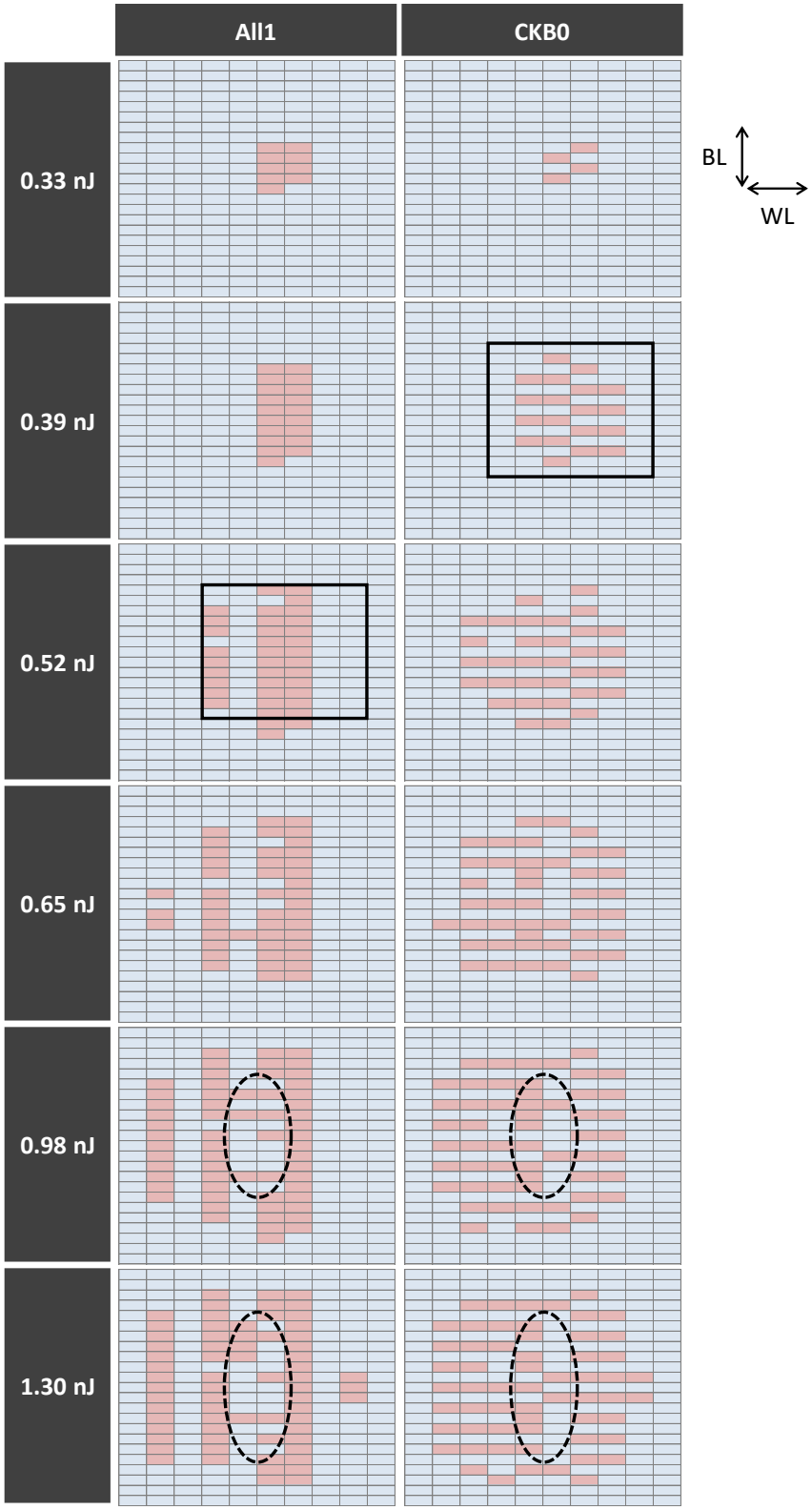

FIGURE 2.6: FBMs for PEs from 0.33 to 1.30 nJ and for All1 and CKB0 patterns. Supply voltage is 0.7 V. Small rectangular cells represent SRAM cells. Blue and red cells correspond to pass and fail bits, respectively. Vertical and horizontal directions are parallel to BL and WL directions, respectively. Each FBM shows the same region of the SRAM array. The focal position is the same for all the FBMs.

2.3.3 Exploration of a Novel MCU Mechanism Based on Fail Bit Patterns

The FBMs marked in bold in Fig. 2.6 were looked into with internal nodes of SRAM cells in Fig. 2.7, where the upper and lower FBMs are for the All1 and CKB0 patterns. In this figure, rectangular cells represent SRAM cells, where the gray cells correspond to fail bits. In each SRAM cell, two internal nodes are depicted by colored boxes. Here, the blue and red boxes represent the voltage levels of low (V_{SS}) and high (V_{DD}), respectively. Note that the node voltages depicted in Fig. 2.7 are the initial states before the laser irradiation. The orange cross in each FBM indicates the center of the laser spot, i.e., the center of TPA-induced charge deposition, which was estimated from the spatial distribution of fail bits in a series of FBMs. The FBMs shown in Fig. 2.8 are the same as those in Fig. 2.7, but the node voltages depicted are the states after the laser irradiation.

A key finding in these FBMs was that, in each cell, the voltage level of the internal node closer to the center of TPA-induced charge deposition tended to be low (V_{SS}) after the laser irradiation, which was observed for both the All1 and CKB0 patterns, as seen in Fig. 2.8. To understand this finding, the transitions of node voltages are examined with a focus on nMOS transistors in p-wells because the dominant contributor for SEU occurrence is nMOS transistors in high nodes, as explained in Sec. 1.3.2. In Fig. 2.7, three p-wells are labeled as p-well 1, p-well 2, and p-well 3. In the p-well 1, it was found that almost all the cells whose high nodes were located in the p-well 1 became fail bits in the FBMs for both the All1 and CKB0 patterns. This type of fail bit pattern can be explained by PBEs. Since the PBEs are triggered by well potential perturbation, as described in Sec. 1.3.6, the fail bits in the p-well 1 can be interpreted to be due to the PBEs triggered by the potential perturbation in the p-well 1. However, in the p-well 2 and p-well 3, the fail bits cannot be explained simply by the PBEs. In the case of the All1 pattern, the cells in the right side of the p-well 3 were pass bits even though their high nodes can be affected by the PBEs in the p-well 3. Similarly, in the case of the CKB0 pattern, the cells whose high nodes were located in the right side of the p-well 2 were pass bits even though these cells can be affected by the PBEs in the p-well 2. Therefore, the unique arrangement of node voltages observed in Fig. 2.8 cannot be attributed simply to the PBEs.

On the basis of this finding, the mechanism underlying the observed unique topologies of fail bit patterns is investigated in Fig 2.9. This investigation focuses on the four SRAM cells marked in bold in Fig. 2.7 and 2.8, in the case of the CKB0 pattern. The schematic layout of the four SRAM cells is illustrated in Fig. 2.9 (b) and (e), where the horizontal direction is parallel to the WL direction. Here, Fig. 2.9 (b) and (e) represent the node voltages before and after the laser irradiation, respectively. These four cells are numbered from 1 to 4 for ease of explanation. As estimated in Fig. 2.8, the center of TPA-induced charge deposition is located between the cells 2 and 3. In this case, the spatial distribution of the charge deposition can be considered as shown in Fig. 2.9 (a), where the amount of deposited charge is the most abundant

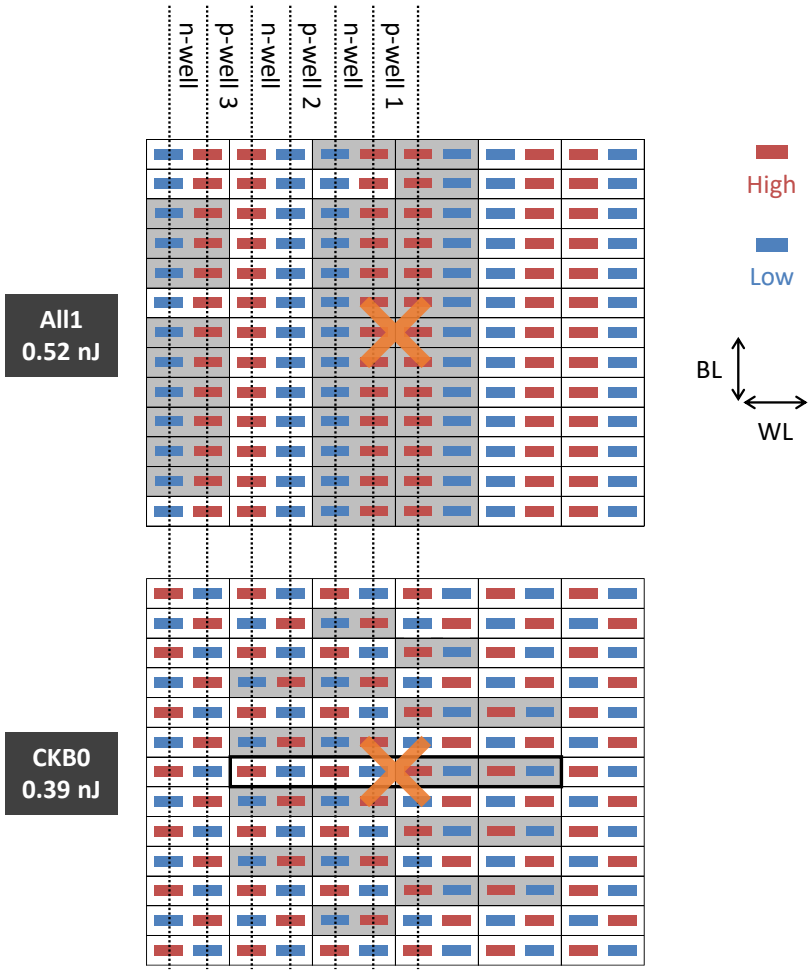

FIGURE 2.7: FBMs with internal node voltages before laser irradiation for All1 (upper) and CKB0 (bottom) patterns. PEs for the All1 and CKB0 patterns are 0.52 and 0.39 nJ, respectively. These FBMs correspond to the regions enclosed by bold lines in Fig. 2.6. Rectangular cells represent SRAM cells. The gray cells correspond to fail bits. In each cell, blue and red boxes depict low (V_{SS}) and high (V_{DD}) voltages of internal nodes, respectively. The orange cross is the estimated position of the center of the laser spot.

between the cells 2 and 3. A key point here is the imbalance of well potential perturbation in p-wells. Fig. 2.9 (c) and (d) illustrate the cross-sectional view along the dotted line in Fig. 2.9 (b) and the potential rise in the corresponding p-wells, respectively. As indicated in Fig. 2.9 (d), the potential of all the p-wells can rise due to deposited holes. Here, the potential rise is probably larger the closer to the center of the charge deposition because the amount of deposited holes is abundant in the center region. Moreover, the duration of the potential rise is also probably longer in the center region [63].

From the investigation in Fig. 2.9, the transition of node voltages from the initial state (Fig. 2.9 (b)) to the final state (Fig. 2.9 (e)) can be explained by a novel MCU mechanism based on the imbalance of PBEs in nMOS transistors. As explained in Sec. 1.3.6, the p-well potential rise indicated in Fig. 2.9 (d) activates the PBEs in

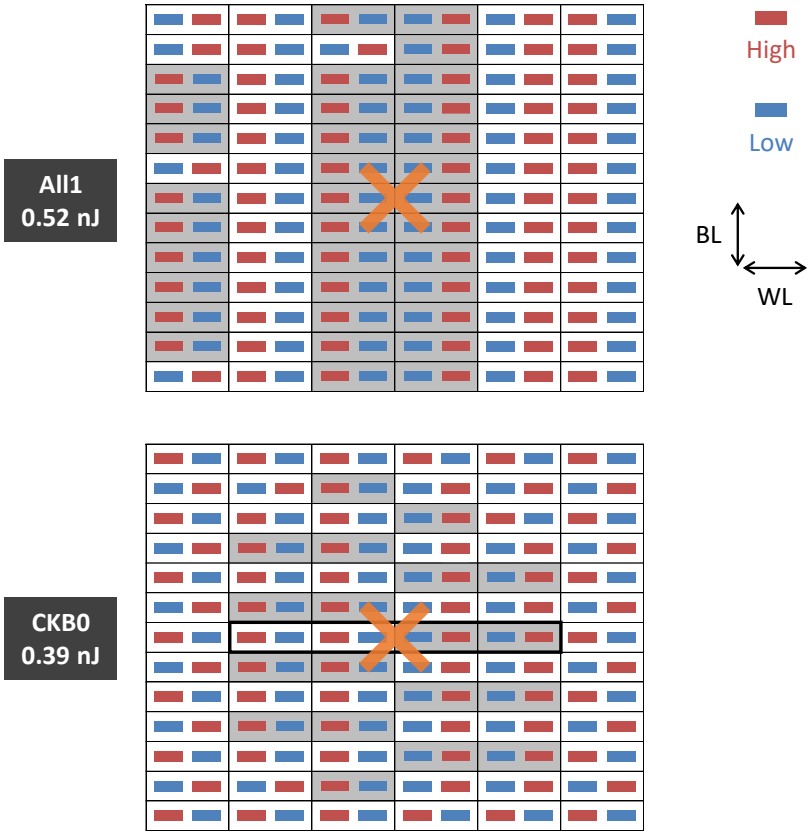

FIGURE 2.8: FBMs with internal node voltages after laser irradiation for All1 (upper) and CKB0 (bottom) patterns. PEs for the All1 and CKB0 patterns are 0.52 and 0.39 nJ, respectively. These FBMs correspond to the regions enclosed by bold lines in Fig. 2.6. Rectangular cells represent SRAM cells. The gray cells correspond to fail bits. In each cell, blue and red boxes depict low (V_{SS}) and high (V_{DD}) voltages of internal nodes, respectively. The orange cross is the estimated position of the center of the laser spot.

the nMOS transistors of the four SRAM cells, which pull down the node voltages. An important point here is that this pull-down strength is larger for higher p-well potential rise. The pull-down strength is illustrated by blue arrows in Fig. 2.9, where the filled arrows indicate the stronger side in each cell. From this illustration, it is suggested that, in each SRAM cell, the node closer to the center of the charge deposition is finally pulled to the low voltage. As a result, the node voltages after the laser irradiation can become as shown in Fig. 2.9 (e). In this case, the cells 3 and 4 are fail bits because their internal node voltages are changed form their original ones, whereas the cells 1 and 2 are pass bits. It can be found that this fail bit pattern is identical to the the observed pattern marked in bold in Fig. 2.7 for the CKB0 pattern. Furthermore, most of the fail bits observed in Fig. 2.6 are consistent with the above scenario. It is therefore probable that the above mechanism underlies the unique topologies in fail bit patterns observed. The MCU mechanism presented here is named as multi-well coupled potential unbalancing (MWCPU).

It should be noted that the MWCPU mechanism is essentially different from

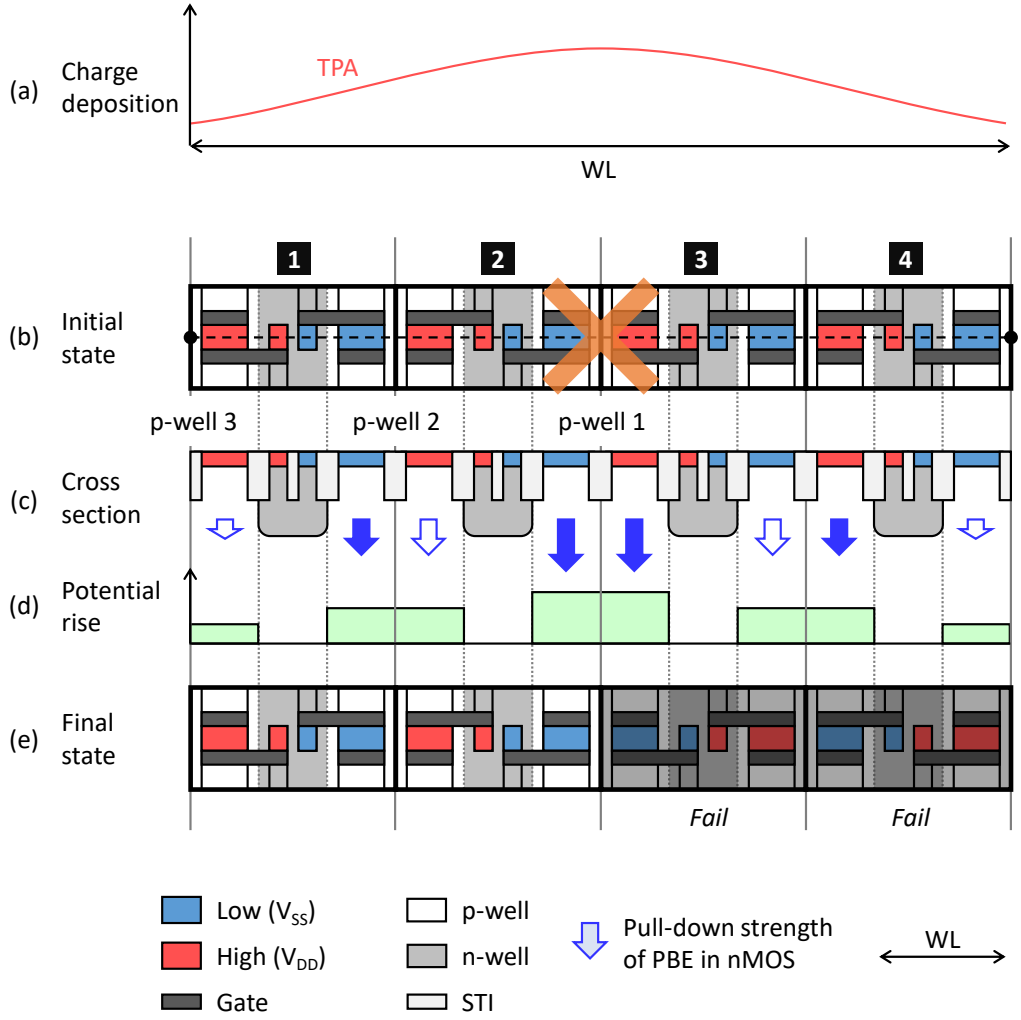

FIGURE 2.9: MWCPU-induced node voltage transition for four SRAM cells in the case of CKB0 pattern. (a) Distribution of TPA-induced charge deposition along the WL direction. (b) Schematic layout of the four SRAM cells marked in bold in Fig. 2.7, where the orange cross indicates the center of the laser spot. (c) Cross-sectional illustration along the dotted line in (b). (d) Potential rise in p-wells due to the charge deposition. (e) Schematic layout of the four SRAM cells marked in bold in Fig. 2.8, which is same as (b) but with node voltages after the laser irradiation. The gray cells correspond to fail bits. Blue and red regions depict low (V_{SS}) and high (V_{DD}) voltages of the internal nodes, respectively. Blue arrows represent pull-down strength of PBEs in nMOS transistors, where the filled arrows indicate the stronger side in each SRAM cell.

MCU mechanisms reported so far. The key features of the MWCPU mechanism are that internal node voltages of SRAM cells are determined by the imbalance of PBEs in multiple p-wells, and that particular fail bit patterns can occur depending on the relative position between internal nodes and the distribution of charge deposition. As mentioned in Sec. 1.3.6, it has been reported that PBEs in multiple SRAM cells can trigger MCBI and WCSI mechanisms, which can lead to the occurrence of

particular fail bit patterns [54], [56]. These mechanisms are based on potential perturbation in a single well, where SRAM cells sharing the well are affected. In other words, the extent of these mechanisms is limited to a single BL or two adjacent BLs. The MWCPU mechanism, on the other hand, is based on potential perturbation in multiple wells, where the imbalance of the potential perturbation leads to particular fail bit patterns along the WL direction over several BLs. Hence, the MWCPU mechanism is essentially different from the MCBI and WCSI mechanisms.

It is worthwhile to emphasize that the FBMs at higher PEs exhibited irregular fail bit patterns that cannot be explained by the MWCPU mechanism, as seen in Fig. 2.6, where the corresponding region is marked with dotted lines. One possible reason for these irregular patterns is the strong activation of PBEs in pMOS transistors due to the large amount of deposited holes. Here, the PBEs in pMOS transistors are triggered by the potential drop of n-wells. The key point is that, in contrast to PBEs in nMOS transistors, the PBEs in pMOS transistors pull up node voltages. In this case, the PBEs in nMOS and pMOS transistors can compete at the higher PE, which results in the irregular fail bit patterns. Another possible reason is competition of PBEs in two nMOS transistors on both sides an SRAM cell. The higher PE provides a broader distribution of charge deposition, and hence these two nMOS transistors can be covered with its center region. This region has a smaller spatial gradient of charge density, which lessens the difference between their pull-down strengths. Therefore, the PBEs in the two nMOS transistors can compete. This kind of competition was suggested and used to explain similar irregularity observed in [77].

Another point to note here is that the displacement of the laser spot can lead to the above-mentioned irregular fail bit patterns. As seen in the FBMs shown in Fig. 2.6, the spatial distribution of fail bits extended slightly more to the left than to the right region at higher PEs. This possibly indicates that the center of the laser spot, or the center of the charge deposition, was shifted toward the left direction with increasing PE.

A possible configuration is that the center of the laser spot is located in the middle of an n-well at the higher PEs, as depicted in Fig. 2.10 (a). In this figure, four SRAM cells along the BL direction is illustrated with node voltages before the laser irradiation in the case of the CKB0 pattern, where the cells are numbered from 1 to 4. For this configuration, two possible cases of fail bit patterns are explored in Fig. 2.10 (b) and (c). Fig. 2.10 (b) shows the case where PBEs in the nMOS transistors (marked with dotted circles) are dominant. In this case, in each cell, the node where the nMOS transistor is closer to the center of the laser spot can be pulled down: the right nodes in the cells 1 and 4, the left nodes in the cells 2 and 3. Hence, the cells 3 and 4 become fail bits. On the other hand, Fig. 2.10 (c) shows the case where PBEs in the pMOS transistors (marked with dotted circles) are dominant. In this case, in each cell, the node where the pMOS transistor is closer to the center of the laser spot can be pulled up: the right nodes in the cells 1 and 4, the left nodes in the cells 2 and 3. As a result, the cells 1 and 2 become fail bits. These processes can play a role in

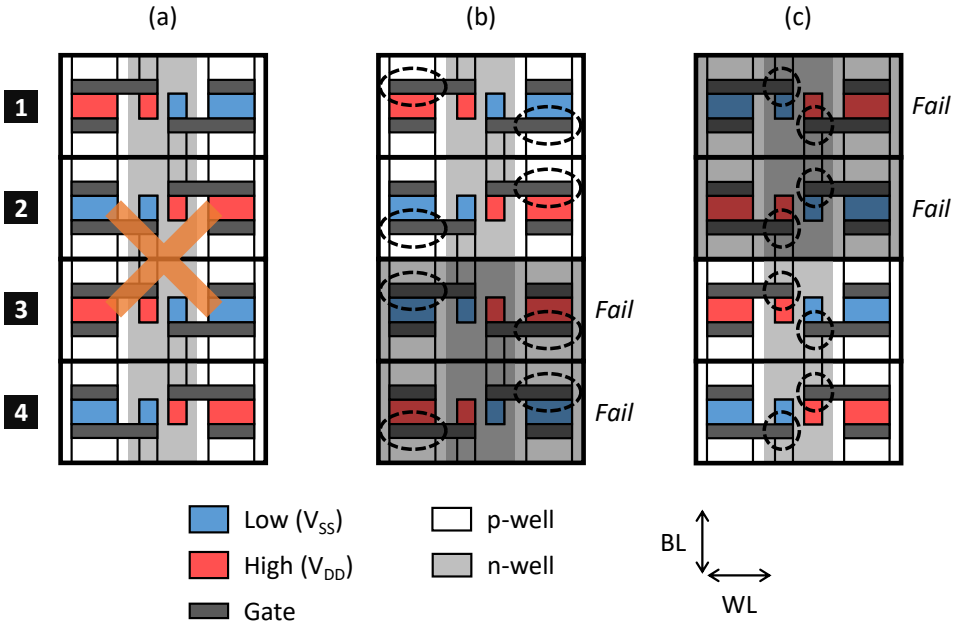

FIGURE 2.10: Fail bit patterns along the BL direction caused by well potential perturbation. (a) Schematic layout of four SRAM cells with node voltages before the laser irradiation in the case of the CKB0 pattern, where the orange cross indicates the center of the laser spot. (b) The four SRAM cells with node voltages after the laser irradiation when PBEs in the nMOS transistors (marked with dotted circles) are dominant. (c) Same as (b), but when PBEs in the pMOS transistors (marked with dotted circles) are dominant. Blue and red regions depict low (V_{SS}) and high (V_{DD}) voltages of the internal nodes, respectively. Gray cells correspond to fail bits.

making the fail bit pattern irregular. Here, the case of Fig. 2.10 (c) corresponds to the WCSI mechanism [56].

2.3.4 MCU Response to Multiple Single-Pulse Laser Irradiation

The important nature of the MWCPU mechanism is that fail bit patterns along the WL direction are determined by the relative position between the distribution of charge deposition and the internal nodes of SRAM cells, as discussed in the previous section. To verify this nature, MCU responses against multiple-pulse laser irradiation was investigated in terms of fail bit patterns and their transitions. In this investigation, the SRAM chip was irradiated by a single laser pulse four times consecutively at the same position. The key point here is that the fail bit patterns are expected to remain unchanged after the second and later irradiation when the MWCPU mechanism is dominant. This is because the relative position between the laser spot and the internal nodes in the second and later irradiation is basically the same as that in the first irradiation. On the other hand, when the MWCPU mechanism is less significant, the fail bit patterns are expected to change after every irradiation because, for example, fail bits induced in the first irradiation can become pass bits in the second irradiation.

TABLE 2.1: Category of bit state transition.

Name	Description
Fail	New fail bits in 2nd or later cycles
Pass	Bits changed to pass after undergoing "Fail"
Re-Fail	Bits changed to fail after undergoing "Pass"
Re-Pass	Bits changed to pass after undergoing "Re-Fail"

FBMs obtained through the multiple-pulse laser irradiation revealed that fail bit patterns were dominated by the MWCPU mechanism. Fig. 2.11 presents the FBMs for the All1 and CKB0 patterns. As illustrated in this figure, consecutive hold and read cycles were repeated four times after the data pattern was written. The single laser pulse irradiation was performed in each hold cycle, where the PEs were 0.52 and 0.98 nJ for the All1 and CKB0 patterns, respectively. The FBM was obtained in each read cycle. These FBMs clearly demonstrated that the fail bit patterns were almost unchanged after every irradiation in both the All1 and CKB0 patterns. From the above description, this result is considered to indicate that the dominant mechanism underlying the observed MCUs is the MWCPU mechanism. It is also interesting to note that the topology of the fail bit patterns for the All1 pattern in Fig. 2.11 was different from that in Fig. 2.6. This difference is probably due to the different position of the laser spot. In the same way as in Fig. 2.7, the center of the laser spot in the multiple-pulse irradiation was estimated to be located in a p-well where low nodes were placed, which corresponds to the p-well 2 in Fig. 2.7. In this case, the fail bit patterns for the All1 pattern in Fig. 2.11 can be understood by the MWCPU mechanism in a similar way to Fig. 2.9.

The analysis of the state transition of each bit also confirmed the dominance of the MWCPU mechanism. In this analysis, the state transition was categorized into four types: "Fail," "Pass," "Re-Fail," and "Re-Pass," as described in Table 2.1. The number of bits for each category was extracted from the FBMs shown in Fig. 2.11. In Fig. 2.12, the extracted numbers are shown as a function of test cycle, where Fig. 2.12 (a) and (b) are for the All1 and CKB0 patterns, respectively. The total number of fail bits is also presented by circle symbols in Fig. 2.12, where the left axis corresponds to this total number. This analysis clearly demonstrated that the variation of the total number of fail bits was only a few percent, and that only a few bits underwent the state transition in the second or later cycles. These results are consistent with the expected characteristics of the MWCPU mechanism, supporting the dominance of this mechanism in the observed MCUs.

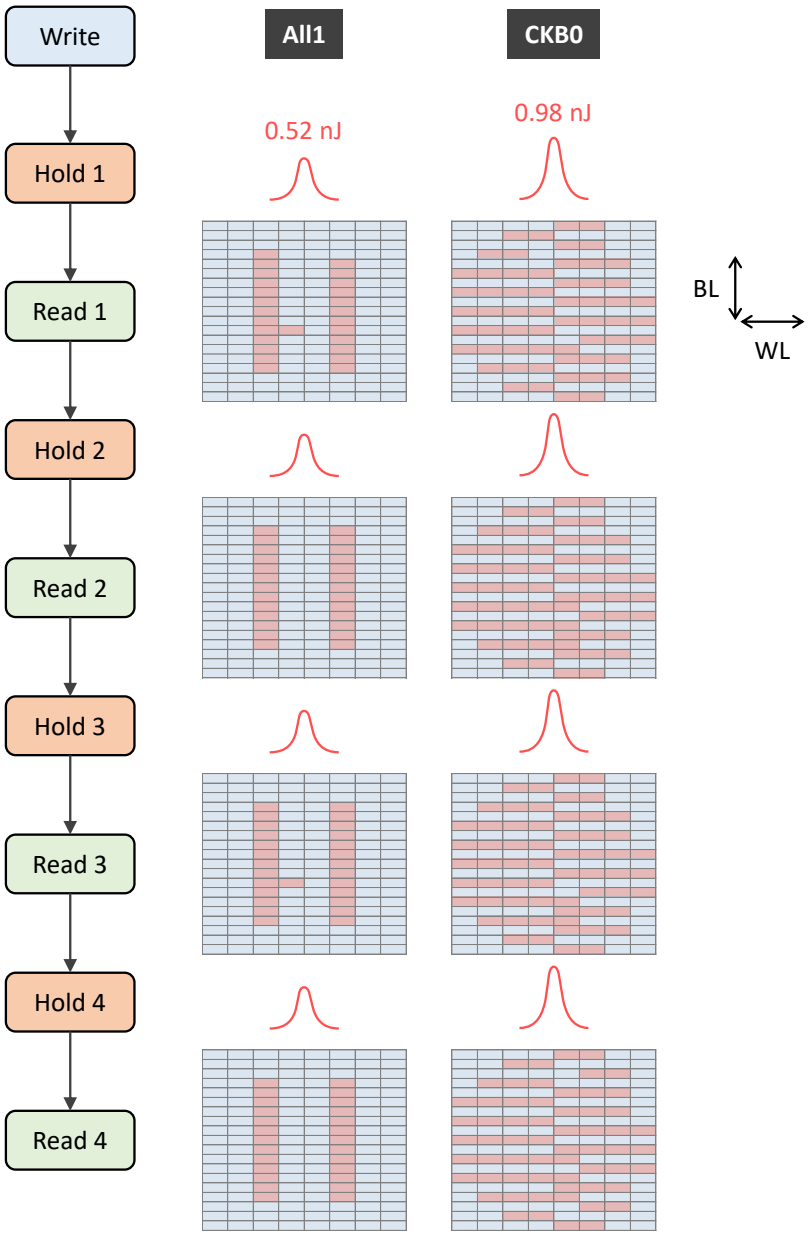

FIGURE 2.11: FBMs in multiple-pulse laser irradiation for All1 and CKB0 patterns. The left and right FBMs are for the All1 and CKB0 patterns, respectively. Small rectangular cells represent SRAM cells. Blue and red cells correspond to pass and fail bits, respectively. Vertical and horizontal directions are parallel to Bl and WL directions, respectively. The PEs for the All1 and CKB0 patterns are 0.52 and 0.98 nJ, respectively. The measurement flow is depicted in the left part. Supply voltage is 0.7 V. Note that the focal position is different from that in Fig. 2.6.

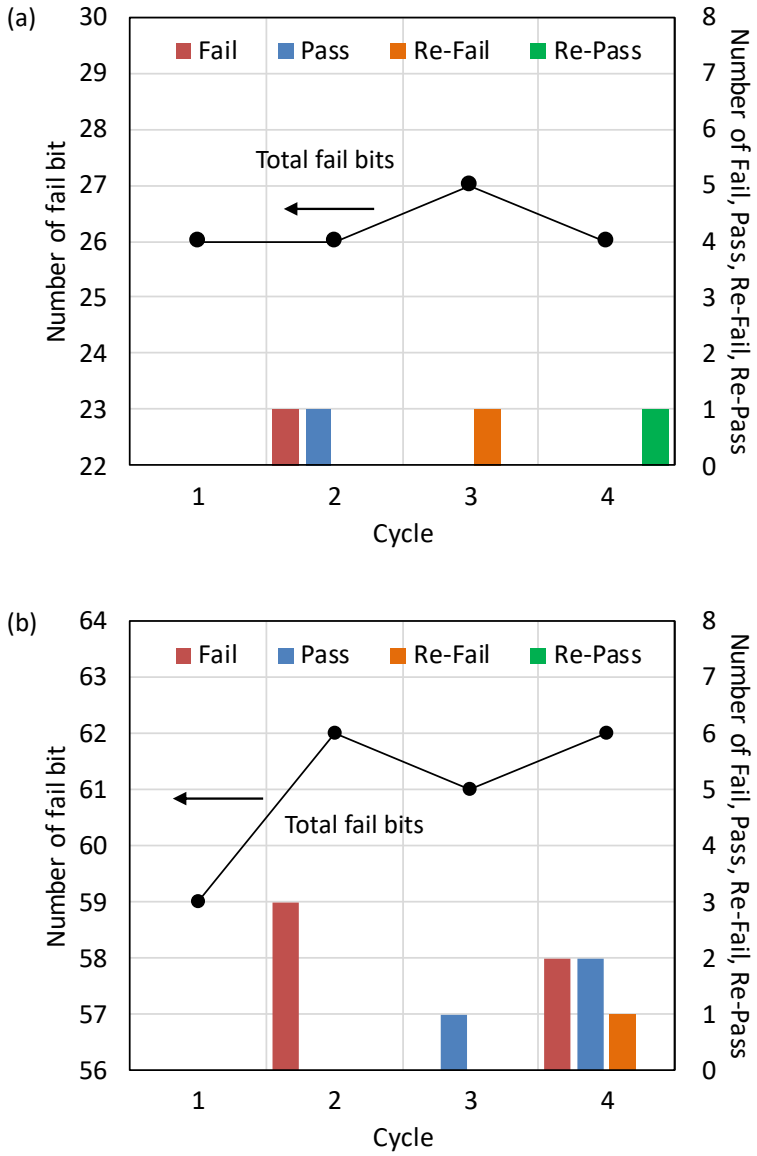

FIGURE 2.12: Numbers of total fail bits and bit state transition as a function of test cycle in multiple-pulse laser irradiation. These numbers are based on the FBMs shown in Fig. 2.11, (a) and (b) are for the All1 and CKB0 patterns, respectively. Black circle symbols are the total number of fail bits. Color bars represent the number of bit state transition categorized as in Table 2.1: "Fail" (red), "Pass" (blue), "Re-Fail" (orange), and "Re-Pass" (green).

2.4 Conclusion

In this chapter, the pulse laser irradiation experiments have unveiled the novel MCU mechanism named MWCPU. It has been demonstrated that charge deposition on multiple wells can trigger the MWCPU mechanism through the unbalanced activation of PBEs in multiple wells, and that the MWCPU mechanism causes particular fail bit patterns that strongly depend on the relative position between the internal nodes of SRAM cells and the distribution of charge deposition.

The laser irradiation experiments have been performed on the 20-nm bulk planar SRAMs by using the single-pulse TPA system. The basic characteristics of the TPA-induced SEUs have been investigated by the single laser pulse irradiations with varying the focal position, PE, and supply voltage. The observed SEU characteristics have been consistent with the typical characteristics of TPA-induced charge deposition. The FBM analyses have revealed that particular fail bit patterns are induced by the charge deposition on multiple SRAM cells, and that the topology of the fail bit patterns is significantly different between the All1 and CKB0 patterns. It has been found that these observations can be explained by the imbalance of PBEs across multiple p-wells. On the basis of this finding, the MWCPU mechanism has been proposed. The significant contribution of the MWCPU mechanism on the observed MCUs has been confirmed in the results of the multiple single-pulse laser irradiation.

In conclusion, this study has demonstrated that the MWCPU mechanism is one of the important MCU mechanisms affecting the MCU characteristics, and its contribution can increase with technology scaling. This is because the size scaling of SRAM cells results in the higher probability of charge deposition on multiple wells. It should be noted that the MWCPU mechanism is not specific for the laser irradiation. As mentioned in Sec. 2.1, the ion incidence angle and the radial charge distribution can be the factors leading to charge deposition on multiple wells. For high-energy neutrons, their grazing incidence is one of the cases where the MWCPU mechanism is expected to be significant. In this case, the charge deposition on multiple wells can easily occur due to the forward emission of secondary ions. This point is investigated in the next chapter.

Chapter 3

Angular Sensitivity of Neutron-Induced SEUs in Planar SRAMs

This chapter studies the impact of incidence angle on high-energy neutron-induced SEUs in 20-nm bulk planar SRAMs. [1] Irradiation experiments are performed using a terrestrial environment-compatible source with varying incidence angle. The results reveal that, although the SEU rate decreases at grazing incidence, the MBU rate significantly increases at grazing incidence. This result indicates that the efficiency of ECCs can be reduced depending on the device orientation in the terrestrial environment. The analyses of MCU characteristics demonstrate that the forward emission of secondary ions, the geometry of SRAM cells, and PBEs are key factors determining the angular sensitivity of high-energy neutron-induced MCUs. Furthermore, the analyses of fail bit patterns unveil an unique data pattern dependence in the occurrence probability of gap structures in fail bit patterns. On the basis of the discussion in Chap. 2, the MWCPU mechanism is found to be the plausible mechanism underlying the gap structures. The detailed analyses of fail bit arrangements with consideration of internal node voltages demonstrate that the configurations of the observed gap structures are consistent with the configuration induced by the MWCPU mechanism.

3.1 Introduction

MCUs are critical issues in the reliability of SRAM devices, as described in Sec. 1.3.3. The high-risk cases of the MCUs are MBUs, which cannot be corrected by simple ECCs. From the viewpoint of the estimation and prediction of the efficiency of SEU mitigation techniques, such as ECCs and bit-interleaving methods, it is essential to explore and understand factors affecting the probability and characteristics of the MCUs and the MBUs in SRAM devices.

The size of SRAM cells is a well-known factor affecting the probability of MCU occurrence. The scaling of SRAM cells has increased their susceptibility to MCUs

[1] This chapter is based on [78].

[51], [52], [61]. As mentioned in Sec. 1.3.5, this is mainly due to the increased probability that an ion passes through multiple SRAM cells and deposits charge on these cells, which can result in multiple fail bits along the ion track. This also leads to the increased probability of MBU occurrence.

The incidence angle of ions has been reported to have a considerable impact on MCU characteristics [55], [79]–[83]. Musseau *et al.* [55] demonstrated that the spatial range of heavy ion-induced MCUs becomes large at grazing incidence. Ikeda *et al.* [80] showed that, for proton irradiation, MCU CSs increase at grazing incidence in a 180-nm bulk SRAM, where the relevance between fail bit patterns and the physical arrangement of sensitive transistors was indicated. Tipton *et al.* [82] demonstrated that, for heavy ion irradiation, MCU CSs increase at grazing incidence in a 65-nm bulk SRAM, and that the spatial distribution of fail bits depends on the incidence angle. Tonfat *et al.* [83] reported the angular effect for heavy ion irradiation in a 28-nm SRAM-based field-programmable gate array (FPGA), demonstrating that the MBU CS depends on the rotation angle of the FPGA.

In the terrestrial environment, high-energy neutrons are the major source for MCUs in SRAM devices. As is the case with protons and heavy ions, high-energy neutron-induced MCUs have been reported to be sensitive to the incidence angle [57]–[59]. Tipton *et al.* [57] demonstrated that the MCU probability increases with the angle of neutron incidence in a 90-nm bulk SRAM. Harada *et al.* [58] and Hirokawa *et al.* [59] also demonstrated that MCU rates increase at grazing incidence of neutrons in 65-nm bulk SRAMs. Although MCUs are important events in determining the SEU tolerance of SRAM devices, there have been only a few reports on the angular sensitivity of high-energy neutron-induced MCUs. Since, as mentioned above, the shrinkage of SRAM cells increases the MCU susceptibility, it is worthwhile to investigate and grasp the angular sensitivity of MCUs and MBUs in more advanced SRAM devices.

The important point in investigating MCUs in advanced SRAM devices is to consider the underlying mechanisms. This is because, as SRAM cells and the constituting transistors have scaled down, the physical mechanisms causing MCU events have become more complicated. As mentioned in Sec. 1.3.6, PBEs has been identified as a mechanism having a significant impact on MCU characteristics. Osada *et al.* [63] demonstrated that the PBEs triggered by p-well potential perturbation increase the MCU probability in a 130 nm bulk SRAM. Gasiot *et al.* [64] also showed the considerable contribution of PBEs in p-wells on the MCU probability for a 65 nm bulk SRAM. In addition to the impact of PBEs on MCU probabilities, it has been reported that MCU events with particular fail bit patterns can be caused by the combination of multiple PBEs, such as MCBI and WCSI mechanisms [54], [56]. Furthermore, as demonstrated in Chap. 2, the MWCPU mechanism triggered by potential perturbation in multiple p-wells can also cause MCU events with particular fail bit patterns. Therefore, it is meaningful to explore the angular sensitivity of MCUs in terms of both occurrence probability and fail bit patterns in advanced SRAM devices.

This study experimentally investigates high-energy neutron-induced SEUs in 20 nm bulk SRAMs for several angles of neutron incidence. The impact of the incidence angle on the SEU, MCU, and MBU rates is evaluated by irradiating SRAM chips with atmospheric-like neutrons. The characteristics of MCU events are statistically analyzed in terms of their sizes and fail bit patterns. The underlying MCU mechanism is then discussed on the basis of the incidence angle and data pattern dependence of the MCU characteristics. In order to explain the unique data pattern dependence of gaps observed in fail bit patterns, the impact of the MWCPU mechanism is examined. Finally, FBMs, which provide information on fail bit arrangements, are analyzed to explore the physical configurations that can trigger the MWCPU mechanism.

3.2 Experimental Setup

3.2.1 Tested Device and Operation

The test vehicles were SRAM chips fabricated in a 20-nm bulk planar CMOS process. The package type was a standard quad flat package. Note that the SRAM chips used in this study were the same as that used in Chap. 2.

The SRAM operation consisted of, in order, write, hold, and read cycles. All tests were performed in a static mode, with no write and read functions during the hold cycles. The number and physical locations of fail bits caused by high-energy neutron irradiation were obtained in the read cycle. The supply voltage in the hold cycle was varied from 0.6 V to 1.0 V to investigate the voltage dependence of SEU, MCU, and MBU responses.

In the SRAM operation, two types of data patterns were employed: All0 and CKB0. In the case of the All0 pattern, a logical "0" was written in all the bits. In the case of the CKB0 pattern, logical "0" and "1" were physically arranged in a checkerboard pattern, where "0" was written in the first bit. The arrangements of node voltages for the All0 and CKB0 patterns are illustrated in Fig. 3.1(a) and (b), respectively. In each figure, a 4×4 SRAM cell array is depicted with rectangular cells, where blue and red boxes represent low (V_{SS}) and high (V_{DD}) states of internal nodes, respectively. Since the states of "0" and "1" are physically identical in the symmetric cell structure, as explained in Sec. 1.3.1, the All0 pattern is topologically equivalent to the All1 pattern used in Chap. 2.

3.2.2 High-Energy Neutron Irradiation

High-energy neutron irradiation testing was performed at the Research Center for Nuclear Physics (RCNP), Osaka University. All tests were carried out using the spallation neutron beam at the WN course [84]. As shown in Fig. 3.2, the energy spectrum of the neutron beam was similar to the terrestrial one in the energy range from 1 to 300 MeV [18]. The integral neutron flux above 10 MeV was $\sim 2.5 \times 10^9$

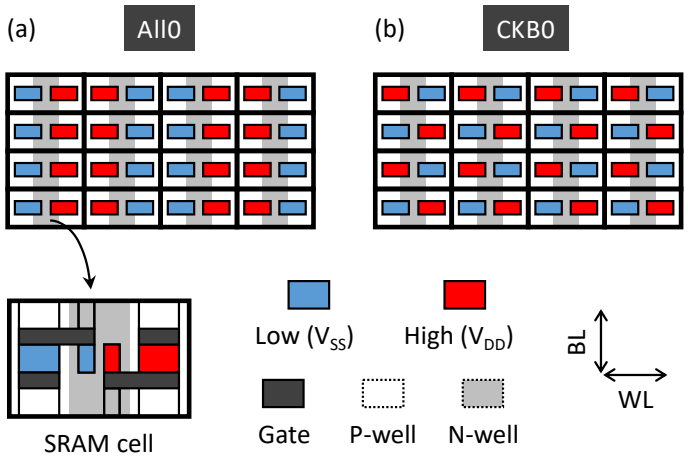

FIGURE 3.1: SRAM node voltages for (a) All0 and (b) CKB0 patterns. Rectangular cells correspond to SRAM cells. The schematic illustration of the cell layout is shown in the lower part. Vertical and horizontal directions are parallel to BLs and WLs, respectively. Blue and red rectangular boxes inside the SRAM cells depict internal nodes of low (V_{SS}) and high (V_{DD}) voltages, respectively. White and gray regions represent p-wells and n-wells, respectively.

cm^2/h, which was higher that the terrestrial neutron flux by more than eight orders of magnitude.

The SRAM chips were irradiated by the neutron beam at four angles of incidence: 0°, 45° (WL), 90° (WL), and 90° (BL). The irradiation geometries for these conditions are schematically illustrated in Fig. 3.3. The angle of 0° corresponds to the incidence direction normal to the silicon die [see Fig. 3.3(a)]. The angles of 90° (WL) and 90° (BL) correspond to the incidence directions parallel to the WLs and BLs of SRAM cells, respectively [see Fig. 3.3(c) and (d)]. The angle of 45° (WL) is the midpoint between the angles of 0° and 90° (WL) [see Fig. 3.3(b)]. These configurations were obtained by changing the setting direction of test boards (chips) with respect to the direction of the neutron beam.

3.2.3 Rate Calculation

For the calculation of SEU, MCU, and MBU rates, SBU, MCU, and MBU events were distinguished according to the spatial distribution of fail bits. Here, the SEU events correspond to the sum of the SBU and MCU events. The MBU events correspond to the MCU events in which multiple fail bits occur in the same WL. It should be noted that the number of fail bits observed in one read cycle was kept small to sufficiently suppress the contamination of pseudo-MCU events, which can be induced by the superposition of SBU events.

The calculation of the SEU, MCU, and MBU rates was performed according to the JEDEC standard [18]. As explained in Sec. 1.3.4, the event rate is given as $\sigma_{\mathrm{event}} \times \phi_{\mathrm{n}}$, where σ_{event} and ϕ_{n} are the event cross sections and the neutron flux of interest, respectively Here, the event means SEUs, MCUs, and MBUs. The cross section σ_{event}

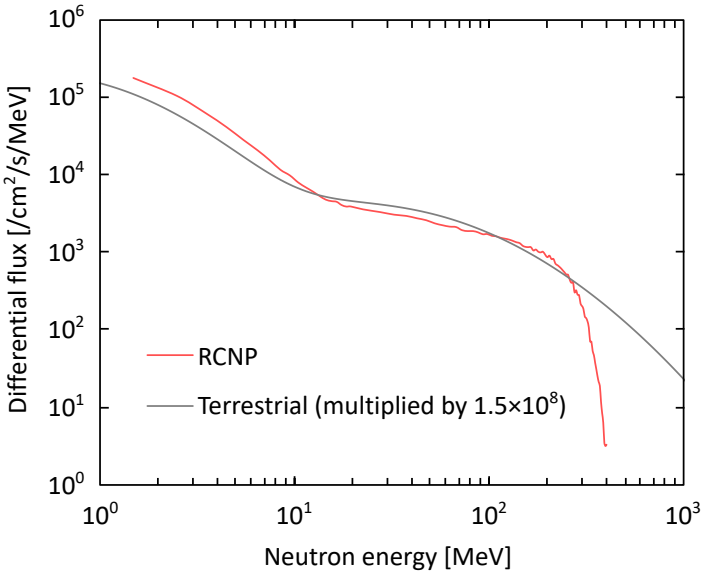

FIGURE 3.2: Neutron energy spectrum of spallation neutron beam at the WN course, RCNP (red line) [84] and terrestrial neutron at sea level, New York City (black line) [18]. The flux of the terrestrial neutron is multiplied by 1.5×10^8.

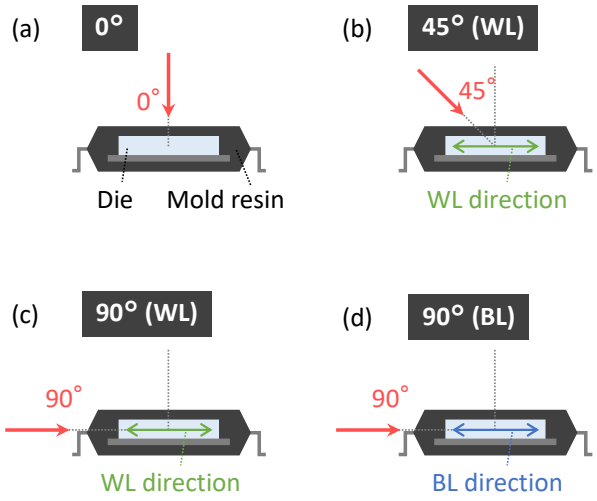

FIGURE 3.3: Four incidence angles of high-energy neutron irradiation: (a) 0°, (b) 45° (WL), (c) 90° (WL), and (d) 90° (BL). (a) 0° is normal incidence from the top of the chip. (c) 90° (WL) and (d) 90° (BL) correspond to incidence directions parallel to the WLs and BLs of SRAM cells, respectively. (b) 45° (WL) is the midpoint between 0° and 90° (WL).

was obtained as $N_{\text{event}}/(\Phi_{\text{n}} \times N_{\text{bit}})$, where N_{event} is the number of the observed events, Φ_{n} is the incident neutron fluence, N_{bit} is the number of bits irradiated.

3.3 Results and Discussion

3.3.1 Angular Dependence of SEU, MCU, and MBU Rates

The high-energy neutron irradiation with varying the incidence angle clearly showed the angular dependence of SEU, MCU, and MBU rates. The SEU, MCU, and MBU rates are presented as a function of the supply voltage in Fig. 3.4(a), (b), and (c), respectively. In each graph, the rates for the incidence angles of 0°, 45° (WL), 90° (WL), and 90° (BL) are shown by the red, orange, green, and blue symbols, respectively. Note that these rates are the values averaged over the All0 and CKB0 patterns.

The SEU rate decreased with increasing angle of incidence for all voltage conditions, as confirmed in Fig. 3.4(a). This is obvious from the geometrical configuration of irradiation, where the number of neutrons passing through the SRAM chip in a unit of time is reduced at grazing incidence. This directly leads to the reduction in the frequency of secondary ion production at grazing incidence, and hence the SEU rate decreases. The coincidence observed between the SEU rates at the angles of 90° (WL) and 90° (BL) can also be explained by the the number of passing neutrons because the number of passing neutrons is the same between these incidence angles, supporting the above geometrical consideration.

It is interesting to focus on the quantitative differences among the SEU rates for the four angles of neutron incidence. From Fig. 3.4(a), the ratio of the SEU rate for the angle of 45° (WL) to that for the angle of 0° was estimated as $\sim$0.81. This value was slightly larger than the ratio between these visible CSs of the test chip to the neutron beam, which can be easily calculated as $\cos(\pi/4) = 0.71$. This difference means that the probability that one neutron induces an SEU event is higher at the incidence angle of 45° (WL) than that at the angle of 0°. One possible reason for this is the angular distribution of secondary ion emission. As explained in Sec. 1.2.1, secondary ions produced through high-energy neutron-induced spallation reactions tend to be emitted forward. Since the SRAM cells are arranged in a two-dimensional (2D) array at the surface of the silicon substrate, the secondary ions produced at grazing incidence are more likely to generate longer tracks in the SRAM array compared to the normal incidence case (0°). This leads to higher probability of charge deposition on the sensitive regions of SRAM cells at grazing incidence. Another possible reason is the increased track length of neutrons inside the chip at grazing incidence. This results in the increased probability that one neutron interacts with device materials while traveling inside the chip including the package structure. Similarly, the above mechanisms could be significant at the angles of 90° (WL) and 90° (BL). These results indicate that, in the grazing incidence case, SEU rates can be higher than that predicted from the ratio of visible CSs.

For the MCU rate, the angular dependence was weak compared to the SEU rate, as confirmed in Fig. 3.4(b). On the other hand, the strong angular dependence was demonstrated in MCU ratios, which were calculated by dividing the MCU rate with the SEU rate. In Fig. 3.5, the MCU ratios for the four incidence angles are presented

as a function of the supply voltage. It was seen that the MCU ratios substantially increased with increasing angle of neutron incidence. This result indicates that secondary ions produced at grazing incidence tend to cause MCU events. This is probably due to the forward emission of secondary ions, which leads to charge deposition on multiple SRAM cells at grazing incidence. Similar observations were reported in [57]–[59]. Another important observation in Fig. 3.5 was the difference between the angles of 90° (WL) and 90° (BL), where the MCU ratio for the angle of 90° (BL) was higher than that for the angle of 90° (WL). This point is discussed in the next section.

For the MBU rate shown in Fig. 3.4(c), it was found that the MBU rate significantly increased at the incidence angles of 45° (WL) and 90° (WL), in contrast to the decrease in the SEU rate at these angles [see Fig. 3.4(a)]. On the other hand, the MBU rate at the angle of 90° (BL) showed no increase, although the MCU ratio at this angle was the highest among the four incidence angles. The detailed analysis for this point is presented in the next section.

From the point of view of practical applications, the observed angular dependence of MBU rates gives an important insight into the implementation of ECCs. Since, as described in Sec. 1.2.1, the large proportion of terrestrial neutrons is directed downward at sea level, this result indicates that the efficiency of ECCs can be limited in the case where SRAM chips are vertically mounted and the WLs are vertical to the ground [10]. This is because this condition corresponds to the experimental condition of the angle of 90° (WL). According to the results of Fig. 3.4(c), the high-energy neutron SER of the vertically mounted SRAM devices with ECCs can be doubled compared to the horizontally mounted ones.

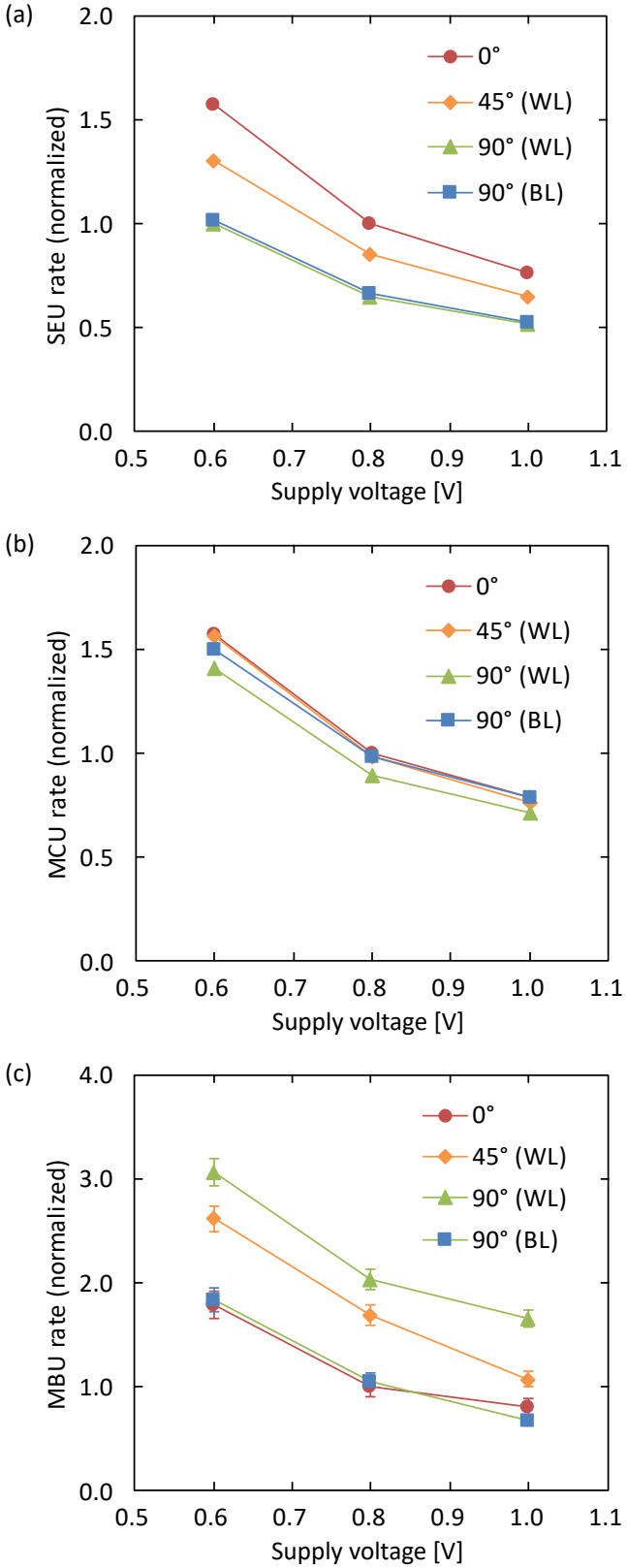

FIGURE 3.4: (a) SEU rate, (b) MCU rate, and (c) MBU rate as a function of supply voltage for the neutron incidence angles of 0°, 45° (WL), 90° (WL) and 90° (BL). Each rate is normalized by the value at 0.8 V for the angle of 0°. All rates are the values averaged over the All0 and CKB0 patterns. Error bars are shown when larger than the symbol size and represent one standard error.

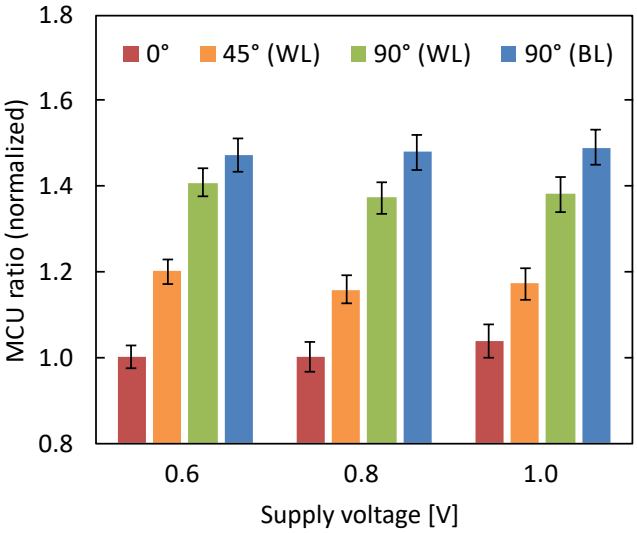

FIGURE 3.5: MCU ratio as a function of supply voltage for the neutron incidence angles of 0°, 45° (WL), 90° (WL) and 90° (BL). All ratios are the values averaged over the All0 and CKB0 patterns. Error bars represent one standard error.

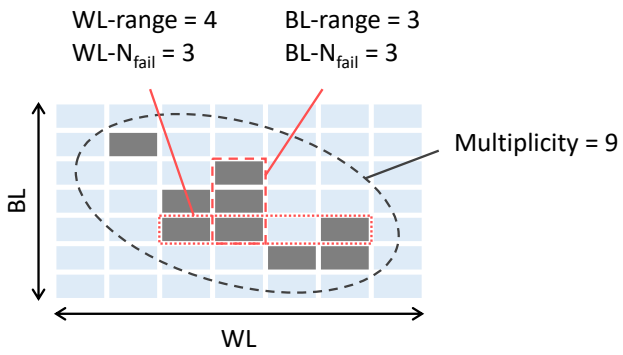

FIGURE 3.6: Example for the characterization of an MCU event. Rectangular cells are SRAM cells. Gray cells represent fail bits Vertical and horizontal directions are parallel to BL and WL directions.

3.3.2 Characterization of MCU Events

As observed in the previous section, the angular dependence of the MCU and MBU rates is different from that of the SEU rate. To understand this difference, the MCU events were statistically analyzed in terms of the size and topology of fail bits. The parameters examined in the characterization of MCU events were multiplicity, WL-range, BL-range, WL-N_{fail}, and BL-N_{fail}. The multiplicity is the number of fail bits included in an MCU event. The WL-range and BL-range are the maximum ranges of a fail bit pattern along the WL and BL, respectively. The WL-N_{fail} and BL-N_{fail} are the number of fail bits included in the regions corresponding to the WL-range and BL-range, respectively. An example of the MCU characterization is demonstrated in Fig. 3.6, where the rectangular cells are SRAM cells, and gray cells represent fail bits. Here, the vertical and horizontal directions are parallel to the BLs and WLs, respectively. In this example, the multiplicity of the MCU event is 9. The regions corresponding to the WL-range and BL-range are marked with red lines. As denoted in Fig. 3.6, this MCU event can be parameterized as WL-range $= 4$, BL-range $= 3$, WL-$N_{fail} = 3$, and BL-$N_{fail} = 3$.

The multiplicity distribution shown in Fig. 3.7 clearly demonstrated that the ratio of the MCU events with high multiplicities increases at grazing incidence of high-energy neutrons. In Fig. 3.7, the multiplicity distributions for the incidence angles of 0°, 45° (WL), 90° (WL), and 90° (BL) are presented, where the ratio of 100% corresponds to the total MCU events. Here, the ratios of events with the multiplicity of ≥ 9 are separately shown in the inset. As confirmed in this figure, the ratios for the angles of 90° (WL), and 90° (BL) were considerably higher than that for the angle of 0° at the multiplicities higher than three. At the same time, the ratio for the angle of 45° (WL) was intermediate between the ratios of the 0° and 90° (WL) angles. These results indicate the effect of the forward emission of secondary ions. As described above, due to this forward emission, the secondary ions produced at grazing incidence can generate longer tracks in the SRAM array and hence can deposit charge on multiple SRAM cells. Obviously, this leads to the increased number of fail bits in an MCU event, i.e., the higher multiplicity.

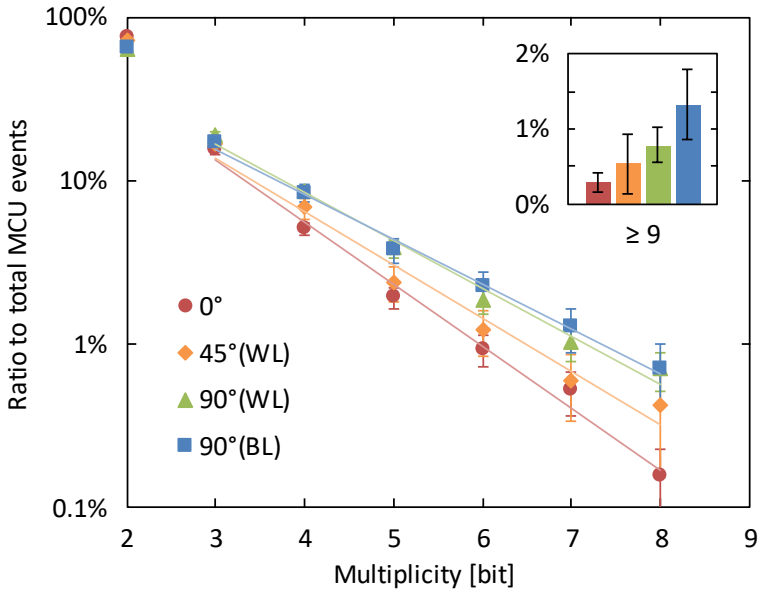

FIGURE 3.7: Multiplicity distributions of high-energy neutron-induced MCU events. Red, orange, green, and blue symbols correspond to the incidence angles of 0°, 45° (WL), 90° (WL) and 90° (BL), respectively. The ratios for the multiplicity of $\geq$ 9 are shown in the inset (bar diagram). All ratios are the values averaged over the All0 and CKB0 patterns and all voltage conditions. Lines are exponential fits for eye guide. Error bars represent one standard error.

When focusing on the multiplicity of $\geq$ 9 shown in the inset of Fig. 3.7, it is seen that the ratio for the angle of 90° (BL) was higher than that for the angle of 90° (WL). This difference is probably due to the interrelationship between the forward emission of secondary ions and the geometry of SRAM cells, as suggested in [57]–[59]. As depicted in Fig. 3.6, the SRAM cells were of rectangular shape, where the short side was parallel to the BLs. In this configuration, an ion with a given track length can pass more number of the SRAM cells when the ion travels along the BLs. At the same time, because of the forward emission of secondary ions, this situation is more likely to occur when the incidence direction of high-energy neutrons is parallel to the BLs. The higher ratio observed for the angle of 90° (BL) at the multiplicity of $\geq$ 9 is consistent with this picture. Similarly, the higher MCU ratio for the angle of 90° (BL) seen in Fig. 3.5 is probably attributed to the above situation.

As regards the spatial ranges of MCU events, the BL-range and WL-range were analyzed for the All0 and CKB0 patterns separately. The distributions of the BL-range and WL-range for the two data patterns are presented in Fig. 3.8 and 3.9, respectively. In each figure, the upper (a) and lower (b) graphs correspond to the All0 and CKB0 patterns, respectively. To understand the results of the comparison between the All0 and CKB0 patterns, it is worthwhile to focus here on the arrangement of internal node voltages for these patterns, which are illustrated in Fig. 3.1. Since nMOS transistors in high nodes are generally vulnerable to charge collection, as described in Sec. 1.3.2, the physical arrangement of high nodes has significant

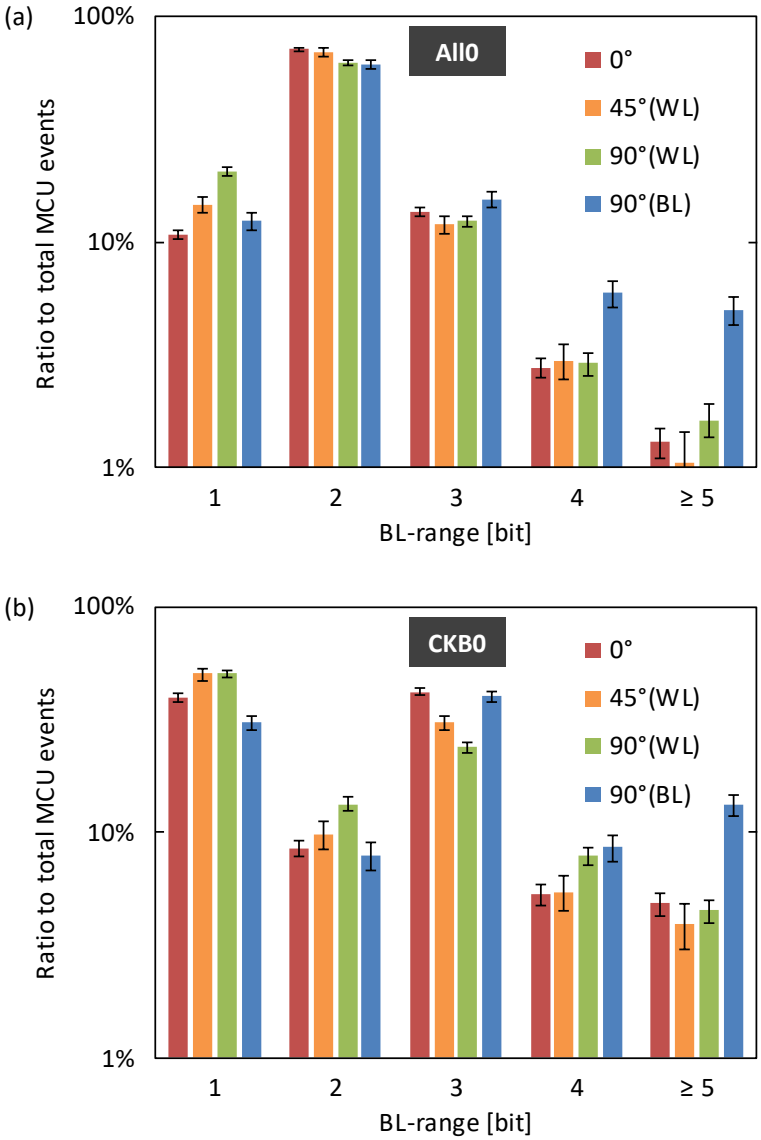

FIGURE 3.8: BL-range distributions of high-energy neutron-induced MCU events for (a) All0 and (b) CKB0 patterns. Red, orange, green, and blue bars correspond to the incidence angles of 0°, 45° (WL), 90° (WL) and 90° (BL), respectively. All ratios are the values averaged over all voltage conditions. Error bars represent one standard error.

influence on fail bit patterns, i.e the BL-range and WL-range. As seen in Fig. 3.1, in the case of the All0 pattern, the nMOS transistors in high nodes are densely packed in the p-wells. On the other hand, in the case of the CKB0 pattern, those are equally distributed across all the p-wells.

The BL-range distribution was different for the different incidence angles of neutrons and the different data patterns, as observed in Fig. 3.8. In this figure, the BL-range distributions for the angles of 0°, 45° (WL), 90° (WL), and 90° (BL) are presented for the All0 and CKB0 patterns. As for the comparison between the angles of 90° (WL) and 90° (BL), the ratios at the BL-ranges of ≥ 3 were larger for the angle of 90° (BL) in both the data patterns. This strongly indicates the impact of the forward

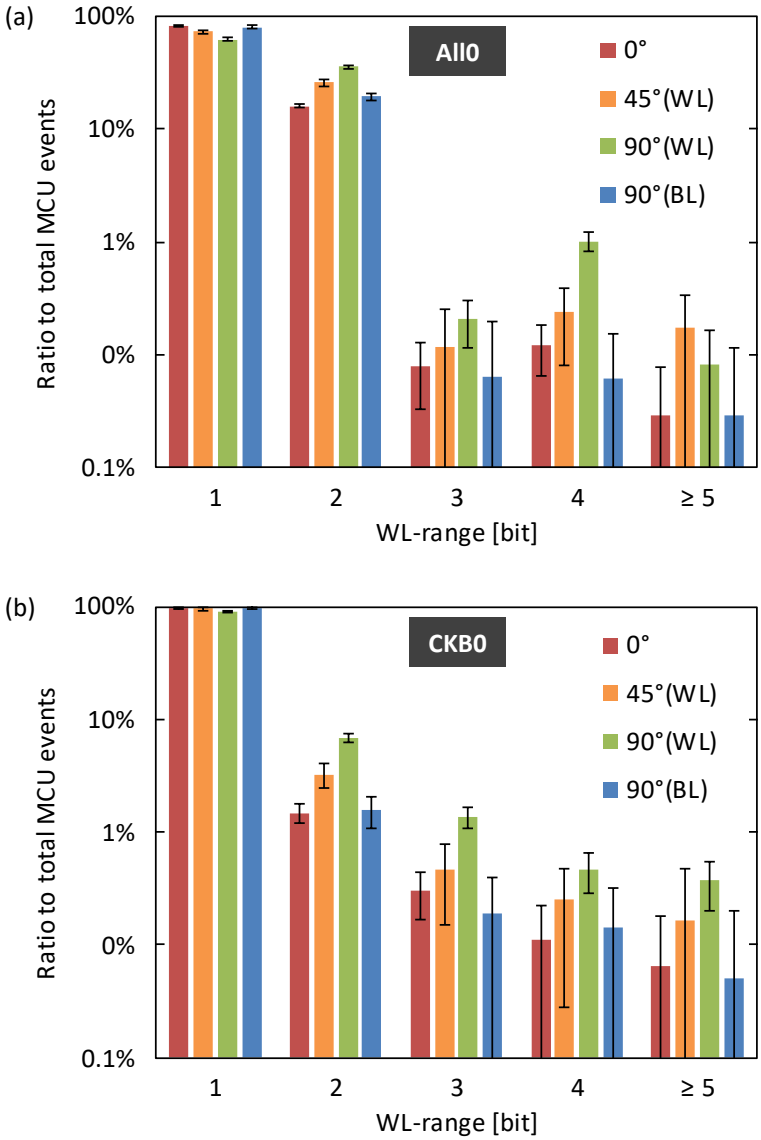

FIGURE 3.9: WL-range distributions of high-energy neutron-induced MCU events for (a) All0 and (b) CKB0 patterns. Red, orange, green, and blue bars correspond to the incidence angles of 0°, 45° (WL), 90° (WL) and 90° (BL), respectively. All ratios are the values averaged over all voltage conditions. Error bars represent one standard error.

emission of secondary ions because the incidence angle of 90° (BL) can cause the long tracks of the ions along the BL direction. As for the comparison between the All0 and CKB0 patterns, the large difference was found in the BL-range from 1 to 3 for all the incidence angles. In the case of the All0 pattern, the most frequent BL-range was 2. In contrast, in the case of the CKB0 pattern, the ratios of the BL-ranges of 1 and 3 were high. This discrepancy can be understood by the configuration of node voltages described above, together with PBEs in p-wells. The key point here is that, since p-wells are continuous along the BL direction, potential perturbation in a p-well can activate PBEs in multiple nMOS transistors along the BL direction. In this case, the difference in the physical arrangement of high nodes in the p-well

results in the different BL-range distribution. In the case of the All0 pattern [see Fig. 3.1(a)], the nearest SRAM cell having the high node in the same p-well is the first neighbor cell (the vertically or horizontally adjacent cell). On the other hand, in the case of the CKB0 pattern [see Fig. 3.1(b)], it is the second neighbor cell (the diagonally adjacent cell). This different arrangement results in the decrease in the ratio at the BL-range of 2 for the CKB0 pattern, and the ratios at the BL-ranges of 1 and 3 increase in comparison, as observed in Fig. 3.8.

The WL-range distribution was also different among the incidence angles and the data patterns, as confirmed in Fig. 3.9. In this figure, the WL-range distributions are presented in the same manner as in Fig. 3.8. It was observed that the ratios at the WL-ranges of $\geq$ 2 tend to increase as the incidence direction approached the WL direction. Similar to the discussion in the BL-range distribution, this can be understood by the forward emission of secondary ions. The point to note here is that the events with the WL-ranges of $\geq$ 2 correspond to MBU events. Therefore, the considerable increase in the MBU ratio at the angles of 45° (WL) and 90° (WL) seen in Fig. 3.4(c) can be interpreted as the impact of the forward emission. For the comparison between the All0 and CKB0 patterns, it was observed that, in the case of the All0 pattern, the ratio at the WL-range of 2 was higher than that in the case of the CKB0 pattern. This observation can be explained by the arrangement of high nodes and PBEs in p-wells, as similarly discussed in the BL-range distribution. As seen in Fig. 3.1, in the case of the All0 pattern, high nodes of horizontally adjacent SRAM cells are located in the same p-well. This configuration can increase the ratios in the WL-ranges of odd numbers because the potential perturbation in the p-well can activate PBEs in these two adjacent cells simultaneously.

Futhermore, the analyses of the BL-N_{fail} and WL-N_{fail} revealed the interesting data pattern dependence of the topology of fail bit patterns for the incidence angle of 90° (WL). Fig. 3.10 shows the ratio of MCU events whose BL(WL)-range is larger than the BL(WL)-N_{fail}: BL(WL)-range $>$ BL(WL)-N_{fail}. These MCU events correspond to the events that have gap structures in the fail bit patterns. For example, the MCU event depicted in Fig. 3.6 is the event with WL-range $>$ WL-N_{fail}, where a gap can be seen in the region corresponding to the WL-range. In Fig. 3.10, these ratios are compared between the All0 and CKB0 patterns. Note that 100% corresponds to all events with the BL(WL)-range of $\geq$ 3 in this graph. As for the ratio of BL-range $>$ BL-N_{fail} [see the left side in Fig. 3.10], the large difference was found between the All0 and CKB0 patterns. The ratio for the All0 pattern was significantly smaller than that for the CKB0 pattern. This is apparently due to the difference in the physical arrangement of high nodes, as discussed in Fig. 3.8. As for the ratio of WL-range $>$ WL-N_{fail} [see the right side in Fig. 3.10], it was found that the ratio for the All0 pattern was higher than that for the CKB0 pattern. This indicates that the probability of occurrence of the gap structures along the WL direction is higher for the All0 pattern than for the CKB0 pattern. This difference cannot be explained simply by the physical arrangement of high nodes. To understand this difference,

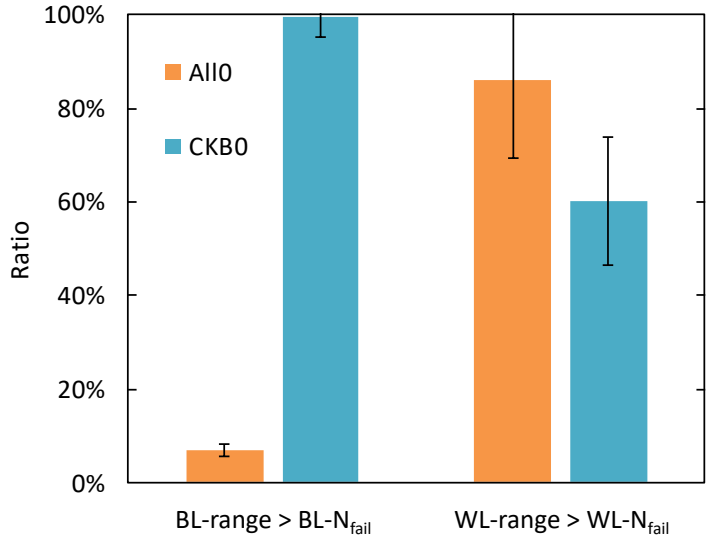

FIGURE 3.10: Ratios of events with BL(WL)-range $>$ BL(WL)-N_{fail} at the incidence angle of 90° (WL). Orange and cyan bars correspond to the All0 and CKB0 patterns, respectively. 100% corresponds to all events with BL(WL)-range $\geq$ 3. All ratios are the values averaged over all voltage conditions. Error bars represent one standard error.

the underlying mechanism is explored in the next section.

3.3.3 Exploration of the MCU Mechanism

A possible mechanism underlying the higher probability of gap structures along the WL direction for the All0 pattern is the MWCPU mechanism that is identified in Chap. 2. As seen in Fig. 2.6 and 2.11, gap structures along the WL direction were observed in the case of the All1 pattern, which is physically equivalent to the All0 pattern. In the following, the gap structure of fail bit patterns induced by the MWCPU mechanism is examined for the All0 pattern in the same manner as in Fig. 2.9 (the CKB0 pattern).

Fig. 3.11 demonstrates that the MWCPU mechanism can induce the gap structure along the WL direction in the case of the All0 pattern. In this figure, the schematic layout of four SRAM cells along a WL is depicted, where each cell is numbered from 1 to 4. Fig. 3.11(a) shows the initial state of internal node voltages for the All0 pattern. The cross-section of the SRAM cells along the dotted line is illustrated in Fig. 3.11(b), where the p-wells are labeled as p-well 1, 2, and 3. Here, it is assumed that the potential in multiple wells are perturbed by charge deposition, and that the potential rise in the p-well 2 is higher than that in the p-wells 1 and 3, as depicted in Fig. 3.11(c). In this case, the imbalance of PBEs in nMOS transistors results in the asymmetric pull-down strength in each cell. This situation is indicated by blue arrows depicted between Fig. 3.11(b) and (c), where the pull-down strength is expressed by the length of the arrow. In this configuration, in each cell, the nodes closer to the center region are finally pulled to the low state, the positions of which are indicated by

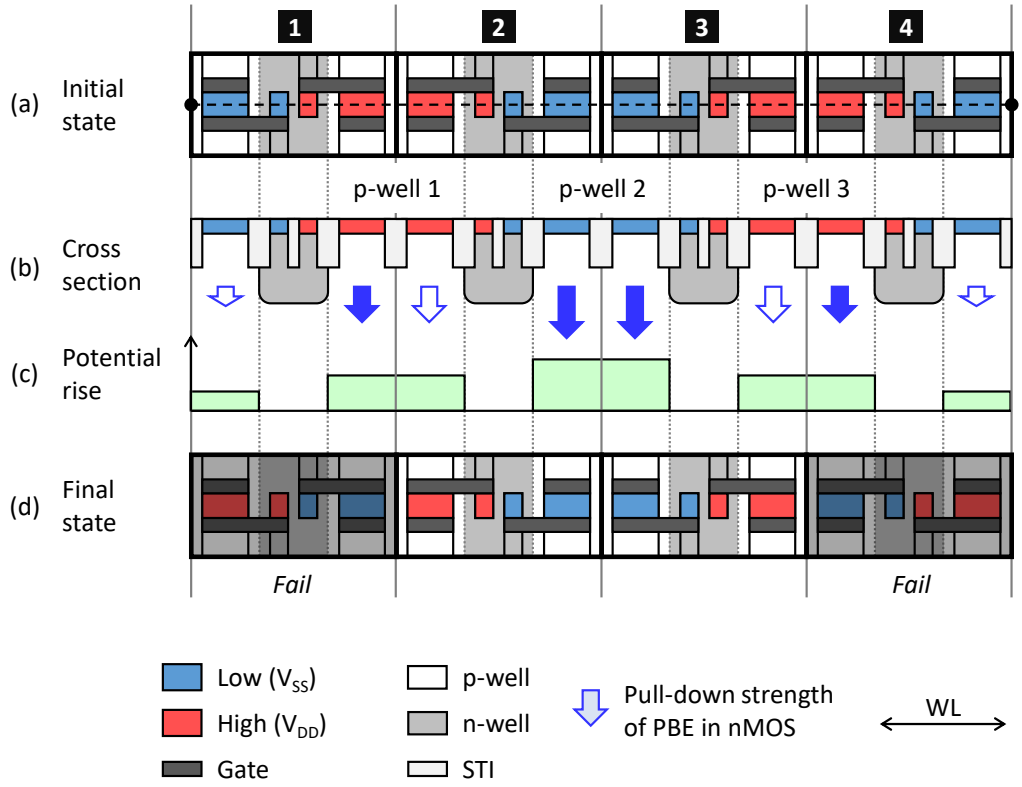

FIGURE 3.11: Conceptual illustration of gap formation in a fail bit pattern through the MWCPU mechanism in the case of the All0 pattern. (a) Schematic layout of four SRAM cells along a WL, which are numbered from 1 to 4. Blue and red regions correspond to low (V_{SS}) and high (V_{DD}) regions, respectively. Internal node voltages are the initial state for the All0 pattern. (b) Cross-sectional illustration along the dotted line in (a). (c) Potential rises in the p-wells assumed here. Blue arrows between (b) and (c) depict pull-down strength, where the longer length means the strong pull-down strength. The filled blue arrows indicate the stronger side in each SRAM cell. (d) Four SRAM cells same as (a), but with node voltages changed through the MWCPU mechanism. Note that the similar figure in the case of the CKB0 pattern is presented in Fig. 2.9.

filled blue arrows. The node voltages finally result in the state shown in Fig. 3.11(d). Thus, the cells 1 and 4 become fail bits. The cells 2 and 3, on the other hand, are pass bits because their node voltages are identical to the initial ones. As a result, the gap structure along the WL direction occurs in this fail bit pattern due to the MWCPU mechanism.

The important point here is that the possible fail bit patterns induced by the MWCPU mechanism are different between the All0 and CKB0 patterns, as illustrated in Fig. 3.12. Similarly to Fig. 3.11, four SRAM cells along a WL are depicted with internal node voltage in this figure, where the SRAM cells are simplified. Fig. 3.12(a) and (b) are the cases of the All0 pattern. Fig. 3.12(c) is the case of the CKB0 pattern. In each figure, the upper and lower cells represent the initial and final states of node voltages, respectively. The blue arrows indicate the position of the p-well where the potential rise is assumed to be higher than the other p-wells. Here, Fig.

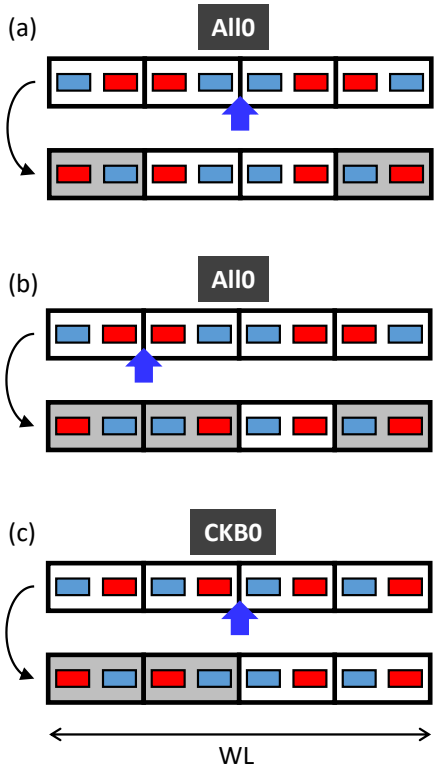

FIGURE 3.12: Fail bit patterns induced by the MWCPU mechanism. (a) and (b) are the cases for the All0 pattern. (c) is the case for the CKB0 pattern. Rectangular cells correspond to SRAM cells. Blue and red rectangular boxes denote internal nodes of low and high voltages, respectively. The upper and lower cells depict the initial and final states of node voltages, where gray cells represent fail bits. Blue arrows indicate the position of the largest potential rise among the p-wells. (a) corresponds to the case explained in Fig. 3.11.

3.12(a) corresponds to the case demonstrated in Fig. 3.11. Fig. 3.12(b) is another case for the All0 pattern, where the p-well containing high nodes is the position of the highest potential rise. This corresponds to the situation where, in Fig. 3.11, the potential rise is the highest in the p-well 1. In this case, the cells 1, 2, and 4 become fail bits, as depicted in the lower part of Fig. 3.12(b). Fig. 3.12(c) is the same case as Fig. 2.9, where the left two cells become fail bits. The key observation here is that the MWCPU mechanism does not induce gap structures in fail bit patterns in the case of the CKB0 pattern. Therefore, the MWCPU mechanism can lead to the increased probability of occurrence of gap structures along the WL direction only in the case of the All0 pattern. This feature is consistent with the results shown in Fig. 3.10.

It should be noted that the data pattern dependence of gap structures does not originate from the variability of SRAM cells. As explained in Sec. 1.3.1, the SRAM circuit consists of two inverters, which are designed to be geometrically and electrically identical. In practice, process variation can distort this balanced configuration, resulting in the variability of SRAM cell characteristics [85]. It has been reported that this cell-to-cell variation in electric characteristics is related to the cell-to-cell

variation in SEU susceptibility [86]. Similarly, this could lead to the cell-to-cell difference in the preferred state ("0" or "1") reached after well potential is significantly perturbed. Therefore, such cell-to-cell variation can cause gaps in fail bit patterns. On the other hand, the key feature is that, in general, this cell-to-cell variation is randomly distributed in space. The probability of gap occurrence due to this variation is therefore expected to be independent of the physical arrangement of node voltages, i.e., data patterns. However, as seen in Fig. 3.10, the results clearly demonstrated that the ratio of gap occurrence depends on the data patterns. Hence, the contribution of the cell-to-cell variation can be considered as small in the results.

The ion strike events that can trigger the MWCPU mechanism are examined in Fig. 3.13. As described in Fig. 3.11, the key factor of the MWCPU mechanism is the imbalance of well potential perturbation across multiple p-wells. In each event shown in Fig. 3.13, the possible potential rise in p-wells is depicted. Fig. 3.13(a) shows the event where an ion passes through four SRAM cells at an angle with respect to the WL direction. The potential rise along the dotted line is depicted in the lower part. In this case, the potential rise in the center p-well is estimated to be larger than the other p-wells. This is because the amount of charge deposited in the center p-well is the most abundant. This potential distribution is the same configuration as in Fig. 3.11, and hence the fail bit pattern can be influenced by the MWCPU mechanism. Fig. 3.13(b) shows the event where an ion passes through multiple wells at an angle with respect to the silicon surface. This event can also lead to the imbalance of potential rise along the dotted line, which corresponds to the device active region. Fig. 3.13(c) shows the event related to the intrinsic property of charge deposition inside the silicon. In this event, an ion passes through multiple wells in parallel to the WL direction, and stops in the middle of a p-well. Since the charge deposition increases at the Bragg peak, as explained in Sec. 1.2, it is possible that the p-well coincident with the position of the Bragg peak undergoes a large potential rise.

3.3.4 Indication of the MWCPU Contribution in FBMs

To elucidate the contribution of the MWCPU mechanism, the FBMs of neutron-induced MCU events were analyzed with internal node voltages. Fig. 3.14 presents typical FBMs exhibiting gap structures along the WL direction. These FBMs are illustrated in the same manner as in Fig. 3.12, where the internal node voltages are the initial states. The orange line in each FBM represents an ion track, which is speculative, based on the entire fail bit arrangement in each FBM. Note that these FBMs are obtained at the incidence angles of 45° (WL) and 90° (WL) in the case of the All0 pattern.

In these FBMs, it was observed that fail bits include several cells at a distance from the ion track, and that the fail bits are arranged in block-like structures. For example, the FBM shown in Fig. 3.14(g), the fail bit pattern can be viewed as consisting of three blocks. The important observation was that the center of these block-like

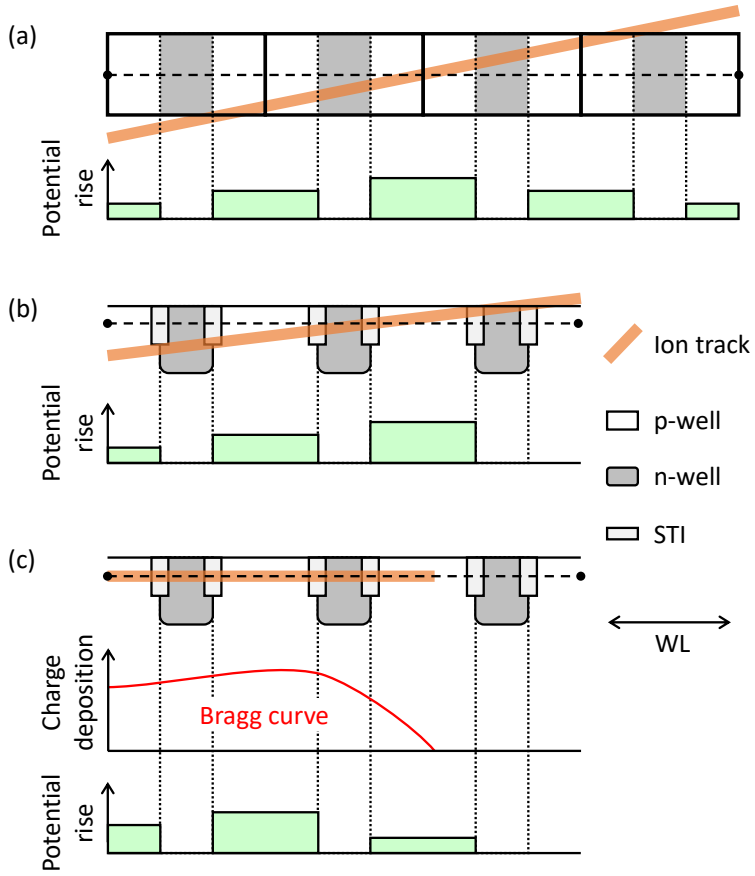

FIGURE 3.13: Ion strike events triggering potential perturbation in multiple p-wells. (a) An ion strikes at an angle with respect to a WL. (b) An ion strikes at an angle with respect to the silicon surface. (c) An ion strikes horizontally and stops in the middle of a p-well. Expected potential rise along dotted lines is depicted in each lower part.

structures was the p-well containing high nodes. This result directly indicates that the potential perturbation in the p-well activates PBEs simultaneously in multiple nMOS transistors belonging to the p-well, which leads to the block-like structure of fail bits. Moreover, since the spatial distribution of fail bits covered several cells along the WL direction, as confirmed in Fig. 3.14, it can be considered that potential rise was induced in multiple p-wells.

The key finding in these FBMs was that some SRAM cells did not fail even when the ion track appeared to overlap these cells or when PBEs were expected, which resulted in gap structures. For the FBMs of Fig. 3.14(c) and (d), the potential rise in the p-wells is speculated from the configuration of the ion tracks. The lower part of these figures depict the speculated potential rise at the position of the dotted line. In the case of Fig. 3.14(c), an ion was speculated to pass through SRAM cells at an angle with respect to the WL direction. This is the same situation as Fig. 3.13(a), and hence the MWCPU mechanism demonstrated in Fig. 3.11 is expected. The fail bit pattern along the dotted line is identical to the one expected from Fig. 3.11. This indicates that the observed gap structure along the WL direction originates from the

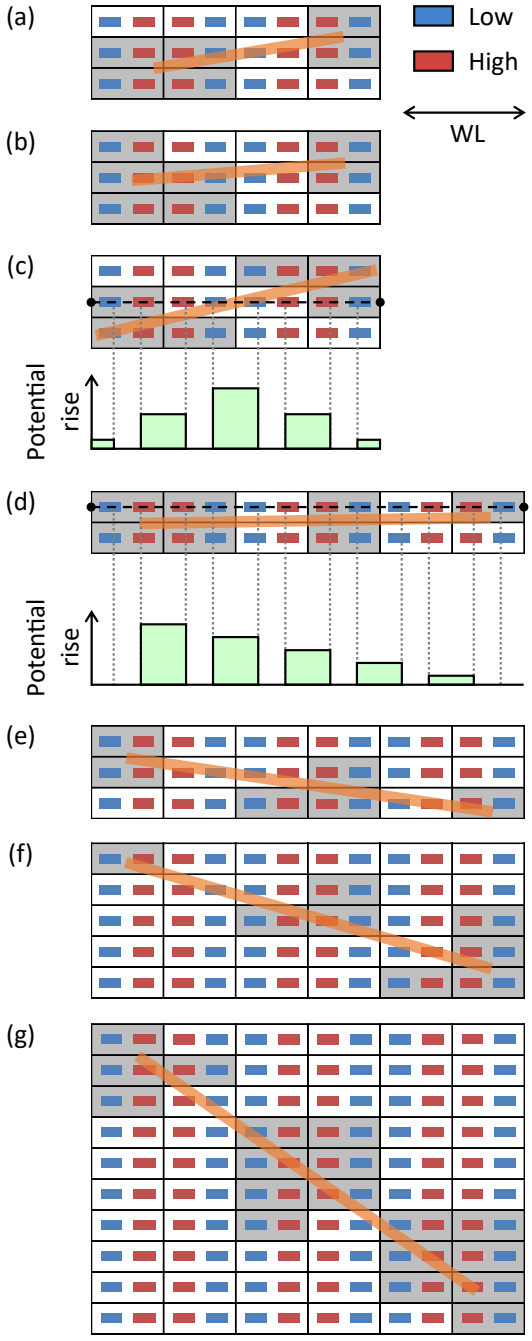

FIGURE 3.14: Experimental FBMs of neutron-induced MCU events at the incidence angles of 45° (WL) and 90° (WL) in the case of the All0 pattern. Rectangular cells represent SRAM cells. Gray cells correspond to fail bits. Initial node voltages are depicted by small rectangular boxes, where blue and red boxes denote low and high voltages, respectively. Orange lines are speculated ion tracks. Speculated potential rise in p-wells is depicted for (c) and (d).

MWCPU mechanism. As for the case of Fig. 3.14(d), the ion track was speculated to be almost parallel to the WL direction. In this case, Fig. 3.13(b) and (c) are the possible situations, and hence the potential rise in the p-wells can be imbalanced. The observed fail bit pattern is the same as that shown in Fig. 3.12(b). The gap structures

observed in the other FBMs can also be understood by the MWCPU mechanism.

From the above considerations, it is probable that the MWCPU mechanism can be triggered by high-energy neutrons especially at grazing incidence, and that the MWCPU mechanism plays an important role in the MCU characteristics in terms of the topology of fail bit patterns. In particular, the data pattern dependence in the occurrence of gap structures arises from the MWCPU mechanism, as demonstrated in Fig. 3.10

3.4 Conclusion

In this chapter, the high-energy neutron irradiation experiments at several incidence angles have demonstrated the strong angular sensitivities of SEU, MCU, and MBU responses in the 20-nm bulk planar SRAMs. Furthermore, the characterization of MCU events and the analyses of FBMs have revealed that the MWCPU mechanism identified in Chap. 2 affects the characteristics of the high-energy neutron-induced MCUs especially at grazing incidence.

The neutron irradiation experiments have been performed by using the spallation neutron source with varying the incidence angle. The angular dependence of the SEU, MCU, and MBU rates have been statistically evaluated. It has been demonstrated that, although the SEU rate decreases with increasing angle of incidence, the MBU rate increases at grazing incidence. According to this result, it has been suggested that the efficiency of ECCs can be limited depending on the mounting orientation of SRAM devices, where the worst-case scenario is where the WLs of SRAM cells are normal to the ground. The MCU events have been thoroughly characterized in terms of the size and the spatial topology of fail bits. The results have clearly confirmed that the angular dependence of MCU characteristics stems from the interplay of the forward-emission of secondary ions, the geometry of SRAM cells, and the PBEs in p-wells. At the same time, it has been found that the probability that fail bit patterns contain gap structure along the WL direction is higher for the All0 pattern than for the CKB0 pattern. From the consideration of potential perturbation in multiple p-wells, this difference has been explained by the MWCPU mechanism, which can induce the gap structure along the WL direction only in the case of the All0 pattern. Finally, the contribution of the MWCPU mechanism has been indicated through the analyses of FBMs with internal node voltages.

In conclusion, this study has demonstrated that, for high-energy neutrons, the incidence angle has a significant impact on SEU susceptibility and MCU characteristics in scaled planar SRAMs. In the terrestrial environment, the incidence angle basically corresponds to the orientation of SRAM devices because the terrestrial high-energy neutrons are largely directed downward. It is therefore essential to consider the device orientation in advanced technologies not only for the practical estimation of event rates, but also for the better selection of mitigation techniques. As mentioned in Sec. 1.3.5, advanced SRAM devices have employed FinFETs, the geometry of

which is significantly different from that of planar FETs, shown in Fig. 1.1. This difference potentially leads to the different angular sensitivity between the FinFET SRAMs and the planar SRAMs. The next chapter addresses this point.

Chapter 4

Angular Sensitivity of Neutron-Induced SEUs in FinFET SRAMs

This chapter studies the angular sensitivity of high-energy neutron-induced SEUs in 12-nm bulk FinFET SRAMs with comparison to that in the 20-nm bulk planar SRAMs, which has been demonstrated in Chap. 3. [1] Irradiation experiments are performed using a terrestrial environment-compatible source with varying incidence angle in the same way as in Chap. 3. The analyses of the SEU and MBU rates demonstrate that, although the SEU rate decreases at grazing incidence, the MBU rate increases when the incidence direction is parallel to the WL direction, as similarly observed in the 20-nm planar SRAMs. It is found that the angular response of MCUs is different between the 12-nm FinFET and 20-nm planar SRAMs. The comparative analysis of the voltage dependence of the MCU ratio reveals that this difference is due to the different contribution of PBEs, which is more significant in the 20-nm planar SRAMs. It is also indicated that, in the 12-nm FinFET SRAMs, the contribution of PBEs is relatively large when the incidence angle is parallel to the WL direction. The validity of this picture is confirmed through the characterization of the MCU events, where pattern-wise MCU ratios are analyzed.

4.1 Introduction

In advanced CMOS technologies, FinFETs have been employed to further increase the performance of semiconductor devices. As mentioned in Sec. 1.3.5, the FinFET technologies have shown a drastic improvement in SEU tolerance compared to conventional bulk planar technologies [42], [45], [88]–[93]. This improvement is mainly due to the fin structures of the FinFETs [see Fig. 1.1]. The reduced silicon volume of the FinFET results in decreased charge deposition and hence the decreased SEU susceptibility [91], [94], [95]. Another remarkable aspect of the fin structure is strong anisotropy in the fin shape.

[1] This chapter is based on [87].

It has been reported that the structural anisotropy of the fin leads to unique angular sensitivity of heavy ion-induced SEUs in bulk FinFET devices [96], [97]. Zhang *et al.* [96] investigated the angular response of SEU cross-sections for heavy ions using 16-nm bulk FinFET flip-flops. They showed that the angular sensitivity was different for particles with different LETs, where for low-LET particles the SEU CS decreased at grazing incidence along the direction perpendicular to the fin. Nsengiyumva *et al.* [97] also investigated the angular response for heavy ions using 14-/16-nm bulk FinFET latches. They clearly demonstrated that the SEU CS depends on the incidence angle only for low-LET particles, where the SEU CS increased (decreased) at grazing incidence when the incidence direction is parallel (perpendicular) to the fin.

For high-energy neutron-induced SEUs, such angular sensitivity has not been investigated in bulk FinFET SRAMs, although the high-energy neutrons are the major source for SEU events in the terrestrial environment. As for bulk planar SRAMs, there have been several reports investigating the impact of the neutron incidence direction on SEUs [57]–[59]. As demonstrated for the 20-nm bulk planar SRAMs in Chap. 3, the forward emission of secondary ions is the key mechanism for the angular sensitivity. Similarly, this mechanism could affect the angular sensitivity in the FinFET SRAMs. In addition, as mentioned above, the angular sensitivity in the FinFET devices was demonstrated to be significant for low-LET particles [96], [97]. This indicates the possibility of the notable angular sensitivity in the FinFET SRAMs because most of the secondary ions produced by high-energy neutrons are low-LET particles. Therefore, it is worthwhile to investigate the angular sensitivity of neutron-induced SEUs in the FinFET SRAMs.

On the analogy of the angular sensitivity observed in bulk planar SRAMs, it is expected that the incidence direction of high-energy neutrons has a significant impact on MCUs in bulk FinFET SRAMs. As mentioned in Sec. 1.3.3, the MCUs are a serious concern for SRAM reliability, where MBUs can degrade the efficiency of ECCs. For the bulk planar SRAMs, it has been demonstrated that the characteristics of neutron-induced MCUs are strongly dependent on the incidence angle of neutrons, where the occurrence probability of MCUs increases at grazing incidence [57]–[59]. Moreover, in Chap. 3, it has been found that the MBU rate increases when the incidence direction is parallel to the WL direction in the 20-nm bulk planar SRAMs. For the bulk FinFET SRAMs, several studies have reported the MCU characteristics [93], [98], [99]. However, the impact of the incidence direction on neutron-induced MCUs has not been explored. Since the structural anisotropy increases from the planar FETs to the FinFETs, the FinFET SRAMs could possess different types of angular sensitivity in the MCUs.

At the same time, the structural difference between the planar FETs and the FinFETs can result in the different mechanism underlying high-energy neutron-induced MCUs between the planar and FinFET SRAMs. As described in Sec. 1.3.6, in scaled

SRAMs, the contribution of PBEs have become an important factor in MCU occurrence. In the planar SRAMs, it has been demonstrated that the PBEs significantly affect the MCU characteristics [54], [56], [63], [64]. As presented in Chap. 3, the significant impact of the PBEs has also been confirmed in the 20-nm bulk planar SRAMs. In the FinFET SRAMs, on the other hand, there have been no studies analyzing the MCU characteristics from the point of view of the PBE contribution. Hence, it should be meaningful to investigate the angular sensitivity of MCU characteristics in terms of both structural effects and PBEs.

This study experimentally investigates high-energy neutron-induced SEUs in 12-nm bulk FinFET SRAMs for several angles of incidence. The angular dependence of the SEU, MCU, and MBU events are evaluated by irradiation tests using an atmospheric-like neutron beam. The occurrence rates of these events are statistically analyzed in terms of their dependence on the supply voltage and the incidence angle. To find out the difference in the angular sensitivity between planar and FinFET SRAMs, the obtained results are compared with the results for the 20-nm bulk planar SRAMs presented in Chap. 3. On the basis of the difference observed in the voltage dependence of the MCU ratio between the 12-nm FinFET and 20-nm planar SRAMs, the underlying mechanism is discussed, focusing on the contribution of PBEs. Furthermore, the MCU characteristics are thoroughly analyzed with respect to the size and fail bit pattern of the MCU events. The contribution of PBEs is also examined in terms of the voltage dependence of pattern-wise MCU ratios.

4.2 Experimental Setup

4.2.1 Tested Device and Operation

The test vehicles were SRAM chips fabricated in a 12-nm bulk FinFET CMOS process. The package was a standard plastic package similar to the 20-nm bulk planar SRAM chips used in Chap. 3.

The SRAM operation was basically the same as the one described in Sec. 3.2.1, except for the supply voltage condition. The operation was the static mode that consists of write, hold, and read cycles in this order. The supply voltage in the hold cycle was varied from 0.5 V to 0.9 V. The All0 and CKB0 patterns were used to investigate the data pattern dependence of MCU characteristics. As explained in Fig. 3.1, the physical arrangement of internal node voltages is different between the two data patterns. In the case of the All0 pattern, two high nodes or two low nodes of two horizontally adjacent SRAM cells share the same p-well, as seen in Fig. 3.1(a). In the case of the CKB0 pattern, a high node and a low node share the same p-well in every two horizontally adjacent cells, as seen in Fig. 3.1(b).

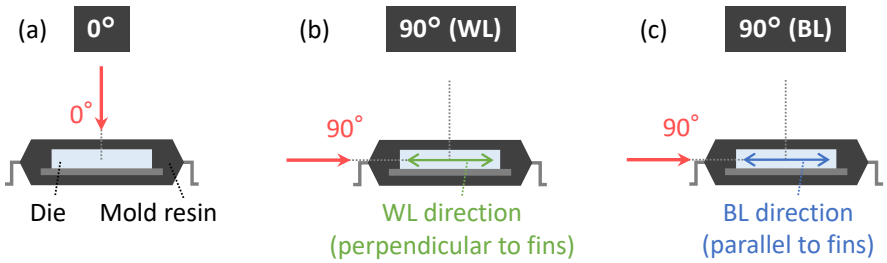

FIGURE 4.1: Neutron incidence angles of three irradiation conditions: (a) 0°, (b) 90° (WL), and (c) 90° (BL). Red arrows represent the direction of neutron beam. (a) 0° is the normal incidence from the top. (b) 90° (WL) and (c) 90° (BL) are for incidences parallel to WLs and BLs, respectively. Note that (c) 90° (BL) is the case where the direction of neutron beam is parallel to the fins of FinFETs.

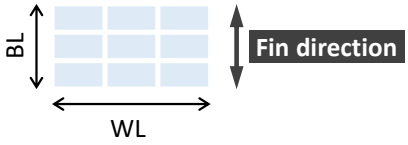

FIGURE 4.2: Fin direction in SRAM cells. Rectangular cells represent the SRAM cells. Vertical and horizontal directions are parallel to BL and WL directions, respectively. The fin direction is parallel to the BL direction.

4.2.2 High-Energy Neutron Irradiation

High-energy neutron irradiation testing was performed at the RCNP, Osaka University in the same way as in Chap. 3. The spallation neutron beam was used in all the tests. As explained in Fig. 3.2, the energy spectrum is similar to the terrestrial one in the energy range from 1 to 300 MeV [84]. The integral flux above 10 MeV was $\sim 2.5 \times 10^9$ cm^2/h.

The SRAM chips were irradiated by the neutron beam at three angles of incidence: 0°, 90° (WL), and 90° (BL). These geometrical configurations are schematically illustrated in Fig. 4.1(a)–(c). The angle of 0° is the direction normal to the silicon die [see Fig. 4.1(a)]. The angles of 90° (WL) and 90° (BL) are the directions parallel to the WLs and BLs of the SRAM cells, respectively [see Fig. 4.1(b) and (c)]. Note that these irradiation configurations are the same as those shown in Fig. 3.3(a), (c), and (d).

It is worthwhile to note here that the fins of the FinFET SRAMs are arranged along the BL direction, as explained in Fig. 4.2. In this case, the incidence angles of 90° (BL) and 90° (WL) correspond to the cases where the neutron beam is parallel and perpendicular to the fins, respectively, as denoted in Fig. 4.1(b) and (c).

4.2.3 Rate Calculation

The SBU, MCU, and MBU events were separately extracted in the same way as in Chap. 3. The event extraction was based on the spatial distribution of fail bits, where

the SEU events are the sum of the SBU and MCU events. It should be noted that, the number of fail bits accumulated during one hold cycle was kept small enough to avoid the misinterpretation of multiple SBU events as an MCU event.

The calculation of the SEU, MCU, and MBU rates was performed according to the JEDEC standard, as described in Sec. 3.2.3. [18]. The event rates were calculated as $\sigma_{\mathrm{event}} \times \phi_{\mathrm{n}}$ for the SEU, MCU, and MBU events. Here, the event CS σ_{event} was estimated as $N_{\mathrm{event}}/(\Phi_{\mathrm{n}} \times N_{\mathrm{bit}})$ through the irradiation tests.

4.3 Results and Discussion

4.3.1 Angular Dependence of SEU, MCU, and MBU Rates

The angular dependence of SEU, MCU, and MBU rates was clearly confirmed in the 12-nm FinFET SRAMs through the high-energy irradiation testing. In Fig. 4.3, the SEU, MCU, and MBU rates at the incidence angles of 0°, 90° (WL), and 90° (BL) are presented in the same manner as in Fig. 3.4. In each graph, the rates for the 12-nm FinFET and 20-nm planar SRAMs are shown by the closed and open symbols, respectively.

For the comparison between the 12-nm FinFET and 20-nm planar SRAMs, the SEU rate for the 12-nm FinFET SRAMs was lower than that for the 20-nm planar SRAMs by approximately one order of magnitude, as observed in Fig. 4.3(a). This difference is consistent with the previous report and probably due to the structure transition from planar FETs to FinFETs [42]. The angular dependence of the SEU rate appeared similar between the two SRAMs, as seen in Fig. 4.3(a). For both the SRAMs, the SEU rate decreased at grazing incidence. On the other hand, the angular dependence of the MCU rate exhibited a noticeable difference between the two SRAMs, as confirmed in Fig. 4.3(b). These points are discussed later.

For the MBU rate shown in Fig. 4.3(c), the incidence angle of 90° (WL) had the highest rate in the 12-nm FinFET SRAMs, as is the case in the 20-nm planar SRAMs. This observation can be explained by the stochastic tendency of the forward emission of secondary ions because MBU events are the events where multiple fail bits occur along a WL, as discussed in Chap. 3. This is an important result indicating that, in the terrestrial environment, the orientation of SRAM devices can be a significant factor for determining the efficiency of ECCs in the 12-nm FinFET SRAMs, as well as in the 20-nm planar SRAMs. This is because, as described in Sec. 1.2.1, the angular distribution of terrestrial neutrons is anisotropic, where the large number of neutrons strike perpendicular to the ground [10]. From the above results, it can be deduced that the vertically mounted SRAM devices with the WLs perpendicular to the ground are the worst condition in terms of the efficiency of ECCs in both the 12-nm FinFET and 20-nm planar technologies.

To highlight the angular dependence of the SEU, MCU, and MBU rates, the ratios of these rates at the angles of 90° (WL) and 90° (BL) to those at the normal incidence

(0°) are plotted as a function of the supply voltage in Fig. 4.4. As shown in Fig. 4.4(a), all the ratios for the SEUs were less than one. This is obvious from the difference in the visible CS of the test chip to the neutron beam. As described in Chap. 3, the number of neutrons passing through the SRAM cells in a unit of time decreases at grazing incidence, and hence the SEU rate decreases.

For the ratio of the SEU rate shown in Fig. 4.4(a), it was interesting that, at 0.5 V, the ratio at the angle of 90° (BL) was considerably higher than that at the angle of 90° (WL) in the 12-nm FinFET SRAMs. A key observation here was that this difference was significant only at the low voltage, 0.5 V. Since, as described in Sec. 1.3.2, the lower supply voltage corresponds to the lower critical charge, it can be considered that the contribution of secondary ions with low-LET is relatively larger at the lower voltage. In this case, the above difference is qualitatively consistent with Nsengiyumva's results of heavy-ion irradiation experiments, where, for low-LET ions, the SEU CS increased at grazing incidence when the incidence direction was parallel to the fins. [97]. This behavior was explained from the relative geometry between the fin shape and the ion track. The essence of this geometrical effect is that the ion incidence parallel to the fin results in the long track inside the fin, which increases charge deposition on the FinFET.

Similarly to the discussion in [97], the higher ratio of the SEU rate at the angle of 90° (BL) in the 12-nm FinFET SRAMs can be understood by the fin shape and the tracks of secondary ions. Since the secondary ions produced by high-energy neutrons tend to be emitted forward, their tracks are more likely to be longer along the neutron incidence direction. Here, as described above, long tracks parallel to the fins lead to large charge deposition, and hence the SEU rate can increase compared to the case of long tracks perpendicular to the fins. As explained in Fig. 4.1, the angle of 90° (BL) corresponds to the incidence direction parallel to the fins. Therefore, the observed difference between the angles of 90° (WL) and 90° (BL) is consistent with the above geometrical consideration based on the anisotropy of the FinFET structure.

For the ratio of the MCU rate presented in Fig. 4.4(b), there were two interesting differences between the 12-nm FinFET and 20-nm planar SRAMs. One difference was observed in the magnitude of the ratio. The ratio for the 20-nm planar SRAMs was slightly less than 1, whereas that for the 12-nm FinFET SRAMs reached 1.6 at 0.9 V. Another difference was found in the voltage dependence of the ratio. In the 20-nm planar SRAMs, the voltage dependence was small and similar between the angles of 90° (WL) and 90° (BL). On the other hand, in the 12-nm FinFET SRAMs, the voltage dependence was different between these angles, where the ratio at the angle of 90° (WL) clearly increased with increasing the voltage. These results indicate that the angular sensitivity of MCUs is more significant for the 12-nm FinFET SRAMs than for the 20-nm planar SRAMs. The reasons for these differences are examined in the next section.

For the ratio of the MBU rate shown in Fig. 4.4(c), an interesting difference was also found between the 12-nm FinFET and 20-nm planar SRAMs. At the angle of 90°

(BL), the ratio was approximately 1 and almost the same between the two SRAMs. On the other hand, at the angle of 90° (WL), the ratio was meaningfully higher for the 12-nm FinFET SRAMs than the 20-nm planar SRAMs at 0.9 V. This implies the possibility that the efficiency of ECCs in the 12-nm FinFET SRAMs is more dependent on the angle of neutron incidence and hence on the mounting orientation on the ground.

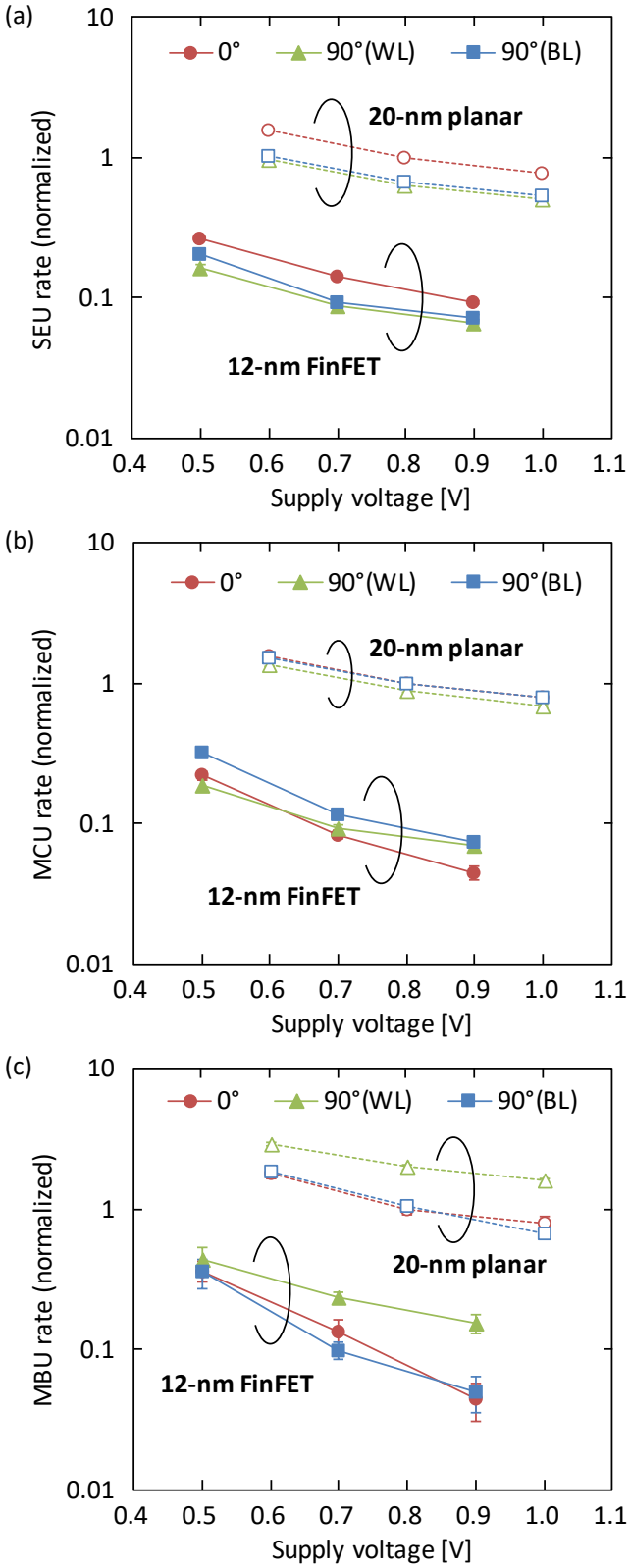

FIGURE 4.3: (a) SEU, (b) MCU, (c) MBU rates as a function of supply voltage at the neutron incidence of 0°, 90° (WL), and 90° (BL). Closed and open symbols are for 12-nm FinFET and 20-nm planar SRAMs, respectively. Each rate is normalized by the value at 0.8 V of 20-nm planar SRAMs at the angle of 0°. All rates are the values averaged over the All0 and CKB0 patterns. Error bars represent one standard error.

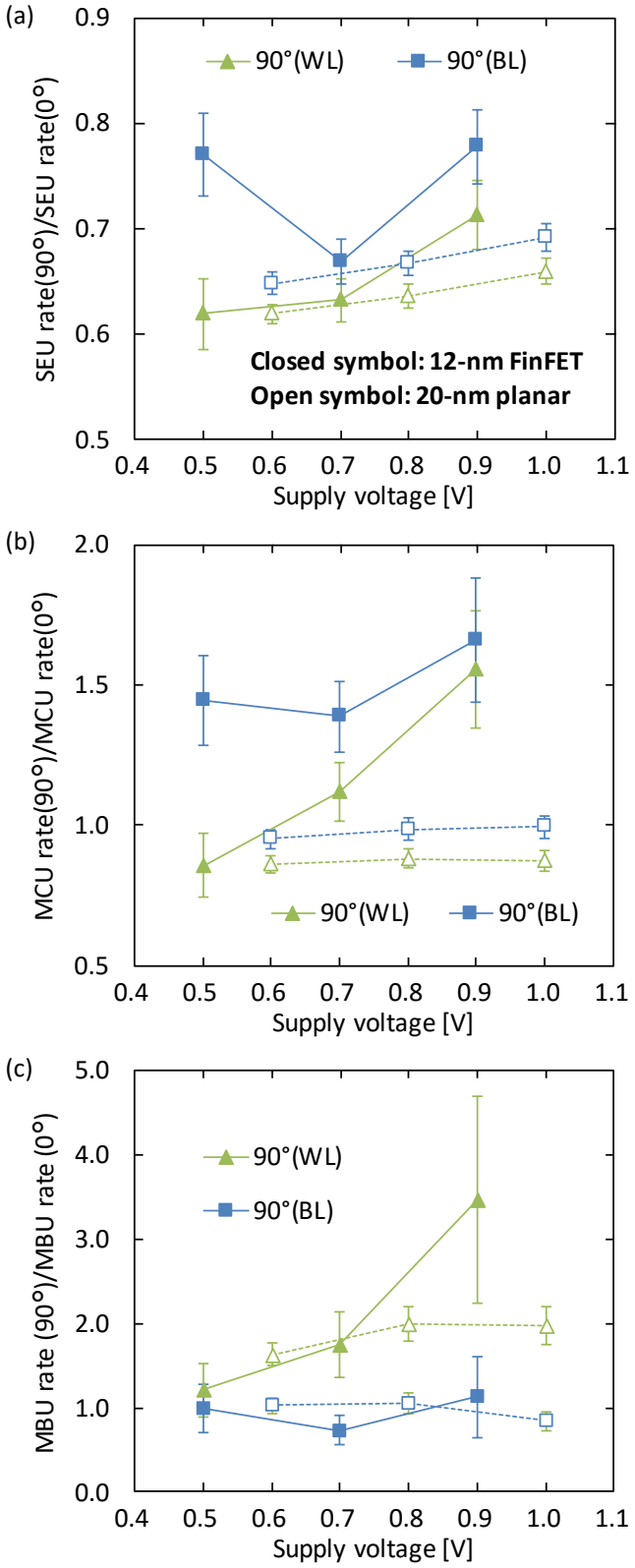

FIGURE 4.4: Ratios of (a) SEU, (b) MCU, (c) MBU rates at the incidence angles of 90° (WL) and 90° (BL) with respect to the normal incidence case (0°) as a function of supply voltage. Closed and open symbols are for 12-nm FinFET and 20-nm planar SRAMs, respectively. All rates and ratios are values averaged over the All0 and CKB0 patterns. Error bars represent one standard error. Note that the vertical scales differs.

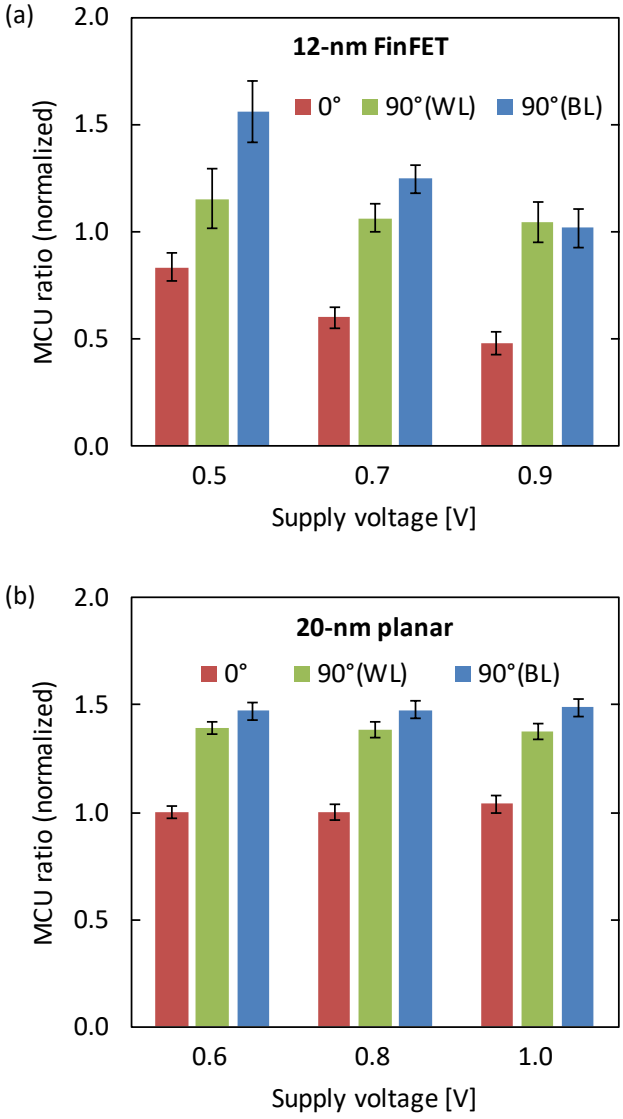

FIGURE 4.5: MCU ratios for (a) 12-nm FinFET and (b) 20-nm planar SRAMs at the neutron incidence angles of 0°, 90° (WL), and 90° (BL). The values are normalized by the value at 0.8 V of 20-nm planar SRAMs in the angle of 0°. All ratios are the values averaged over the All0 and CKB0 patterns. Error bars represent one standard error.

4.3.2 Analyses of MCU Ratios and Mechanism Investigation

To understand the large difference observed in the angular dependence of the MCU rate between the 12-nm FinFET and 20-nm planar SRAMs, MCU ratios were analyzed in Fig. 4.5. Here, the MCU ratios were calculated by dividing the MCU rate with the SEU rate. The results for the 12-nm FinFET and 20-nm planar SRAMs are shown in Fig. 4.5(a) and (b), respectively.

For both the two SRAMs, it was observed that the MCU ratios were higher at the angles of 90° (WL) and 90° (BL) than at the angle of 0°, where the angle of 90° (BL) exhibited the highest ratio. As discussed in Chap. 3, this difference among the incidence angles means that the angular sensitivity of neutron-induced MCUs

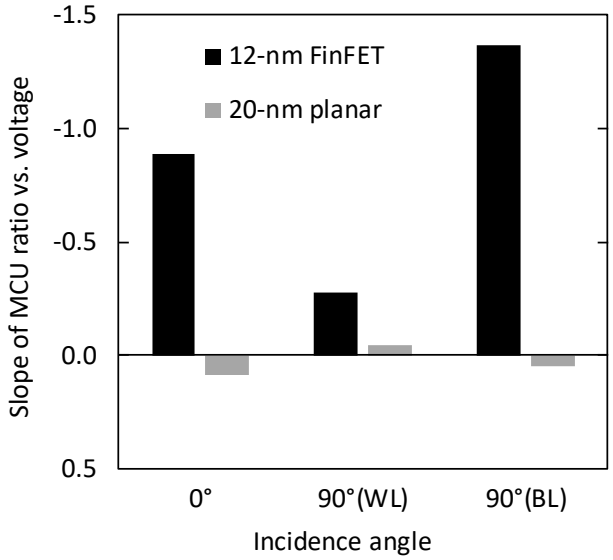

FIGURE 4.6: Slope of the linear fitting of MCU ratio versus supply voltage (Fig. 4.5). Black and gray bars correspond to 12-nm FinFET and 20-nm planar SRAMs, respectively. Note that the vertical axis is inverted: the upper side is negative and means a decreasing trend with voltage.

is primarily determined by the geometrical relationship between the forward emission of secondary ions and the rectangular shape of SRAM cells. Therefore, this result indicates that this geometrical relationship is the primary factor for the angular sensitivity in the 12-nm FinFET SRAMs, as well as in the 20-nm planar SRAMs.

It was found that the MCU ratio was higher for the 20-nm planar SRAMs than for the 12-nm FinFET SRAMs in almost all angle and voltage conditions, and that the voltage dependence of the MCU ratio was different between the 12-nm FinFET and 20-nm planar SRAMs. In the 20-nm planar SRAMs, the MCU ratio was almost independent of the voltage, as seen in Fig. 4.5(b). In the 12-nm FinFET SRAMs, on the other hand, the MCU ratio tended to decrease with increasing the voltage, as confirmed in Fig. 4.5(a). This different voltage dependence is emphasized in Fig. 4.6, where the slopes of the voltage dependence are compared. Here, the slopes were extracted by linear fitting of the MCU ratio versus the voltage. Fig. 4.6 clearly showed that the slopes are nearly 0 regardless of the incidence angle in the 20-nm planar SRAMs, and that the slopes are negative values in the 12-nm FinFET SRAMs. Another noteworthy feature in Fig. 4.6 is the difference in the slopes among the incidence angles in the 12-nm FinFET SRAMs. It is clearly observed that the voltage dependence of the MCU ratio is smaller at the angle of 90° (WL) than at the angle of 90° (BL).

The observed differences in the MCU ratio between the 12-nm FinFET and 20-nm planar SRAMs can be attributed to the different contribution of PBEs because the PBEs affect both the magnitude and voltage dependence of the MCU ratio ratios [65], [100]. As described in Sec. 1.3.6, the PBEs and tend to cause MCU events. Hence, the

large contribution of the PBEs can lead to the increased MCU ratio. Moreover, the PBEs become more active with increasing the supply voltage. For these reasons, in terms of the slope of the MCU ratio versus the supply voltage, the slope is expected to increase positively as the contribution of PBEs becomes significant.

From the results in Fig. 4.5 and 4.6, the contribution of PBEs can be considered to be lower for the 12-nm FinFET SRAMs than for the 20-nm planar SRAMs. As seen in these figures, the MCU ratio was lower in the 12-nm FinFET SRAMs and the slope of the voltage dependence was a more negative value in the 12-nm FinFET SRAMs. On the basis of the features of the PBEs described above, these observations can be interpreted to be the weak PBE in the 12-nm FinFET SRAMs, which is reasonable from the structural viewpoint. In FinFET structures, the potential inside the fin is well-controlled by the surrounding gate. This can lead to the suppression of the PBEs because the PBEs are induced by the perturbation of the potential.

As for the difference observed between the incidence angles of 90° (WL) and 90° (BL) in the 12-nm FinFET SRAMs, it can be deduced that the PBEs are less significant at the angle of 90° (BL) compared to the angle of 90° (WL) because the slope is a higher negative value for the angle of 90° (BL), as seen in Fig. 4.6. Here, the incidence angles of 90° (WL) and 90° (BL) tend to cause the emission of secondary ions along the WL and BL directions, respectively. At the same time, in the case of the normal incidence (0°), the fractions of secondary ions emitted in the WL and BL directions can be assumed to be equal. In this view, the average slope of the angles of 90° (WL) and 90° (BL) is expected for the normal incidence case when the emission direction is a key factor for the PBEs. As observed in Fig. 4.6, the slope at the angle of 0°, -0.89, is approximately an average value between the angles of 90° (WL) and 90° (BL), which is calculated to be -0.82. Therefore, the different contribution of the PBEs among the incidence angles can be due to the difference in the emission direction of secondary ions.

A noteworthy point here is that the difference in the slope between the angles of 0° and 90° (WL) leads to the large difference in the MCU ratio at higher voltages, as seen in Fig. 4.5(a). The strong voltage dependence in the angular sensitivity of MCUs at the angle of 90° (WL), which was shown in Fig. 4.4(b), reflects this slope difference. In other words, the difference in the angular sensitivity of MCUs observed in Fig. 4.4(b) possibly due to the different contribution of PBEs.

It could be helpful to note that the observed differences in the voltage dependence of the MCU ratio cannot be explained by critical charge. Since the critical charge increases with increasing the voltage for both the two SRAMs, the effect of the critical charge can lead to the suppression of MCU occurrence at higher voltages. At the same time, obviously, the critical charge does not depend on the direction of neutron incidence. Thus, the critical charge is not a dominant factor to explain the differences discussed above.

4.3.3 Angular Response of MCU Characteristics

To explore the different angular sensitivity of MCUs between the the 12-nm FinFET and 20-nm planar SRAMs observed in the previous section, the MCU events were characterized in terms of the multiplicity and the fail bit patterns. The obtained MCU characteristics were compared between the incidence angles and between the 12-nm FinFET and 20-nm planar SRAMs.

The multiplicity distributions for the 12-nm FinFET and 20-nm planar SRAMs are shown in Fig. 4.7(a) and (b), respectively. In each graph, the multiplicities at the incidence angles of 0°, 90° (WL), and 90° (BL) are plotted, where 100% corresponds to the total MCU events. As seen in Fig. 4.7(a), the ratio of the MCU events with multiplicity higher than three increased at the angles of 90° (WL) and 90° (BL) in the 12-nm FinFET SRAMs, as was the case in the 20-nm planar SRAMs. As discussed in Chap. 3, this observation can be understood by the forward emission of secondary ions, where the secondary ions produced at grazing incidence can induce charge deposition on multiple SRAM cells.

An interesting observation was that the ratios of high-multiplicity events were higher for the 20-nm planar SRAMs than for the 12-nm FinFET SRAMs. One possible reason for this observation is the difference in the secondary ions contributing to SEU events between the two SRAMs. It has been demonstrated that the contribution of high-LET ions to SEU events in FinFET devices is relatively larger than that in planar devices [92]. Among the secondary ions produced by neutron-induced spallation reactions, the scattering ranges of high-LET ions are shorter than that of low-LET ions, such as protons and alpha particles, as shown in Fig. 1.5. Hence, the larger contribution of the high-LET ions can lead to the smaller range of charge deposition and hence to the lower ratio of high-multiplicity events. Another possible reason is the impact of PBEs. As indicated in the previous section, the contribution of PBEs is higher for the 20-nm planar SRAMs than for the 12-nm FinFET SRAMs. In this case, the observed difference in the ratio of high-multiplicity events is consistent with the difference in the PBE contribution because the PBEs can increase not only the total MCU ratio but also the occurrence probability of high-multiplicity events [64].

The fail bit patterns were analyzed according the pattern classification shown in Fig. 4.8. There were five MCU groups with different fail bit patterns, which were named as "BL-range $\times$ WL-range(multiplicity)". Note that the mirror images of each pattern are included in the same group. The ratios of these MCU groups are presented in Fig. 4.9 for the All0 pattern and Fig. 4.10 for the CKB0 pattern, where (a), (b), and (c) are for the angles of 0°, 90° (WL), and 90° (BL), respectively.

It was observed that the probability distribution of the MCU groups strongly depends on the data patterns in each angle of incidence. This is due to the difference in the spatial arrangement of internal node voltages of SRAM cells. As described in Sec. 1.3.2, in SRAM circuits, nMOS transistors of high nodes are generally vulnerable to charge collection. In the case of the All0 pattern, the relative location of the nearest neighbor high nodes corresponds to the $2 \times 1(2)$ group [see Fig. 3.1(a)]. In the case

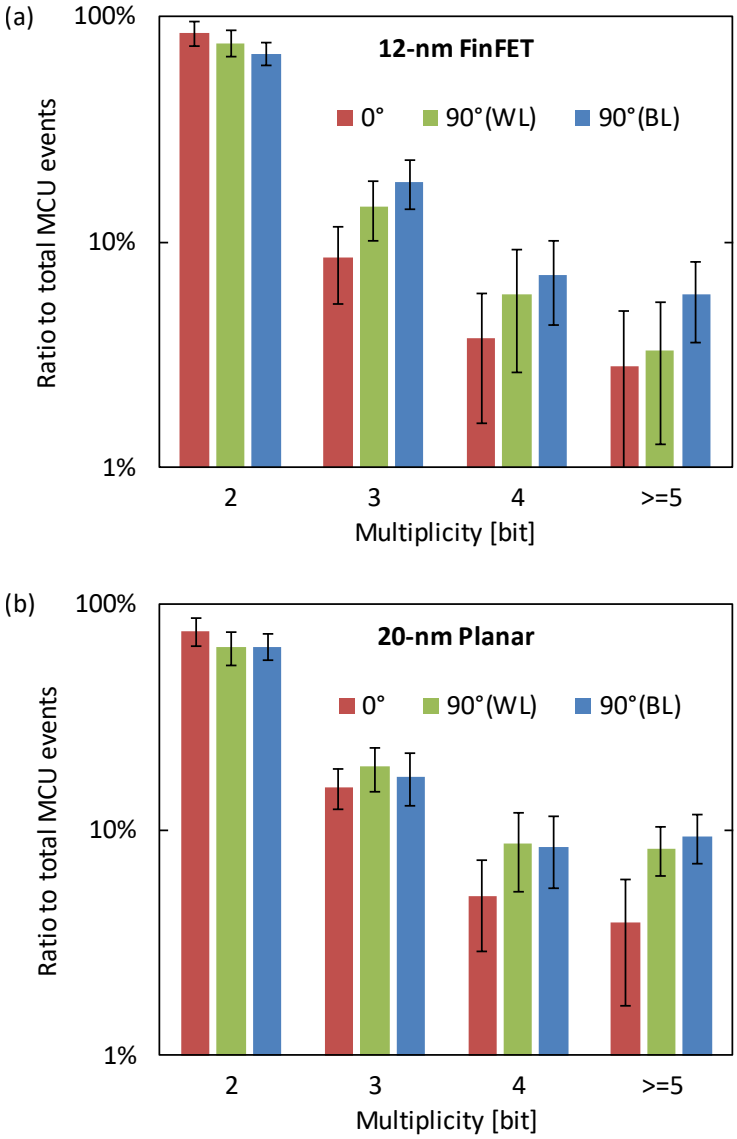

FIGURE 4.7: Multiplicity distributions of neutron-induced MCU events. (a) and (b) are for 12-nm FinFET and 20-nm planar SRAMs, respectively. Red, green, and blue bars correspond to the incidence angles of 0°, 90° (WL) and 90° (BL), respectively. All ratios are the values averaged over the All0 and CKB0 patterns and all voltage conditions. Error bars represent one standard error.

of the CKB0 pattern, this corresponds to the $2 \times 2(2)$ group [see Fig. 3.1(b)]. The impact of this different arrangement was clearly demonstrated in Fig. 4.9 and 4.10, where the occurrence ratios of the $2 \times 1(2)$ and $2 \times 2(2)$ groups were relatively high for the All0 and CKB0 patterns, respectively.

It is worthwhile to note that the contribution of pMOS transistors on the MCU characteristics appeared to be small, although the pMOS transistors of low nodes are sensitive to charge collection. For example, if the pMOS transistors are the dominant contributor in determining fail bit patterns, the ratio of the $2 \times 1(2)$ group is expected

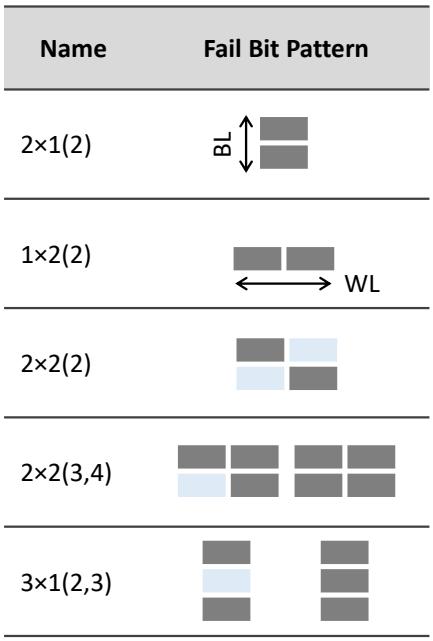

FIGURE 4.8: Groups of fail bit patterns. Rectangular cells represent SRAM cells. Gray cells correspond to fail bits. Vertical and horizontal directions are parallel to BL and WL directions, respectively. The mirror images of each pattern are included in the same group.

to be similar between the All0 and CKB0 patterns. This is because the relative position of two sensitive pMOS transistors in two adjacent SRAM cells along a BL is similar between the two data patterns [see Fig. 3.1]. Contrary to this expectation, the significant difference in the ratio of the $2 \times 1(2)$ group was found between the two data patterns. Therefore, the dominant contributor to the MCU characteristics was indicated to be the nMOS transistors of high nodes in both the 12-nm FinFET and 20-nm planar SRAMs.

For the angular sensitivity of fail bit patterns, it was observed that the spatial range of the fail bit patterns becomes longer in the direction of neutron incidence in both the 12-nm FinFET and 20-nm planar SRAMs. For example, the ratios of the $1 \times 2(2)$ and $3 \times 1(2,3)$ groups are relatively high at the incidence angles of 90° (WL) and 90°(BL), respectively. This observation is consistent with the results presented in Chap. 3, where the distributions of BL-range and WL-range have been analyzed. Therefore, the variations among the incidence angles observed in Fig. 4.9 and 4.10 are probably due to the forward emission of secondary ions.

The important observation in the above pattern analyses was that, as a whole, the probability distribution of fail bit patterns is similar between the 12-nm FinFET and 20-nm planar SRAMs. This indicates that the physical arrangement of node voltages and the forward emission of secondary ions are the significant factors determining the MCU characteristics and their angular sensitivity in the 12-nm FinFET SRAMs, as well as in the 20-nm planar SRAMs.

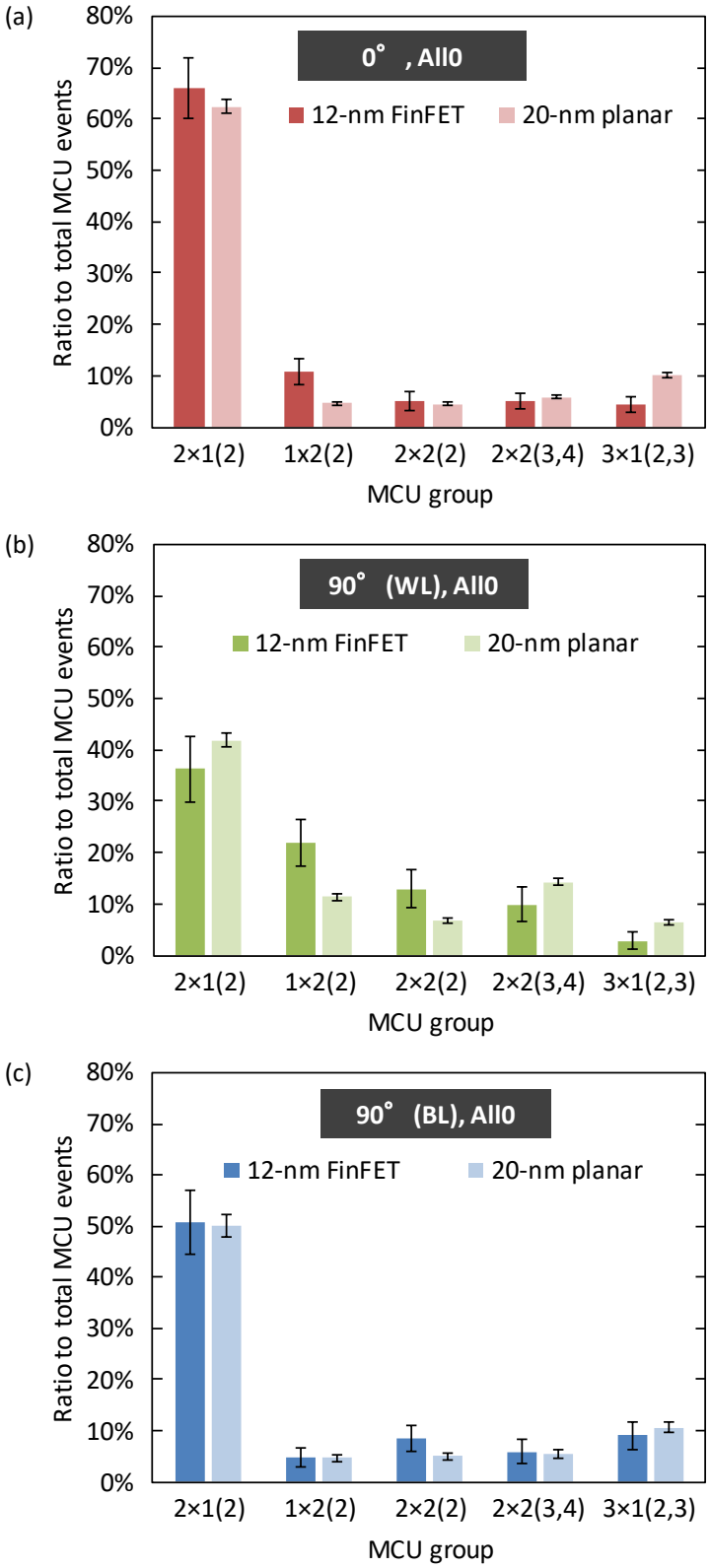

FIGURE 4.9: Ratios for MCU groups shown in Fig. 4.8 in the case of the All0 pattern. (a), (b), and (c) are for the incidence angles of 0°, 90° (WL), and 90° (BL). Dark and light colored bars are for 12-nm FinFET and 20-nm planar SRAMs. All ratios are the values averaged over all VDD conditions. 100% corresponds to the total MCU events. Error bars represent one standard error.

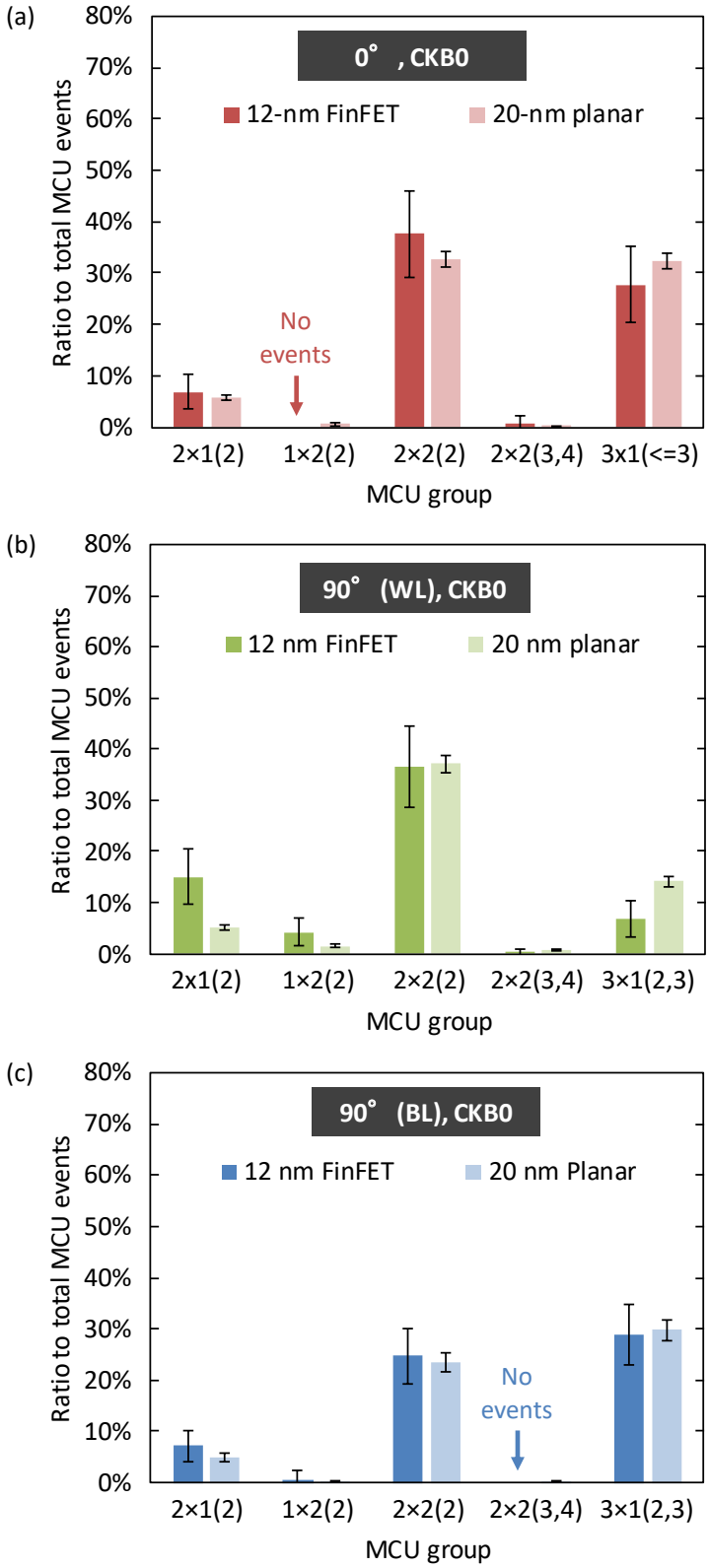

FIGURE 4.10: Ratios for MCU groups shown in Fig. 4.8 in the case of the CKB0 pattern. (a), (b), and (c) are for the incidence angles of 0°, 90° (WL), and 90° (BL). Dark and light colored bars are for 12-nm FinFET and 20-nm planar SRAMs. All ratios are the values averaged over all VDD conditions. 100% corresponds to the total MCU events. Error bars represent one standard error.

4.3.4 Voltage Dependence of Pattern-Wise MCU Ratios

For investigating the contribution of PBEs further, this section looks into the voltage dependence of MCU ratios for respective fail bit patterns, i.e., pattern-wise MCU ratios. As mentioned earlier, the PBEs affect both the voltage dependence of the MCU ratio and the fail bit patterns. Hence, the difference in the PBE contribution could result in the different voltage dependence of the MCU ratio for different fail bit patterns.

In this investigation, the pattern-wise MCU ratios were analyzed for the MCU events in the case of the All0 pattern. This is because the impact of the PBEs can be more significant for the All0 pattern than the CKB0 pattern. As explained in Fig. 3.1, the difference between the two data patterns originates from the arrangement of internal node voltages. An important point to be considered here is that potential perturbation in a p-well can activate the PBEs in multiple nMOS transistors in the p-well. Since the nMOS transistors of high nodes are vulnerable to charge collection, the node voltage arrangement where the high nodes are densely packed in a p-well is highly susceptible to the PBEs. This arrangement corresponds to the case of the All0 pattern.

Among the fail bit patterns extracted in the previous section [see Fig. 4.8], this analysis focused on the MCU events with the range of 2×2 bits for the All0 pattern. There are two groups of the patterns with 2×2, as seen in Fig. 4.8. One is a group named as $2 \times 2(2)$, where two fail bits are diagonally arranged. Another is a group named as $2 \times 2(3,4)$, where three or four fail bits are included. A key point here is that, in contrast to MCU events caused by direct charge collection along ion tracks, the PBEs can cause MCU events with L-shaped and block-like patterns of fail bits because potential perturbation in a p-well can activate PBEs in multiple nMOS transistors simultaneously, as discussed in Chap. 3. Therefore, in the MCU groups of $2 \times 2(2)$ and $2 \times 2(3,4)$, it can be considered that the PBE contribution is larger for the $2 \times 2(3,4)$ group than for the $2 \times 2(2)$ group.

Fig. 4.11 shows the ratios of the $2 \times 2(2)$ and $2 \times 2(3,4)$ groups as a function of the supply voltage. Fig. 4.11(a) and (b) are for the incidence angles of 90° (WL) and 90° (BL), respectively. In the 20-nm planar SRAMs (open symbols), the voltage dependence for the two groups were very similar at both the incidence angles. In the 12-nm FinFET SRAMs (closed symbols), on the other hand, the large discrepancy was found between the two groups at the angle of 90° (BL). As can be seen in Fig. 4.11(b), the ratio of the $2 \times 2(3,4)$ group obviously decreased with increasing the voltage in the 12-nm FinFET SRAMs. In contrast, the ratio of the $2 \times 2(2)$ group was almost independent on the voltage. At the same time, at the angle of 90° (WL), the difference between the ratios of the two groups were not significant and there was no decreasing trend with respect to the voltage, as seen in Fig. 4.11(a).

From the different behavior of the pattern-wise MCU ratios between the angles of 90° (WL) and 90° (BL) observed in Fig. 4.11, it can be deduced that, in the 12-nm FinFET SRAMs, the PBE contribution is smaller at the angle of 90° (BL) than at the

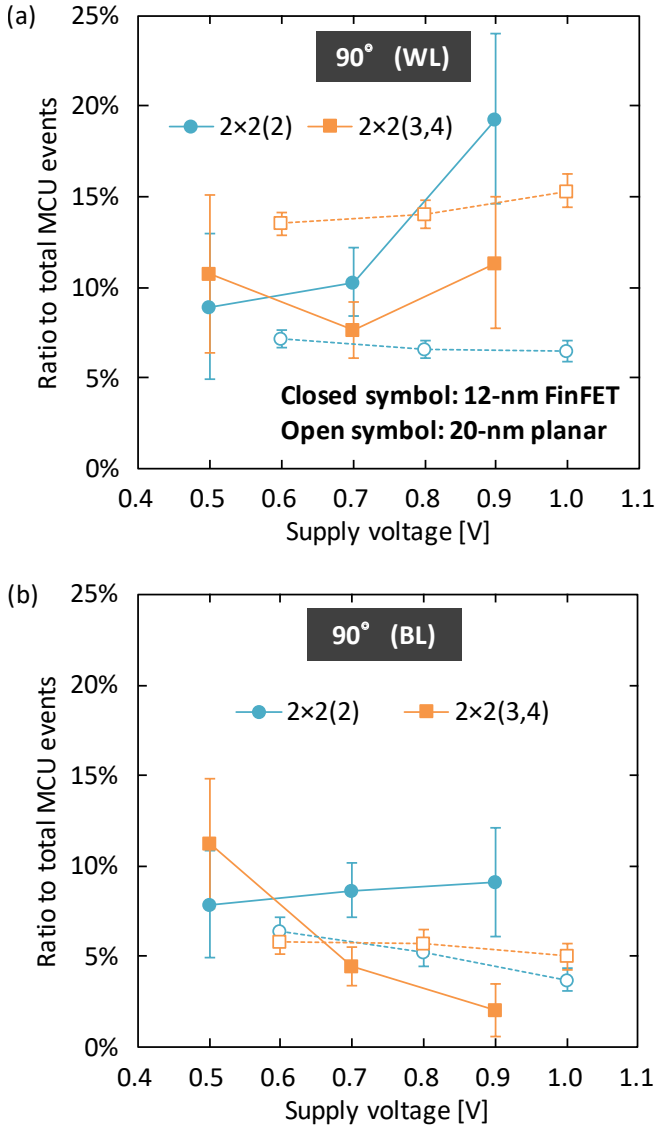

FIGURE 4.11: Ratios of MCU events with 2×2 fail bit patterns as a function of supply voltage in the case of the All0 pattern. (a) and (b) are the ratios at the angles of 90° (WL) and 90° (BL), respectively. Cyan and orange symbols correspond to the groups of $2 \times 2(2)$ and $2 \times 2(3,4)$, respectively. Closed and open symbols are for 12-nm FinFET and 20-nm planar SRAMs, respectively. 100% corresponds to the total MCU events. Error bars represent one standard error.

angle of 90° (WL). Here, a key point is that the large contribution of PBEs results in the positive increase in the slope of the voltage dependence of the MCU ratio, as discussed in Sec. 4.3.2. In this case, it is expected that the $2 \times 2(3,4)$ group has a more positive value of the slope compared to the $2 \times 2(2)$ group when the PBE contribution is significant. As observed in Fig. 4.11, in the 12-nm FinFET SRAMs, the ratio for the $2 \times 2(3,4)$ group apparently decreased with the voltage at the angle of 90° (BL), i.e., the negative value of the slope. Therefore, in the 12-nm FinFET SRAMs, the PBE contribution can be considered to be less significant at the angle of 90° (BL) compared to at the angle of 90° (WL).

The above result is consistent with the discussion in Sec. 4.3.2 and it reinforces the observation that, in the 12-nm FinFET SRAMs, the difference in the MCU response between the angles of 90° (WL) and 90° (BL) stems from the different contribution of PBEs, which makes the angular sensitivity different from the 20-nm planar SRAMs. From the results in this study, it is highly probable that the PBEs are one of the key factors for the angular sensitivity on high-energy neutron-induced MCUs in the 12-nm FinFET SRAMs.

4.4 Conclusion

In this chapter, the high-energy neutron irradiation experiments at several incidence angles have clearly demonstrated the angular sensitivities of SEU, MCU, and MBU responses in the 12-nm bulk FinFET SRAMs. By comparing these results with the results of the 20-nm bulk planar SRAMs presented in Chap. 3, the angular sensitivity of MCUs has been found to be different between the 12-nm FinFET and 20-nm planar SRAMs, where the different contribution of PBEs has been indicated to be a key factor.

The neutron irradiation experiments have been performed by using the same spallation neutron source as in Chap. 3. The SEU, MCU, and MBU rates have been evaluated at three angles of neutron incidence. It has been demonstrated that, although the number of incident neutrons decreases at grazing angle, the MBU rate increases when the incidence direction is parallel to the WL direction, as similarly observed in the 20-nm planar SRAMs. This result suggests that, in the case where the SRAM devices are mounted with their WLs being vertical to the ground, the efficiency of ECCs can be degraded because the most part of terrestrial neutrons are directed downward. It has been revealed that the angular response of MCUs is different between the 12-nm FinFET and 20-nm planar SRAMs. In particular, the voltage dependence of the MCU ratio in the 12-nm FinFET SRAMs is considerably dependent on the incidence angle, whereas it is not in the 20-nm planar SRAMs. Through the comparison of the MCU characteristics, this different angular response has been attributed to the different contribution of PBEs, where the PBE contribution is more significant in the 20-nm planar SRAMs. At the same time, it has been indicated that, in the 12-nm FinFET SRAMs, the PBE contribution becomes relatively large when the incidence angle is parallel to the WL direction.

In conclusion, this study has demonstrated that the incidence angle of high-energy neutrons significantly affects SEU susceptibility and MCU characteristics in the 12-nm FinFET SRAMs, as well as in the 20-nm planar SRAMs. Therefore, the device orientation needs to be considered in evaluating the SEUs and MCUs in the terrestrial environment. At the same time, the structural difference between planar FETs and FinFETs results in the difference in the PBE contribution between the planar and FinFET SRAMs, leading to the different angular sensitivity of MCUs.

Chapter 5

Muon-Induced SEUs With Comparison to Other Terrestrial Radiations

This chapter studies negative and positive muon-induced SEUs in 20-nm bulk planar SRAMs. Muon irradiation is performed using a mono-energetic source with varying the muon energy. The energy dependence of the SEU and MCU CSs shows the significant contribution of muon capture reactions for the negative muons, as reported in previous studies. Interestingly, MCU events are found for the positive muons, in contrast to the previous studies. The CSs for the negative and positive muons are compared with that for high-energy neutrons investigated in Chap. 3 and for the other terrestrial radiations: thermal neutrons and alpha particles. The voltage dependence of the SEU CS, together with the empirical model for charge collection, demonstrates the difference in the contributing secondary ions among the negative muons, the high-energy neutrons, and the thermal neutrons. The MCU events are thoroughly analyzed in terms of the MCU ratio and the fail bit patterns. The results reveal that the MCU characteristics for the negative muons are different from that for the other terrestrial radiations due to the muon capture reactions, where PBEs and the isotropic emission of secondary ions are important factors.

5.1 Introduction

Muons have received increasing attention as a source of soft errors in the terrestrial environment, where negative and positive muons are produced as secondary cosmic-rays through interactions between primary cosmic-rays and the atmosphere. One reason for this increased attention is that scaled semiconductor devices have become sensitive to low-LET particles due to the decreased critical charge, as described in Sec. 1.3.2. Another reason is that the muons are the most abundant particles among secondary cosmic-rays [see Table 1.1]. As a result, as mentioned in Sec. 1.3.5, there is a growing concern that the negative and positive muons could become a significant source of the terrestrial soft errors [13], [14].

Recent irradiation experiments demonstrated that both the negative and positive muons induce SEUs in deep-submicron SRAM devices [48]–[50], [101]. One of the important observations in these experiments was that the SEU CS is higher for the negative muons than for the positive muons, although the LET is nearly identical between the negative and positive muons. This higher CS for the negative muons was clearly explained by muon capture reactions, which are absent for the positive muon. As presented in Eq. (1.4), through this capture reactions, the negative muons can produce secondary ions with higher-LET than the negative muon itself.

In particular, it was shown that the negative muons induce considerable MCUs in 65-nm and 28-nm bulk planar SRAMs, while the positive muons do not [49], [50]. As mentioned in Sec. 1.3.3, the MCUs are a reliability concern in SRAM devices because MBUs can cause malfunctions even when ECCs are implemented. The important points here are that the MCU susceptibility increases with the shrinkage of the SRAM cells, and that due to the miniaturization of transistors the MCU mechanism becomes complicated, such as PBEs induced by well potential perturbation [63], [64]. Therefore, it is required to investigate the muon-induced MCUs in more advanced SRAMs for reliability assurance.

In the terrestrial environment, neutrons and alpha particles have been recognized as major sources of the SEUs and MCUs in recent SRAM devices, as explained in Sec. 1.2. The neutrons are secondary cosmic-rays and include high-energy and thermal components [see Fig. 1.3]. Unlike the high-energy neutrons, the sensitivity to the thermal neutrons depends on the abundance of ^{10}B atoms in device materials [102]. It has been reported that recent manufacturing processes cause the introduction of the ^{10}B atoms, which makes SRAM devices sensitive to the thermal neutrons [29], [43], [44]. The alpha particles are emitted from radioisotopic impurities naturally present in device materials, such as packages [see Table 1.2].

To characterize the muon-induced SEUs and MCUs, it would be beneficial to compare them with those for the other terrestrial radiations: the high-energy neutrons, the thermal neutrons, and the alpha particles. Furthermore, since the SEU mechanisms of the neutrons and the alpha particles are well-established, this comparison will provide the better understanding of the mechanism of the muon-induced SEUs. Gasiot *et al.* [103] experimentally characterized SEUs induced by the positive muons, the high-energy neutrons, the thermal neutrons, and the alpha particles in 28-nm bulk and SOI SRAMs. Liao *et al.* [104] experimentally demonstrated the similarity in SEU and MCU characteristics between the negative muons and the high-energy neutrons in 65-nm bulk SRAMs. However, at the present time, there have been no experimental studies comparing SEU and MCU characteristics for the negative and positive muons with that for all the other terrestrial radiations.

In this context, this study investigates the negative and positive muon-induced SEUs and MCUs in 20-nm bulk planar SRAMs, along with comparison to the high-energy neutrons, the thermal neutrons, and the alpha particles. The SEU and MCU CSs are statistically evaluated by irradiation tests using mono-energetic muon beams,

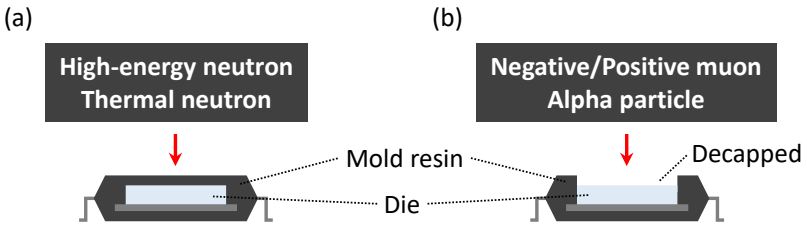

FIGURE 5.1: Irradiation configurations for (a) high-energy and thermal neutrons, (b) negative and positive muons, and alpha particles. The chips were irradiated from the top as indicated by red arrows. In the cases of negative and positive muons, and alpha particles, the package was decapsulated.

atmospheric-like neutron beams, and an alpha-ray source. The CSs for the muons are analyzed in terms of their energy and supply voltage dependence, and are then compared with that for the other particles. To explore the MCU characteristics, the MCU events are thoroughly analyzed with respect to the multiplicity and the fail bit pattern. The underlying mechanisms are discussed through the characterization of the muon-induced SEU and MCU events.

5.2 Experimental Setup

5.2.1 Tested Device and Operation

The test vehicle was SRAM chips fabricated in a 20-nm bulk planar CMOS process, which were the same as Chap. 2 and 3. The package type was a standard plastic quad flat package. As illustrated in Fig. 5.1, the SRAM chips were irradiated from the top. The chips for muon and alpha particle irradiations were decapsulated [see Fig. 5.1(b)].

The SRAM operation was basically the same as the one described in Sec. 3.2.1, except for the supply voltage condition. The operation during the irradiation consisted of write, hold, and read cycles in this order. This operation was a static mode with no write and read functions during the hold cycle. The supply voltage in the hold cycle was varied from 0.35 V to 1.0 V to investigate the voltage dependence of the SEU and MCU CSs. The number and physical addresses of fail bits were collected in the read cycle.

In this operation, the SRAM chips were written with the All0 and CKB0 pattern in the same way as Chap. 3. In the case of the All0 pattern, a logical “0” was written in all the bits. In the case of the CKB0 pattern, logical “0” and “1” were physically arranged in a checkerboard fashion, where “0” was written in the first bit. The arrangements of node voltages for the All0 and CKB0 patterns have been explained in Fig. 3.1(a) and (b), respectively.

TABLE 5.1: Incident Particles and Irradiation Facilities.

Incident particle	Energy	Facility
Negative/Positive muon	Monoenergetic	MUSE [105]
High-energy neutron	Atmospheric-like	RCNP [84]
Thermal neutron	Atmospheric-like	KUR [106]
Alpha particle	5.4 MeV	Lab. (^{241}Am)

5.2.2 Particle Irradiation

Irradiation tests were carried out for the negative muons, the positive muons, the high-energy neutrons, the thermal neutrons, and the alpha particles. The incident particles and the corresponding facilities are summarized in Table 5.1.

Negative and Positive Muons

The negative and positive muon irradiations were performed using a monoenergetic muon beam at the muon science establishment (MUSE), Japan Proton Accelerator Research Complex (J-PARC) [105]. The energy distribution was Gaussian with a standard deviation of $\sim$ 5%. To minimize muon scattering that occurs before the muons reach the Si die, the irradiations were conducted in helium gas and the mold resin above the Si die was removed [see Fig. 5.1(b)]. To investigate the energy dependence of the SEU and MCU CSs, the muon energy was varied from 0.84 MeV to 1.46 MeV, which corresponds to the momentum range from 13.4 MeV/c to 17.7 MeV/c. The muon flux was estimated for each energy by measuring muon decay electrons and positrons, and also by analyzing muonic X-rays using a graphite specimen [107]. The estimated flux at 1.46 MeV, for example, was $\sim 1 \times 10^2$ /cm^2/s.

High-Energy Neutron

The high-energy neutron irradiation was performed using a spallation neutron beam at the RCNP, Osaka University [84]. The energy spectrum of this beam was similar to that of the terrestrial neutron in the energy range from 1 MeV to 300 MeV, as shown in Fig. 5.2. The integral neutron flux above 10 MeV was $\sim 7.0 \times 10^6$ /cm^2/s. Note that the most of data for the high-energy neutron irradiation was based on the results in Chap. 3.

Thermal Neutron

The thermal neutron irradiation was performed using a neutron irradiation field at the Heavy Water Neutron Irradiation Facility (HWNIF) of the Kyoto University Research Reactor (KUR) [106]. The energy spectrum of this beam was similar to that of the terrestrial neutron in the thermal energy range, as presented in Fig. 5.2. The integral neutron flux below 0.5 eV, which was measured using gold activation

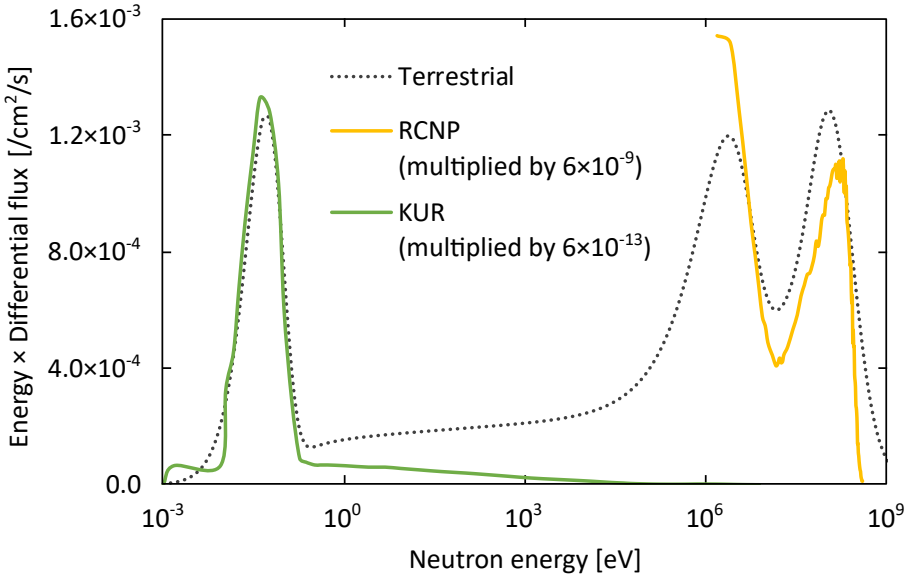

FIGURE 5.2: Energy spectra of the terrestrial neutron [12], the spallation neutron beam at RCNP [84], and the thermal neutron beam at KUR [106].

wires, was $\sim 2.0 \times 10^8$ /cm^2/s. The thermal neutron sensitivity of the test chip was confirmed by performing the irradiations with and without boron shields that can attenuate the thermal neutrons.

Alpha Particle

The alpha particle irradiation was performed using an ^{241}Am source. The nominal energy of the emitted alpha particles was 5.4 MeV. The source was placed above the decapped chip [see Fig. 5.1(b)]. The particle flux at the surface of the Si die was estimated as $\sim 2.9 \times 10^2$ /cm^2/s.

5.2.3 CS Calculation

The SBU and MCU events were extracted separately according to the spatial distribution of the fail bits. In addition, the MBU events, which correspond to the MCU events with multiple fail bits in the same WL, were also analyzed. It should be noted that the number of the fail bits accumulated during one hold cycle was kept small enough to avoid misinterpreting multiple SBU events as an MCU event.

The SEU, SBU, MCU, and MBU CSs were calculated as $N_{\mathrm{event}}/(\Phi \times N_{\mathrm{bit}})$, where Φ and N_{bit} are the incident particle fluence and the number of SRAM bits irradiated, respectively. N_{event} is the number of observed events for the SEUs, SBUs, MCUs, and MBUs. Here, the SEU events correspond to the sum of the SBU and MCU events.

5.3 Results and Discussion

5.3.1 Muon Energy Dependence of SEU, SBU, and MCU CSs

The muon irradiation with varying the incident energy confirmed the strong energy dependence of the CSs for the negative and positive muons. Fig. 5.3(a), (b), and (c) present the energy dependence of the SEU, SBU, and MCU CSs, respectively. In this investigation, to maximize the SEU response to the energy change, the supply voltage was set to 0.35 V, which was much lower than the typical operation range. The data pattern was the All0 pattern.

The SEU CS showed a clear peak at 1.02 MeV for both the negative and positive muons, as seen in Fig. 5.3(a). This CS-peak energy probably corresponds to the case where the position of the Bragg peak of the muon beam is close to the position of the transistors of the SRAM cells. In this case, the charge deposition due to the direct ionization of the muons becomes maximum at the transistors, and hence the SEU events are more likely to occur. The results clearly demonstrated the coincidence of the CS-peak energy between the negative and positive muons. This reflects the almost identical ranges and LETs of these muons. The similar energy dependence was observed in the previous studies [48], [49].

Although the SBU CS was comparable between the negative and positive muons, the MCU CS for the negative muons was significantly higher than that for the positive muons, as seen in Fig. 5.3(b) and (c). This difference stems from the muon capture reactions of the negative muons, as discussed in [49]. This capture reactions can produce secondary ions whose LETs are higher than that of the primary muons. This results in the large amount of charge deposition on the transistors. Furthermore, the produced ions are emitted isotropically regardless of the incident direction of the negative muons. In this case, some of these ions travel along the plane of the SRAM array, and hence their tracks can cover the multiple SRAM cells. Therefore, the higher MCU CS for the negative muons than for the positive muons obviously indicates the considerable contribution of the capture reactions for the negative muons.

An interesting observation was that MCU events were found in the positive muon irradiation, as confirmed in Fig. 5.3(c). In Liao's results previously reported for 65-nm bulk planar SRAMs, no MCU events were observed even at the low voltage condition of 0.4 V [49]. In the results for the 20-nm bulk planar SRAMs, on the other hand, the MCU events were observed at 0.35 V and 0.6 V [see also Fig. 5.3(b)]. This discrepancy can be understood as the scaling effect of the SRAM cells, where the smaller cells are more susceptible to the MCUs induced by charge sharing [62]. The present results thus suggest that the positive muons becomes a possible source of the MCUs in highly-scaled SRAM devices.

In the following investigations, the muon energy was fixed to the CS-peak energy, 1.02 MeV, for both the negative and positive muons. This aims to fully capture

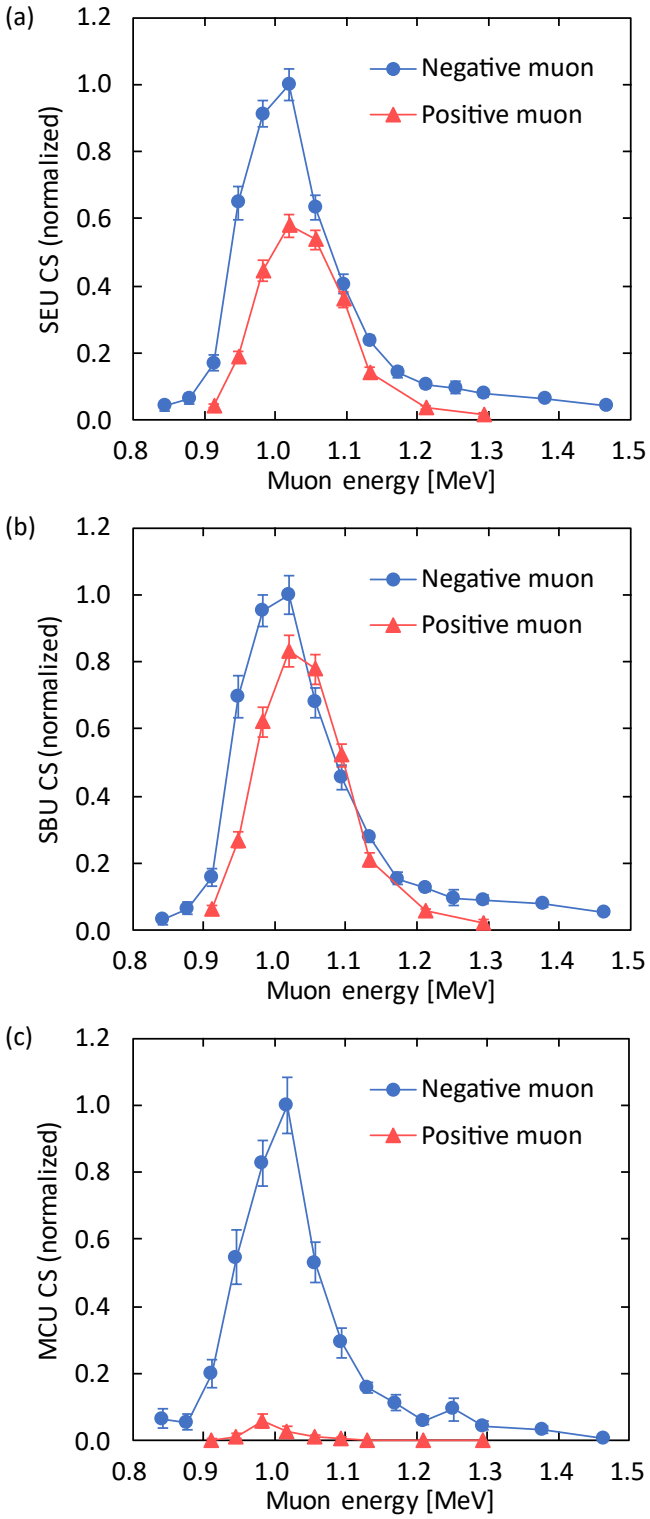

FIGURE 5.3: (a) SEU, (b) SBU, and (c) MCU CSs as a function of muon energy. Blue and red symbols are for negative and positive muons, respectively. Each CS is normalized by the CS value at 1.02 MeV of the negative muon. Supply voltage and data pattern are 0.35 V and All0, respectively. Error bars represent one standard error.

the muon-specific characteristics and to consider the worst-case situation for the SEU and MCU occurrence.

5.3.2 Supply Voltage Dependence of SEU, MCU, and MBU CSs

The comparison of the CSs among the incident particles demonstrated similarities and differences in the voltage dependence. Fig. 5.4(a), (b), and (c) present the voltage dependence of the SEU, MCU, and MBU CSs, respectively. Each graph includes the CSs for the particles listed in Table 5.1. The data pattern was the All0 pattern. To emphasize the similarities and differences, the CSs were normalized in each particle by the respective CS value at 0.6 V.

For all the particles, the SEU CS exhibited an exponential decrease with the voltage, as seen in Fig. 5.4(a). Such exponential dependence has been represented in the empirical model,

$$\text{SEU CS} \propto \exp(-Q_{\text{crit}}/Q_{\text{coll}}), \tag{5.1}$$

where Q_{crit} and Q_{coll} denote critical charge and collected charge, respectively [108]. As described in Sec. 1.3.2, with a first order approximation, the critical charge can be expressed as the product of the supply voltage and the capacitance of internal nodes: $Q_{\text{crit}} \sim V_{\text{DD}} \times C_{\text{node}}$. Moreover, the collected charge increases with increasing the charge deposited by the particles. Hence, the difference in the charge deposition among the incident particles can be evaluated by comparing the slope of the CS to the voltage: the steeper the slope, the smaller the charge deposition.

The SEU CS for the positive muons drastically decreased with the voltage, which was significantly different from the other particles, as observed in Fig. 5.4(a). The charge deposition by the positive muons is solely due to the direct ionization, in which the LET is low [see Fig. 1.10]. This obviously results in the small deposited charge compared to the other particles. From Eq. (5.1), this small charge deposition leads to a steeper slope for the positive muons than for the other particles, which is consistent with the observed result.

In the case of the negative muons, the voltage dependence of the SEU CS was very similar to that for the high-energy neutrons, as confirmed in Fig. 5.4(a). The muon energy in this investigation was the CS-peak energy at which the contribution of the muon capture reactions is significant, as discussed in the previous section. In this case, the variety of the produced secondary ions and their LETs probably results in the broad distribution of the charge deposition, which is completely different from the positive muon case. From Eq. (5.1), the similarity in the slope can be interpreted as the similar charge deposition. Therefore, it is indicated that the distribution of the charge deposition caused by the negative muons is similar to that caused by the high-energy neutrons.

It is worth mentioning here that the similarity in the voltage dependence of the CSs between the negative muons and the high-energy neutrons was reported in [104], where the experiments were performed mostly using a monoenergetic neutron source. The experiments in this study, on the other hand, demonstrated the similarity using the spallation neutron source with the atmospheric-like energy spectrum.

In contrast to this similarity, the voltage dependence of the SEU CS for the negative muons was different from that for the thermal neutrons and the alpha particles. This would be explained by the difference in the charge deposition. Here, the similarity between the thermal neutrons and the alpha particles is reasonable because the LET of the alpha particles is comparable to that of the secondary ions produced by the thermal neutrons, where an alpha particle and a Li ion are produced through a neutron capture reaction of ^{10}B atoms [see Fig. 1.8 and Fig. 1.11]. The key observation was that the slope for the negative muons was steeper than that for the thermal neutrons and the alpha particles. Since the steeper slope corresponds to the smaller deposited charge as indicated by Eq. (5.1), this result suggests that, in the case of the negative muons, the observed SEU events include the events induced by the smaller charge deposition than the alpha particles.

To understand the steeper slope for the negative muons than for the thermal neutrons and the alpha particles, the CS difference between the negative and positive muons was analyzed. In Fig. 5.4(a), the voltage dependence of the CS difference between the muons is shown with open circles, where the CS for the positive muons was subtracted from that for the negative muons. Since the LET of direct ionization is almost identical between the negative and positive muons, the CS difference between the muons can be considered as the contribution of the capture reactions for the negative muons. As confirmed in Fig. 5.4(a), the voltage dependence for this CS difference was similar to that for the thermal neutrons and the alpha particles. This clearly demonstrates that the muon direct ionization differentiated the voltage dependence of the SEU CS for the negative muons from that for the thermal neutrons and the alpha particles, which is consistent with the above suggestion.

It is also interesting that the slope for the high-energy neutrons was steeper than that for the CS difference between the negative and positive muons. The key observations here are that the slope for the CS difference between the muons was similar to that for the alpha particles, and that the slope for the high-energy neutrons was steeper than that for the alpha particles. It can be deduced from these observations and Eq. (5.1) that the steeper slope for the high-energy neutrons than for the CS difference between the muons is caused by lower-LET ions than the alpha particles, i.e. protons. This is consistent with spallation reactions induced by the high-energy neutrons, where the protons are the most abundant secondary ions, as presented in Fig. 1.4. This result therefore indicates that the voltage dependence of the SEU CS induced by the muon capture reactions is different from that induced by the high-energy neutrons due to this proton contribution. In other words, the observed similarity in the voltage dependence between the negative muons and the high-energy neutrons possibly stems from the compensation between the proton contribution for the high-energy neutrons and the direct ionization contribution for the negative muons. This view seems reasonable because the LET of the muon is similar to that of the proton, as seen in Fig. 1.10.

As regards the MCU and MBU CSs shown in Fig. 5.4(b) and (c), their voltage dependence was apparently different from the SEU CS and also between the MCU and MBU CSs. For example, the slope for the alpha particles was steeper than that for the negative muons, in contrast to the case of the SEU CS. These results indicate that the difference in the MCU and MBU responses among the particles cannot be explained simply by the difference in the amount of the charge deposition. Moreover, since the MBU events are the MCU events with specific fail bit patterns, the difference between the MCU and MBU responses suggests the difference in the spatial distribution of the charge deposition and the MCU mechanism among the particles. This point is discussed in the following sections.

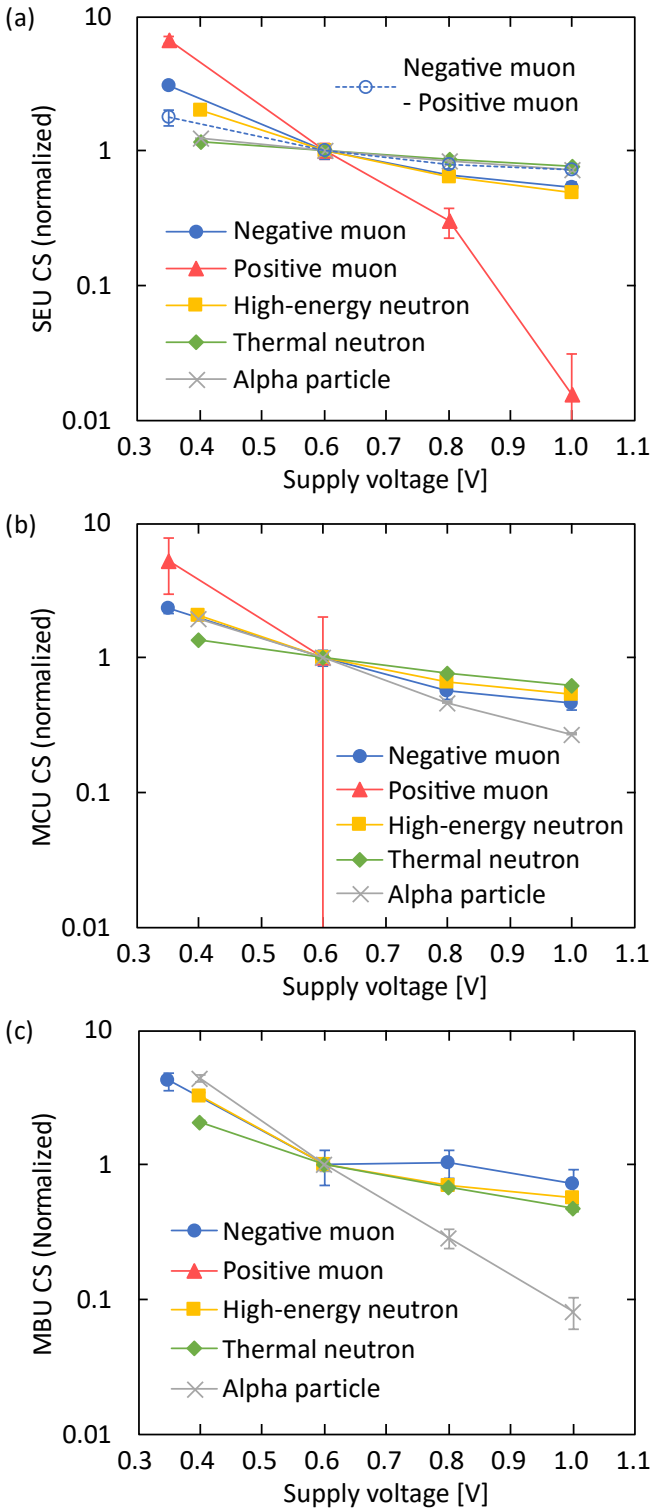

FIGURE 5.4: (a) SEU, (b) MCU, and (c) MBU CSs as a function of supply voltage. Blue and red symbols are for negative and positive muons, respectively. Yellow and green symbols are for high-energy and thermal neutrons, respectively. Gray symbols are for alpha particles. Open circles are for the difference between the negative and positive muons: CS(negative muon) − CS(positive muon). The CSs are normalized in each particle by the respective CS value at 0.6 V. The muon energy is 1.02 MeV. Data pattern is All0. Error bars represent one standard error.

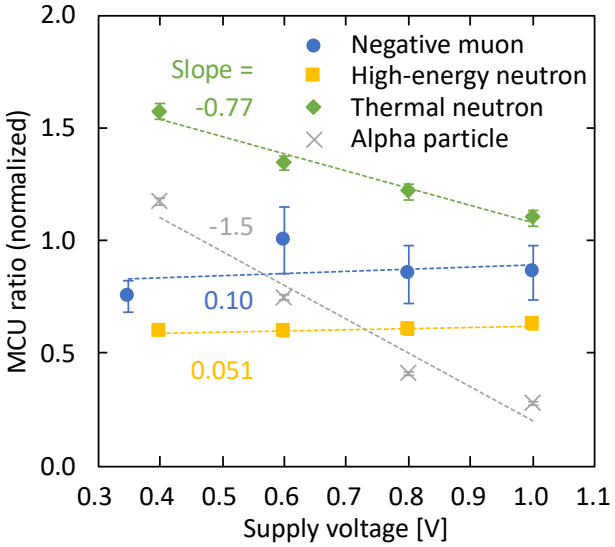

FIGURE 5.5: MCU ratio as a function of supply voltage. Symbols are same as Fig. 5.4. The values are normalized by the value at 0.6 V of negative muon. Data pattern is All0. Error bars represent one standard error. Broken lines correspond to linear fitted curves, where the values of the slopes are noted.

5.3.3 Analysis of MCU Ratios

MCU ratios, which were calculated by dividing the MCU CS with the SEU CS, were compared among the incident particles to investigate the difference in the MCU mechanism. The voltage dependence of the MCU ratio is compared in Fig. 5.5, where the data pattern was the All0 pattern. The data pattern dependence is then examined in Fig. 5.6. Note that the result for the positive muons is omitted because its MCU CS was significantly low.

The MCU ratio for the negative muons was larger than that for the high-energy neutrons over the entire voltage range, as seen in Fig. 5.5. This probably reflects the difference in the emission direction of secondary ions between the muon capture reactions and the neutron spallation reactions. In the case of the muon capture reactions, the secondary ions are emitted isotropically. In contrast, in the case of the neutron spallation reactions, the secondary ions tend to be emitted in the forward direction [22]. Since the high-energy neutron irradiation was conducted at normal incidence, the tracks of the secondary ions in the plane of the SRAM array should be shorter for the high-energy neutrons than for the negative muons, which results in less chance to cause MCU events for the high-energy neutrons. This leads to the higher MCU ratio for the negative muons than for the high-energy neutrons, which agrees with the observed difference.

At the same time, the MCU ratio for the negative muons was lower than that for the thermal neutrons over the entire voltage range. In the case of the neutron capture reaction in ^{10}B atoms, the secondary ions are emitted isotropically, as in the case of the muon capture reactions. One important point here is the location of the

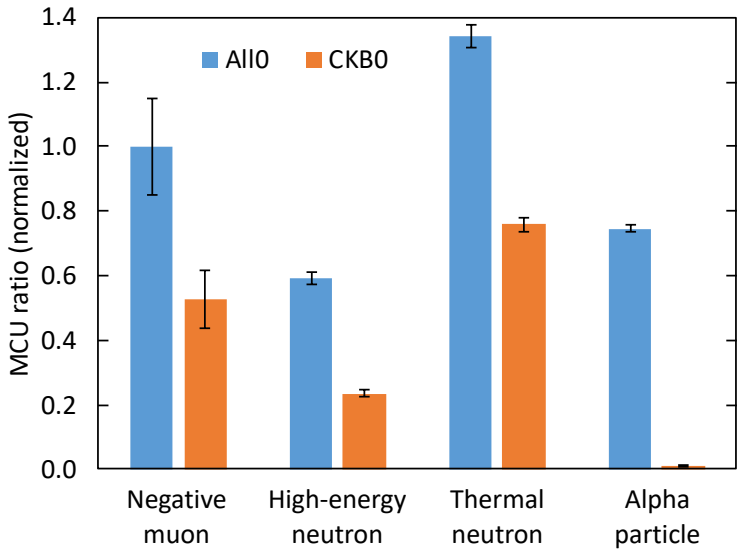

FIGURE 5.6: Data pattern dependence of MCU ratio at 0.6 V. Cyan and orange bars are for All0 and CKB0 patterns, respectively. The values are normalized by the value of negative muon for the All0 pattern. Error bars represent one standard error.

^{10}B atoms. As described in Sec. 1.2.1, it was reported that, in advanced technologies, the ^{10}B atoms are introduced during the manufacturing process of W plugs, and hence the ^{10}B atoms are localized on the transistors within the depth range of a few hundred nanometers [26], [29], [44]. Another important point is the position of the muon stopping because the muon capture reactions can occur when the negative muon stops. Due to the energy spread of the muon beam, which includes the effect of scattering by the metal layer, the depth range of the stopping position was estimated to be larger than that of the ^{10}B atom position. It is geometrically obvious that the isotropic emissions occurred near the plane of the SRAM array are more likely to invoke the ion tracks covering the multiple SRAM cells. Therefore, the localized distribution of the ^{10}B atoms results in the higher MCU ratio for the thermal neutrons compared to the negative muons, as observed in Fig. 5.5.

Another important finding in the voltage dependence of the MCU ratio was the difference in the slopes, the values of which are noted in Fig. 5.5. The slope for the negative muons was similar to that for the high-energy neutrons and was ~ 0. On the other hand, the slopes for the thermal neutrons and the alpha particles were large negative values. The possible reason for this difference is the different contribution of the PBE. It is known that the PBE increases the MCU ratio and becomes more effective with increasing the voltage [65]. Hence, in terms of the slope of this voltage dependence, the negative slope can be interpreted as the small contribution of the PBE. From the results in Fig. 5.5, it is speculated that the PBE contribution for the thermal neutrons and the alpha particles is less significant than that for the negative muons and the high-energy neutrons. This is consistent with the PBE mechanism, where relatively large charge deposition is required for well potential perturbation. Since

the muon capture reactions produce the secondary ions with higher-LET than alpha particles and Li ions, the PBE contribution can be larger for the negative muons than for the thermal neutrons and the alpha particles. At the same time, the similarity in the slope between the negative muons and the high-energy neutrons indicates that the PBE contribution is comparable between them.

The data pattern dependence of the MCU ratio also showed interesting differences among the incident particles. Fig. 5.6 presents the MCU ratio for the All0 and CKB0 patterns at 0.6 V. For all the particles, the MCU ratio for the All0 pattern was higher than that for the CKB0 pattern. This reflects the difference in the arrangement of node voltages between the data patterns [see Fig. 3.1]. Since, as described in Sec. 1.3.2, SEU occurrence in SRAM cells is basically dominated by charge collection in nMOS transistors of high nodes, a smaller distance between neighboring high nodes results in a higher probability in MCU occurrence. In this case, the distance between the neighboring high nodes is smaller for the All0 pattern than for the CKB0 pattern, leading to the higher MCU ratio for the All0 pattern.

The key observation in this data pattern dependence was the difference in the relative magnitude between the MCU ratios for the All0 and CKB0 patterns. In the case of the negative muons, the MCU ratio for the CKB0 pattern was approximately half that for the All0 pattern, which was almost the same as the case of the thermal neutrons. In the case of the high-energy neutrons, the ratio for the CKB0 pattern was less than half that for the All0 pattern. In the case of the alpha particles, the ratio for the CKB0 pattern was significantly low. From the comparison between the thermal neutrons and the alpha particles, it can be deduced that, for the thermal neutrons, the relatively high MCU ratio for the CKB0 pattern is due to the isotropic emission of the secondary ions because the LET of the alpha particles is comparable to that of the secondary ions produced by the thermal neutron. Therefore, the similarity between the negative muons and the thermal neutrons possibly indicates the impact of the isotropic ion emission of the muon capture reactions on the MCU response.

5.3.4 Analysis of MCU Characteristics

In the previous section, it is indicated that the factors contributing to the negative muon-induced MCUs are the PBE and the isotropic emission of the secondary ions. To explore these factors in more detail, the MCU events were analyzed in terms of the multiplicity and the fail bit pattern, in a similar way as in Sec. 4.3.3. This analysis was conducted for the All0 pattern.

In the multiplicity distribution shown in Fig. 5.7, the negative muons exhibited a similar trend with the high-energy neutrons and the thermal neutrons, where the MCU events with high multiplicities were found. In the case of the alpha particles, almost all the MCU events were with the multiplicity of 2. This result clearly demonstrates that the high-multiplicity events for the negative muons were induced by the secondary ions produced through the muon capture reactions.

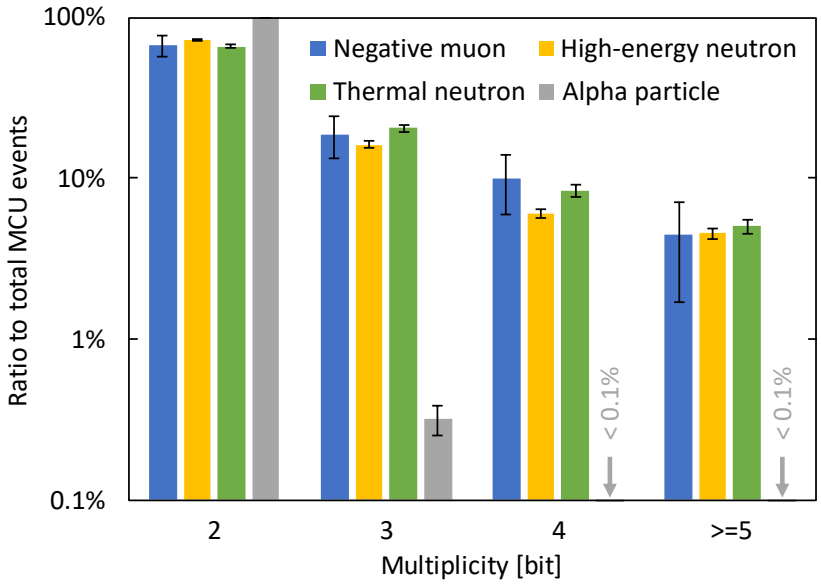

FIGURE 5.7: Multiplicity distribution of MCU events. Blue bars are for negative muons. Yellow and green bars are for high-energy and thermal neutrons, respectively. Gray bars are for alpha particles. All ratios are the values averaged in the range $\geq$ 0.6 V. 100% corresponds to the total MCU events. Data pattern is All0. Error bars represent one standard error.

When focusing on the difference between the high-energy neutrons and the thermal neutrons, the ratios at the multiplicities of 3 and 4 were higher for the thermal neutrons, whereas the ratio at the multiplicity of $\geq$ 5 is similar between them. This can be explained by the larger contribution of the PBE for the high-energy neutrons because the PBE increases the multiplicity of MCU events [64]. For the negative muons, the PBE contribution is indicated to be comparable to that for the high-energy neutrons in the previous section. On the other hand, no distinguishable difference was observed in the multiplicity distribution between the negative muons and the thermal neutrons. To elucidate this point, the fail bit patterns were compared.

The fail bit patterns of the MCU events were analyzed according to the classification shown in Fig. 5.8, where the five groups were named as "BL-range$\times$WL-range(multiplicity)". The ratios of these MCU groups for the incident particles are presented in Fig. 5.9.

The ratio of the 2 $\times$ 1(2) group was the highest for all the particles. This is obvious from the physical range of the fail bit pattern. As illustrated in Fig. 5.8, due to the rectangular shape of the SRAM cells, the physical range of the 2 $\times$ 1(2) group is the shortest among the five groups. In the case of the alpha particles, the ratio of this 2 $\times$ 1(2) group was approximately 98%. As discussed in Fig. 5.6, the difference between the thermal neutrons and the alpha particles can be considered as the impact of the isotropic ion emission. Therefore, for the thermal neutrons, the relatively high ratios in the other four groups are very likely due to the isotropic ion emission.

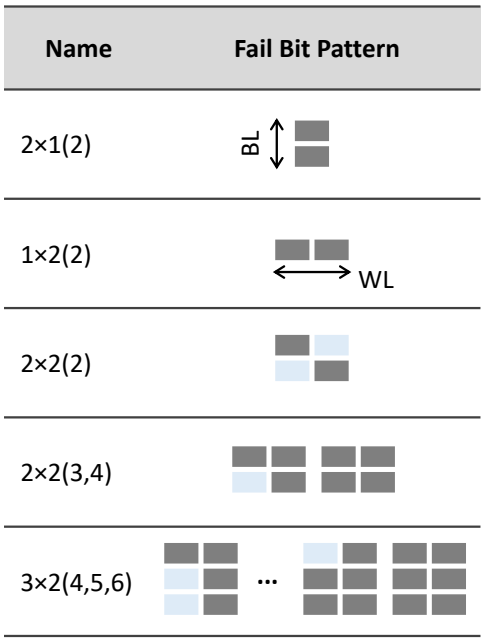

FIGURE 5.8: Groups of fail bit patterns. Rectangular cells are SRAM cells. Gray cells represent fail bits. Vertical and horizontal directions are parallel to BL and WL directions, respectively. The mirror images of each pattern are included in the same group.

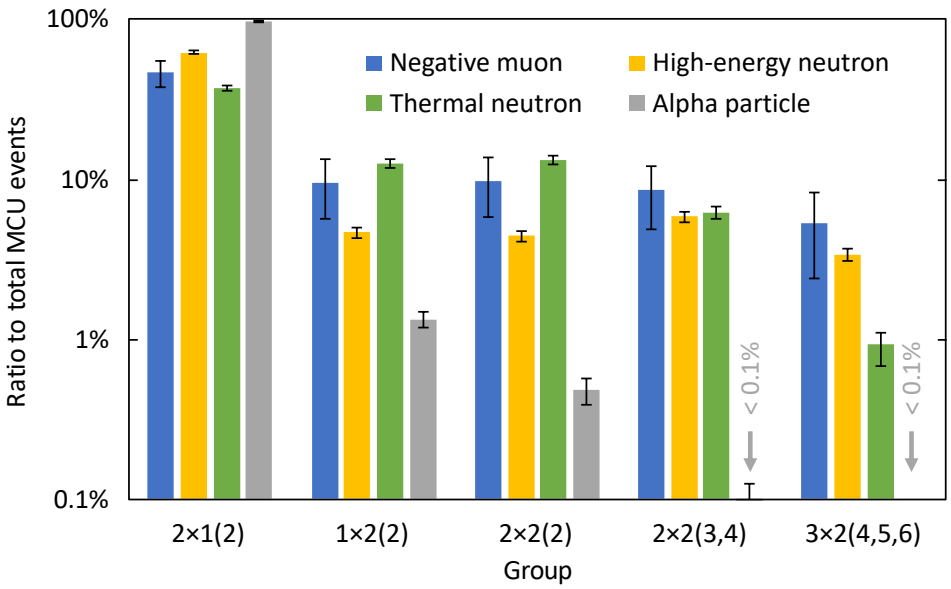

FIGURE 5.9: Ratios for MCU groups shown in Fig. 5.8. The color for each particle is the same as used in Fig. 5.7. All ratios are the values averaged in the range $\geq$ 0.6 V. 100% corresponds to the total MCU events. Data pattern is All0. Error bars represent one standard error.

In the $1 \times 2(2)$ and $2 \times 2(2)$ groups, the ratio for the negative muons was similar to that for the thermal neutrons, rather than that for the high-energy neutrons. This indicates that, for the negative muons, these MCU groups were mainly due to the isotropic emission of the secondary ions. Similarly, the impact of the isotropic emission was suggested in the data pattern dependence of the MCU ratio in Fig. 5.6,

where the MCU ratio for the CKB0 pattern was relatively high. This is consistent with this pattern analysis because the $2 \times 2(2)$ group corresponds to the pattern of neighboring high nodes in the CKB0 pattern [see Fig. 3.1(b)].

In the $2 \times 2(3,4)$ and $3 \times 2(4,5,6)$ groups, on the other hand, the ratio for the negative muons was comparable to that for the high-energy neutrons. In particular, in the $3 \times 2(4,5,6)$ group, the ratio for the thermal neutrons was apparently lower than that for the negative muons and the high-energy neutrons. The common feature of the $2 \times 2(3,4)$ and $3 \times 2(4,5,6)$ groups is the non-linear shape of the fail bit patterns, which cannot be explained by linear ion tracks. The key point here is that this type of patterns increase with increasing the PBE contribution because the PBE is activated by well potential perturbation and multiple nodes in a same well can be simultaneously affected by the PBE, as discussed in Chap. 4. The observed ratios of these groups therefore indicate that the PBE contribution is higher for the negative muons and the high-energy neutrons than for the thermal neutrons. This agrees with the discussion in the previous section, where the higher PBE contribution for the negative muons and the high-energy neutrons was indicated in the voltage dependence of the MCU ratio in Fig. 5.5.

From the above results, it is probable that, for the negative muons, the MCU characteristics is dominated by the nature of the muon capture reactions, where both the isotropic ion emission and the PBE triggered by high-LET ions are important factors. The high-energy neutrons do not possess the isotropic emission of the secondary ions. The thermal neutrons do not produce the secondary ions with LET enough for triggering the PBE. For these reasons, the MCU response to the negative muons is different from that to the high-energy neutrons and the thermal neutrons, as observed in this study.

A key insight from the comparison of the MCU characteristics is that mitigation techniques for the neutron-induced SEUs are also effective for the negative muon-induced ones. As mentioned in Sec. 1.3.3, ECCs are commonly used to reduce the neutron-induced SEUs in SRAM devices. The efficiency of the ECCs depends on the MCU characteristics, where the high probability of MBU occurrence leads to degrade the ECC efficiency. In the MCU groups shown in Fig. 5.8, the groups of $1 \times 2(2)$, $2 \times 2(3,4)$, and $3 \times 2(4,5,6)$ correspond to the MBU events. As confirmed in Fig. 5.9, the ratios of these groups for the negative muons were comparable to those for the high-energy neutrons or the thermal neutrons. At the same time, the MCU ratio for the negative muons was intermediate between that for the high-energy neutrons and that for the thermal neutrons, as seen in Fig. 5.5. These results suggest that the ECC techniques can mitigate the negative muon-induced SEUs to a similar extent as the neutron-induced SEUs.

5.4 Conclusion

In this chapter, the muon irradiation experiments have demonstrated the SEU, MCU, and MBU responses to the negative and positive muons in the 20-nm bulk planar SRAMs. The similarities and differences in these characteristics between the muons and the other terrestrial radiations have been revealed through the comparative analyses with the high-energy neutron, thermal neutron, and alpha particle irradiations, where the capture reactions of the negative muons have been found to particularly affect the MCU characteristics.

The negative and positive muon irradiation experiments have been performed by using the monoenergetic muon beam. The SEU, MCU, and MBU CSs have been evaluated with varying the energy. The muon energy dependence of the CSs has clearly confirmed the Bragg peak effect for both the negative and positive muons and the significant contribution of the muon capture reactions to the MCU CS for the negative muons, as similarly reported in the previous studies. It has been found that the positive muons induce the MCU events in the 20-nm planar SRAMs, whereas no MCU events were observed in the previous studies of the 65-nm and 28-nm planar SRAMs. This difference has been attributed to the scaling of the SRAM cells, which suggests that the positive muon-induced MCUs may increase in more scaled devices. The CSs for the muons have been compared with those for the high-energy neutrons, the thermal neutrons, and the alpha particles. On the basis of the empirical relation between the SEU CS and the charge collection, the similarities and differences in the voltage dependence of the SEU CS among the particles have been explained by the contributing secondary ions and their LETs. The comparative analyses of the MCU ratio and the fail bit patterns among the particles have revealed that both the PBE and the isotropic emission of the secondary ions have an important role for the characteristics of the negative muon-induced MCUs.

In conclusion, this study has demonstrated that the SEU and MCU responses to the negative and positive muons are essentially different from that to the other terrestrial radiations: the high-energy neutrons, the thermal neutrons, and the alpha particles. In particular, this study has determined that the unique nature of the muon capture reactions, i.e., the high-LET ion production and the isotropic ion emission, differentiates the MCU characteristics for the negative muons from that for the high-energy neutrons and the thermal neutrons. Furthermore, the detailed comparison of the MCU characteristics has suggested that the ECC technique used to mitigate the neutron-induced SEUs are also an effective strategy to mitigate the muon-induced SEUs.

Chapter 6

Conclusion

This thesis has provided a comprehensive and insightful understanding of the terrestrial radiation-induced SEUs in the advanced planar and FinFET SRAMs through a variety of studies based on irradiation experiments. The particle irradiation experiments have been successfully performed for all the terrestrial radiations that are considered as sources of the SEUs, i.e., high-energy neutrons, thermal neutrons, negative muons, positive muons, and alpha particles. Furthermore, the laser irradiation experiments have been conducted to explore the unknown mechanism.

The studies in this thesis have focused on the impact of technology advances of SRAM devices on the SEU responses, where the key factors addressed have included size scaling, critical charge reduction, and transistor geometry change. In particular, the studies have thoroughly investigated the complex MCU mechanism, the sensitivity to neutron incidence angles, and the susceptibility to negative and positive muons. Each investigation has yielded new knowledge and valuable insights into the SEU and MCU responses of advanced SRAM devices, which are associated with the above factors.

6.1 Findings and Contributions

The studies have started with the exploration of the MCU mechanism complicated by the scaling of SRAM cells. In this exploration, the single-pulse TPA laser irradiations have been performed in the 20-nm bulk planar SRAMs. By leveraging the capability of the laser technique in controlling the position and amount of charge deposition, the MCU responses to multiple-cell charge deposition have been investigated in terms of the number and spatial pattern of fail bits. The detailed FBM analyses have unveiled the anomalous dependence of fail bit patterns on data patterns, where their spatial topologies have been found to be significantly different between the All1 and CKB0 patterns. On the basis of this topological difference, this study has identified the novel MCU mechanism originating from the imbalance of PBE strength among multiple wells, which has been named as MWCPU. The validity of the MWCPU mechanism has been confirmed through the multiple single-pulse laser irradiations, where the observed MCU responses have indicated that the MWCPU

mechanism dominates the transitions of internal node voltages under multiple-cell charge deposition.

With the new understanding of the MCU mechanism, the angular sensitivity of high-energy neutron-induced SEUs has been studied in the 20-nm planar SRAMs. In this study, the high-energy neutron irradiations have been performed at several incidence angles by using the atmospheric-like neutron source. The evaluation of the SEU, MCU, and MBU rates has demonstrated that the MBU rate considerably increases when the incidence direction is parallel to the WL direction (at grazing incidence), although the SEU rate decreases with increasing the incidence angle. The thorough analyses of MCU events have showed that the angular dependence of MCU characteristics is attributed to the interplay of the forward-emission of secondary ions, the rectangular shape of SRAM cells, and the PBEs in p-wells. This complex interplay has been found to result in the increased MBU rate at grazing incidence. Furthermore, the fail bit patterns at grazing incidence have exhibited the unique dependence of gap occurrence on data patterns. Through the detailed FBM analyses, this data pattern-dependent gap occurrence has been found to be caused by the MWCPU mechanism, where the grazing incidence of high-energy neutrons can increase the events of multiple-cell charge deposition.

The angular sensitivity of high-energy neutron-induced SEUs has also been studied in the 12-nm FinFET SRAMs, and the impact of structural change from planar FETs to FinFETs has been investigated. In this study, the high-energy neutron irradiations have been performed in the same way as the above study in the 20-nm planar SRAMs. The comparison of the SEU, MCU, and MBU rates between the 12-nm FinFET and 20-nm planar SRAMs has demonstrated that, similarly to the 20-nm planar SRAMs, the MBU rate increases when the incidence direction is parallel to the WL direction in the 12-nm FinFET SRAMs. At the same time, the MCU response has been found to be different between the 12-nm FinFET and 20-nm planar SRAMs. The analyses of MCU ratios have revealed that this different response originates from the different contribution of PBEs, where the PBE contribution is less significant for the 12-nm FinFET SRAMs owing to their fin structures. Moreover, unlike the PBEs in the 20-nm planar SRAMs, the PBE contribution in the 12-nm FinFET SRAMs was observed to be dependent on the incidence angles of high-energy neutrons. This angle-dependent PBE contribution has also been indicated by the analyses of the voltage dependence of pattern-wise MCU ratios.

The last part of this thesis has studied the muon-induced SEUs with comparison to the SEUs induced by the other terrestrial radiations: high-energy neutrons, thermal neutrons, and alpha particles. In this study, the negative and positive muon irradiations have been performed in the 20-nm planar SRAMs by using the monoenergetic muon source. The comparison of the SBU and MCU CSs between the negative and positive muons has confirmed the significant contribution of muon capture

TABLE 6.1: Contributions of This Thesis.

Understanding of SEU	**Previous studies**	**Studies in this thesis**
MCU mechanism based on well potential perturbation	Potential perturbation in a *single* well (MCBI, WCSI)	Potential perturbation in *multiple* wells (MWCPU)
Angular sensitivity for high-energy neutrons	$\geq$65-nm planar SRAM	20-nm planar SRAM, 12-nm FinFET SRAM
Negative muon susceptibility	$\geq$28-nm planar SRAM	20-nm planar SRAM
Comparison among all terrestrial radiations	No study	20-nm planar SRAM

reactions on the MCUs for the negative muons. This study has found that the positive muons cause MCU events, indicating the possible increase in the positive muon-induce MCUs in more scaled SRAMs. On the basis of the empirical relation between the SEU CS and the charge collection, the similarities and differences observed in the voltage dependence of the SEU CS among the particles have been understood by the contributing secondary ions and their LETs. The comparative analyses of MCU ratio and fail bit patterns have revealed that the characteristics of the negative muon-induce MCUs are different from that of the neutron-induced MCUs due to the unique nature of the capture reactions, i.e., the isotropic emission of secondary ions and the high-LET ion production.

The major contributions of this thesis are summarized in Table. 6.1. For the MCU mechanism, the conventional mechanisms, such as MCBI and WCSI, considered well potential perturbation in a single well. In contrast, this thesis has considered the perturbation in multiple wells and has identified the MWCPU mechanism. For the angular sensitivity of high-energy neutron-induced SEUs, this thesis has clarified that in the 20-nm planar and 12-nm FinFET SRAMs, which are significantly advanced compared to the SRAMs in previous studies. Similarly, for the muon susceptibility, this thesis has demonstrated the negative muon-induced SEUs in the scaled 20-nm planar SRAMs. More important, this thesis has revealed, for the first time, similarities and differences in the SEU responses among all the terrestrial radiations: high-energy neutrons, thermal neutrons, negative muons, positive muons, and alpha particles. As a result, this thesis has achieved meaningful progress in understanding the terrestrial radiation-induced SEUs in advanced SRAM devices. At the same time, this thesis has established a baseline for future studies addressing further advanced devices or other radiations. In such future studies, comparative investigations based on the results presented in this thesis will provide valuable insights to resolve the questions raised there.

6.2 Suggestions for SEU Mitigation

The findings in this thesis are important not only for understanding SEU phenomena, but also for developing effective mitigation strategies. On the basis of the obtained results, some suggestions can be provided for SEU mitigation.

The study on the angular sensitivity for high-energy neutron-induced SEUs has yielded the useful insight that the MBU rate increases when the SRAM devices are mounted with their WL directions being vertical to the ground for both the planar and FinFET SRAMs. From this insight, the efficiency of ECCs can be maximized by avoiding such mounting configurations. From a practical point of view, several SRAM blocks are usually implemented in a chip. Moreover, multiple chips can be assembled on a circuit board. In such cases, an ideal strategy is to align the WL directions of the SRAM blocks, i.e., co-designing. This type of co-design, however, may be difficult due to layout restrictions, and hence the WLs of each SRAM block can be oriented to different directions. Nevertheless, risk analyses based on the usage and capacity of each SRAM block could determine the SRAM block that should be protected with priority. In this case, one effective strategy is to avoid its WL direction being vertical to the ground.

The study on the muon-induced SEUs have demonstrated that the probability of MBU events induced by the negative muons is comparable to that induced by the high-energy and thermal neutrons for the planar SRAMs. This result suggests that the ECC techniques for the neutron-induced SEUs are capable of mitigating the muon-induced SEUs. It is worthy of note here that, in this comparison, the incidence direction of the high-energy neutrons has been normal to the SRAM chip. As demonstrated in the study on the angular sensitivity, the high-energy neutron-induced MBUs increase when the incidence direction is parallel to the WL direction. In contrast, the negative muon- and thermal neutron-induced MBUs are probably independent of the incidence direction because of the isotropic emission of secondary ions. This means that the MBU probability can become higher for the high-energy neutrons than for the thermal neutrons and the negative muons when the SRAM chips are vertically mounted with the WLs perpendicular to the ground. In this case, the ECC strategy should focus more on the characteristics of the high-energy neutron-induced MBUs.

Another key characteristics for mitigation strategies are the data pattern dependence of MCU occurrence. In the studies on the high-energy neutron-induced SEUs and the muon-induced SEUs, the two data patterns, All0 and CKB0, have been used, and the MCU characteristics have been compared between the All0 and CKB0 patterns. This comparison has demonstrated that the probabilities of MCU and MBU events are considerably smaller for the CKB0 pattern than for the All0 pattern in both the planar and FinFET SRAMs. The important point here is that the reason for this data pattern dependence is the difference in the physical arrangement of high nodes of nMOS transistors. Here, the MCU probability increases when the high nodes are

densely adjacent to each other, which corresponds to the case of the All0 pattern. This understanding strongly suggests that the non-dense arrangement of the high nodes can suppress the MCU occurrence. To achieve this configuration, appropriate randomization techniques for write data could be utilized.

These suggestions will be helpful to establish the reliability of future SRAM devices and hence the dependability of future electronic systems in which the high robustness to the terrestrial radiations should be demanded.

6.3 Future Directions

Although this thesis has advanced the understanding of the terrestrial radiation-induced SEUs in the scaled planar and FinFET SRAMs, there are still unresolved issues mainly concerning the FinFET SRAMs.

In the study on the MCU mechanism, the MWCPU mechanism has been identified in the 20-nm planar SRAMs, whereas the MWCPU mechanism has not been examined in the FinFET SRAMs. Since this mechanism is based on the PBEs, the different contribution of the PBEs can result in the difference in the significance of the MWCPU mechanism. As demonstrated in the study on the angular sensitivity of high-energy neutron-induced SEUs, the PBE contribution is larger for the 20-nm planar SRAMs than for the 12-nm FinFET SRAMs. This can lead to the suppression of the MWCPU mechanism in the 12-nm FinFET SRAMs. In contrast, the size scaling of SRAM cells in FinFET technologies increases the probability of charge deposition on multiple wells, which can lead to the enhancement of the MWCPU mechanism. Therefore, the significance of the MWCPU mechanism in the FinFET SRAMs could be determined by the competition between the PBEs and the size scaling. The future work on this point will provide new understanding of the MCUs in the FinFET SRAMs.

Similarly, the study on the muon-induced SEUs has dealt only with the 20-nm planar SRAMs. On the analogy of the results of the high-energy neutron-induced SEUs, the negative and positive muon-induced SEUs can be considerably decreased in the FinFET SRAMs. However, at the same time, the difference in the PBE contribution between the planar and FinFET SRAMs could lead to the different MCU characteristics because, in the study on the muon-induced SEUs, the characteristics of the negative muon-induced MCUs have indicated the impact of the PBEs in the 20-nm planar SRAMs. Moreover, the continuous reduction in critical charge increases the susceptibility to the direct ionization of the muons. Therefore, it will be valuable to investigate the muon-induced SEUs in the FinFET SRAMs in the future.

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