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Study of SiO_2/4H-SiC interface nitridation by post-oxidation annealing in pure nitrogen gas

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An alternative and effective method to perform interface nitridation for 4H-SiC metal-oxide-semiconductor (MOS) devices was developed. We found that the high-temperature post-oxidation annealing (POA) in N_2 ambient was beneficial to incorporate a sufficient amount of nitrogen atoms directly into thermal SiO_2/SiC interfaces. Although N_2-POA was ineffective for samples with thick thermal oxide layers, interface nitridation using N_2-POA was achieved under certain conditions, i.e., thin SiO_2 layers (< 15 nm) and high annealing temperatures (> 1350°C). Electrical characterizations of SiC-MOS capacitors treated with high-temperature N_2-POA revealed the same evidence of slow trap passivation and fast trap generation that occurred in NO-treated devices fabricated with the optimized nitridation conditions. [http://dx.doi.org/10.1063/1.4930980]

Traditional power devices have suffered from performance limits due to the physical properties of silicon (Si). Hence, silicon carbide (SiC) has been a promising semiconductor for developing next-generation power devices.[1] SiC provides silicon dioxide (SiO_2) by thermal oxidation as a gate insulator in metal-oxide-semiconductor field-effect-transistors (MOSFETs), which is similar to Si-MOS technology. However, the channel mobility of SiC-MOSFETs ordinarily deteriorates because of several miscellaneous defects in the thermal SiO_2 and at SiO_2/SiC interfaces notwithstanding the conclusive physical understandings.[2] Some standard procedures were employed to minimize the defect density by passivating electrical defects with particular atomic species, e.g., hydrogen,[3,4] nitrogen,[5–10] and phosphorus.[11] The interface state density (D_{it}) was markedly reduced below 10^{12} cm^{-2} eV^{-1} near the conduction band edge by using post-oxidation annealing (POA) in reactive nitrogen-containing gases, i.e., nitric oxide (NO),[5] nitrous oxide (N_2O),[6] and ammonia (NH_3).[7] The reduction of D_{it} is thought to be closely related to the quantity of piled-up nitrogen atoms at the SiO_2/SiC interfaces.[8–10] Recently, NO has become the main species responsible for interface nitridation of mass-produced SiC-MOSFETs despite its toxicity. The most effective NO-POA is, however, limited to the annealing temperature of 1250°C,[9] because NO molecules may dissociate at temperatures higher than 1300°C.[12]

Other than performing post-oxidation nitridation for SiO_2/SiC structures, Shirasawa *et al.* proposed a method to passivate bare 6H-SiC surfaces with nitrogen atoms by applying high-temperature annealing in high-purity (N_2) nitrogen gas.[13] They demonstrated the formation of atomically thin silicon nitride (SiN) layers on SiC surfaces by N_2 annealing at 1350°C for 30 min as the optimal condition. The SiN layers containing high-density nitrogen atoms bonding with Si atoms on the SiC surfaces were well recognized based on physical analyses done using scanning tunneling microscopy (STM),[13] low-energy electron diffraction (LEED),[13] x-ray diffraction (XRD),[14] and photoemission spectroscopy (PES).[15,16] It is suggested that the nitrided SiC surfaces may be suitable for making SiC-MOSFETs with deposition of gate insulators.[17] However, the interface quality

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improvement in MOS devices with SiO_2 deposited on the nitride surface is not sufficient compared with the NO-treated devices, probably because of unintentional reactions between the atomically thin nitride layers and the growing SiO_2 film.

In this study, we systematically investigated the interface nitridation by POA in pure N_2 ambient for 4H-SiC substrates containing thermally grown oxides (SiO_2/SiC). The incorporation of nitrogen atoms into SiO_2/SiC interfaces was demonstrated by physically characterizing the interfaces using x-ray photoelectron spectroscopy (XPS). We report the threshold requirements including the proper oxide thicknesses and annealing temperatures that facilitate interface nitridation by N_2-POA. Next, the electrical properties of MOS devices were connected to reveal the correlation between the amount of nitrogen and the defect states at SiO_2/SiC interfaces.

The samples used in this study were fabricated on 4°-off-axis 4H-SiC(0001) Si-face substrates with epitaxially grown *n*-type layers ($N_d = 1 \times 10^{16}$ cm^{-3}). Piranha ($H_2SO_4 + H_2O_2$) and standard RCA cleanings were done to prepare non-contaminated wafers before the high-temperature processes. Then, sacrificial oxides were formed on the SiC wafers by dry oxidation at 1100°C for 1 h inside a quartz furnace tube. The sacrificial oxide layers were subsequently removed by dipping into 5% HF solution. Next, the samples were oxidized using the same furnace tube at 1150°C to obtain thin and thick thermal SiO_2 layers ranging from approximately 3 to 40 nm by changing the oxidation time. SiO_2/SiC samples were then subjected to identical POA at 1350°C for 30 min in N_2 ambient, in reference to the typical nitridation conditions for 6H-SiC surfaces using pure N_2 gas.[13–16] Note that vacuum pumping was conducted to remove the ambient gas inside the annealing furnace before introducing high-purity N_2 gas (99.9999%). The oxide thicknesses were then confirmed using ellipsometry. The SiO_2/SiC structures after N_2-POA were analyzed by using XPS. In order to observe the chemical states near/at the SiO_2/SiC interfaces, the SiO_2 layers were thinned down by wet etching in diluted HF (1%) solution prior to XPS measurement. The monochromatic Al Kα line (1486.6 eV) was used to acquire core-level spectra of Si 2p and N 1s. The photoelectron take-off angle (TOA) was normal to the sample surfaces (90°).

Figure 1 shows the Si 2p and N 1s core-level spectra taken from N_2-POA treated SiO_2/SiC samples with varying oxide thicknesses (3–40 nm). After performing identical N_2-POA at 1350°C for 30 min, the oxide layers were partially (thinner than 1.5 nm) or fully etched back before XPS measurement. To compare the XPS spectra, the spectral intensity was normalized by the peak intensity of Si 2p core-level spectra at a binding energy (BE) of 101.8 eV, which is the Si-C bond (Si^{0+}) signal arising from bulk SiC substrates. We observed the chemical shift components in the Si 2p spectra at a higher BE of about 104.5 eV that was attributable to the Si-O bonds (Si^{4+}) of the remaining oxides (see Fig. 1(a)). The results from the 4H-SiC wafer without thermal oxide (0 nm) annealed in N_2 gas in the same conditions are also shown in Figs. 1(a) and 1(b). The N 1s peak at 398.1 eV indicates nitridation of the SiC surface. As for the 40-nm-thick SiO_2/SiC structure, no nitrogen signal was detected from the oxide interface, as shown in Fig. 1(b). This is simply explained by poor reactivity and low diffusivity of N_2 in the SiO_2 network.[18] In contrast, we observed notable nitrogen content when the initial oxide thickness was less than 15 nm. It should be noted that the peak intensity and the BE position of N 1s core-level spectra changed insignificantly following oxide etching, indicating that the Si-N network was formed at SiO_2/SiC interfaces by high-temperature N_2-POA. Moreover, this nitrided interlayer was hard to remove using the HF solution, which is similar to the results in some previous studies on NO-POA.[8,10] These results imply that nitrogen atoms can be incorporated into the SiO_2/SiC interfaces by conventional N_2-POA when choosing appropriately thin SiO_2 layers.

In order to understand the dependence of interface nitridation on the temperature by N_2-POA, we examined another set of samples subjected to N_2-POA with different annealing temperatures. Nearly identical 15-nm-thick thermal oxide layers were grown on clean 4H-SiC wafers by dry oxidation at 1150°C for 90 min. After that, the SiO_2/SiC samples were treated with N_2-POA at different temperatures ranging from 1300–1400°C for 30 min. The N 1s core-level spectra of the samples after completely removing the SiO_2 layers are shown in Fig. 2. The photoelectron spectra were likewise normalized by the peak signals in Si 2p core-level spectra (data not shown). We found that the N_2-POA at 1300°C was ineffective to cause interface nitridation, and that, the annealing temperature at 1350°C seems to be the fundamental requirement that facilitates interface nitridation

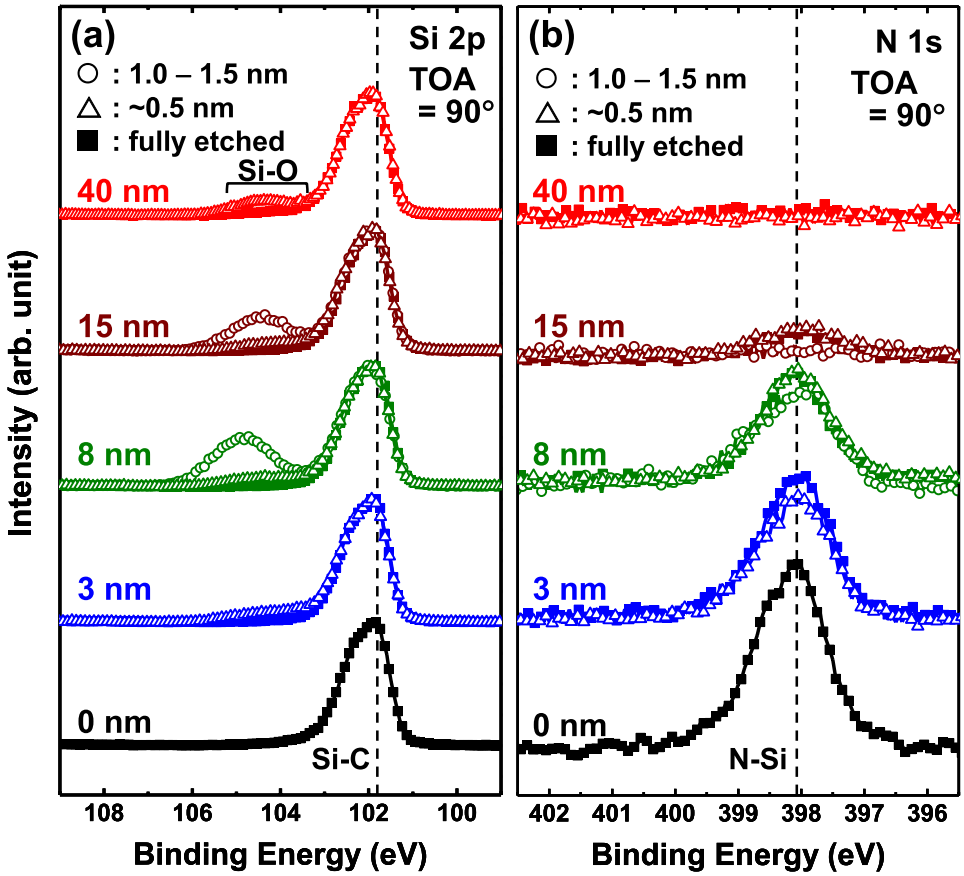

FIG. 1. Change in core-level spectra of (a) Si 2p and (b) N 1s obtained from N_2-POA treated SiO_2/SiC(0001) while varying the initial oxide thickness from 3 to 40 nm. Results from the bare SiC surface without oxide (0 nm) are also shown for comparison. After all samples were annealed in high-purity N_2 at 1350°C for 30 min, the oxides were partially etched to a thickness of about 1.0–1.5 nm (open circles) or thinner than 0.5 nm (open triangles), and entirely etched (filled squares) prior to the XPS measurement. The XPS spectra were normalized by the Si 2p component from SiC substrate (Si–C bond).

by pure N_2 annealing. It is probably difficult for stable nitrogen molecules to react at the interfaces under the inadequate annealing temperatures below 1350°C. Moreover, the N 1s peak intensities taken from the samples with N_2-POA at 1400°C increased considerably.

Next, we summarized the amounts of the nitrogen content at the SiO_2/SiC interfaces in terms of the intensity ratio between the N-Si bond and the SiC bulk signals ($I_{N\ 1s}/I_{Si\ 2p}$) after completely removing the SiO_2. Figure 3 plots the $I_{N\ 1s}/I_{Si\ 2p}$ ratios as a function of the initial oxide thickness (Fig. 3(a)) and the annealing temperature of N_2-POA (Fig. 3(b)). We found that the amount of interface nitrogen decreased as the oxide thickness increased. When nitric oxide (NO) is used for POA, interface nitridation can be achieved even for thick oxide samples at 1250°C. A typical nitrogen intensity ratio for the 75-nm-thick SiO_2/SiC samples treated with the optimized NO-POA conditions (at 1250°C for 90 min)[10] is indicated by the dashed line in Fig. 3. It is clear that despite the poor reactivity of N_2, the N_2-POA allows us to incorporate a larger amount of nitrogen atoms than the NO-POA, particularly for thin oxide samples (< 15 nm). Figure 3(b) illustrates the conclusive results for N_2-POA when the annealing temperatures were varied for samples with an identical initial oxide thickness of about 15 nm. The annealing temperature below 1350°C could not incorporate any notable amount of nitrogen atoms, as stated previously (see Fig. 2). However, a remarkable amount of nitrogen content was observed for the samples with N_2-POA at 1350°C, and is close to the amount with NO-POA at 1250°C. Furthermore, compared with the NO-POA, the N_2-POA at 1400°C was very promising for incorporating approximately twofold amounts of nitrogen atoms at the SiO_2/SiC interface. It must be remarked for the NO-POA that the nitrogen density

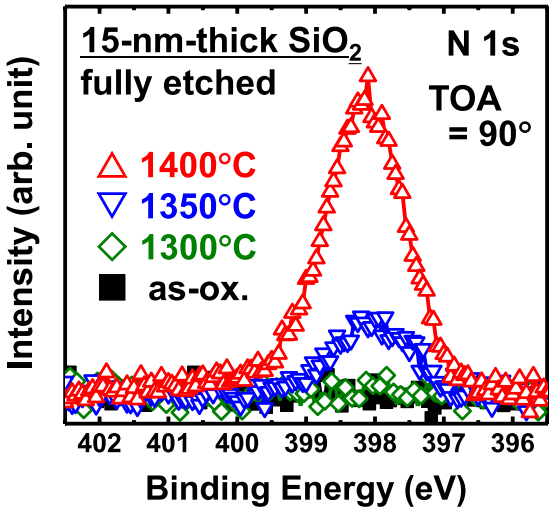

FIG. 2. Change in the N 1s core-level spectra obtained from the N_2-POA treated SiC samples with 15-nm-thick thermal SiO_2 layers after complete SiO_2 removal. The POA in pure N_2 ambient was done for 30 min at different temperatures, i.e. 1400°C (upward red triangles), 1350°C (downward blue triangles), and 1300°C (green rhombuses). The as-oxidized SiO_2/SiC sample without post annealing (black filled squares: as-ox.) is also shown for comparison. Peak intensity was normalized by the Si 2p peak intensities (not shown).

at SiO_2/4H-SiC decreases at annealing temperatures higher than 1300°C because NO molecules begin to dissociate into N_2 and O_2.[12] Active oxidation causing oxide etching should be a concern when a small amount of O_2 mixtures exist in an annealing furnace during NO-POA.[19] In this work, we also observed oxide etching even for N_2-POA samples with annealing temperatures higher than 1420°C, probably due to active oxidation by a very small amount of residual oxygen in an annealing apparatus.

To provide insight into the electrical characteristics of SiC-MOS devices, we fabricated SiC-MOS capacitors by depositing circular Al gate electrodes (200 μm diameter) and back contacts.

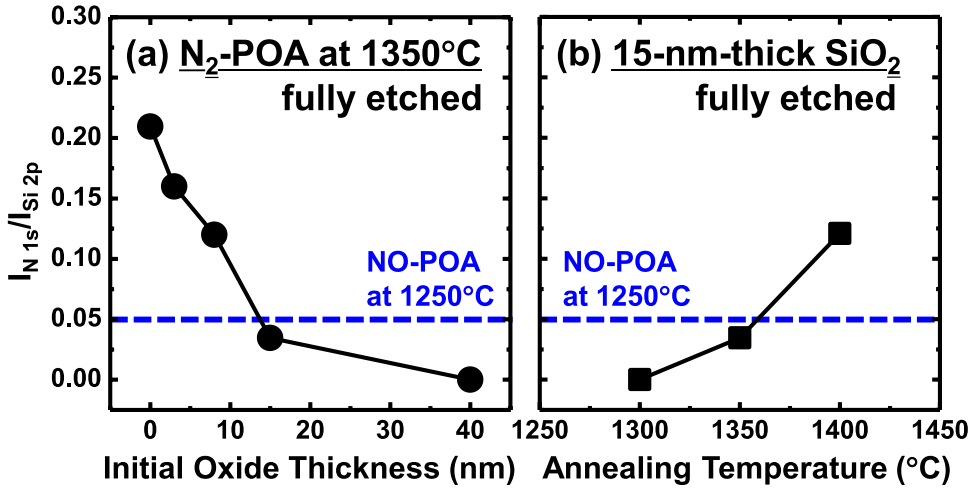

FIG. 3. (a) Change in ratios between peak intensities of N 1s and Si 2p spectra ($I_{N\ 1s}/I_{Si\ 2p}$) of SiO_2/SiC samples plotted as a function of the initial oxide thickness ranging from 3 to 40 nm (see Fig. 1). The N_2-POA was performed at 1350°C for 30 min. (b) Change in $I_{N\ 1s}/I_{Si\ 2p}$ ratios of the 15-nm-thick SiO_2/SiC samples by varying the annealing temperature in the range from 1300 to 1400°C (see Fig. 2). A typical peak intensity ratio for 75-nm-thick SiO_2/SiC samples receiving NO-POA at 1250°C, which was optimized from the peak carrier mobility of SiC-MOSFETs,[10] is also shown for comparison (blue dashed horizontal line). All samples were subjected to HF etching to completely remove oxide layers before XPS measurement.

Capacitors with identical 15-nm-thick oxides and subjected to N_2-POA at 1300, 1350, and 1400°C were chosen in order to characterize their capacitance-voltage (C–V) curves in comparison with the capacitor without nitridation (as-ox.). Figure 4(a) represents bidirectional C-V curves measured at 1 MHz while gate voltages were swept forward from depletion (−5 V) to accumulation (+5 V), and then backward to depletion. The positively shifted flatband voltage (V_{FB}) of about 0.69 V in the as-ox. sample compared with the ideal position (V_{FB} = 0.43 V) indicates negative fixed charges in the SiO_2/SiC structure after dry oxidation of SiC substrates. Moreover, the as-ox. sample clearly showed C–V hysteresis with clockwise direction (ΔV_{FB} = 0.14 V) due to the electron injection from the substrate into defects at as-oxidized SiO_2/SiC interfaces. It is clear that high-temperature N_2-POA over 1300°C effectively suppressed the C–V hysteresis. Furthermore, we also found that the C–V curve of the capacitor with N_2-POA at 1300°C still exhibited a stretched-out shape, which is similar to the earlier report on N_2-POA at 1110°C.[20] Since N_2-POA at moderate temperatures does not cause interface nitridation, only a slight improvment in the SiO_2/SiC interface quality was obtained. In contrast, the capacitors treated at 1350 and 1400°C showed steeper C–V slopes, indicating improved interface quality. It is generally known that unusual slow traps are found at

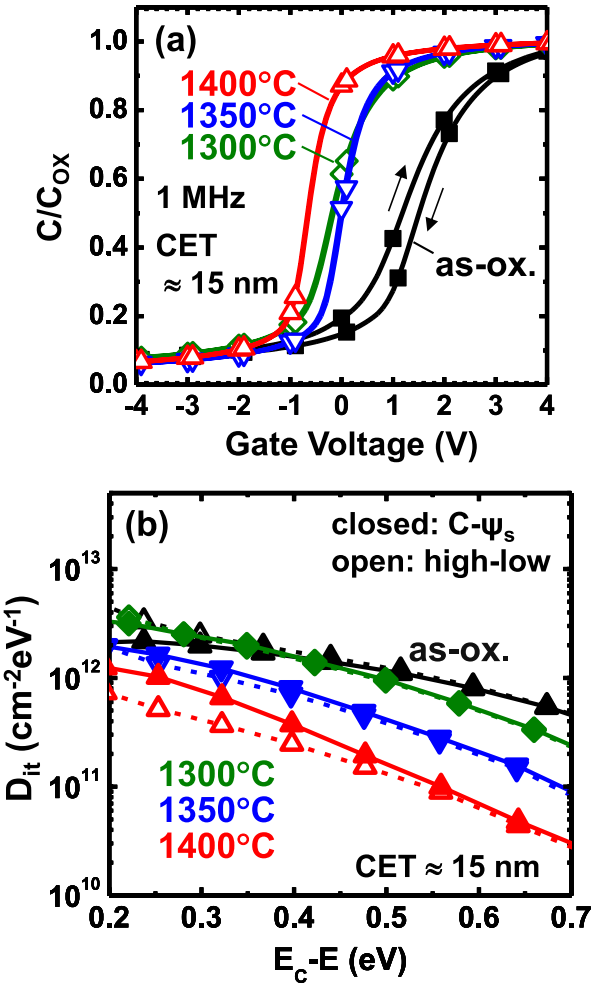

FIG. 4. (a) Bidirectional high-frequency (1 MHz) C–v curves of SiC-MOS capacitors obtained by biasing gate voltages from depletion (−5 V) to accumulation (+5 V), and vice versa. The capacitors with N_2-POA at 1300 (green rhombuses), 1350 (downward blue triangles), and 1400°C (upward red triangles); and without POA (black filled squares: as-ox.) were examined. The capacitance values were normalized by the maximum capacitance (C_{OX}). The capacitance equivalent thicknesses (CETs) were about 15 nm for all capacitors. (b) Energy distributions of D_{it} estimated from high-low (open symbols) and the C–ψ_S method (closed symbols).[23]

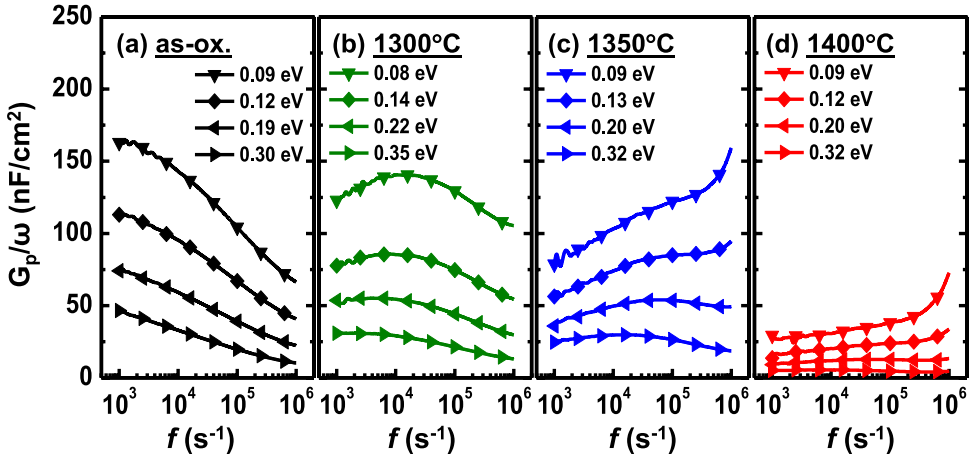

FIG. 5. G_p/ω versus f curves obtained from SiC-MOS capacitors (a) without post-annealing (as-ox.) and with N_2-POA at (b) 1300, (c) 1350, and (d) 1400°C. As indicated in the figures, the energy levels were varied near the conduction band edge (0.08 eV ≤ E_C-E ≤ 0.35 eV). To generate the conductance curves, the probe oscillation was swept from 1 kHz to 1 MHz under constant surface potentials. The measurement was conducted at room temperature.

as-oxidized SiO_2/SiC interfaces. These slow traps make it difficult to emit carriers from the interfaces that end up with voltage shifts, causing the stretched-out C–V shape. Interface nitridation by NO-POA is the most common approach to passivate the slow traps at SiO_2/SiC interfaces.[9,10,21,22] It should be noted that similarly to the NO-POA, the well-behaved C–V curves were obtained by incorporating nitrogen with N_2-POA over 1350°C. Figure 4(b) represents the energy distribution of D_{it} for SiO_2/SiC structures estimated by the conventional high-low method, and the recently proposed C–ψ_S method[23] that captures entire traps, including fast traps at shallow energy levels. It was found that both methods showed a reduced D_{it} with an increase in N_2-POA temperatures. Interestingly, the D_{it} value for N_2-POA at 1400°C was significantly reduced to below 10^{11} cm^{-2} eV^{-1} at deep energy levels ($E_C - E > 0.5$ eV). However, the magnitude of D_{it} reduction at shallow energy levels ($E_C - E < 0.5$ eV) estimated using the C–ψ_S method was not very significant compared with that estimated using the high-low method. On the basis of the D_{it} discrepancy between the high-low and C–ψ_S methods, the results shown in Fig. 4(b) suggest the presence of fast interface traps caused by the high-temperature N_2-POA.

We further examined conductance characteristics of the same sample set to understand the interface trap behaviors. Figure 5 illustrates conductance (G_p/ω) curves plotted as a function of probe oscillation (f) for the shallow energy levels (0.08 eV ≤ E_C-E ≤ 0.35 eV). The conductance curves acquired at room temperature were normalized by the gate area in order to unbiasedly compare the trap density. As shown in Fig. 5(a), the conductance peaks of the as-ox. sample mainly appear at frequencies less than 1 kHz. This coincides well with the presence of interface states with long time constants demonstrated by the remarkable stretching-out of the C-V curve in Fig. 4(a). As shown in Figs. 5(b)-5(d), the peak intensity of slow traps apparently decreased after N_2-POA, as expected from the D_{it} reduction in Fig. 4(b). The N_2-POA at 1400°C was the most advantageous to eliminate the conductance signals attributable to the slow traps (Fig. 5(d)), thus improving interface quality. However, we noticed that parts of the conductance signals increased at very high frequencies (f > 1 MHz). We think that these signals are associated with the fast traps at SiO_2/SiC due to nitridation, similar to previous reports on NO-POA.[9] The fast trap signals began to appear when the annealing temperature was higher than 1350°C (Fig 5(c)), which agrees well with the threshold condition for interface nitridation by N_2-POA.

In summary, we demonstrated an alternative method to effectively incorporate nitrogen atoms into the SiO_2/SiC interface by high-temperature POA in pure N_2 ambient. It was revealed that nitridation of the interface is achievable similarly to the case with a bare SiC surface following N_2 annealing at 1350°C. These nitrided structures were not chemically reactive to the HF wet etching. We also affirmed that the essential requirements for achieving interface nitridation under

pure N_2 ambient were a suitable initial oxide thickness (less than 15 nm) and a sufficient thermal budget (higher than 1350°C). The interface nitridation was likely to be enhanced by increasing the annealing temperature. The electrical properties of the SiC-MOS devices were examined and found to have benefits of N_2-POA that were analogous to the previous reports on NO-POA. Although a certain amount of fast states were generated at the SiO_2/SiC interfaces, just as with the conventional NO-POA, the proposed N_2-POA was found to be beneficial for incorporating a larger amount of nitrogen atoms and passivating dominant slow traps at the interface even under the harmless conditions.

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