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Excellent electrical properties of $TiO_2/HfSiO/SiO_2$ layered higher-*k* gate dielectrics with sub-1 nm equivalent oxide thickness

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Equivalent oxide thickness (EOT) scaling, as well as improved interface properties, of metal/higher-*k* gate stacks for the sub-1 nm region was achieved using a $TiO_2/HfSiO/SiO_2$ layered dielectric structure. Ti diffusion into the bottom oxides was found to form electrical defects, which lead to an increase of leakage current, fixed charge, interface trap density (D_{it}), and reliability degradation of the gate stacks. By controlling Ti diffusion and terminating Ti-induced defects using forming gas annealing, we successfully obtained a superior interface property ($D_{it}=9.9\times10^{10}$ eV^{-1} cm^{-2}) and reduced gate leakage ($J_g=7.2\times10^{-2}$ A/cm^2) at the 0.71-nm-EOT region.
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As complimentary metal-oxide-semiconductor (CMOS) devices are aggressively scaled, various high permittivity (high-*k*) gate dielectrics are being intensely studied as alternatives of conventional SiO_2 dielectrics. It has been reported that Hf-silicate (HfSiO), has good electrical properties and the stacked structure with SiO_2 underlayers improves interface properties with Si substrates.[1] However, for future CMOS devices, more sophisticated gate stacks of the sub-1 nm equivalent oxide thickness (EOT) region is required. Although EOT scaling can be achieved by simply reducing the physical thickness of SiO_2 underlayers or by high-*k*/Si direct contact, deterioration of the interface properties that causes degradations in carrier mobility and reliability of MOS devices is inevitable, especially for the sub-1 nm EOT region.[2] Thus, the development of noble-layered gate dielectrics, with higher permittivity (higher-*k*) oxides and thinner high-quality SiO_2 underlayers of a few angstroms thick, is indispensable for gaining scaling merits of CMOS devices.

The addition of Ti into the Hf-based oxides has been recently studied because Ti-based oxides exhibit an extremely high dielectric constant.[3–6] We have also investigated what the effects are of adding Ti into the Hf-based oxides and found that TiO_2 capping on the HfSiO dielectrics rather than HfTiSiO compound is preferable from the viewpoint of leakage current (J_g) reduction since the Ti-induced defects in the gate oxides create current leakage paths and lead to poor EOT-J_g characteristics.[7] By precisely controlling the Ti profile and reducing carbon contamination using a physical-vapor-deposition (PVD)-based *in situ* fabrication method, we demonstrated excellent EOT-J_g characteristics of the $TiO_2/HfSiO/SiO_2$ layered gate dielectrics. However, details of the interface quality and the effects of Ti diffusion to the bottom HfSiO and SiO_2 underlayers have not yet been clarified. In this study, we investigated the nature of Ti-induced defects by electrically measuring higher-*k* capacitors and by microscopic scanning capacitance microscopy (SCM) observations, and we demonstrated the use of forming gas annealing (FGA) for both terminating Ti-induced defects and improving EOT-J_g characteristics while also improving interface properties even for the sub-1 nm region.

We fabricated MOS capacitors with $TiO_2/HfSiO/SiO_2$ layered gate dielectrics using an *in situ* method with a cluster tool.[7–9] We formed 1.2- or 1.4-nm-thick SiO_2 underlayers on *p*-Si(100) substrates. A metal Hf layer (0.5 nm) was deposited on the SiO_2 underlayer with low-damage PVD equipment and annealed *in situ* to form a HfSiO layer by solid phase interface reaction between the metal Hf and the SiO_2 underlayer at 850 °C. We formed the TiO_2 capping layer by *in situ* oxidation of a 0.5-nm-thick Ti layer deposited on the HfSiO dielectric at 400–600 °C for 1 min. The TiN metal gate electrodes were then continuously deposited by reactive sputtering, and FGA treatment was carried out at 450 °C for 30 min (3% H_2 diluted by N_2). EOT-J_g characteristics of the gate stacks were determined from capacitance-voltage (*C*-*V*) and current-voltage (*I*-*V*) measurements by taking quantum mechanical effects into account.[10] Interface trap density (D_{it}) of the MOS devices was estimated by a conductance method. We also studied the local charge trapping properties of the $TiO_2/HfSiO/SiO_2$ layered gate dielectrics by using SCM and discussed the origins of the fixed charges and interface traps. Our SCM system with a self-sensing metal probe yielded simultaneous images of the surface topography and distance differential capacitance (dC/dZ), which revealed local static capacitance.[11]

The EOT-J_g characteristics of the $TiO_2/HfSiO/SiO_2$ layered dielectrics with TiN gate electrodes are summarized in Fig. 1. As we previously reported, the basic electrical properties of the gate stacks depend on both the SiO_2 underlayer thickness and Ti-oxidation temperature. Physical characterization using back-side x-ray photoelectron spectroscopy revealed that, while the EOT increase caused by high-temperature Ti-oxidation annealing is attributed to the interfacial oxide growth, the J_g increase is due to the formation of Ti-induced defects in the gate oxides. When Ti diffusion to the bottom oxides was suppressed by low-temperature oxidation at 400 °C and by utilizing thinner

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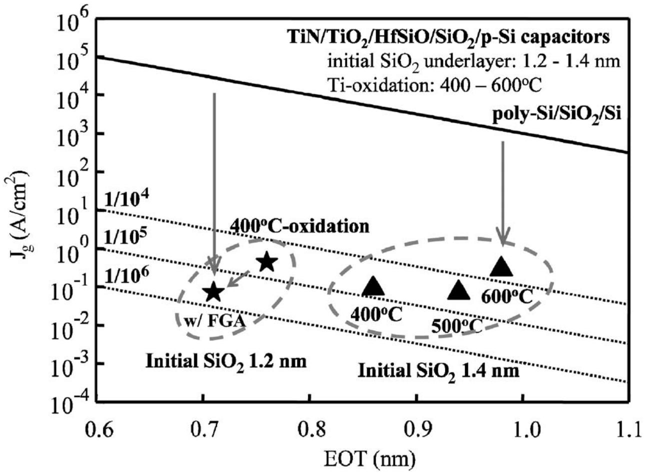

FIG. 1. EOT-J_g characteristics of $TiO_2/HfSiO/SiO_2$ layered dielectrics with TiN gate electrodes. The TiO_2 capping layers on the Hf-based oxides were fabricated by oxidation of 0.5-nm-thick metal Ti layers at various temperatures ranging from 400 to 600 °C. The leakage current was estimated at gate bias $V_g = V_{fb} - 1$ (V) and FGA treatment was carried out at 450 °C.

SiO_2 underlayers (1.2 nm), we could extend the trend of the leakage merit of four orders of magnitude to 0.76-nm-EOT. Moreover, FGA treatment was found to be very effective in further improving EOT-J_g characteristics, which is probably due to the film densification and termination of Ti-induced defects. Consequently, we successfully achieved thinner EOT (0.71 nm) and reduced J_g $(7.2\times10^{-2}\ \mathrm{A/cm^2})$ corresponding to the leakage merit of over five orders of magnitude compared to conventional poly-$Si/SiO_2/Si$ gate stacks.

Figure 2 shows typical *C-V* curves measured at 100 kHz with and without FGA treated capacitors indicated by star symbols in Fig. 1. Although frequency dispersion caused by the interface traps was observed before FGA treatment (dotted line), the FGA treatment apparently improved it, and a minimum D_{it} value of $9.9\times10^{10}\ \mathrm{eV^{-1}\,cm^{-2}}$ was realized. These results demonstrate the use of $TiO_2/HfSiO/SiO_2$ layered higher-*k* dielectrics combined with conventional FGA treatment for EOT scaling, J_g reduction, and superior interface properties even for the sub-1 nm EOT region.

To understand the effects of Ti diffusion and the role of the FGA treatment on higher-*k* dielectrics, we first focused on changes in the interface properties and fixed charges depending on the Ti-oxidation temperature. Figure 3 shows the

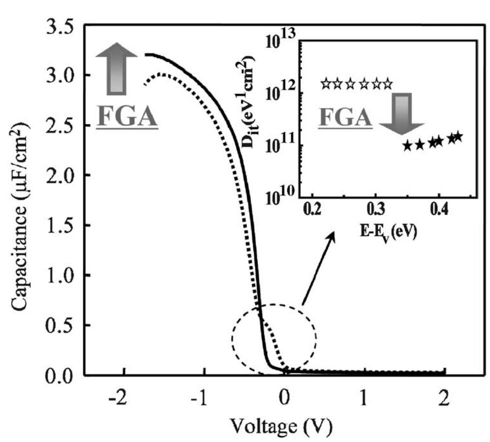

FIG. 2. Typical *C-V* curves of the $TiN/TiO_2/HfSiO/SiO_2/p$-Si capacitors with and without FGA treatment. The *C-V* measurement was performed at 100 kHz. The change in the D_{it} due to FGA treatment is also shown.

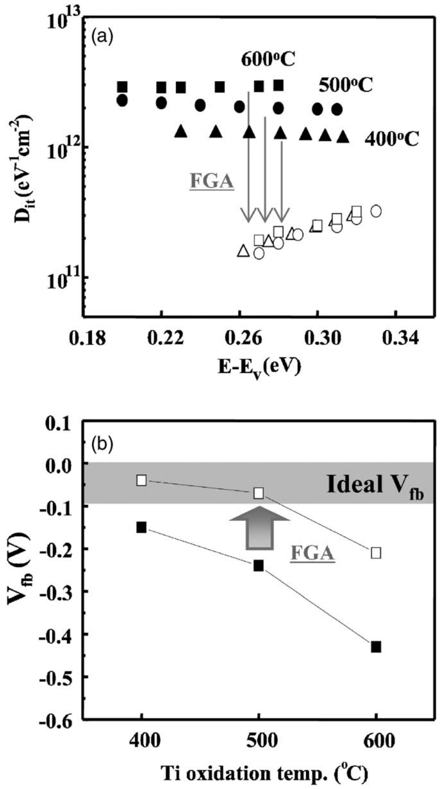

FIG. 3. Electrical degradation of the $TiO_2/HfSiO/SiO_2$ layered gate dielectrics depending on Ti-oxidation temperature and its drastic recovery using FGA treatment. (a) Changes in D_{it} with and without FGA treated samples. (b) V_{fb} change as a function of Ti-oxidation temperature.

changes in D_{it} and flat band voltage (V_{fb}) of the TiN/higher-*k* capacitors indicated by filled triangles in Fig. 1. It is clear that, without FGA treatment, D_{it} was over $1\times10^{12}\ \mathrm{eV^{-1}\,cm^{-2}}$ and it increased when the Ti-oxidation temperature increased. We also observed a marked negative V_{fb} shift as the oxidation temperature increased [filled squares in Fig. 3(b)]. Considering that, for the HfSiO gate dielectrics without TiO_2 capping, high-temperature post-deposition treatment is supposed to improve interface properties and that there is no need to consider serious V_{fb} shift due to Fermi level pinning of high work function (*p*-type) metals below 700 °C,[12] we can conclude that both interface defects and positive fixed charges causing negative V_{fb} shifts are attributed to Ti diffusion to the bottom insulators and SiO_2/Si interfaces. Note that the FGA treatment drastically improved interface properties. The D_{it} value was reduced about one order of magnitude, and the resultant value was found to be independent of the initial Ti-oxidation temperatures as indicated by open symbols in Fig. 3(a). Furthermore, the negative V_{fb} shift was also recovered with FGA treatment close to the ideal position. These results mean that most of the interface traps and positive fixed charges originating from Ti diffusion can be effectively terminated with FGA treatment.

Next, we examined the local charge trapping phenomena of the $TiO_2/HfSiO/SiO_2$ gate dielectrics using SCM. We have reported that SCM observation of high-*k* gate dielectrics provides information on initial local charge distribution and the reliability against electrical stressing.[13,14] Figures 4(a) and 4(b) represent dC/dZ images and Figs. 4(c) and 4(d) are corresponding cross-sectional profiles obtained from the $TiO_2/HfSiO/SiO_2$ layered dielectric surfaces prepared

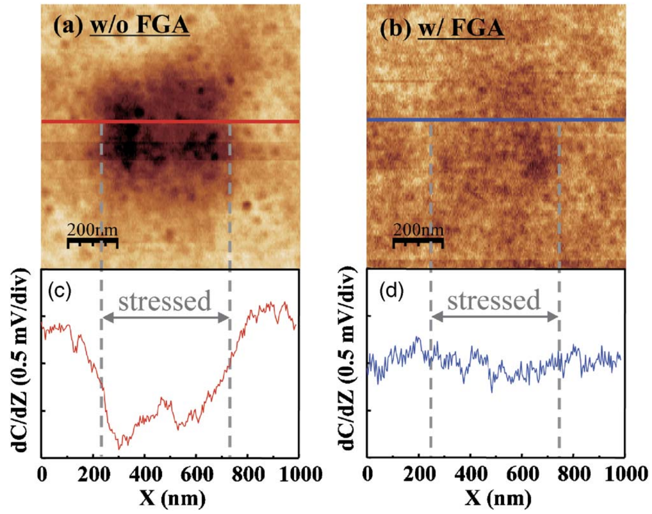

FIG. 4. (Color online) SCM observation of $TiO_2/HfSiO/SiO_2$ layered dielectrics fabricated by Ti oxidation at 600 °C with and without FGA treatment. (a) and (c) show a dC/dV image and a cross-sectional profile across the stressed area, respectively, for the dielectric sample without FGA treatment. (b) and (d) show the results from the FGA-treated sample. The electrical stressing was done by applying −3 V to the substrates. The SCM observation was performed in high vacuum without applying a sample bias.

by Ti-oxidation at 600 °C with and without FGA treatment. Drastic improvement on the reliability of the higher-k dielectrics by FGA treatment was observed when we compared local charge distribution after electrical stressing, as shown in Fig. 4. In this experiment, a 500 nm^2 area of the $TiO_2/HfSiO/SiO_2$ dielectric was first stressed by scanning the SCM probe tip while applying a substrate bias of −3 V. The scan area was then enlarged to 1 μm square without applying a substrate bias to analyze stressing phenomena. For the non-FGA-treated sample [Figs. 4(a) and 4(c)], the dC/dZ signal decreased at the stressed area. Since there were no changes in the surface morphology and in the maximum capacitance due to electrical stressing (data not shown), the decrease in the dC/dZ signal can be ascribed to positive fixed charges in the gate oxide (or a release of trapped electrons from the oxide) that lead to carrier depletion in the p-type Si substrate. In contrast, we did not see any contrast change in the dC/dZ image for the FGA treated sample under the same stressing conditions [Fig. 4(b)].

According to these macro- and microscopic analyses, we can conclude that Ti diffusion to the bottom layers induces current leakage paths, interface traps, positive fixed charges, and pre-existing charge trapping or detrapping centers, which are activated by electrical stressing. A recent density functional theory calculation study showed that substitutional Ti atoms in the HfO_2 network create deep levels that act as electron traps.[15] Thus, we can simply explain the increase in J_g caused by Ti diffusion to the bottom HfSiO dielectric by taking into account the similarity between HfO_2 and HfSiO networks. Moreover, from looking at the increase in D_{it} caused by high-temperature oxidation and its recovery with FGA treatment [Fig. 3(a)], a possible candidate for these Ti-induced defects may be related to the Si dangling bonds within the SiO_2 underlayers. Based on this assumption, the origin of the initial positive fixed charges (hole traps) and their recovery with FGA treatment could also be attributed to oxygen vacancies in the SiO_2 and hydrogen termination of the Si dangling bonds, as previously discussed for the pure SiO_2 dielectrics. Since Ti atoms tend to bond with oxygen atoms, Si dangling bonds in the SiO_2 underlayer could be generated by Ti diffusion through the HfSiO layer. Moreover, we need to think about the role of oxygen vacancies in the HfSiO layer because the resultant defect levels can also act as current leakage paths and release electrons to become charged states.[16] Although the oxygen vacancies in the HfSiO layers could also be a possible origin for the Ti-induced defects, further study is required to understand the role of the FGA treatment on silicate dielectrics.

In summary, we demonstrated the use of $TiO_2/HfSiO/SiO_2$ layered higher-k gate dielectrics and investigated Ti-induced defects by means of macroscopic electrical properties and local charge trapping phenomena. We found that Ti-induced defects, which cause increases in J_g and D_{it}, fixed charges, and additional charge trappings by electrical stressing, can be suppressed by optimizing Ti-oxidation conditions and FGA treatment. We achieved aggressive EOT scaling down to 0.71 nm and reduced gate leakage of 7.2×10^{-2} A/cm^2, while reducing D_{it} to the order of 10^{10} eV^{-1} cm^{-2} and keeping the ideal V_{fb} position.

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