

Title	Origin of flatband voltage shift and unusual minority carrier generation in thermally grown GeO2/Ge metal-oxide-semiconductor devices		
Author(s)	Hosoi, Takuji; Kutsuki, Katsuhiro; Okamoto, Gaku et al.		
Citation	Applied Physics Letters. 2009, 94(20), p. 202112		
Version Type	VoR		
URL	https://hdl.handle.net/11094/85485		
rights	This article may be downloaded for personal use only. Any other use requires prior permission of the author and AIP Publishing. This article appeared in Appl. Phys. Lett. and may be found at https://doi.org/10.1063/1.3143627.		
Note			

## Osaka University Knowledge Archive : OUKA

https://ir.library.osaka-u.ac.jp/

Osaka University

## Origin of flatband voltage shift and unusual minority carrier generation in thermally grown GeO<sub>2</sub>/Ge metal-oxide-semiconductor devices

Cite as: Appl. Phys. Lett. 94, 202112 (2009); https://doi.org/10.1063/1.3143627 Submitted: 20 April 2009 • Accepted: 06 May 2009 • Published Online: 22 May 2009

Takuji Hosoi, Katsuhiro Kutsuki, Gaku Okamoto, et al.





## ARTICLES YOU MAY BE INTERESTED IN

Evidence of low interface trap density in  $GeO_2$  / Ge metal-oxide-semiconductor structures fabricated by thermal oxidation

Applied Physics Letters 93, 032104 (2008); https://doi.org/10.1063/1.2959731

Desorption kinetics of GeO from GeO<sub>2</sub>/Ge structure

Journal of Applied Physics 108, 054104 (2010); https://doi.org/10.1063/1.3475990

Effective electrical passivation of Ge(100) for high-k gate dielectric layers using germanium

Applied Physics Letters 91, 082904 (2007); https://doi.org/10.1063/1.2773759

**P**QBLOX



**Shorten Setup Time Auto-Calibration More Qubits** 

**Fully-integrated Quantum Control Stacks** Ultrastable DC to 18.5 GHz Synchronized <<1 ns Ultralow noise



100s qubits

visit our website >



## Origin of flatband voltage shift and unusual minority carrier generation in thermally grown GeO<sub>2</sub>/Ge metal-oxide-semiconductor devices

Takuji Hosoi, <sup>1,2,a)</sup> Katsuhiro Kutsuki, <sup>1</sup> Gaku Okamoto, <sup>1</sup> Marina Saito, <sup>1</sup> Takayoshi Shimura, <sup>1</sup> and Heiji Watanabe <sup>1,2</sup>

(Received 20 April 2009; accepted 6 May 2009; published online 22 May 2009)

Improvement in electrical properties of thermally grown  $GeO_2/Ge$  metal-oxide-semiconductor (MOS) capacitors, such as significantly reduced flatband voltage ( $V_{FB}$ ) shift, small hysteresis, and minimized minority carrier response in capacitance-voltage (C-V) characteristics, has been demonstrated by *in situ* low temperature vacuum annealing prior to gate electrode deposition. Thermal desorption analysis has revealed that not only water but also hydrocarbons are easily infiltrated into  $GeO_2$  layers during air exposure and desorbed at around 300 °C, indicating that organic molecules within  $GeO_2/Ge$  MOS structures are possible origins of electrical defects. The inversion capacitance, indicative of minority carrier generation, increases with air exposure time for  $Au/GeO_2/Ge$  MOS capacitors, while maintaining an interface state density ( $D_{it}$ ) of about a few  $10^{11}$  cm<sup>-2</sup> eV<sup>-1</sup>. Unusual increase in inversion capacitance was found to be suppressed by  $Al_2O_3$  capping ( $Au/Al_2O_3/GeO_2/Ge$  structures). This suggests that electrical defects induced outside the Au electrode by infiltrated molecules may enhance the minority carrier generation, and thus acting as a minority carrier source just like MOS field-effect transistors. © 2009 American Institute of Physics. [DOI: 10.1063/1.3143627]

Germanium is an attractive channel material for future metal-oxide-semiconductor (MOS) field-effect transistors because it has higher carrier mobility than conventional silicon. However, compared with silicon oxide gate insulator, germanium oxide is difficult to integrate into a MOS fabrication process due to its poor thermal stability and water solubility. Thermal decomposition of GeO<sub>2</sub> is caused by GeO molecule desorption by annealing at above 425 °C. It has been pointed out that abstracting Ge from a Ge substrate at a GeO<sub>2</sub>/Ge interface is essential for GeO molecule formation, and this interface reaction leads to GeO<sub>2</sub>/Ge interface property seriously deteriorating.<sup>2</sup> This thermal instability is one reason Dit values of thermally grown GeO2/Ge interface reported to date are scattered widely  $(10^{11}-10^{12} \text{ cm}^{-2} \text{ eV}^{-1})$ . Meanwhile, it has recently been reported that a GeO<sub>2</sub> insulator formed by high pressure thermal oxidation at 550 °C, which can suppress the GeO volatilization, exhibits improved electrical properties.<sup>3</sup> Matsubara et al.<sup>4</sup> also demonstrated that  $D_{it}$  values of less than  $10^{11}$  cm<sup>-2</sup> eV<sup>-1</sup> were obtained for GeO<sub>2</sub>/Ge interfaces formed by a standard dry oxidation at about 550-575 °C. A good interface property of as-oxidized GeO<sub>2</sub>/Ge(100) interface at above 500 °C was predicted from a simple calculation on the basis of viscoelastic properties of GeO<sub>2</sub>. Our first-principles total energy calculation of the GeO<sub>2</sub>/Ge interface during thermal oxidation also suggests a superior interface property because of a low Ge emission probability at the interface during oxidation.<sup>o</sup> However, experimental verification of these predictions on the standard thermal GeO<sub>2</sub>/Ge interface is demonstrated in only a few reports.<sup>4,7,8</sup> This may be attributed to the fact that Ge MOS characteristics are highly sensitive to fabrication

Remarkable inversion capacitance in Ge MOS capacitors is generally considered to originate from a much shorter minority carrier response time and higher minority carrier generation-recombination rate, due to the smaller band gap of Ge. However, in many previous reports on Ge MOS devices, frequency dispersion of C-V curves in the inversion region is not unique and seems to depend on process conditions. This fact suggests that the minority carrier generation is caused not only by intrinsic thermal excitation across the Ge band gap but also by another excitation process, such as defect-assisted band tunneling. Furthermore, although a negative  $V_{\rm FB}$  shift is often observed for Ge MOS capacitors, its origin has not yet been addressed. In this study, we have systematically investigated the correlation between electrical characteristics of Ge MOS devices and hygroscopic property of GeO<sub>2</sub>. The impact of in situ low-temperature vacuum annealing prior to gate electrode deposition on Ge MOS characteristics was examined in terms of  $V_{\rm FB}$  shift, C-V hysteresis, and interface quality. We also discuss a minority carrier generation mechanism on the basis of time evolution of C-V characteristics of Ge MOS capacitors with/without Al<sub>2</sub>O<sub>3</sub> capping on GeO<sub>2</sub> insulators (Au/GeO<sub>2</sub>/Ge or  $Au/Al_2O_3/GeO_2/Ge)$  during air exposure.

The starting substrates were p-type Ge(100) wafers with a resistivity of 0.1–0.5  $\Omega$  cm. The substrates were cleaned using cyclic 10% HF dip and ultrapure water rinse. After

<sup>&</sup>lt;sup>1</sup>Department of Material and Life Science, Graduate School of Engineering, Osaka University, 2-1 Yamadaoka, Suita, Osaka 565-0871, Japan

<sup>&</sup>lt;sup>2</sup>Research Center for Ultra-Precision Science and Technology, Graduate School of Engineering, Osaka University, 2-1 Yamadaoka, Suita, Osaka 565-0871, Japan

process conditions due to hygroscopic and volatile properties of  $GeO_2$ . In addition, since the minority carrier response is more pronounced in Ge MOS capacitors, the difficulty in obtaining accurate  $D_{it}$  values using a conventional conductance method has been pointed out. Thus, to minimize the minority carrier generation, low temperature measurements are widely used.

a)Electronic mail: hosoi@mls.eng.osaka-u.ac.jp.

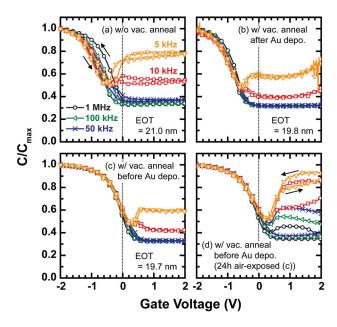


FIG. 1. (Color online) Bidirectional normalized C-V curves of the as-fabricated Au/GeO $_2$ /Ge MOS capacitors (a) without vacuum annealing but with *in situ* vacuum annealing (b) after and (c) before Au deposition. (d) C-V curves of the Au/GeO $_2$ /Ge MOS capacitor with *in situ* vacuum annealing prior to the Au deposition measured after air exposure for 24 h.

blow-drying, the samples were loaded into a furnace tube and subjected to dry oxidation in an O<sub>2</sub> ambient at 550 °C for 2 h to form a GeO<sub>2</sub> layer. Then the samples were immediately transferred from the furnace to a vacuum evaporation chamber in order to minimize water absorption from the air. Au films were deposited through a shadow mask to define gate electrodes at room temperature. Some of the samples were in situ annealed at 300 °C for 30 min under a vacuum of  $6 \times 10^{-4}$  Pa either before or after Au deposition. Al backside electrodes were also formed by the vacuum evaporation. The C-V characteristics were measured from inversion to accumulation at frequencies ranging from 1 kHz to 1 MHz using an Agilent 4284 LCR meter. An equivalent oxide thickness,  $V_{\rm FB}$ , and hysteresis were estimated from high frequency C-V curves, and  $D_{\mathrm{it}}$  values were extracted by a lowtemperature conductance method.

Figure 1 shows the bidirectional C-V curves of the  $\text{Au}/\text{GeO}_2/\text{Ge}$  MOS capacitors fabricated under various conditions. The extracted values of  $V_{\text{FB}}$  and hysteresis are listed in Table I. Considering a Fermi level of Ge substrates and Au work function of 5.0 eV, the ideal  $V_{\text{FB}}$  of the  $\text{Au}/\text{GeO}_2/\text{Ge}$  MOS capacitor is estimated to be about 0.5 V. A negative  $V_{\text{FB}}$  shift, large C-V hysteresis, and remarkable inversion capacitance depending on the measured frequency were observed

TABLE I. Extracted values of  $V_{\rm FB}$  and hysteresis from the C-V curves measured at 1 MHz of the fabricated Au/GeO $_2$ /Ge MOS capacitors shown in Fig. 1.

	Sample	$V_{ m FB} \ ( m V)$	Hysteresis (mV)
(a)	without vac. anneal	-0.76	320
(b)	with vac. anneal after Au depo.	-0.90	114
(c)	with vac. anneal before Au depo. with vac. anneal before Au depo.	-0.14	88
(d)	(after air exposure for 24 h)	-0.20	90

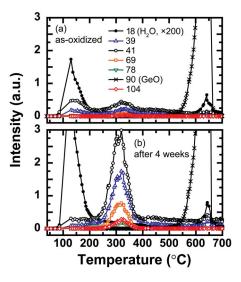


FIG. 2. (Color online) Thermal desorption spectra taken from (a) an asoxidized sample and (b) a sample exposed to air for 4 weeks after oxidation.

for the capacitor without vacuum annealing [Fig. 1(a)]. An in situ vacuum annealing after Au deposition effectively improved C-V hysteresis and suppressed minority carrier response but had almost no effect on  $V_{\rm FB}$  [Fig. 1(b)]. In addition to these improvements, the negative  $V_{\rm FB}$  shift was significantly reduced by in situ vacuum annealing prior to Au deposition [Fig. 1(c)]. However, the frequency dispersion of C-V curves in the inversion region arose again after air exposure for 24 h, while maintaining small  $V_{\rm FB}$  shift and hysteresis [Fig. 1(d)]. These results indicate that hygroscopic property of GeO<sub>2</sub> strongly affects the electrical characteristics of Ge MOS capacitors. Since the C-V hysteresis was reduced by vacuum annealing regardless of an existing Au electrode, carrier trapping sites in GeO<sub>2</sub> are considered to have been decreased due to temperature-induced structural change [see Figs. 1(b) and 1(c)]. The  $V_{\rm FB}$  closer to the ideal value was obtained only by in situ vacuum annealing prior to Au deposition and was stable when exposed to air [see Figs. 1(c) and 1(d)]. Furthermore, we found that when it took a few hours after oxidation to introduce a sample into the vacuum evaporation chamber, the resulting C-V curve shifted much more negatively. These results suggest that infiltrated molecules into GeO<sub>2</sub> layer are a possible origin of the negative  $V_{\rm FB}$  shifts, such as fixed sheet charge generation, and can be removed by low temperature vacuum annealing.

To characterize the infiltrated molecules, thermal desorption spectroscopy (TDS) analyses were carried out for both an as-oxidized sample and a sample exposed to air for 4 weeks after oxidation, as shown in Fig. 2. It was found that the several mass numbers, such as 39, 41, 69, 78, and 104, were detected at around 300 °C and that the amount of those molecules significantly increased as the time passed after oxidation (air exposure time). Although it was difficult to identify these peaks as specific molecules only from TDS spectra, recent infrared absorption spectroscopy analysis on Ge(100) surfaces revealed that a large amount of hydrocarbons (CH<sub>x</sub>) were incorporated by air exposure with a growth of native oxide. <sup>13</sup> Therefore, we think that several molecules desorbed at low temperatures were attributable to organic molecules in  $GeO_2$ .

Next, we examined time evolution of the *C-V* characteristics during air exposure. It was found that although minor-

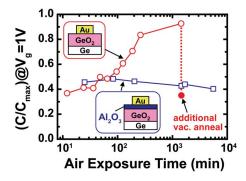


FIG. 3. (Color online) Time evolution of normalized inversion capacitance at the gate voltage of 1 V taken from the forward *C-V* curves measured at 10 kHz for both Au/GeO<sub>2</sub>/Ge and Au/Al<sub>2</sub>O<sub>3</sub>/GeO<sub>2</sub>/Ge MOS capacitors.

ity carrier response was suppressed by in situ vacuum annealing both with and without an Au electrode, it became more and more pronounced during air exposure, as indicated by red open circles in Fig. 3. In contrast, the values of  $V_{\rm FR}$ and C-V hysteresis did not show any notable change even after air exposure for 24 h, as shown in Fig. 1(d). This indicates that while an Au electrode blocks the organic molecules from diffusing into the bottom GeO<sub>2</sub> layer, the outer region exposed to the air deteriorates. The remarkable increase in inversion capacitance due to air exposure was drastically reduced again by additional vacuum annealing, as indicated by the red filled circle in Fig. 3. This situation is quite similar to in situ vacuum annealing after Au deposition [Fig. 1(b)]. Furthermore, to completely exclude any influence from air exposure, we fabricated the Au/Al<sub>2</sub>O<sub>3</sub>/GeO<sub>2</sub>/Ge MOS capacitor. Right after the vacuum annealing, an Al<sub>2</sub>O<sub>3</sub> capping layer was formed on GeO<sub>2</sub> by oxidizing a thin metal Al layer at 400 °C under low oxygen partial pressure conditions. As shown in Fig. 3, the Au/Al<sub>2</sub>O<sub>3</sub>/GeO<sub>2</sub>/Ge MOS capacitor exhibited a stable inversion capacitance against air exposure. From these results, it can be concluded that the infiltrated molecules into GeO<sub>2</sub> layer in the uncovered region induces electrical defects, thus enhancing minority carrier generation. One of the possible mechanisms is that the electrical defects near GeO<sub>2</sub>/Ge interface caused by infiltrated molecules assisted the valence electron tunneling in the Ge substrate, hence generated electrons were supplied to a depletion layer just beneath the Au electrode under inversion conditions, just like MOS fieldeffect transistors.

Finally, the impact of in situ vacuum annealing, air exposure, and Al<sub>2</sub>O<sub>3</sub> capping layer formation on GeO<sub>2</sub>/Ge interface properties was also evaluated. As shown in Fig. 4, there was almost no difference in  $D_{\rm it}$  values (2  $\times 10^{11}$  cm<sup>-2</sup> eV<sup>-1</sup>) between with and without *in situ* vacuum annealing, implying that the GeO<sub>2</sub>/Ge interface was not deteriorated by air exposure for a short time. The  $D_{it}$  values remained unchanged even after air exposure for 24 h because the Au electrode just above the measured region of the GeO<sub>2</sub>/Ge interface blocked the molecules. Au/Al<sub>2</sub>O<sub>3</sub>/GeO<sub>2</sub>/Ge MOS capacitor exhibited slightly lower Dit, but further investigation is required to conclude whether Al<sub>2</sub>O<sub>3</sub> capping improves the GeO<sub>2</sub>/Ge interface quality or not. Among these measurements, low  $D_{it}$  values were obtained for GeO<sub>2</sub>/Ge interface, which were compa-

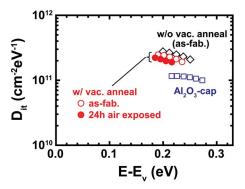


FIG. 4. (Color online) Energy distribution of  $D_{\rm it}$  for  ${\rm GeO_2/Ge}$  interfaces in situ vacuum annealed prior to Au electrode deposition, subsequent air exposure for 24 h, and  ${\rm Al_2O_3}$  capping layer formation, measured by low temperature conductance method.

rable to the reported values.<sup>4,7</sup> This indicates the inherently superior interface quality of GeO<sub>2</sub>/Ge interface without any interface passivation technique.

In summary, we have demonstrated a significant improvement in electrical properties of  ${\rm GeO_2/Ge~MOS}$  capacitors, such as a reduced flatband voltage shift, small C-V hysteresis, suppression of minority carrier response, and low  $D_{\rm it}$  of about a few  $10^{11}~{\rm cm^{-2}~eV^{-1}}$ , by in situ low temperature vacuum annealing prior to gate electrode deposition. We also found that organic molecules infiltrating into  ${\rm GeO_2}$  layers during air exposure strongly affects the  $V_{\rm FB}$  and minority carrier generation. These results provide a useful processing guideline for achieving  ${\rm Ge~MOS}$  technologies.

This research was partly supported by a Grant-in-Aid for Scientific Research on Priority Area (Grant No. 18063012) from the Ministry of Education, Culture, Sports, Science, and Technology in Japan.

<sup>1</sup>K. Prabhakaran, F. Maeda, Y. Watanabe, and T. Ogino, Thin Solid Films **369**, 289 (2000).

<sup>2</sup>K. Kita, S. Suzuki, H. Nomura, T. Takahashi, T. Nishimura, and A. Toriumi, Jpn. J. Appl. Phys. 47, 2349 (2008).

<sup>3</sup>C. H. Lee, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, Extended Abstract of the 2008 International Conference on Solid State Devices and Materials, 2008 (unpublished), p. 16.

<sup>4</sup>H. Matsubara, T. Sasada, M. Takenaka, and S. Takagi, Appl. Phys. Lett. **93**, 032104 (2008).

<sup>5</sup>M. Houssa, G. Pourtois, M. Caymax, M. Meuris, M. M. Heyns, V. V. Afanas'ev, and A. Stesmans, Appl. Phys. Lett. **93**, 161909 (2008).

<sup>6</sup>S. Saito, T. Hosoi, H. Watanabe, and T. Ono (unpublished).

A. Delabie, F. Bellenger, M. Houssa, T. Conard, S. Van Elshocht, M. Caymax, M. Heyns, and M. Meuris, Appl. Phys. Lett. 91, 082904 (2007).
 F. Bellenger, M. Houssa, A. Delabie, V. Afanasiev, T. Conard, M. Caymax, M. Meuris, K. De Meyer, and M. M. Heyns, J. Electrochem. Soc. 155, G33 (2008).

<sup>9</sup>Y. Fukuda, T. Ueno, S. Hirono, and S. Hashimoto, Jpn. J. Appl. Phys., Part 1 44, 6981 (2005).

<sup>10</sup>N. Taoka, K. Ikeda, Y. Yamashita, N. Sugiyama, and S. Takagi, Extended Abstract of the 2006 International Conference on Solid State Devices and Materials, 2006 (unpublished), p. 396.

<sup>11</sup>P. Batude, X. Garros, L. Clavelier, C. Le Royer, J. M. Hartmann, V. Loup, P. Besson, L. Vandroux, Y. Campidelli, S. Deleonibus, and F. Boulanger, J. Appl. Phys. **102**, 034514 (2007).

<sup>12</sup>K. Martens, C. O. Chui, G. Brammertz, B. D. Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, IEEE Trans. Electron Devices 55, 547 (2008).

<sup>13</sup>S. R. Amy, Y. J. Chabal, F. Amy, A. Kahn, C. Krugg, and P. Kirsch, Mater. Res. Soc. Symp. Proc. **917E**, 0917-E01-05 (2006).