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Charge trapping properties in $TiO_2/HfSiO/SiO_2$ gate stacks probed by scanning capacitance microscopy

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The charge-trapping properties of the high-permittivity titanium oxide–hafnium silicate–silicon dioxide ($TiO_2/HfSiO/SiO_2$) gate stacks have been studied using scanning capacitance microscopy. From the bias stress examination of the gate stacks, we concluded that there were electron traps within the films, and these trap densities increased with an increase in the oxidation temperature used for the fabrication of TiO_2 top dielectrics. Furthermore, we found that the distribution of these charged defects was inhomogeneous within the gate stacks. These results are attributed to Ti diffusion through the dielectric layers, which caused electrical defects within the gate stacks.
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The continuous downscaling of Si-based metal-oxide-semiconductor field effect transistors (MOSFETs) will soon require substitutes for conventional SiO_2 as the gate dielectrics. High permittivity (high-*k*) metal oxides are expected to maintain the physical thickness of gate dielectrics, enabling the gate leakage current to be suppressed.[1] Among the several candidates for high-*k* materials, hafnium oxide (HfO_2) and its silicate (HfSiO) films are expected to be promising materials.[2] However, silicate films have lower dielectric constants compared with oxide films. Therefore, an effective approach seems to be to mix the silicate films with other high-*k* materials to further improve the properties of the gate dielectrics. For this purpose, titanium oxide (TiO_2) and its composite or layered structure are attractive because of its very high dielectric constant (50–170).[3] To confirm the reliability of high-*k* gate stacks, charged defects within high-*k* films should be closely investigated because they induce threshold voltage instabilities or trap-assisted leakage current.[4] In the present study, the charge-trapping properties of $TiO_2/HfSiO/SiO_2$ gate stacks and their dependence on the preparation process were characterized through scanning capacitance microscopy (SCM) measurements.

The sample preparation procedure was as follows. After a 1.4-nm-thick SiO_2 underlayer had been formed on a *p*-Si(100) substrate by conventional rapid thermal oxidation, ultrathin 0.5-nm-thick metal Hf layers were deposited by low-damage sputtering on the SiO_2/Si maintained at room temperature. The HfSiO layer was then formed by utilizing a solid phase interface reaction between the metal Hf layer and SiO_2 underlayer by annealing in an oxygen partial pressure (10^{-3} Torr) ambient at 850 °C for 1 min.[5] Then, 0.5-nm-thick metal Ti layers were deposited on the HfSiO layer and oxidized by annealing in an oxygen partial pressure (10^{-3} Torr) ambient at 400 °C (sample 2) and 600 °C (sample 3) for 1 min.[6] To verify what effects TiO_2 capping would have on the dielectric properties, we prepared $HfSiO/SiO_2$ (1.8 nm SiO_2 thickness) gate stacks as a reference sample 1.

These fabricated gate stacks were examined using SCM measurements in a vacuum (10^{-4} Pa) at room temperature. The detailed setups of our SCM using the quartz oscillator were described in a previous study.[7,8] Our SCM yielded simultaneous images of the topography and distance differential capacitance (dC/dZ). The dC/dZ signal sensed the static capacitance of the nanometric MOS structure formed by the SCM probe tip, surface oxides, and *p*-Si substrate.[8]

In the studies presented here, localized regions within the gate stacks were electrically stressed. A 500-nm-square area was initially stressed by scanning the probe tip while applying positive or negative bias (V_{dc}) to the sample's back electrode. Then, the scan area was increased to 1 μm square and the V_{dc} was reduced to 0 V to image the stressed center area along with the surrounding unstressed regions. The results of this experiment are shown in Fig. 1, which has pairs of simultaneously obtained topographic and dC/dZ images. Each image pair shows sample 1 [(a) and (b)], 2 [(c) and (d)], and 3 [(e) and (f)] after being initially stressed at a V_{dc} of +3 V. As can be seen from the topographic images in Figs. 1(a), 1(c), and 1(e), there are no apparent topographic anomalies in the bias-stressed region. The surface roughness of all samples was almost the same and lower than 0.12 nm in terms of the rms value. However, all dC/dZ images in Figs. 1(b), 1(d), and 1(f) has distinctive bright contrast area corresponding to the bias-stressed region.

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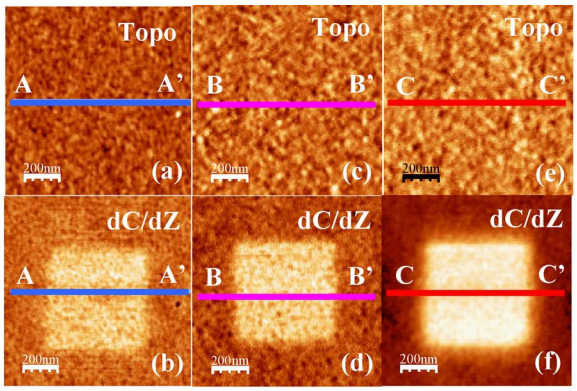

FIG. 1. (Color online) Topography and corresponding dC/dZ images of samples 1 (reference $HfSiO/SiO_2$ gate stacks), 2 ($TiO_2/HfSiO/SiO_2$ gate stacks annealed at 400 °C), and 3 ($TiO_2/HfSiO/SiO_2$ gate stacks annealed at 600 °C) after positive bias stressing. (a) Topography of sample 1, (b) dC/dZ of sample 1, (c) topography of sample 2, (d) dC/dZ of sample 2, (e) topography of sample 3, and (f) dC/dZ of sample 3. Each pair, (a) and (b), (c) and (d), and (e) and (f) were simultaneously scanned. Measurement parameters: stressing bias=+3 V, stressed regions were 500×500 nm, scanning areas were 1×1 μm, oscillation amplitude of SCM probe tip $=2$ $nm_{P\text{-}P}$, dc offset bias (V_{dc})=0 V, and feedback setpoint (Δf)= +100 mHz.

The effect of bias stressing on the surface morphology and dC/dZ images can clearly be assessed by inspecting the cross-sectional cuts along the A-A' line [Figs. 1(a) and 1(b)], B-B' [(c) and (d)], and C-C' [(e) and (f)]. The topographic and dC/dZ-signal profiles along these lines are summarized in Figs. 2(a) and 2(b). No intrinsic topographic changes could be observed between the stressed and unstressed regions in any of the samples, as confirmed by Fig. 2(a). The corresponding dC/dZ-signal profiles in Fig. 2(b), on the other hand, indicate a clear increment in the dC/dZ-signal value within the stressed regions. In the same way, Figs. 2(c) and 2(d) show a series of topographic and dC/dZ-signal profiles for sample 1, 2, and 3 under bias stressing with $V_{dc}=-3$ V. Similar to the previous results, none of the topographic profiles in Fig. 2(c) indicate obvious differences between stressed and unstressed regions. However, the corresponding dC/dZ-signal value indicates a reduction within the stressed region, as shown in Fig. 2(d).

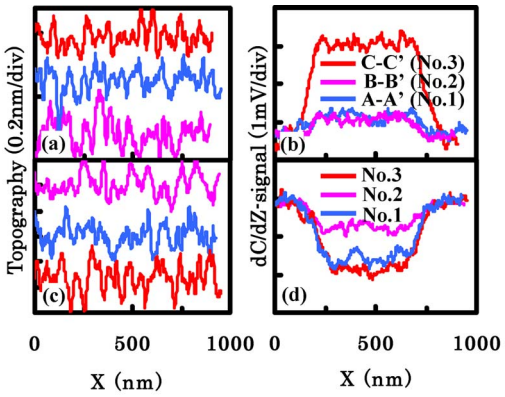

FIG. 2. (Color online) Cross-sectional profiles of bias-stressed topography and corresponding dC/dZ images. (a) and (b) are results for positive bias stressing, and (c) and (d) are derived from negative bias stressed images. Same color in each profile corresponds to same sample. (a) Topography profiles along line A-A' of Fig. 1(a) (blue), B-B' of Fig. 1(c) (pink), and C-C' of Fig. 1(e) (red). (b) dC/dZ-signal profiles along line A-A' of Fig. 1(b) (blue), B-B' of Fig. 1(d) (pink), and C-C' of Fig. 1(f) (red). (c) Topography, and (d) corresponding dC/dZ-signal profiles of samples 1 (blue), 2 (pink), and 3 (red).

There are two important implications to consider the observed dependence of the SCM images on the bias stressing. Positive sample bias stressing induces an increase in the dC/dZ signal, and negative bias stressing makes the dC/dZ signal decrease. Second, no changes in the surface topography were observed in the positive or negative bias stressed regions of any of the samples. These two facts indicate that the observed changes in the dC/dZ-signal profiles by bias stressing were certainly due to electrical effects, and not due to the local oxidation or surface abrasion of high-k films. These stress-induced changes in the dC/dZ signal also depend on the samples. For positive bias stressing, the increment in the dC/dZ-signal value between stressed and unstressed regions was ~2 mV for sample 3 (annealed at 600 °C), which is larger than that for the two other samples [~0.5 mV for sample 1 (reference) and sample 2 (annealed at 400 °C)], as shown in Fig. 2(b). For negative bias stressing, the decrease in the dC/dZ-signal value between stressed and unstressed regions was ~0.8 mV for sample 2, which is smaller than that for the other two samples (~1.8 mV for samples 1 and 3), as shown in Fig. 2(d).

The possible charge transfer between the metal probe tip and high-k samples by applying positive or negative sample bias are two ways: under positive bias applied, electrons are injected from the probe tip to the trap sites within high-k films, or holes provided by the p-Si substrate are captured in underlayer SiO_2/Si interface traps. In contrast, trapped electrons are extracted from high-k films to the probe tip, or captured holes are released from the interface traps to the substrate by applying negative sample bias. From the results in Fig. 2(b), we can conclude that electrons are injected from the probe tip to the traps of high-k films by positive bias stressing, and this causes carriers to accumulate within the p-Si substrate; therefore, the dC/dZ-signal, value increases within the stressed region. In a similar way, initially trapped electrons within high-k films might be detrapped by negative bias stressing and, thus, the decrease in the dC/dZ-signal value resulting from carrier depletion within the p-Si substrate [Fig. 2(d)]. Consequently from our findings in Figs. 1 and 2 together with the macroscopic C-V characteristics[6] we can deduce the electron trap properties within $TiO_2/HfSiO/SiO_2$ gate stacks for each sample. Macroscopic C-V curves of sample 1 shows almost no flat band voltage (V_{FB}) shift; whereas sample 2 indicates a little, and sample 3 exhibits obvious negative V_{FB} shift. These results mean that the number of positively charged defects in sample 3 is larger than those in samples 1 and 2. Hence, considering the above, the charging polarity of electron traps and filled traps preexisting within samples 1–3 might be positive and neutral, respectively. The possible origin of such electrical defects within high-k films is oxygen vacancies ($\mathbf{V_O}$)[9,10] which is neutral and is charged ($\mathbf{V_O^{2+}}$) by detrapping. Thus, the electron trapping/detrapping properties of samples 2 and 3, as shown in Figs. 2(b) and 2(d), suggest that both number of $\mathbf{V_O^0}$ and $\mathbf{V_O^{2+}}$ have increased by Ti oxidation annealing at 600 °C. From x-ray photoelectron spectroscopy analysis, we verified that conspicuous Ti diffusion from the TiO_2 layer to the SiO_2 underlayer was caused by 600 °C oxidation annealing.[6] Together with this, Ti diffusion might induce oxygen vacancies within the $TiO_2/HfSiO/SiO_2$ gate stacks due to high-temperature oxidation annealing. Furthermore, in Fig. 2(d),

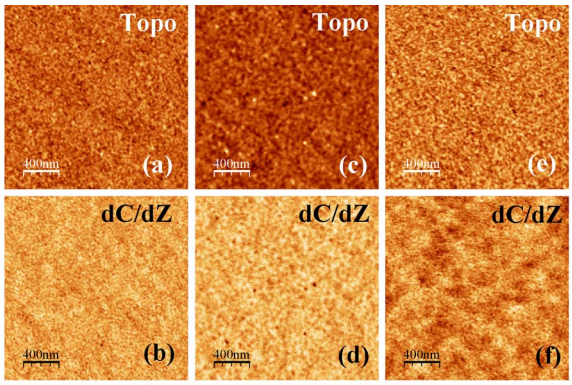

FIG. 3. (Color online) Sets of simultaneously obtained topography and dC/dZ images of samples 1–3. (a) Topography of sample 1, (b) dC/dZ of sample 1, (c) topography of sample 2, (d) dC/dZ of sample 2, (e) topography of sample 3, and (f) dC/dZ of sample 3. Measurement parameters: scanning areas were 2×2 μm, oscillation amplitude of SCM probe tip $=2$ $nm_{P\text{-}P}$, dc offset bias $(V_{dc})=0$ V, and feedback setpoint $(\Delta f)=+100$ mHz.

the decrease in the dC/dZ signal by negative bias stressing for sample 3 seems to be comparable to that observed for sample 1. Although further studies are required to clarify the detailed mechanism of the microscopic trapping/detrapping phenomena, a possible explanation is as follows. The preexisting positive charges within sample 3 induce electric field whose direction is opposite to the externally applied electric field thereby decreasing effective electric field within the gate stacks during the negative bias stressing. Therefore, in Fig. 2(d), the decrease in the dC/dZ signal for sample 3 by negative bias stressing should be underestimated by considering the difference of the effective electric field between samples 1 and 3.

Figure 3 show 2 μm square images of dC/dZ and corresponding topographies of samples 1–3 samples. These images were taken under the same condition of $V_{dc}=0$ V. We observed no specific features either in the topographies or dC/dZ images of sample 1 [Figs. 3(a) and 3(b)] and sample 2 [Figs. 3(c) and 3(d)] samples. However, the dC/dZ image of sample 3 [Fig. 3(f)] shows a corrugated contrast having no correlation with the corresponding surface topography of Fig. 3(e). Our former studies have revealed that the dC/dZ signal is not only related to local variations in gate oxide capacitance (C_{ox}), but also to the local depletion capacitance (C_{dep}) formed by the probe tip.[8] As the positive fixed charges in the gate stacks increase the carrier depletion layer within the p-Si substrate just beneath the SCM probe tip, the dark contrasting regions in the dC/dZ image of Fig. 3(f) can be attributed to the inhomogeneous distribution of positive fixed charges. Furthermore, taking the above discussion into account we can conclude that Ti diffusion within the $TiO_2/HfSiO/SiO_2$ gate stacks due to high-temperature annealing is not a spatially isotropic phenomenon.

In conclusion, we studied the charge-trapping properties of $TiO_2/HfSiO/SiO_2$ gate stacks through dC/dZ imaging by SCM. From an examination of the positive and negative bias stress of gate stacks with different preparation processes, we concluded that there were electron traps and filled traps within the gate stacks. The origin of these charged defects was ascribed to oxygen vacancies, which is caused by the diffusion of Ti during high-temperature annealing. Furthermore, we also found that these charged defects had a spatially inhomogeneous distribution within the gate stacks, indicating that the Ti diffusion was not a spatially isotropic phenomenon.

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