



Title	Systematic study on work-function-shift in metal/Hf-based high-k gate stacks
Author(s)	Kita, Yuki; Yoshida, Shinichi; Hosoi, Takuji et al.
Citation	Applied Physics Letters. 2009, 94(12), p. 122905
Version Type	VoR
URL	https://hdl.handle.net/11094/85488
rights	This article may be downloaded for personal use only. Any other use requires prior permission of the author and AIP Publishing. This article appeared in Appl. Phys. Lett. and may be found at https://doi.org/10.1063/1.3103314 .
Note	

The University of Osaka Institutional Knowledge Archive : OUKA

<https://ir.library.osaka-u.ac.jp/>

The University of Osaka

Systematic study on work-function-shift in metal/Hf-based high- k gate stacks

Cite as: Appl. Phys. Lett. **94**, 122905 (2009); <https://doi.org/10.1063/1.3103314>

Submitted: 20 February 2008 • Accepted: 02 March 2009 • Published Online: 24 March 2009

Yuki Kita, Shinichi Yoshida, Takuji Hosoi, et al.



View Online



Export Citation

ARTICLES YOU MAY BE INTERESTED IN

[Role of point defects and HfO₂/TiN interface stoichiometry on effective work function modulation in ultra-scaled complementary metal-oxide-semiconductor devices](#)

Journal of Applied Physics **114**, 034505 (2013); <https://doi.org/10.1063/1.4816090>

[Metal gate work function engineering using AlN_x interfacial layers](#)

Applied Physics Letters **88**, 112114 (2006); <https://doi.org/10.1063/1.2186517>

[High- \$\kappa\$ gate dielectrics: Current status and materials properties considerations](#)

Journal of Applied Physics **89**, 5243 (2001); <https://doi.org/10.1063/1.1361065>

 QBLOX



1 qubit

Shorten Setup Time

Auto-Calibration
More Qubits

Fully-integrated

Quantum Control Stacks
Ultrastable DC to 18.5 GHz
Synchronized <<1 ns
Ultralow noise



100s qubits

[visit our website >](#)

Systematic study on work-function-shift in metal/Hf-based high-*k* gate stacks

Yuki Kita,¹ Shinichi Yoshida,¹ Takuji Hosoi,¹ Takayoshi Shimura,¹ Kenji Shiraishi,² Yasuo Nara,³ Keisaku Yamada,⁴ and Heiji Watanabe^{1,a)}

¹Graduate School of Engineering, Osaka University, Suita, Osaka 565-0871, Japan

²Graduate School of Pure and Applied Science, University of Tsukuba, Tsukuba, Ibaraki 305-8573, Japan

³Semiconductor Leading Edge Technologies, Inc., Tsukuba, Ibaraki 305-8569, Japan

⁴Nanotechnology Research Laboratories, Waseda University, Shinjuku, Tokyo 162-0041, Japan

(Received 20 February 2008; accepted 2 March 2009; published online 24 March 2009)

Change in the work function (WF) of the gate electrode material caused by the contact with Hf-based high-*k* gate dielectrics was investigated by means of the flat-band voltage (V_{fb}) shift in capacitance-voltage curves, and the interface dipole, which modifies the WF, was characterized by x-ray photoelectron spectroscopy. We observed a negative V_{fb} shift and corresponding interface dipole, which suggest the formation of oxygen vacancy (V_O) in the Hf-based oxides. In contrast, we observed an opposite (positive) V_{fb} shift and interface dipole when Au electrodes were formed on cleaned Hf-based dielectrics. This indicates that Au–Hf bond hybridization at the Au/HfSiON interface also causes effective WF modulation, as theoretically predicted by Shiraishi *et al.* (Tech. - Dig. Int. Electron Devices Meet. 2005, 43). © 2009 American Institute of Physics. [DOI: 10.1063/1.3103314]

It has been an urgent challenge to introduce technology based on the metal/high-*k* combination into a wide variety of practical applications of metal-oxide-semiconductor (MOS) devices.¹ Among the high-*k* dielectrics, Hf-based oxides, such as nitrided Hf-silicates (HfSiON), are the most promising candidate materials. The main concern about high-*k* gate transistors is the controllability of the work function (WF) utilizing various kinds of gate electrode materials. Fermi level pinning (FLP) in *p*-type poly-Si gate electrodes² and oxygen-pressure and temperature-dependent WF of *p*-metals,³ have been reported by several groups. For these cases, the WF of the electrodes decreased, so the threshold voltage (V_{th}) of high-*k* transistors drastically increased in spite of the intrinsic high WF of the electrode materials. In contrast, the WF of inert *p*-metals, that is, Au and Pt, was found to increase under specific interface conditions,⁴ which is quite contradictory to the conventional theories of charge neutrality level (ϕ_{CNL}) and metal induced gap states. Recently, Shiraishi *et al.*^{5,6} proposed models for the unusual behaviors of *p*-type poly-Si and *p*-metal formed on Hf-based gate dielectrics. These models explain both the decrease in WF for *p*-type poly-Si and *p*-metal electrodes and the increase in it for inert *p*-metal electrodes. For the former case, oxygen vacancy (V_O) formation in the Hf-based oxides and resultant electron transfer from the V_O level to the *p*-type electrodes were considered to explain the change in WF (V_O model). In addition, Akasaka *et al.* constructed a modified V_O model to understand process-dependent *p*-metal FLP by taking into account V_O formation due to oxygen transport through the SiO₂ interlayer to the Si substrate.⁷ In contrast, for the latter case, the increase in WF for inert metal electrodes on Hf-based oxides can be explained by interface hybridization between the large occupied state of metal electrodes and the unoccupied Hf 5*d* state of the Hf-based oxides. This interface hybridization causes charge transfer in the opposite direction for the V_O formation, that is, the gen-

eralized charge neutrality level (ϕ_{CNL}^G) model.⁶ Although these models for WF modification of gate electrode material are applicable to each metal/high-*k* system, there still remain controversial reports on WF modification, and so elucidating these complicated phenomena requires systematic experiments that consider both V_O and ϕ_{CNL}^G models using a well defined simple metal/high-*k* system. In this study, we carefully examined the dependence of the WF of gate electrode material and the interface dipole at Au/HfSiON interface on the fabrication and post-treatment conditions.

We used HfSiON gate dielectrics deposited by metal organic chemical vapor deposition on 300 mm *p*-type Si(100) wafers with 0.7-nm-thick SiO₂ underlayers. The Hf ratio [Hf/(Hf+Si)] was 0.6, and the nitridation was carried out by NH₃ annealing. High-temperature postdeposition annealing was also performed to improve the electrical properties. Au electrodes were formed on the HfSiON dielectrics by vacuum evaporation. The Au film thickness was about 80 nm for capacitance-voltage (*C-V*) measurements, and it was less than 10 nm for x-ray photoelectron spectroscopy (XPS) analysis. The HfSiON dielectrics were either annealed at 150 °C for 30 min under a high vacuum or exposed to hydrogen radicals for 10 min at room temperature before Au deposition on the cleaned dielectric surface. The WF of Au in contact with the HfSiON was deduced from conventional *C-V* measurements. The equivalent oxide thickness of the gate stacks typically ranged from 1.2 to 1.5 nm. The hysteresis and frequency dispersion of the *C-V* curves and their dependence on the electrode area were negligible for all samples. High-temperature annealing was carried out up to 950 °C for 30 s in dry nitrogen. We also performed the forming-gas annealing (FGA) at 400 °C for 30 min in reduction atmosphere of H₂/He (1%) mixture. Moreover, we studied the modification in the WF of Au in contact with the HfSiON under various atmospheres. To clarify the possible origins of the changes in flat-band voltage (V_{fb}), we investigated the dipole moment at the Au/HfSiON interface by

^{a)}Electronic mail: watanabe@mls.eng.osaka-u.ac.jp.

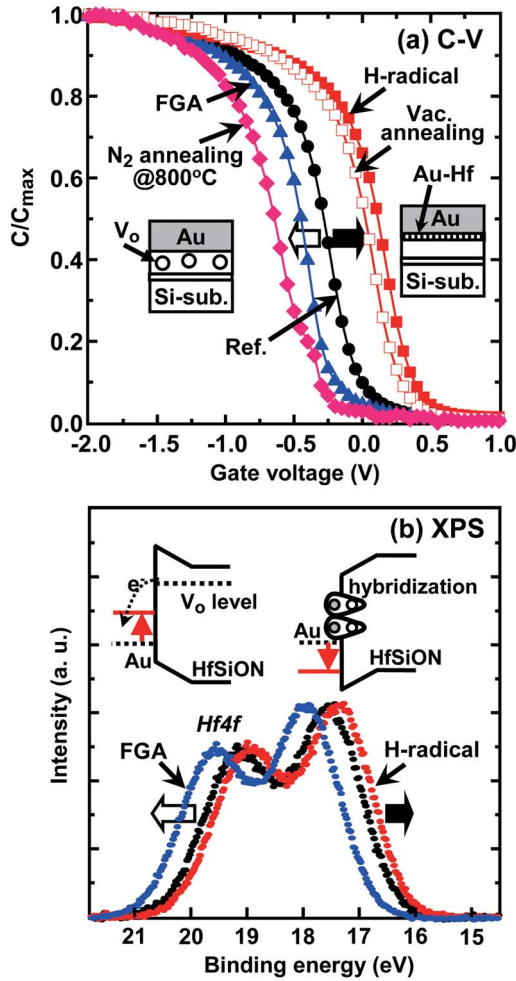


FIG. 1. (Color online) (a) Normalized C - V curves of Au/HfSiON/Si capacitors measured at 100 kHz. (b) Hf 4 f spectra, arising from HfSiON, whose binding energy was calibrated with an ideal binding energy of Au 4 $f_{7/2}$ core level (83.9 eV). Schematic illustration of insets in (a) and (b) represents the basic concepts of V_0 and ϕ_{CNL}^G models, the interface dipole caused by V_0 formation, and Au-Hf hybridization. The reference capacitor was fabricated without any treatment. Surface cleaning of the HfSiON film was performed by hydrogen radical exposure (H-radical) or vacuum annealing at 150 °C (vac. annealing) before Au deposition. The post-treatments were carried out by FGA at 400 °C or high-temperature annealing at 800 °C under nitrogen ambient (N₂ annealing at 800 °C) with Au electrodes.

measuring the binding energy of the Au 4 f and Hf 4 f photoelectron spectra.

Normalized C - V curves of the Au/HfSiON/Si capacitors prepared under various fabrication conditions measured at 100 kHz are shown in Fig. 1(a). The capacitor without any treatment (filled black circles) is used as a reference and exhibits WF of intrinsic Au (around 5.1 eV). We observed a negative shift in V_{fb} for the capacitors annealed at 800 °C in dry nitrogen and for those annealed in forming gas. Figure 2 shows the amount of the negative V_{fb} shift observed for the Au/HfSiON/Si capacitors as a function of annealing temperature. The WF of Au in contact with the HfSiON decreased with increasing annealing temperature, and a significant FLP occurred above 700 °C. Since an inert Au does not react with oxygen, we considered the modified V_0 model, which is based on oxygen transport from Hf-based oxide to the Si substrate, thereby transferring electrons from Hf-based oxide to the p -type electrode. The negative V_{fb} shift also occurred after FGA at 400 °C, as shown in Fig. 1(a). This

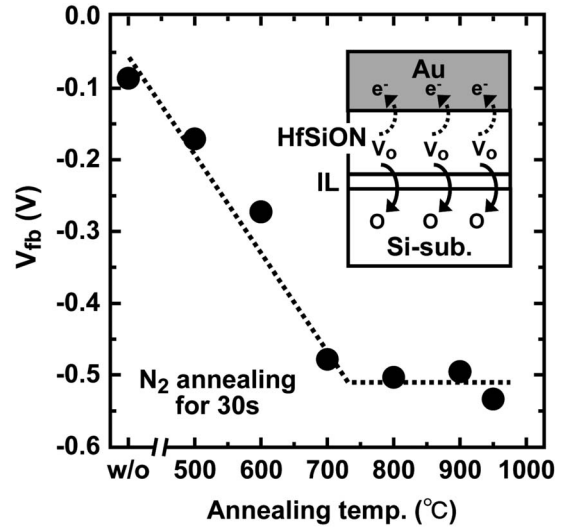


FIG. 2. V_{fb} of Au/HfSiON/Si capacitor as a function of annealing temperature. Each annealing was performed for 30 s. A schematic illustration of the inset shows the modified V_0 model that considers transport of oxygen from HfSiON to the Si substrate.

again indicates V_0 formation by the treatment in reduction atmosphere.

Filled black and blue symbols in Fig. 1(b) represent Hf 4 f photoelectron spectra arising from the reference Au(<10 nm)/HfSiON stack and that annealed in forming gas, respectively. This FGA caused an energy shift toward higher binding energy (leftward), and there was no marked change in the shape and the full width at half maximum of the Au 4 f and Hf 4 f spectra. These results imply the existence of an interface dipole, and that there was no big difference in the fixed charge distribution within the HfSiON films. Although the magnitude of the binding energy shifts in the photoelectron spectra does not exactly match that of the V_{fb} shifts in the C - V curves mainly due to a difference in the thicknesses of the Au layers used for the XPS and C - V measurements, Figs. 1(a) and 1(b) imply that the negative V_{fb} shift is not caused by the fixed charge in the HfSiON dielectrics but caused by the dipole at the Au/HfSiON interface as a result of V_0 formation.

A positive V_{fb} shift was observed when the HfSiON surfaces were exposed to hydrogen radicals before Au deposition or when those were annealed in vacuum at 150 °C [Fig. 1(a)] before Au deposition. The analyses of photoelectron spectra also imply the formation of an interface dipole in the opposite direction in contrast to those expected for the FLP resulting from the V_0 formation [Fig. 1(b)]. Because the WFs of Au in contact with the HfSiON were apparently larger than the WF of intrinsic Au, Fig. 1(b) cannot be simply explained by classical theories. By taking into account the ϕ_{CNL}^G model, we believe that *in situ* surface treatment of high- k dielectrics followed by the Au deposition will lead to the formation of Au-Hf bonds that induce charge transfer. For the Au/HfSiON/Si capacitor without the surface treatment, the Au/HfSiON interface is thought to be stabilized by the adsorbates including oxygen to form Au-O-Hf bonds at the Au/HfSiON interface, thereby suppressing interface hybridization. Therefore, some of the controversial reports on WF modulation seem to be derived from the differences in the atomic bonds at the interface.

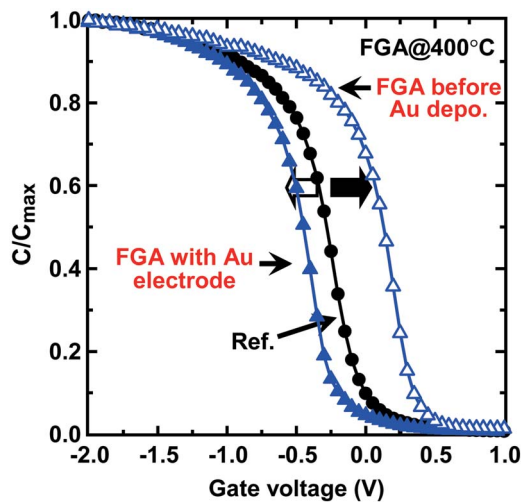


FIG. 3. (Color online) Normalized C - V curves of Au/HfSiON/Si capacitors that received FGA at 400 °C before or after Au deposition.

To confirm the validity of the V_O and ϕ_{CNL}^G models, we examined the role of p -type electrodes in the V_O formation. The FGA induced changes in the C - V curves before or after Au deposition are compared in Fig. 3. It should be noted that a negative V_{fb} shift and corresponding core level shift (data not shown) caused by V_O formation in the Hf-based oxide were not observed when the HfSiON is not covered with Au (open triangles). This result agrees with the V_O model, which claims that the electron transfer to p -type electrodes plays a main role in FPL phenomenon. Moreover, instead of the FLP based on the V_O (V_O based FLP) model, the positive V_{fb} shift can be explained by the ϕ_{CNL}^G model if the surface adsorbates are removed by FGA before Au deposition. Therefore, we can conclude that our experimental results validate both the V_O and ϕ_{CNL}^G models in understanding the WF of Au in contact with the HfSiON.

We confirmed that the negative V_{fb} shift caused by V_O based FLP was independent of air exposure time. This implies that V_O in the Hf-based oxide is stable at room temperature (data not shown). Figure 4 shows the atmosphere-

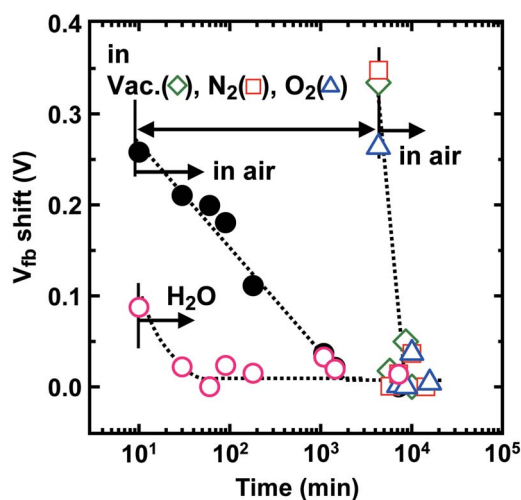


FIG. 4. (Color online) Shifts in V_{fb} of Au/HfSiON/Si capacitors prepared by hydrogen radical cleaning before Au electrode deposition. The V_{fb} shift was plotted as a function of exposure time under air (in air), vacuum (vac.), dry nitrogen (N_2), or oxygen (O_2). In addition, some samples were dipped into de-ionized water for a certain time (H_2O) before C - V measurement.

dependent and time-dependent decreases in V_{fb} of the Au/HfSiON/Si capacitors, which were treated in hydrogen radical before Au deposition. We found that in the case of the exposure to air (filled black circles), although the Au-Hf hybridization induced increase in V_{fb} was observed right after the Au deposition, the shift in V_{fb} gradually decreased and reached zero after the exposure to air for almost 1 day. When the metal/high- k capacitors were kept in vacuum after Au deposition or when they were kept in dry nitrogen (or dry oxygen), the interface dipole was found to be stable even for 3 days, whereas it decreased after exposure to air as indicated by open triangles and squares in Fig. 4. Moreover, we found that the decrease in the interface dipole moment was drastically accelerated when the capacitor was dipped in de-ionized water (open circles). These findings clearly demonstrate that the WF of Au in contact with the HfSiON is strongly dependent on the interface hybridization and imply that the decrease in interface dipole moment is not affected by dry oxygen and dry nitrogen but is affected by the OH species diffused through the gate electrode. Namely, the bridging oxygen between Au and Hf atoms releases the interface hybridization to modify WF of Au in contact with the HfSiON.

In conclusion, the WF of Au in contact with the Hf-based oxides was systematically studied and was found to be described by the V_O and ϕ_{CNL}^G models. The decrease in the WF can be explained by the V_O formation in which oxygen transfers from HfSiON to the Si substrate, thereby transferring electrons from the V_O level to the p -metal. In contrast, the anomalous increase in the WF was found to be dominated by Au-Hf hybridization, which crucially depends on fabrication conditions of Au/HfSiON stacks and on exposure ambient and time. These findings demonstrate the importance of fundamental understanding of the WF of gate electrodes in contact with Hf-based oxides for controlling threshold voltage in future metal/high- k devices.

This work was partly supported by the “High- k Network” in cooperation with academic, industrial, and government institutes, the Grants-in-Aid for Scientific Research (Grant Nos. 18036007 and 19019010), and the Yazaki Foundation for Science and Technology.

¹G. D. Wilk, R. M. Wallace, and J. M. Anthony, *J. Appl. Phys.* **89**, 5243 (2001).

²C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin, *Dig. Tech. Pap. - Symp. VLSI Technol.* **2003**, 9.

³E. Cartier, F. R. McFeely, V. Narayanan, P. Jamison, B. P. Linder, M. Copel, V. K. Paruchuri, V. S. Basker, R. Haight, D. Lim, R. Carruthers, T. Shaw, M. Steen, J. Sleight, J. Rubino, H. Deligianni, S. Guha, R. Jammy, and G. Shahidi, *Dig. Tech. Pap. - Symp. VLSI Technol.* **2005**, 230.

⁴M. Koyama, Y. Kamimuta, T. Ino, A. Kaneko, S. Inumiyama, K. Eguchi, M. Takayanagi, and A. Nishiyama, *Tech. Dig. - Int. Electron Devices Meet.* **2004**, 499.

⁵K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Konno, T. Chikyow, H. Kitajima, and T. Arikado, *Jpn. J. Appl. Phys., Part 2* **43**, L1413 (2004).

⁶K. Shiraishi, Y. Akasaka, S. Miyazaki, T. Nakayama, T. Nakaoka, G. Nakamura, K. Torii, H. Furutou, A. Ohta, K. Ohmori, H. Watanabe, T. Chikyow, M. L. Green, Y. Nara, and K. Yamada, *Tech. Dig. - Int. Electron Devices Meet.* **2005**, 43.

⁷Y. Akasaka, G. Nakamura, K. Shiraishi, N. Umezawa, K. Yamabe, O. Ogawa, M. Lee, T. Amiaka, T. Kasuya, H. Watanabe, T. Chikyow, F. Ootsuka, Y. Nara, and K. Nakamura, *Jpn. J. Appl. Phys., Part 2* **45**, L1289 (2006).