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Development of array-type atmospheric-pressure RF plasma generator with electric on–off control for high-throughput numerically controlled processes

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An array-type atmospheric-pressure radio-frequency (RF) plasma generator is proposed for high-precision and high-throughput numerically controlled (NC) processes. We propose the use of a metal-oxide-semiconductor field-effect transistor (MOSFET) circuit for direct RF switching to achieve plasma on–off control. We confirmed that this type of circuit works correctly using a MOSFET with a small parasitic capacitance between its source and gate. We examined the design method for the distance between adjacent electrodes, which corresponds to the parasitic capacitance between adjacent electrodes and is very important in the individual on–off control of each electrode. We developed a prototype array-type plasma generator apparatus with 19 electrodes and the same number of MOSFET circuits; we then confirmed that each electrode could control its plasma on–off state individually. We also demonstrated that the thickness uniformity of the surface Si layer of a silicon-on-insulator wafer could be processed to less than 1 nm peak to valley by the NC sacrificial oxidation method using the apparatus. *Published by AIP Publishing.* [<http://dx.doi.org/10.1063/1.4964656>]

I. INTRODUCTION

Nanometer-level accuracy is required for leading-edge optical devices and semiconductor wafers for high-performance electronic and photonic devices. In the case of hard X-ray focusing aspherical mirrors, to produce a sub-10-nm spot diameter, the figure error must be less than 1 nm over a length of approximately 100 mm in the longitudinal direction.¹ In the case of a next-generation silicon-on-insulator (SOI) wafer, the thickness distribution of the top thin silicon layer should have a peak-to-valley (P–V) value of less than 1.0 nm over the entire surface of a 450-mm wafer.² Deterministic processing methods, such as ion beam figuring (IBF),^{3,4} numerically controlled (NC) elastic emission machining (EEM),⁵ plasma jet machining (PJM),^{6,7} electrical discharge machining (EDM),^{8,9} NC plasma chemical vaporization machining (PCVM),^{10–12} local wet etching (LWE),¹³ NC sacrificial oxidation,^{14,15} and others, have been developed to achieve such accuracy. Although the processing mechanisms of these machining methods differ, they all consist of two components: a processing head that can process small areas, ranging in diameter from approximately the sub-millimeter range to several millimeters and an X–Y table system that enables the processing head to scan the whole area of a workpiece at a controlled feed speed. Nanometer-level accuracy can be achieved by precise dwell time control of the processing head with a calculated feed speed using

pre-measured figure error data and the removal shape of the processing head without scanning the table. For example, the figure error of an aspherical X-ray mirror can be reduced to approximately 2 nm using NC-EEM¹⁶ and that of an X-ray focusing mirror can be reduced from 61.5 nm to 5.8 nm using IBF.¹⁷ The thickness distribution of the thin silicon layer of an SOI wafer can be reduced from 2.4 nm P–V to 0.9 nm P–V using NC sacrificial oxidation.¹⁸ However, because these methods take a long time for a processing head to scan the whole surface of a workpiece, especially in the case of a workpiece that is much larger than the processing head, it is difficult to apply these methods to mass-production methods. We therefore propose the use of array-type processing heads as an alternative to the use of a single scanning processing head (Fig. 1). Many processing heads are arranged closely together to cover the whole surface, and the processing time of each head can be controlled individually. In the case of a process that relies on the use of atmospheric-pressure plasma, this concept can be implemented by placing many isolated electrodes for plasma generation facing the surface of the workpiece.

According to this method, the spatial resolution of the process depends not only on the size of the electrode but also on the distance between the electrodes and the workpiece. This means that the greater the distance is between the electrodes and the workpiece, the more extensive the plasma under the electrode is, due to broadening of the electric field over the edge of the electrode. An array-type atmospheric-pressure plasma generator whose plasma switching mechanism is lifted up and down to each electrode to make the electric field intensity of each plasma region weaker and stronger was developed in this study and used to demonstrate NC sacrificial

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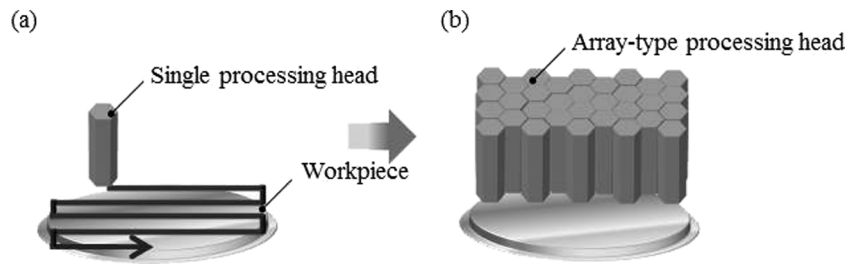


FIG. 1. (a) Schematic of the raster-scan NC processing system with single processing head and (b) schematic of high-throughput simultaneous NC processing system with array-type processing heads.

oxidation processing (Fig. 2(a)).¹⁹ However, the apparatus needs a flat insulator plate between the electrodes and the workpiece to maintain laminar flow of the process gas because of the unevenness of the electrode surface associated with changing the distance between the electrode and the work surface during the NC process. Moreover, the insulator plate must be thick to prevent distortion due to its own weight and the thermal stress from the plasma heat. Because of the existence of the thick insulator, the distance between the electrodes and the workpiece could not be close, so the spatial resolution of the process became greater than the size of the electrode.

We therefore propose a novel array-type atmospheric-pressure plasma generator that can control the on–off state of plasma by an electrical switch circuit, which eliminates the need for an insulator plate because the surface of the electrode module is always flat (Fig. 2(b)). Using this method, the spatial resolution of the process is comparable to the electrode size. In this paper, we describe how to design an array electrode system with an electrical switch, we describe its processing characteristics, and we present a demonstration of the NC process.

II. SYSTEM DESIGN

A. Plasma switching circuit

Figure 3(a) shows the electric circuit connected to each plasma-generated electrode. We used a metal-oxide-semiconductor field-effect transistor (MOSFET) as the switching device. MOSFETs need to be connected in series to control radio-frequency (RF) power because a MOSFET has a parasitic diode. The on and off of the gate voltage of a MOSFET is controlled by a personal computer (PC). As shown in Figs. 3(b)

and 3(c), MOSFETs can be treated as resistors when they are on-state and as capacitors when they are off-state. Because of the capacitance, RF power may be transmitted through a MOSFET even when the gate voltage is off-state. Therefore, the MOSFET must not only be able to withstand high voltage but also have low electrical capacitance. We identified an N channel MOSFET STN1NK60Z (STMicroelectronics) as a commercially available MOSFET that met these requirements. We prepared an atmospheric-pressure plasma generator with one electrode and one switching circuit, as shown in Fig. 4. The distance between the electrode and the workpiece was 200 μm , the process gas was an $\text{He}:\text{O}_2 = 99:1$ gas mixture, and the workpiece was an Si (110) wafer. After purging the gas to the reaction chamber for 5 min, plasma was generated to turn the mechanical relay (OMRON G5V-2) for the gate voltage application on and apply 13.56-MHz RF power (Noda RF technologies NR1NP) to the electrode. Also, the impedance matching circuit is needed to connect between RF power and electrodes because the reflected power and the output power dropping must be prevented. To check the on–off state of the plasma by detecting light from the plasma, a light-detecting circuit with a photodiode was positioned at the place exposed to the light from the plasma, as shown in Fig. 4. In our proposed NC plasma process, plasma is generated under all electrodes in the initial state, and the plasma is dispersed in the order that the areas reach the required process time. Therefore, we evaluated the time lag between the turn-off command from the PC and the actual turn-off moment of the plasma. Figure 5 shows an example of a comparison of the output of the photo sensor and relay signal to the apply-gate voltage of the MOSFET on the same time axis. The observed time lag of approximately 4 ms was considered the response delay of the relay. Because the possible control time scale for the NC plasma process is 1 s, such a time lag has no effect on the process.

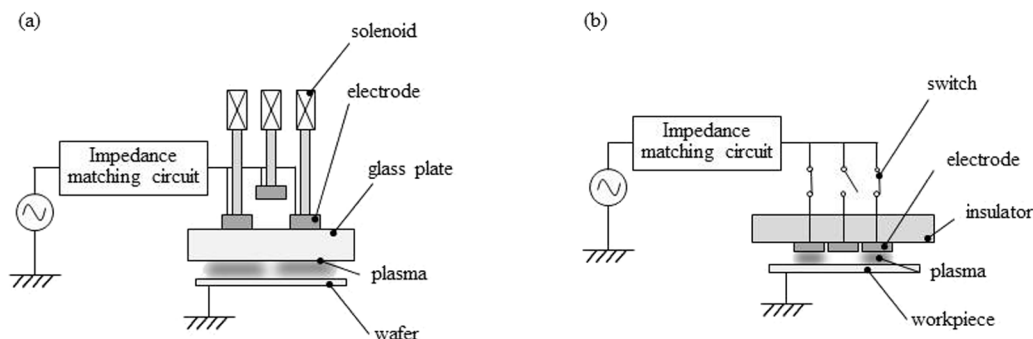


FIG. 2. Schematic of plasma switching method by (a) distance control between the electrode and the workpiece and (b) direct RF switch.

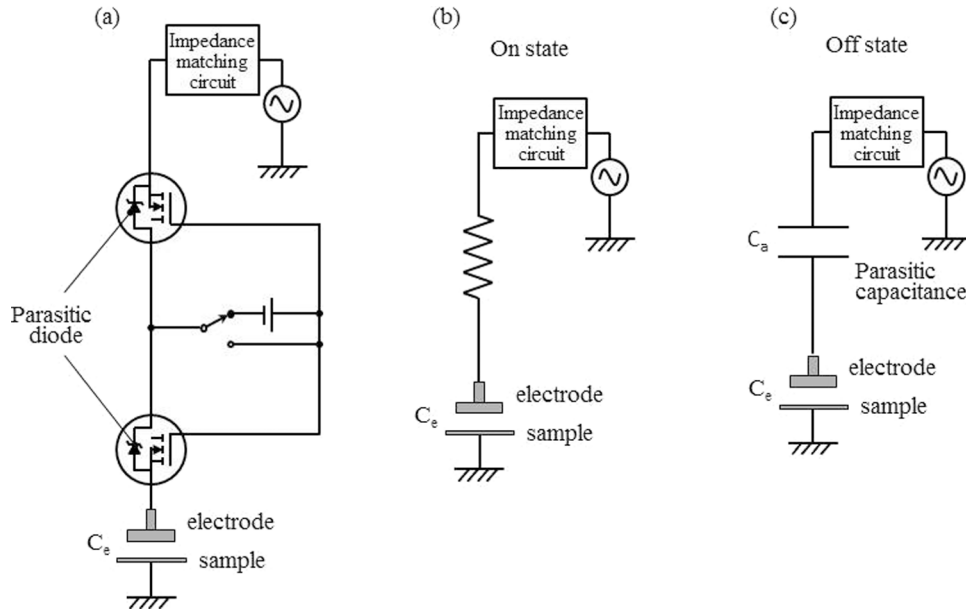


FIG. 3. (a) Schematic of the electrical circuit with MOSFET in series: (b) on-state and (c) off-state.

B. Consideration of the distance between electrodes

The distance between adjacent electrodes is very important in individual plasma switching. Figure 6(a) shows a schematic model of two neighboring on-state and off-state electrodes, and Fig. 6(b) shows the equivalent circuit for this model. C_1 and C_2 are the electric capacitance between the electrodes and the electric capacitance between the electrode and the surface of the sample, respectively. When an on-state electrode receives an applied voltage V , the voltage of the other electrode V' can be expressed as follows:

$$V' = \frac{C_1}{C_1 + C_2} \cdot V. \quad (1)$$

To design a plasma generator to maintain electric independence, V' should be less than the threshold voltage of plasma generation V_{th} . Therefore, it is necessary to satisfy the following equation:

$$V_{th} \geq V' = \frac{C_1}{C_1 + C_2} \cdot V, \quad (2)$$

and Eq. (2) can be rewritten as follows:

$$\frac{V - V_{th}}{V_{th}} \leq \frac{C_2}{C_1}. \quad (3)$$

This equation shows that how high a voltage above the threshold voltage can be applied depends on the C_2/C_1 ratio. In other words, the smaller C_1 is with respect to C_2 , the higher the voltage is that can be applied to the electrode. The electric capacitance between electrodes C_1 can be expressed as follows:

$$C_1 = \frac{\epsilon S}{d} + A, \quad (4)$$

where S is the faced area between electrodes, d is the distance between electrodes, ϵ is the permittivity in air, and A is the floating capacity, which does not depend on the distance between the electrodes. When Eq. (4) is substituted into Eq. (3), the fulfillment requirement can be expressed as follows:

$$\frac{V - V_{th}}{V_{th}} \leq \frac{C_2}{\frac{\epsilon S}{d} + A}. \quad (5)$$

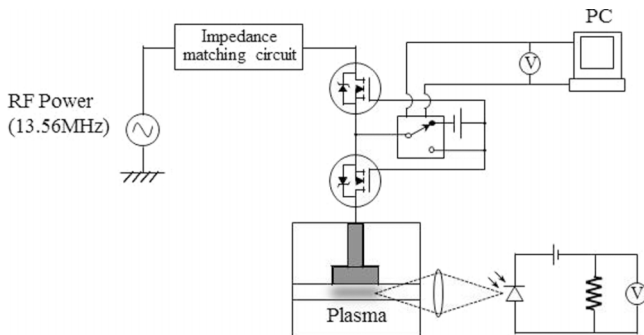


FIG. 4. Schematic of the setup for operation test of plasma switching using MOSFET controlled by PC.

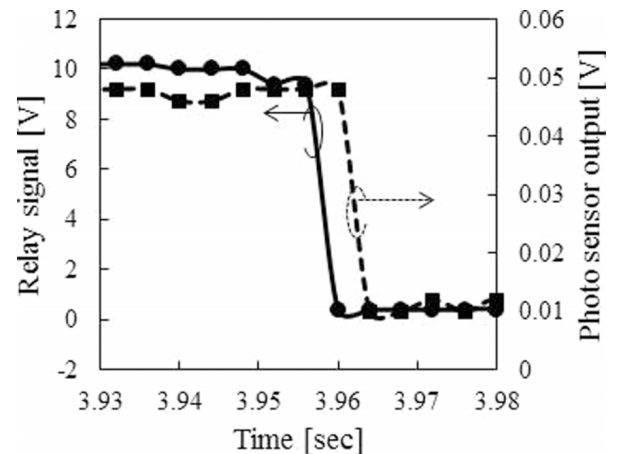


FIG. 5. Turn-off characteristics of plasma. The solid line indicates the relay signal (PC command), and the dashed line indicates the photodiode voltage in the light-detecting circuit.

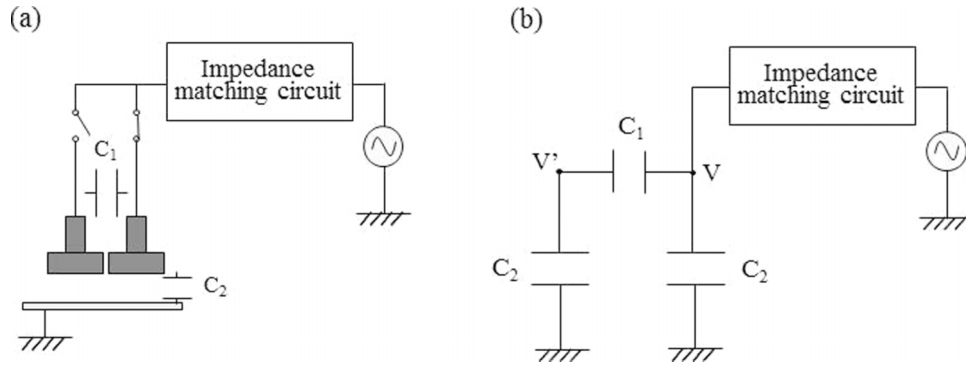


FIG. 6. (a) Schematic of two-electrode model (one is in the on-state and the other is in the off-state) and (b) the equivalent circuit of adjacent electrodes. There are electric capacitances between the electrodes (C_1) and between the electrode and the workpiece (C_2).

Therefore, the distance d between the electrodes should be designed to satisfy Eq. (5) once the required voltage V is determined.

C. Design of d

To design d using Eq. (5), V_{th} and A should be known. Figure 7 shows a schematic of the basic experimental setup in which d can be changed arbitrarily to determine V_{th} and A experimentally. The right electrode E_1 is fixed in the apparatus, and power is applied directly from the RF (13.56-MHz) power source. An RF voltage sensor installed on electrode E_1 can measure the voltage applied to the electrode E_1 . The left electrode E_2 is not hooked up to the power source but can move to the right and left with 10- μm accuracy using the micrometer head attached to electrode E_2 . The He:O₂ = 99:1 mixed gas was used as a process gas with a gas flow rate of 0.5 slm. When the distance between electrode E_1 and E_2 was too short, plasma was generated under the areas of both electrode E_1 and E_2 because RF power was transmitted from E_1 to E_2 through the parasitic capacitance C_1 , whereas when E_2 was located at a sufficient distance from E_1 , the plasma under the area of E_2 disappeared, and plasma continued to be generated under the area of E_1 . We measured the distance between electrodes when the plasma under the area of E_2 disappeared, gradually taking

E_2 away from E_1 on each voltage. Figure 8 shows the relation between the distance d when the plasma under electrode E_2 is dispersed and the applied voltage V . C_2 can be calculated to be 2.1 pF based on the geometric conditions, and Eq. (5) can be rewritten as follows:

$$\frac{V - V_{th}}{V_{th}} = \frac{2.1}{\frac{0.143}{d} + A}. \quad (6)$$

Based on the results shown in Fig. 8, V_{th} and A can be found to be 284.9 V and 5.55 pF, respectively, by curve fitting using Eq. (6).

Although we considered a model for two electrodes, each electrode would be surrounded by several electrodes in an array-type apparatus. When one electrode is surrounded by n pieces of electrodes, C_1 is determined as follows:

$$C_1 = n \frac{\epsilon S}{d} + A, \quad (7)$$

and using Eq. (5), the distance d can be obtained as follows:

$$d \geq \frac{n \epsilon S (V - V_{th})}{C_2 V_{th} - n A (V - V_{th})}. \quad (8)$$

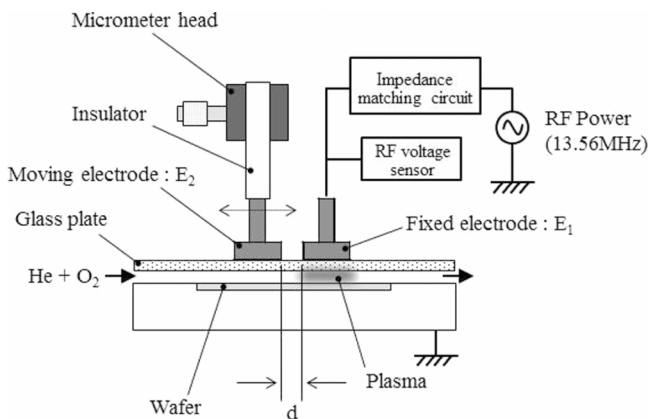


FIG. 7. Schematic of the setup for changing the distance between adjacent electrodes using micrometer in 10- μm increments (where d is the distance between electrodes).

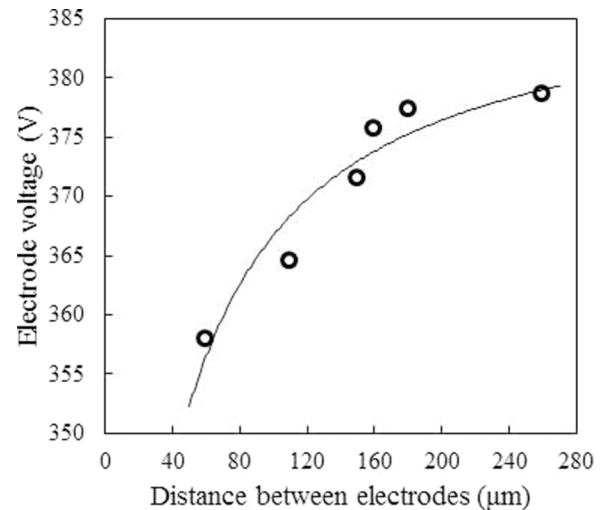


FIG. 8. Relationship between the electrode voltage and the distance between electrodes when plasma is dispersed under the electrode not hooked up (E_2).

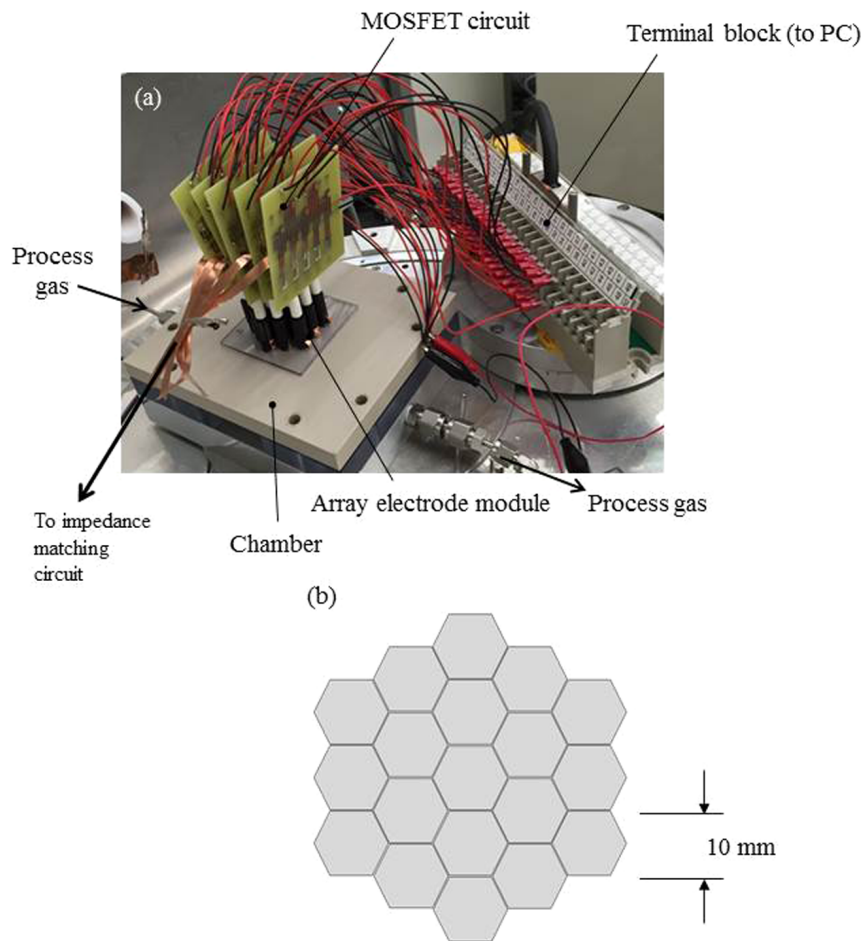


FIG. 9. (a) Photograph of the entire setup. Many MOSFET circuits are connected on the upper side of the electrode module, and they are connected to the terminal block for control of the gate voltage of the MOSFET by the PC. (b) Electrode layout. The bottom shape is hexagonal, and the side-to-opposite-side dimension is 10 mm.

III. PROTOTYPE ARRAY ELECTRODE

To demonstrate an NC process using the proposed array-type atmospheric-pressure plasma generator, we developed a prototype apparatus with 19 hexagonal-array electrodes whose side-to-opposite-side length was 10 mm, as shown in Fig. 9. The electric switching circuit using the MOSFET to control the on-off of the plasma was connected to each electrode, and the distance between adjacent electrodes was

designed to be $300\ \mu\text{m}$ larger than the one from the fitting routine using Eq. (8) to allow a margin. We first performed an experiment to confirm the independence of each electrode, using the on-off pattern shown in Fig. 10(a) in which the gray electrodes were in the on-state and the white electrodes were in the off-state. The electrical power was 110 W, and the gap between the electrodes and the sample was $200\ \mu\text{m}$. We used the $\text{He}:\text{O}_2 = 99:1$ mixed gas as the process gas, and the gas flow rate was 0.2 slm during oxidation. The oxidation time

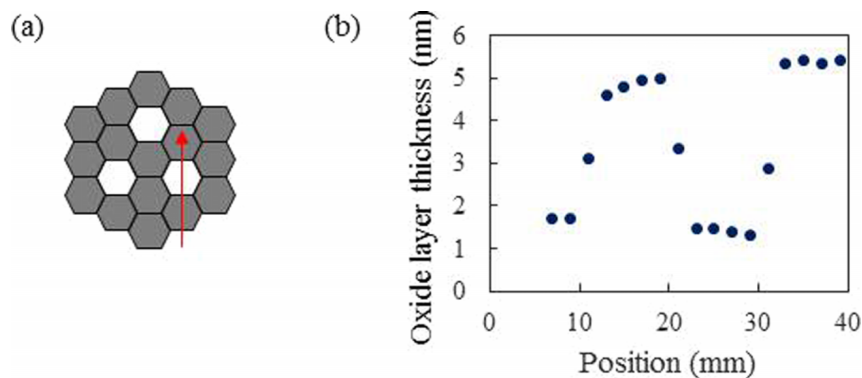


FIG. 10. (a) On-off pattern of the electrode. The gray electrodes were on-state, and the white electrodes were off-state. (b) Oxide layer thickness distribution along the arrow shown in (a).

was 5 min. The oxide layer thickness was measured using a spectroscopic ellipsometer (SOPRA GES-5M) operating at wavelengths of 300–700 nm. Figure 10(b) shows the oxide layer thickness distribution at the point indicated by the arrow in Fig. 10(a). An oxide layer approximately 5 nm thick was formed under the on-state electrodes, and the oxide layer thickness under the off-state electrodes was equal to the natural oxide thickness. As the results show, plasma was not generated in the area surrounded by the on-state electrodes.

We next investigated the oxidation rate of this setup. The RF power was 130 W, and the other experimental conditions were the same as in the previous experiments. Figure 11 is a graph of the oxidation of the oxide layer thickness over time. The slope of the relation was relatively steep during the first 3 min and gradually became more moderate. The oxide layer thickness was approximately 6 nm after 10 min. We investigated the oxidation characteristics of all of the electrodes because of the individual differences of the switching circuits. We also conducted an NC oxidation experiment using these oxidation characteristics. Commercially available 8-in SOI wafers cut into $65 \times 65 \text{ mm}^2$ sizes were used as workpieces, and the required oxidation time of each area was calculated based on the surface Si layer thickness distribution, measured by spectroscopic ellipsometry, and the oxidation characteristics of each electrode. As Fig. 12 shows, we succeeded in improving the P–V

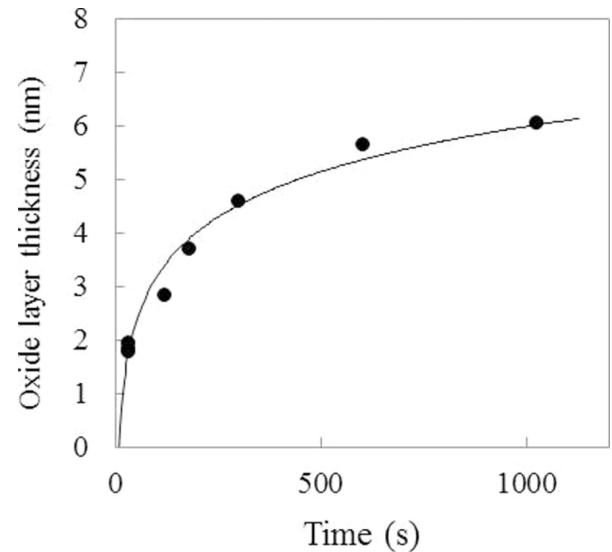


FIG. 11. Example of the oxidation of an electrode. The oxidation rate is very high at the beginning of the process, but it is saturated at approximately 6 nm.

value of the surface Si layer thickness distribution from 2.84 nm to 0.84 nm. The results show that NC processes can be performed using array-type atmospheric-pressure plasma with a MOSFET switching circuit connected to each electrode.

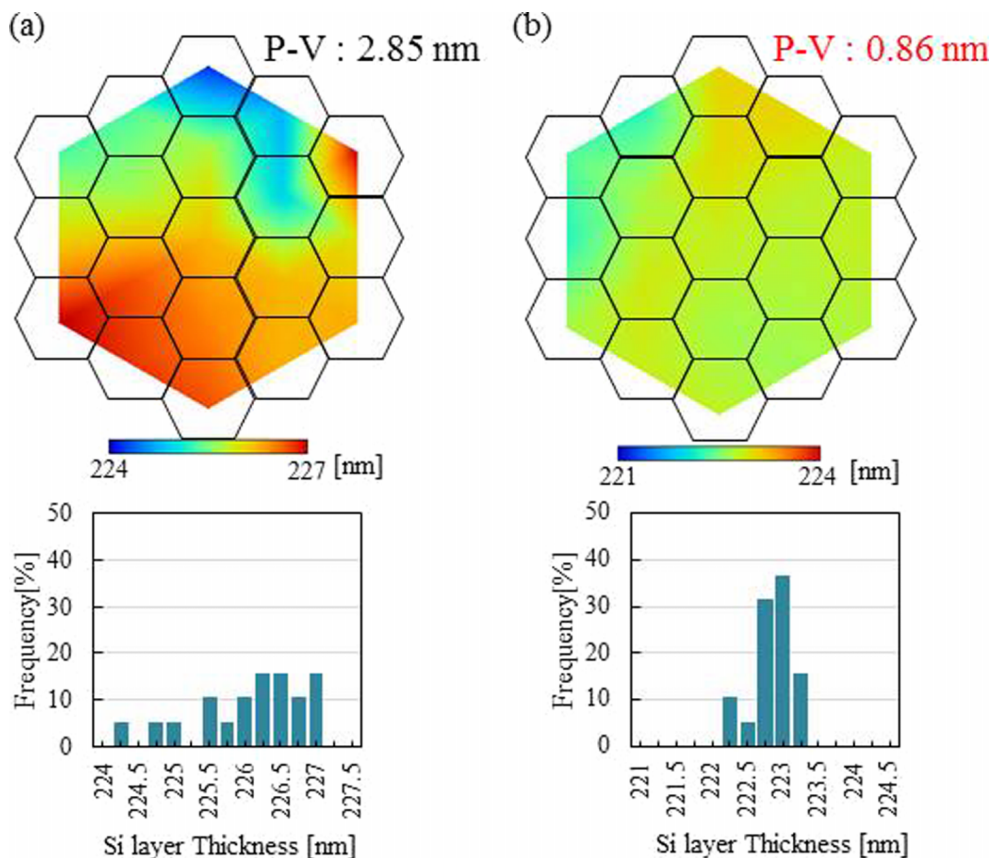


FIG. 12. The surface Si layer thickness distribution (a) before and (b) after the NC process. The hexagonal solid lines show the position of the electrodes. The thickness was measured at the center of each hexagon, and the thicknesses between the centers were calculated by interpolation. The graphs show histograms of the Si layer thickness distribution.

IV. CONCLUSIONS

In this paper, we proposed an array-type atmospheric-pressure plasma generator with a MOSFET switching circuit for use in achieving high-precision and high-throughput NC processes, and we described the development of a prototype 19-electrode system used successfully for NC plasma oxidation. The results of this study show that this is a promising approach to plasma generation for high-precision and high-throughput NC processes, especially for large-area workpieces. When the target is the surface Si layer of an SOI wafer, a side-to-opposite-side electrode size of 10 mm is sufficiently small. However, using a smaller switching circuit, it is possible to make electrodes smaller and thereby improve the space resolution of the process. Except that the one electrode processed area can be narrower when RF power is lower, and the unprocessed area may be induced between electrodes. In the future, this problem will be able to be solved by optimization of RF power and the distance between electrodes and the sample. It will be needed to examine the relation between RF power, the distance between electrodes and the sample, and the spread of atmospheric-pressure plasma. This technique is expected to be applicable in a wide range of fields, such as figure error correction of aspherical lenses in consumer products, thickness uniformization of thin crystals for resonators, and film thickness adjustment for all types of thin films for flat-panel displays.

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- ¹H. Yumoto, H. Mimura, S. Handa, T. Kimura, S. Matsuyama, Y. Sano, H. Ohashi, K. Yamauchi, and T. Ishikawa, *Nucl. Instrum. Methods Phys. Res., Sect. A* **616**(2-3), 203–206 (2010).
- ²See <http://www.itrs2.net/2011-itrs.html> for ITRS, Front End Processes, 2011.
- ³L. N. Allen and H. W. Romig, *Proc. SPIE* **1333**, 22 (1990).
- ⁴F. Frost, R. Fechner, B. Ziberi, D. Flamm, and A. Schindler, *Thin Solid Films* **459**, 100 (2004).
- ⁵Y. Mori, K. Yamauchi, and K. Endo, *Precis. Eng.* **9**, 123–128 (1987).
- ⁶Th. Arnold, G. Bohm, and H. Paetzelt, *Contrib. Plasma Phys.* **54**, 145–154 (2014).
- ⁷J. Meister and T. Arnold, *Plasma Chem. Plasma Process.* **31**, 91–107 (2011).
- ⁸K. H. Ho and S. T. Newman, *Int. J. Mach. Tool. Manuf.* **43**, 1287–1300 (2003).
- ⁹M. Kunieda, A. Hayasaka, X. D. Yang, S. Sano, and I. Araie, *CIRP Ann. Manuf. Technol.* **56**, 213–216 (2007).
- ¹⁰Y. Mori, K. Yamamura, and Y. Sano, *Rev. Sci. Instrum.* **71**, 4620 (2000).
- ¹¹Y. Mori, K. Yamauchi, K. Yamamura, and Y. Sano, *Rev. Sci. Instrum.* **71**, 4627 (2000).
- ¹²Y. Sano, K. Yamamura, H. Mimura, K. Yamauchi, and Y. Mori, *Rev. Sci. Instrum.* **78**, 086102 (2007).
- ¹³K. Yamamura, *Ann. CIRP* **56**, 541 (2007).
- ¹⁴H. Paetzelt, T. Arnold, G. Bohm, F. Pietag, and A. Schindler, *Plasma Processes Polym.* **10**, 416–421 (2013).
- ¹⁵Y. Sano, T. Masuda, H. Mimura, and K. Yamauchi, *J. Cryst. Growth* **310**, 2173–2177 (2008).
- ¹⁶S. Matsuyama, N. Kidani, H. Mimura, J. Kim, Y. Sano, K. Tamasaku, Y. Kohmura, M. Yabashi, T. Ishikawa, and K. Yamauchi, *Proc. SPIE* **8139**, 813905 (2011).
- ¹⁷M. Idir, L. Huang, N. Bouet, K. Kaznatcheev, M. Vescovi, K. Lauer, R. Conley, K. Rennie, J. Kahn, R. Nethery, and L. Zhou, *Rev. Sci. Instrum.* **86**, 105120 (2015).
- ¹⁸Y. Sano, T. Masuda, S. Kamisaka, H. Mimura, S. Matsuyama, and K. Yamauchi, *IEEE Int. SOI Conf.* 165–166 (2008).
- ¹⁹H. Takei, K. Yoshinaga, K. Matsuyama, S. Yamauchi, and Y. Sano, *Jpn. J. Appl. Phys.* **54**, 01AE03 (2015).