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Fabrication of ultrathin and highly uniform silicon on insulator by numerically controlled plasma chemical vaporization machining

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Metal-oxide semiconductor field-effect transistors fabricated on a silicon-on-insulator (SOI) wafer operate faster and at a lower power than those fabricated on a bulk silicon wafer. Scaling down, which improves their performances, demands thinner SOI wafers. In this article, improvement on the thinning of SOI wafers by numerically controlled plasma chemical vaporization machining (PCVM) is described. PCVM is a gas-phase chemical etching method in which reactive species generated in atmospheric-pressure plasma are used. Some factors affecting uniformity are investigated and methods for improvements are presented. As a result of thinning a commercial 8 in. SOI wafer, the initial SOI layer thickness of 97.5±4.7 nm was successfully thinned and made uniform at 7.5±1.5 nm. © *2007 American Institute of Physics.* [DOI: 10.1063/1.2766836]

A silicon-on-insulator (SOI) wafer is a suitable substrate for next-generation semiconductor integrated circuits. Metal-oxide semiconductor field-effect transistors (MOSFETs) fabricated on a SOI wafer operate faster and at a lower power than those fabricated on a bulk silicon wafer. Scaling down, which improves their performances, demands thinner SOI wafers. A SOI layer of less than 20 nm is required for the dynamic random access memory (DRAM) half-pitch node of 50 nm.[1] In addition, the deviation of the thickness is required to be within ±5% because of the need for threshold voltage uniformity.

To fabricate such an ultrathin and highly uniform SOI wafer, conventional polishing methods cannot be applied. Thermal expansion and mechanical vibration render precise thickness control impossible. In addition, a crystallographically deformed layer is introduced into the machined surface because plastic deformation or brittle fracture is utilized as a machining mechanism. We therefore propose the thinning of a SOI layer by numerically controlled plasma chemical vaporization machining (NC-PCVM). PCVM (Ref. 2 and 3) is a gas-phase chemical etching method using reactive species generated in localized atmospheric-pressure plasma. It produces no crystallographic damage on machined surfaces. In NC-PCVM, figuring is performed by controlling the dwelling time of the plasma so that a precise figuring higher than 1 nm is possible as long as the depth to be removed is known with sufficient accuracy. Although the result of thinning a SOI layer to approximately 100 nm by plasma-assisted chemical etching[4] (PACE) has already been reported,[5] there are no results on such thinning up to the order of 10 nm. We have already tried to thin a commercial 6 in. SOI wafer. Although the SOI layer thickness of approximately 200±4 nm has successfully thinned to 13±2 nm using NC-PCVM,[5] this accuracy is still not satisfactory. In this article, some factors affecting uniformity were investigated to obtain a thinner and more uniform SOI layer.

The NC-PCVM system, which was used in this experiment, was described in detail elsewhere.[6,7] It has a sphere-type rotary electrode with a diameter of 200 mm for plasma generation and has a worktable on the *X* and *Y* axes for numerical control. Gas of the composition $He:CF_4:O_2 = 99.98:0.01:0.01$ was used to a chamber up to atmospheric pressure, after evacuating the chamber of air. The machining gap between the electrode and the work was 600 μm, and the supplied rf power was 250 W. The plasma under this condition was approximately 20 mm in diameter. To evaluate the uniformity of machining, a raster scan at a constant velocity was performed on the entire wafer. By scanning at a constant velocity, the removal thicknesses of all the entire wafer should be the same. If a nonuniform removal thickness is observed, it should be researched and improved. The thickness distribution of the SOI layer was measured by spectroscopic ellipsometry (SPORA, GESP-5). The distribution of the machined SOI layer was calculated by subtracting the machined thickness of the SOI layer from the premachined thicknesses.

Firstly, an influence of the chuck plate was investigated. In the course of experiments, some spots with a radius of about 10 mm were observed on the machined SOI wafer. Spectroscopic ellipsometry showed that they form an area whose SOI layer was thicker than that of the surrounding area. It means that the removal thickness of the area was less than that of the surrounding area. They appeared at the same location on the wafer even in different experiments. Thus, we thought that the cause of that is the chuck plate. A vacuum chuck system can be used in the NC-PCVM system because PCVM is carried out at atmospheric pressure. The chuck plate was made of aluminum. The surface of the chuck plate was mirror finished by diamond turning to prevent gas leakage. We found that just under each spot on the SOI wafer, there was a small projection on the chuck plate. Figure 1 shows an example. Figure 1(a) shows a spot and Fig. 1(b) a projection with a height of 12 μm on the chuck plate just under the spot. We also found that each spot disappeared when the projection was removed by additional polishing. Thus, it was clarified that a small projection on the chuck plate causes a decrease in SOI layer removal thickness and forms thicker SOI layer, which result in a spot. Figure 1(c)

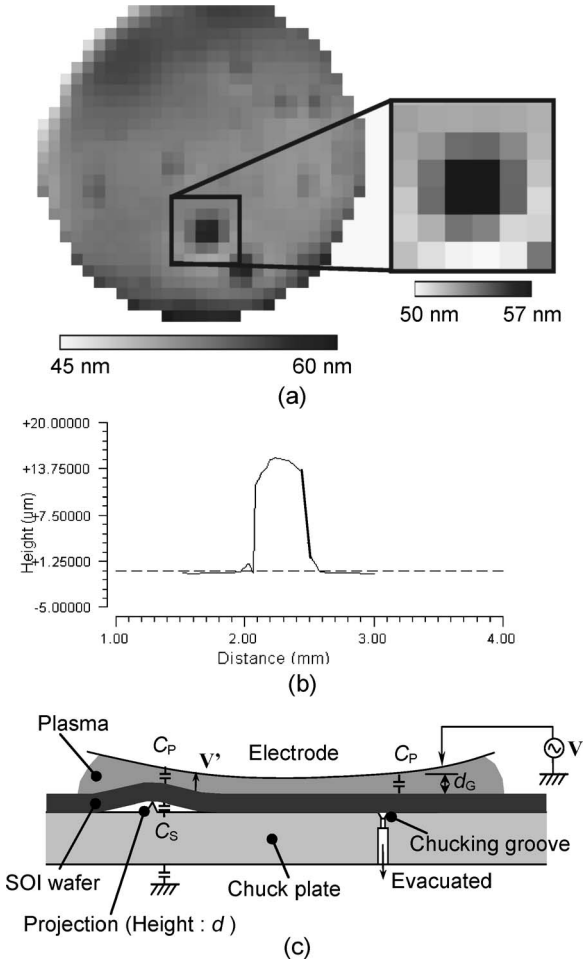

FIG. 1. (a) Example of spot, (b) projection on chuck plate just under spot, and (c) model of chuck plate and wafer.

shows a model of the chuck plate and wafer. Although the in-plane projections was very small (less than 0.5 mm in diameter) compared with the spots, interspaces between the chuck plate and the wafer seem to be generated by the elastic deformation of the wafer. When the power voltage V is supplied to the electrode, the power voltage of the area above the projection, V', is expressed as

$$V' = [C_S/(C_P + C_S)]V = \{1/[1 + (d/(d_G - d)]\varepsilon_r)\}V, \quad (1)$$

where C_S is the capacitance per unit area between the chuck plate and the back side of the wafer, C_P is the capacitance per unit area in the plasma, ε_r is the relative permittivity, d is the height of the projection, and d_G is the machining gap between the electrode and the wafer. Using both d =0.012 mm and d_G=0.6 mm, the ratio of V' to V is expressed as

$$V'/V = 1/(1 + 0.020\varepsilon_r). \quad (2)$$

If there is no plasma (i.e., ε_r=1), the ratio is 98%, which is not so effective for plasma condition. In contrast, if there is plasma and the relative permittivity of the plasma is approximately 10, the ratio decreases to 83%, which seems to be a sufficient decrease for the reduction of the removal depth of the SOI layer. Such projections on the chuck plate seem to be generated during wafer changing and are difficult to prevent. Thus, some better methods of improving the chuck plate should be considered. We suggest inserting a porous polytetrafluoroethylene (PTFE) sheet between the chuck plate and the wafer, so that it can absorb projections and prevent the generation of an interspace around the projections. By simply inserting a sheet with a thickness of 50 μm, no spots were seen anymore.

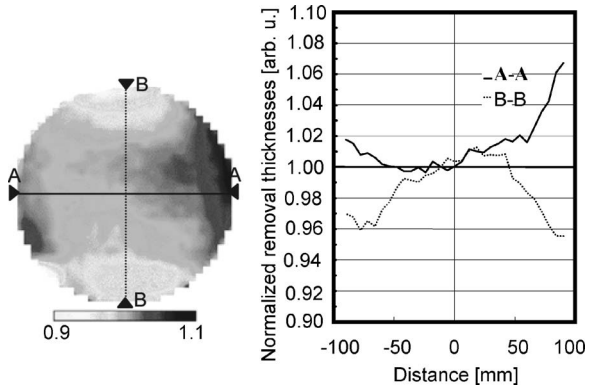

FIG. 2. Distribution of normalized removal thicknesses of 8 in. SOI wafer without any improvements.

Secondly, the distribution of removal thicknesses was investigated using a commercial 8 in. SOI wafer as a sample. Figure 2 shows the distribution of normalized removal thicknesses. Clearly, a saddle-shaped distribution was observed, which was a reproducible result. We checked the vertical accuracy of moving the *X-Y* worktable because a variation in machining gap could change the plasma state and induce nonuniform removal. However, the motion error was about 10 μm, which was negligible compared with the machining gap. We focused on the change in equivalent circuit constant with the moving of the *X-Y* worktable. Figure 3(a) shows an electrical model in the region of the electrode and worktable.

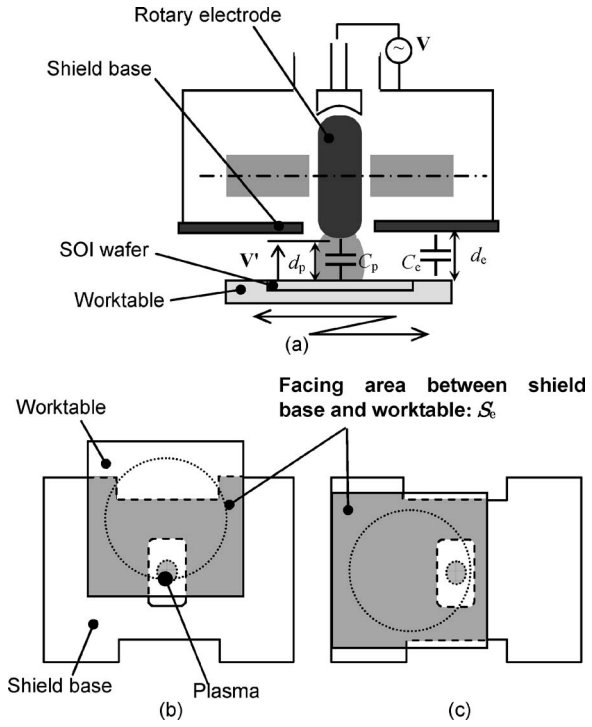

FIG. 3. (a) Electrical model of region of electrode and worktable, (b) worktable position with the smallest area facing the shield base, and (c) that with the largest area facing it.

TABLE I. Calculated results of V'/V in both worktable positions shown in Figs. 3(b) and 3(c).

Case	I	II	III	IV
Position	Fig. 3(b)	Fig. 3(c)	Fig. 3(b)	Fig. 3(c)
d_e (mm)	2.5		0.4	
S_e (cm^2)	512	1024	512	1024
V'/V	0.77	0.87	0.96	0.98
$\Delta V'/V$	0.1 (10%)		0.02 (2%)	

The electrode is covered with a shield to prevent rf radiation. There is a hole at the center of the shield base, from which the electrode faces the worktable. The worktable is electrically connected to the shield base by capacity coupling. The capacitance C_e for coupling is expressed as

$$C_e = \varepsilon_0 (S_e/d_e), \tag{3}$$

where ε_0 is the permittivity of vacuum, d_e is the distance between the shield base and the worktable, and S_e is the area of the shield base facing the worktable, which changes with the position of the worktable [Figs. 3(b) and 3(c)]. When the power voltage V is supplied to the electrode, the power voltage between the electrode and the worktable, V', is expressed as

$$V' = [C_e/(C_e + C_p)]V = [1/(1 + C_p/C_e)]V, \tag{4}$$

where C_p is the capacitance of the plasma, which is simply calculated using the diameter of the plasma (20 mm), the machining gap (0.6 mm), and the relative permittivity of the plasma (10). Table I shows the calculated results of V'/V in both worktable positions shown in Figs. 3(b) and 3(c) (cases I and II, respectively). There was an approximately 10% difference in them. We thought that this difference is the cause of the distribution of normalized removal thicknesses. To reduce this difference, we tried to increase C_e by decreasing d_e. The calculated results are shown in the same table (cases III and IV). By reducing d_e from 2.5 to 0.4 mm, the difference in V' as a result of changing the position of the worktable could be reduced to 2%. Another machining experiment was performed after reducing the gap between the shield base and the worktable to 0.4 mm. As a result, there was no saddle-shaped distribution, and uniform removal thickness was obtained.

Finally, a commercial 8 in. SOI wafer was used for the demonstration of thinning by NC-PCVM. The initial thickness distribution of the SOI layer and its histogram are shown in Fig. 4(a). The deviation of thickness was 97.5±4.7 nm in the area of Φ190 mm and the standard deviation was 2.4 nm. Figure 4(b) shows those of the thinned SOI wafer. The thickness was successfully thinned to 7.5 nm

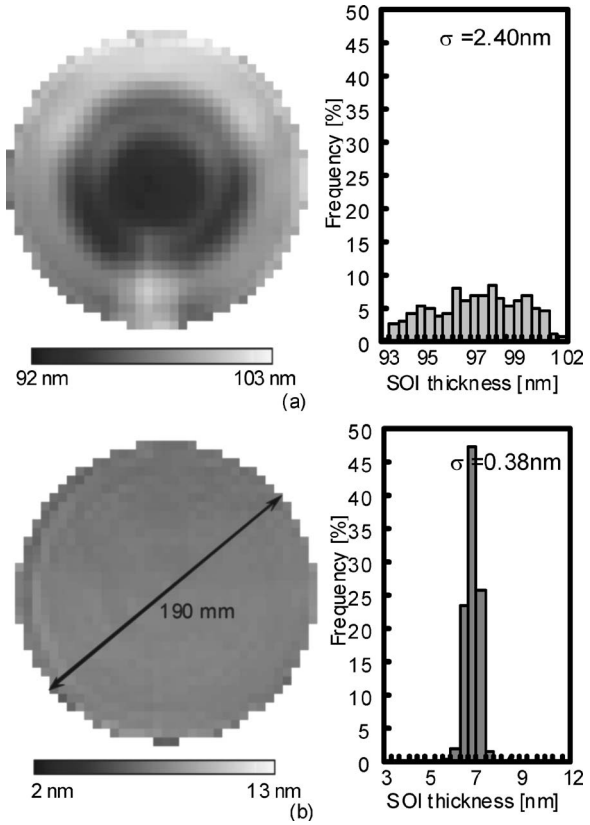

FIG. 4. Thickness distribution of SOI layer and its histogram, (a) initial SOI wafer and (b) thinned SOI wafer.

and the deviation was improved to plus or minus 1.5 nm. The standard deviation was also improved to 0.38 nm. It is clear that the initial thickness distribution was corrected with high accuracy.

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