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Reduction of interface and oxide traps in SiO_2/GaN MOS structures by oxygen and forming gas annealing

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The effect of post-deposition annealing on the electrical characteristics of SiO_2/GaN MOS devices was investigated. While the key to the improvement was using oxygen annealing to form an interfacial GaO_x layer and forming gas annealing to passivate the remaining defects, caution must be taken not to produce fixed charge through reduction of the GaO_x layer. By growing the GaO_x layer with oxygen annealing at 800°C and performing forming gas annealing at a low temperature of 200°C, it became possible to suppress the reduction of GaO_x and to reduce the interface traps, oxide traps, and fixed charge simultaneously.

Gallium nitride (GaN) is suited for high-power and high-frequency device applications owing to its superior material properties, such as wide band gap and high breakdown electric field.[1–3] AlGaN/GaN high electron mobility transistors (HEMTs) which rely on two-dimensional electron gases (2DEGs) at the AlGaN/GaN interface have been developed for high-frequency applications.[2,4,5] In addition to Schottky-gate HEMTs,[4–6] metal-insulator-semiconductor (MIS)-gate HEMTs are a promising means to reduce the gate leakage.[6–9] However, HEMTs are usually normally-on because 2DEGs automatically form at the AlGaN/GaN interface due to piezoelectric and spontaneous polarization.

From this perspective, vertical GaN metal-oxide-semiconductor field effect transistors (MOSFETs) are appealing as they may achieve normally-off operation and also operate at high voltages.[10–13] Various dielectrics such as silicon dioxide (SiO_2),[14,15] aluminum oxide (Al_2O_3),[16,17] and aluminum silicate (AlSiO),[18,19] have been investigated for GaN MOS devices. Among them, SiO_2 is extremely thermally stable and has a wide bandgap of about 9 eV. Thus, sufficiently large conduction and valence band offsets form at the SiO_2/GaN interface, which will prevent gate leakage.

To achieve highly reliable and high-performance MOSFETs, optimization of the MOS structure is necessary. It has been reported that the formation of gallium oxide (GaO_x) at the SiO_2/GaN interface is the key to reducing the interface traps.[20–25] During plasma-enhanced chemical vapor deposition (PECVD) of SiO_2 on GaN, a thin GaO_x layer is produced at the interface due to oxidation of the GaN surface by the plasma.[22,24] With post-deposition annealing in an oxygen ambient (O_2-PDA), the GaO_x layer grows further, which reduces the interface state density of the SiO_2/GaN MOS structure to 10^{10} $cm^{-2}eV^{-1}$.[22,24]

However, there is a drawback to GaO_x formation in terms of threshold voltage (V_{TH}) instability. When forming gas annealing (FGA; hydrogen (H_2) annealing) is performed on a SiO_2/GaN MOS structure with a GaO_x layer, the flat band voltage (V_{FB}) shifts toward negative values.[26,27] This is most likely due to generation of positively charged oxygen vacancies through reduction of the GaO_x layer.[26–31] By performing O_2-PDA and FGA under appropriate temperature conditions, it is possible to reduce the interface traps while suppressing the fixed charge generation.[27] Nevertheless, it is unclear whether this strategy can minimize oxide traps as well. Minimization of oxide traps is needed in order to suppress unwanted V_{TH} drift during operation of MOS devices and guarantee long-term reliability.

Therefore, in this study, we further investigated the effect of O_2-PDA and FGA on the interface properties and reliability of GaN MOS devices. We fabricated MOS structures under various annealing conditions to control the oxidation and reduction reactions occurring at the SiO_2/GaN

interface. Interface properties and reliability were characterized through capacitance-voltage (*C-V*) measurements and bias stress tests (or charge injection stress tests), respectively. Our aim was to minimize the interface traps, fixed charge, and oxide traps simultaneously towards the goal of fabricating highly reliable and high-performance GaN MOS devices.

MOS devices were fabricated on freestanding GaN (0001) substrates with *n*-type GaN epilayers ([Si]: 2×10^{16} cm^{-3}). The samples were first cleaned with acetone and 50%-hydrofluoric (HF) acid. After that, SiO_2 was deposited on the GaN by PECVD using a gas mixture of tetraethyl orthosilicate (TEOS) and O_2. In the initial deposition stage, a nitrogen-incorporated SiO_2 layer of about 5-nm thick was formed by introducing nitrogen (N_2) gas into the chamber; this layer prevents Ga from diffusing into the SiO_2 dielectric.[24] Then, a normal SiO_2 layer about 80-nm thick was deposited (total oxide thickness: 85 nm). After the deposition, O_2-PDA was performed at 600–800°C for 30 min, followed by FGA (3% H_2/N_2) at 200–500°C for 30 min. Table 1 describes the annealing conditions of samples prepared in this study. An as-deposited sample without any annealing treatment was also prepared for comparison. For these SiO_2/GaN samples, MOS capacitors with Ni gate electrodes (100 μm in diameter) and Al back contacts were fabricated for electrical characterization.

Figure 1(a) shows the bidirectional *C-V* characteristics of the fabricated SiO_2/GaN MOS capacitors. For the as-deposited sample (as-depo.), a positive V_{FB} shift with respect to its ideal position (dashed line) and clockwise hysteresis were observed in the *C-V* characteristics. This shift was due to the large number of electron traps at the interface. After O_2-PDA at 800°C ($O_2$800), a decrease in the V_{FB} shift as well as hysteresis occurred that was due to the GaO_x growth at the interface.[22,24] However, a significant negative V_{FB} shift was observed when additional FGA was carried out at 500°C ($O_2$800-$H_2$500). This was likely caused by the reduction of the GaO_x layer, which would have formed positive fixed charge related to oxygen vacancies.[26–31] Figure 1(b) describes the impact of O_2-PDA and FGA. While the growth of the GaO_x layer by O_2-PDA is helpful in passivating the interface traps, the layer will produce positive fixed charge when it is subjected to FGA. There are two ways to deal with this situation. The first way is to lower the O_2-PDA temperature to suppress the growth of the GaO_x layer ($H_2$500, $O_2$600-$H_2$500). As shown in Fig. 1(a), a mostly ideal V_{FB} position was indeed obtained for $H_2$500 and $O_2$600-$H_2$500. In particular, for $O_2$600-$H_2$500, the V_{FB} shift and hysteresis were as small as 40 mV (negative) and 98 mV, respectively. The second way is to lower the FGA temperature to suppress the reduction reactions of the GaO_x layer ($O_2$800-$H_2$200). Here, the V_{FB} shift and hysteresis of $O_2$800-$H_2$200 were as small as 59 mV (positive) and 67 mV, respectively. Thus, both methods work quite nicely in terms of the interface properties. This conclusion is also in agreement with our previous

report.[27)]

Next, positive bias stress tests were conducted to investigate the oxide traps that affect the long-term reliability. Figure 2(a) shows a schematic diagram of the measurement scheme. A constant voltage stress (V_{stress}) was applied for up to 1000 s and *C*-*V* characteristics were repeatedly measured to monitor their drift. V_{stress} was selected for each sample such that it corresponded to an oxide field + 4 MVcm^{-1} and was kept fixed during the stress tests. Figure 2(b) shows typical *C*-*V* characteristics obtained during the tests. Positive drift in the *C*-*V* characteristics clearly appears depending on the stress; it was due to electron injection into the oxide traps. The V_{FB} values were determined from the characteristics by extrapolating $1/C_{deep}^2$ to $1/C^2_{max}$, where C_{deep} and C_{max} are the deep-depletion and maximum capacitance, respectively.[32)] In this way, it should be able to minimize the effect of interface traps when evaluating the V_{FB} position.

Figure 3 shows the stress-time dependence of V_{FB} for the fabricated SiO_2/GaN MOS capacitors. For the as-deposited sample (as-depo.), V_{FB} drifted sharply in the positive direction even after a short stress period. Here, vacancy defects and carbon impurities would be present in the SiO_2 film immediately after the deposition,[33–35)] which may act as electron traps. On the other hand, O_2-PDA and FGA made the situation better. Comparing the samples subjected to O_2-PDA at different temperatures and FGA at 500°C ($H_2$500, $O_2$600-$H_2$500, and $O_2$800-$H_2$500) reveals that the combination is effective in suppressing the V_{FB} drift; the drift after 1000 s of stress was 7.15, 3.73, and 0.54 V for $H_2$500, $O_2$600-$H_2$500, and $O_2$800-$H_2$500, respectively. Since O_2-PDA and FGA are both effective in reducing the traps causing the drift, the traps are removable by either oxygen or hydrogen. The fact that both O_2-PDA and FGA are needed to sufficiently reduce the traps implies that they consist of multiple defects including vacancies, carbon impurities, and dangling bonds. As the O_2-PDA temperature increased, the V_{FB} drift got smaller. However, when the O_2-PDA temperature was increased to 800°C ($O_2$800-$H_2$500), V_{FB} showed negative values (about −8 V; see Fig. 1(a)), which was due to reduction of the GaO_x layer. Therefore, once a positive fixed charge forms, it seems to be difficult to inject electrons to cancel it out. Next, we compared samples that were subjected to O_2-PDA at 800°C and FGA at different temperatures ($O_2$800, $O_2$800-$H_2$200, and $O_2$800-$H_2$500). The V_{FB} drift after 1000 s of stress was 3.90, 0.85, and 0.54 V for $O_2$800, $O_2$800-$H_2$200, and $O_2$800-$H_2$500, respectively. Notably, for $O_2$800-$H_2$200, not only did V_{FB} show a small drift (0.85 V), it was close to its ideal value (within 0.9 V). Therefore, from the viewpoints of interface properties and long-term reliability, it would be good to form the GaO_x layer with O_2-PDA at a relatively high temperature (800°C) and then perform FGA at a temperature where the reduction of the GaO_x layer does not take place (200°C). Another solution might be to perform O_2-PDA at temperature in between 600°C and 800°C and then FGA at 500°C,

which we did not investigate in this study.

Finally, we investigated the temperature dependence of the V_{FB} drift. Figures 4(a)–(c) show the V_{FB} drift obtained at different measurement temperatures (RT, 100°C, and 150°C) for $O_2$800, $O_2$800-$H_2$200, and $O_2$800-$H_2$500. Note that the figures plot not V_{FB} but rather the drift of V_{FB} with respect to its initial position (ΔV_{FB}) in order to compare the V_{FB} drifts of the samples on an equal footing. While the sample subjected to O_2-PDA at 800°C ($O_2$800) exhibited a significant increase in V_{FB} drift at elevated measurement temperatures, the increase was suppressed to less than 2.6 V after FGA was performed at or above 200°C ($O_2$800-$H_2$200 and $O_2$800-$H_2$500). Note that, while the drift was significantly suppressed for $O_2$800-$H_2$500, the V_{FB} values were negative (Fig. 3), which will make the MOS device normally-on. Therefore, the optimum condition was again $O_2$800-$H_2$200, which offers not only a nearly ideal V_{FB} position (Fig. 3) but also high immunity against bias temperature stress (Fig. 4).

In summary, we investigated the effect of post-deposition oxygen annealing and forming gas annealing on the electrical characteristics of SiO_2/GaN MOS devices. Capacitance-voltage measurements and bias temperature stress tests were conducted to evaluate the interface properties and long-term reliability, respectively. It was found that both oxygen and forming gas annealing were effective in passivating the interface traps as well as oxide traps. In particular, the key to optimizing the SiO_2/GaN MOS structure is to form an interfacial GaO_x layer by using oxygen annealing and then to passivate the remaining defects by using forming gas annealing. However, when both oxygen and forming gas annealing were performed at high temperatures (i.e., 800 and 500°C, respectively), reduction of the GaO_x layer occurred, resulting in the appearance of a positive fixed charge. From the viewpoints of the interface properties and long-term reliability, the solution to this problem is to form a GaO_x layer by annealing in oxygen at high temperature (800°C) and then to perform forming gas annealing at a low temperature (200°C) where reduction of the GaO_x layer does not take place. In this way, interface traps, oxide traps, and fixed charge can be simultaneously reduced, leading to improved reliability even at elevated temperatures.

Acknowledgements

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Figure Captions

Table 1. Annealing conditions of samples in this study.

Fig. 1. (a) Bidirectional capacitance-voltage (*C*-*V*) characteristics of SiO_2/GaN MOS structures subjected to O_2-PDA and FGA. The ideal V_{FB} position is indicated by the dashed line. (b) Schematic image describing the impact of O_2-PDA and FGA.

Fig. 2. (a) Measurement flow of electron injection stress test. A constant voltage stress was applied for up to 1000 s and *C*-*V* characteristics were repeatedly acquired to evaluate the long-term reliability. (b) Typical *C*-*V* characteristics acquired during the stress measurements (sample: $O_2$800).

Fig. 3. V_{FB} position as a function of stress time for SiO_2/GaN MOS structures. A constant stress voltage corresponding to an oxide field of + 4 $MVcm^{-1}$ was applied. The ideal V_{FB} position is indicated by the dashed line.

Fig. 4. Drift in V_{FB} (ΔV_{FB}) as a function of stress time for SiO_2/GaN MOS structures: the sample after (a) O_2-PDA at 800°C, (b) O_2-PDA at 800°C followed by FGA at 200°C, and (c) O_2-PDA at 800°C followed by FGA at 500°C. Measurement temperature was RT, 100, or 150°C.

Label	O_2-PDA (ºC)	FGA (ºC)
as-depo.		
$H_2$500		500
$O_2$600-$H_2$500	600	500
$O_2$800	800	
$O_2$800-$H_2$200	800	200
$O_2$800-$H_2$500	800	500

Table 1.

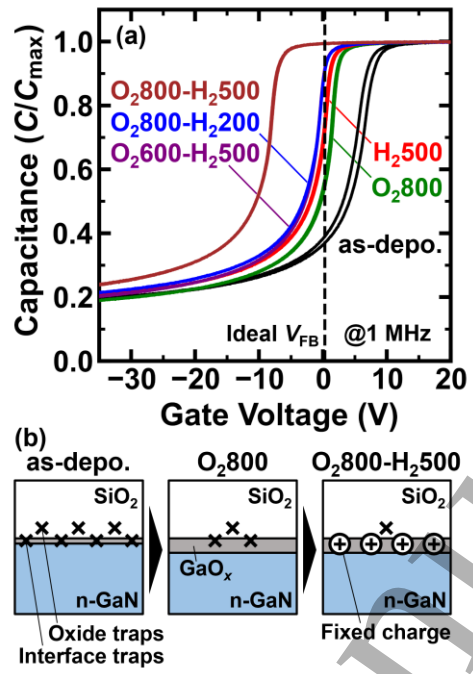

Fig. 1.

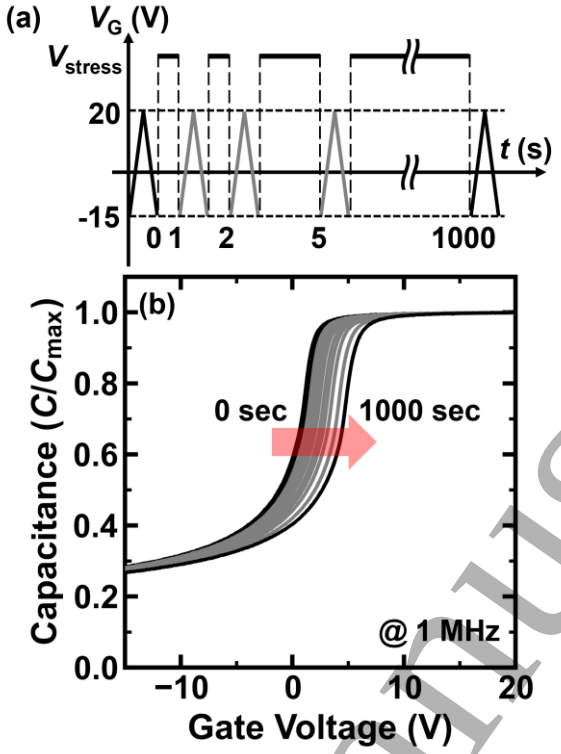

Fig. 2.

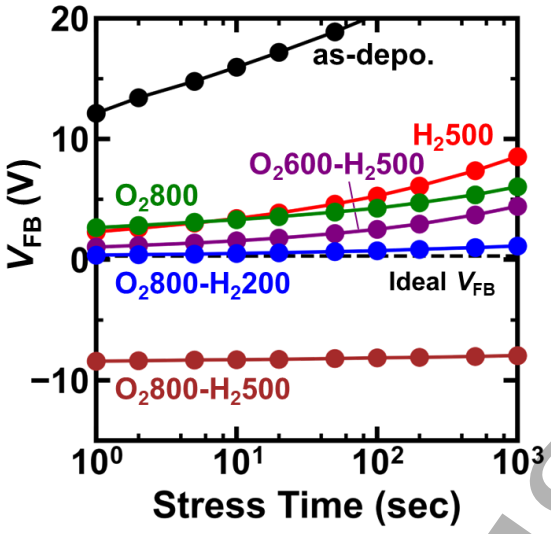

Fig. 3.

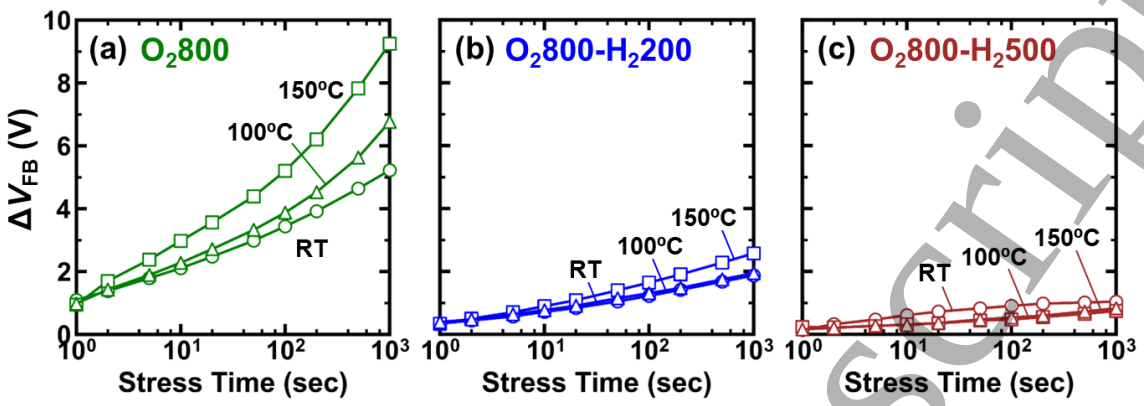

Fig. 4.