Japanese Journal of Applied Physics

The Japan Society of Applied Physics

ACCEPTED MANUSCRIPT

Formation of high-quality SiO_2/GaN interfaces with suppressed Ga-oxide interlayer via sputter deposition of SiO_2

To cite this article before publication: Kentaro Onishi *et al* 2023 *Jpn. J. Appl. Phys.* in press https://doi.org/10.35848/1347-4065/acd1ca

Formation of high-quality SiO_2/GaN interfaces with suppressed Ga-oxide interlayer via sputter deposition of SiO_2

Kentaro Onishi[1*], Takuma Kobayashi[1*], Hidetoshi Mizobata[1], Mikito Nozaki[1], Akitaka Yoshigoe[2], Takayoshi Shimura[1], and Heiji Watanabe[1]

[1]*School/Graduate School of Engineering, Osaka University, 2-1 Yamadaoka, Suita, Osaka 565-0871, Japan*

[2]*Japan Atomic Energy Agency, 1-1-1 Kouto, Sayo-cho, Sayo-gun, Hyogo 679-5148, Japan*

[*]E-mail: onishi@ade.prec.eng.osaka-u.ac.jp, kobayashi@prec.eng.osaka-u.ac.jp

While the formation of a GaO_x interlayer is key to achieving SiO_2/GaN interfaces with low defect density, positive fixed charge is rather easily generated through the reduction of GaO_x layer if the annealing conditions are not properly designed. In this study, we minimized the unstable GaO_x layer by sputter SiO_2 deposition. Negligible GaO_x growth was confirmed by synchrotron radiation X-ray photoelectron spectroscopy, even when post-deposition oxygen annealing up to 600°C was performed. A MOS device with negligible capacitance-voltage hysteresis, stable flat-band voltage, and low leakage current was demonstrated by performing oxygen and forming gas annealing at temperatures of 600°C and 400°C, respectively.

Gallium nitride (GaN) is a suitable material for power switching devices due to its superior material properties such as a wide bandgap, high critical electric field, and high electron saturation velocity[1–3]. AlGaN/GaN high electron mobility transistors (HEMTs), which utilize two-dimensional electron gas at the AlGaN/GaN heterointerface, have been adapted for high frequency applications[4,5]. While standard AlGaN/GaN HEMTs with a Schottky-gate suffers from gate leakage, the application of a metal-oxide-semiconductor (MOS)-gate structure is effective in reducing the leakage[6–8]. GaN MOS field-effect transistors (MOSFETs) are also appealing as a switching device with normally-off operation[9–11].

A variety of oxides have been investigated as a candidate dielectric of GaN MOS structure so far; e.g., SiO_2[12–15], Al_2O_3 [16–18], AlSiO[19,20], SiON[21,22], and AlON[7,8]. Since GaN has a wide bandgap of 3.4 eV, oxides are limited to those with a sufficiently wide bandgap. Furthermore, the oxide needs to be thermally stable because post-deposition annealing (PDA) is usually required to improve the dielectric properties of the oxide[23]. From these viewpoints, SiO_2 is promising owing to its extremely wide bandgap (9 eV) as well as high-temperature stability. Plasma-enhanced chemical vapor deposition (PECVD)[12–13,21] and atomic layer deposition (ALD)[14,15] of SiO_2 on GaN have been intensively investigated. For these methods, the surface of GaN was found to be oxidized with oxygen plasma during the deposition, generating a few nm-thick GaO_x layer at the SiO_2/GaN interface[15,21,24,25]. The formation of the GaO_x layer at the interface and its further growth by oxygen annealing are effective in improving the interface properties of the SiO_2/GaN MOS structure[25]. However, two problems arise accordingly; first, the GaO_x layer is easily reduced during post annealing treatment even at relatively low temperatures (e.g. 400°C), producing a positive fixed charge likely related to oxygen vacancies[26–28]. This leads to a threshold voltage instability of MOS devices[29,30]. Even if GaO_x layer is present at the interface, it is able to avoid the fixed charge generation by lowering the temperature of forming gas annealing (FGA) to 200°C[31]. However, it would be advantageous if we can perform post-annealing processes at higher temperatures in MOS device fabrication. To enable high temperature annealing, an excessive growth of the unstable GaO_x layer should be suppressed. Second, along with the growth of

the GaO_x layer, the Ga atoms diffuse into the oxide, which degrades the oxides' dielectric property[25,32]. Thus, in achieving a stable GaN MOS device with a small gate leakage, it would be better to minimize the growth of the GaO_x layer.

Therefore, this study aims to minimize the GaO_x layer at the SiO_2/GaN interface, while preserving superior interface properties. To this end, SiO_2 was deposited by sputtering, which is one of the physical vapor deposition methods, in pure Ar atmosphere without oxygen. To improve the interface and dielectric properties of the MOS structure, PDA in oxygen and forming gas ambient was performed. In addition to electrical measurements, a series of physical analyses based on synchrotron radiation X-ray photoelectron spectroscopy (SR-XPS) and secondary ion mass spectrometry (SIMS) were carried out to reveal the underlying physics that dominate the electrical characteristics.

We started from a free-standing GaN(0001) substrate with an *n*-type epilayer ([Si]: 2×10^{16} cm^{-3}). The samples' surface was cleaned with acetone and 50%-hydrofluoric (HF) acid. After that, SiO_2 was deposited by radio frequency (RF) magnetron sputtering. The sputtering target, ambient, chamber pressure, substrate temperature, and RF input power were SiO_2, Ar, 0.3 Pa, room temperature, and 100 W, respectively. A sample with PECVD-deposited SiO_2 was also prepared as a reference[25]. The SiO_2 thickness was either about 20 nm (electrical measurements and SIMS) or about 2 nm (SR-XPS). After the deposition, a number of samples were subjected to post-deposition annealing in oxygen ambient (O_2-PDA) at 200–800°C for 30 mins. For the MOS capacitors, circular Ni gate electrodes (diameter: 50–100 μm) and Al back contacts were formed by vacuum evaporation. Then, post-metallization FGA (3% H_2/N_2) at 400°C was carried out for 30 mins. Capacitance-voltage (*C*-*V*) and current-voltage characteristics of the capacitors were measured at room temperature. SR-XPS measurements of SiO_2/GaN samples were performed with a radiation energy of 1253.6 eV and photoelectron take-off-angle (TOA) of 90° at BL23SU in SPring-8[33]. The binding energy of the acquired Ga $2p_{3/2}$ spectra was calibrated by the peak energy of the N 1*s* core level (397.5 eV) corresponding to the Ga-N binding component of the GaN substrate. SIMS measurements were carried out using O^{2+} primary ion beam with an incident energy of 1 keV.

Figure 1 shows the Ga $2p_{3/2}$ core-level spectra of as-deposited SiO_2/GaN structures obtained by SR-XPS: samples with (a) PECVD-deposited and (b) sputter-deposited SiO_2. After the Shirley-type background[34] was subtracted from the signals, the signal intensity was normalized. The spectra were deconvoluted into two peak components; Ga-N (peak energy: 1118.4 eV) and Ga-O (peak energy: 1119.0 eV) components originating from the GaN substrate and GaO_x layer, respectively. Now, we can evaluate the thickness of the GaO_x layer from the intensity ratio of the two components (i.e. $I_{Ga\text{-}O}/I_{Ga\text{-}N}$). For PECVD deposition (Fig. 1(a)), the formation of GaO_x inevitably occurs because the GaN surface is oxidized due to oxygen radicals. However, the $I_{Ga\text{-}O}/I_{Ga\text{-}N}$ ratio is about three times smaller in the sputter-deposited sample (Fig. 1(b)), indicating that the GaO_x growth is indeed suppressed for sputter deposition. Considering that the GaO_x thickness is about 2 nm for a typical PECVD-deposited sample[25], the thickness would be a few monolayers for sputter deposition. Therefore, sputter deposition is indeed effective in suppressing the unstable GaO_x layer at the SiO_2/GaN interface.

Figure 2 shows the bidirectional *C*-*V* characteristics of sputter-deposited SiO_2/GaN MOS capacitors (measurement frequency: 1 MHz). The as-deposited sample (as-depo.) exhibited a large *C*-*V* hysteresis (0.9 V) as well as stretch-out caused by electron trapping. This indicates a large number of interface and near-interface oxide traps. O_2-PDA and FGA are effective in passivating the traps, leading to a decrease in hysteresis and stretch-out. However, when the O_2-PDA temperature was increased to 800°C, a negative shift of *C*-*V* characteristics occurred after FGA, corresponding to a positive fixed charge density of 1.1×10^{12} cm^{-2}. This is due to the generation of a positive fixed charge likely related to oxygen vacancies[27] caused by the reduction of the GaO_x layer[29]. Such an effect is negligible when the O_2-PDA temperature is 600°C or less for the sputter-deposited sample.

We then investigated the growth of the GaO_x layer due to O_2-PDA. The Ga $2p_{3/2}$ core-level spectra of SiO_2/GaN samples subjected to O_2-PDA at various temperatures are shown in Fig. 3(a). While no significant GaO_x growth was observed with O_2-PDA up to 600°C, the growth started to proceed at 800°C. Figure 3(b) plots the intensity ratio $I_{Ga\text{-}O}/I_{Ga\text{-}N}$ from XPS and V_{FB} positions of MOS capacitors as a function of O_2-PDA temperature. We can see that,

as the GaO_x growth proceeds, the negative shift in V_{FB} occurs. Thus, it is evident that the reduction of the GaO_x layer is the cause of the fixed charge generation, as described in Fig. 3(c). The O_2-PDA temperature should be 600°C or less to minimize the growth of the unstable GaO_x layer.

Next, SIMS measurements were conducted to evaluate the Ga diffusion into SiO_2 dielectric. Figure 4 shows the depth profile of Ga concentration in the SiO_2/GaN structure evaluated by SIMS. Segregation of Ga atoms was observed in the near-surface region (< 8 nm) even for the as-deposited sample, which would be inevitable. The SIMS profile after O_2-PDA at 600°C is mostly similar to the as-deposited sample, showing negligible Ga diffusion. However, with O_2-PDA at 800°C, it can be seen that a small amount of Ga diffuses into SiO_2. Since the Ga diffusion is triggered by the growth of GaO_x[25], the results of the SIMS analysis are consistent with those of the XPS shown in Figs. 3(a) and (b).

As a result of the electrical measurements and physical analyses previously mentioned, we found that the upper limit of the O_2-PDA temperature where the GaO_x does not grow is 600°C. Figure 5(a) shows the frequency dispersion of *C*-*V* characteristics of SiO_2/GaN MOS structure, where O_2-PDA and FGA were conducted at 600 and 400°C, respectively. Negligible frequency dispersion, small *C*-*V* hysteresis (0.5 mV), and a small V_{FB} shift (0.3 V, negative) from its ideal position were obtained, indicating a small number of interface/near-interface traps. Although we confirmed that O_2-PDA alone is effective in improving the interface properties to some extent (data not shown), additional FGA is needed to obtain the optimum characteristics. Figure 5(b) shows the current density-oxide field characteristics of the sample in comparison with the as-deposited one. While the as-deposited sample exhibited a relatively low onset field of leakage (about 4.0 $MVcm^{-1}$), the onset was improved to about 5.5 $MVcm^{-1}$ due to O_2-PDA and FGA. This is likely due to passivation of oxide traps such as oxygen vacancies by oxygen annealing. By sputter deposition of SiO_2 and subsequent O_2-PDA and FGA, a stable SiO_2/GaN MOS structure with good interface and dielectric properties was obtained.

In summary, on the basis of sputter deposition of SiO_2, the growth of an unstable GaO_x layer at the SiO_2/GaN interface was effectively minimized in this study. Due to this, either

the negative shift of flat-band voltage due to positive fixed charge generation or the Ga diffusion into SiO_2 dielectric was suppressed during the following annealing treatment. By performing O_2-PDA at 600°C, where the GaO_x growth does not occur, and FGA at 400°C, a MOS device with negligible *C-V* hysteresis, nearly ideal flat-band voltage, and small leakage current was demonstrated.

Acknowledgments

This work was partly supported by the MEXT "Program for Creation of Innovative Core Technology for Power Electronics" (Grant No. JPJ009777), and JSPS KAKENHI (Grant No. 19H00767). The work was partly performed under the Shared Use Program of JAEA Facilities (Proposal Nos. 2022A-E18 and 2022B-E14) with the approval of Advanced Research Infrastructure for Materials and Nanotechnology in Japan Project supported by the Ministry of Education, Culture, Sports, Science and Technology (Proposal Nos. JPMXP1222AE0017 and JPMXP1222AE0030). The synchrotron radiation experiments were performed at JAEA beamline BL23SU in SPring-8 (Proposal Nos. 2022A3833 and 2022B3833).

References

1) S.J. Pearton, J.C. Zolper, R.J. Shul, and F. Ren, J. Appl. Phys. **86**, 1 (1999).
2) B.J. Baliga, Semicond. Sci. Technol. **28**, 074011 (2013).
3) J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, IEEE Trans Power Electron **29**, 2155 (2014).
4) M. Asif Khan, J.N. Kuznia, D.T. Olson, W.J. Schaff, J.W. Burm, and M.S. Shur, Appl. Phys. Lett. **65**, 1121 (1994).
5) Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S.P. Denbaars, and U.K. Mishra, IEEE Electron Device Letters **27**, 713 (2006).
6) M. Asif Khan, X. Hu, A. Tarakji, G. Simin, J. Yang, R. Gaska, and M.S. Shur, Appl. Phys. Lett. **77**, 1339 (2000).
7) R. Asahara, M. Nozaki, T. Yamada, J. Ito, S. Nakazawa, M. Ishida, T. Ueda, A. Yoshigoe, T. Hosoi, T. Shimura, and H. Watanabe, Applied Physics Express **9**, 101002 (2016).
8) K. Watanabe, M. Nozaki, T. Yamada, S. Nakazawa, Y. Anda, M. Ishida, T. Ueda, A. Yoshigoe, T. Hosoi, T. Shimura, and H. Watanabe, Appl. Phys. Lett. **111**, 042102 (2017).
9) M. Kodama, M. Sugimoto, E. Hayashi, N. Soejima, O. Ishiguro, M. Kanechika, K. Itoh, H. Ueda, T. Uesugi, and T. Kachi, Applied Physics Express **1**, 021104 (2008).

10) H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, and H. Ohta, Applied Physics Express **1**, 011105 (2008).
11) T. Oka, Y. Ueno, T. Ina, and K. Hasegawa, Applied Physics Express **7**, 021002 (2014).
12) K. Yamaji, M. Noborio, J. Suda, and T. Kimoto, Jpn. J. Appl. Phys. **47**, 7784 (2008).
13) E. Kim, N. Soejima, Y. Watanabe, M. Ishiko, and T. Kachi, Jpn. J. Appl. Phys. **49**, 04DF08 (2010).
14) S. Takashima, Z. Li, and T.P. Chow, Jpn. J. Appl. Phys. **52**, 08JN24 (2013).
15) K. Aoshima, N. Taoka, M. Horita, and J. Suda, Jpn. J. Appl. Phys. **61**, SC1073 (2022).
16) P.D. Ye, B. Yang, K.K. Ng, J. Bude, G.D. Wilk, S. Halder, and J.C.M. Hwang, Appl. Phys. Lett. **86**, 063501 (2005).
17) S. Huang, S. Yang, J. Roberts, and K.J. Chen, Jpn. J. Appl. Phys. **50**, 110202 (2011).
18) S. Kaneki, J. Ohira, S. Toiya, Z. Yatabe, J.T. Asubar, and T. Hashizume, Appl. Phys. Lett. **109**, 162104 (2016).
19) D. Kikuta, K. Itoh, T. Narita, and T. Mori, J. Vac. Sci. Technol. A **35**, 01B122 (2017).
20) D. Kikuta, K. Ito, T. Narita, and T. Kachi, Applied Physics Express **13**, 026504 (2020).
21) T. Yamada, D. Terashima, M. Nozaki, H. Yamada, T. Takahashi, M. Shimizu, A. Yoshigoe, T. Hosoi, T. Shimura, and H. Watanabe, Jpn. J. Appl. Phys. **58**, SCCD06 (2019).
22) D. Morgan, M. Sultana, H. Fatima, S. Sugiyama, Q. Fareed, V. Adivarahan, M. Lachab, and A. Khan, Applied Physics Express **4**, 114101 (2011).
23) T. Nishiguchi, S. Saito, N. Kameda, M. Kekura, H. Nonaka, and S. Ichimura, Jpn. J. Appl. Phys. **48**, 116509 (2009).
24) E. al Alam, I. Cortés, M.P. Besland, A. Goullet, L. Lajaunie, P. Regreny, Y. Cordier, J. Brault, A. Cazarré, K. Isoird, G. Sarrabayrouse, and F. Morancho, J. Appl. Phys. **109**, 084511 (2011).
25) T. Yamada, K. Watanabe, M. Nozaki, H. Yamada, T. Takahashi, M. Shimizu, A. Yoshigoe, T. Hosoi, T. Shimura, and H. Watanabe, Applied Physics Express **11**, 015701 (2018).
26) M. Fleischer, J. Giber, and H. Meixner, Appl. Phys. A **54,** 560(1992).

27) W. Jochum, S. Penner, K. Föttinger, R. Kramer, G. Rupprechter, and B. Klötzer, J Catal **256**, 268 (2008).
28) T. Kobayashi, T. Gake, Y. Kumagai, F. Oba, and Y.I. Matsushita, Applied Physics Express **12**, 091001 (2019).
29) H. Mizobata, Y. Wada, M. Nozaki, T. Hosoi, T. Shimura, and H. Watanabe, Applied Physics Express **13**, 081001 (2020).
30) H. Mizobata, M. Nozaki, T. Kobayashi, T. Hosoi, T. Shimura, and H. Watanabe, Jpn. J. Appl. Phys. **61**, SC1034 (2022).
31) B. Mikake, T. Kobayashi, H. Mizobata, M. Nozaki, T. Shimura, and H. Watanabe, Applied Physics Express **16**, 031004 (2023).
32) Y. Wada, M. Nozaki, T. Hosoi, T. Shimura, and H. Watanabe, Jpn. J. Appl. Phys. **59**, SMMA03 (2020).
33) Y. Teraoka and A. Yoshigoe, Appl. Surf. Sci. **169-170**, 738 (2001).
34) D.A. Shirley, Phys. Rev. **B5**, 4709 (1972).

Figures Captions

Fig. 1. Ga $2p_{3/2}$ core-level spectra of as-deposited SiO_2/GaN samples evaluated by SR-XPS: samples with (a) PECVD-deposited and (b) sputter-deposited SiO_2. The measurement data after background subtraction (open circles) were described by the sum (green) of Ga-N (blue) and Ga-O (red) peak components. The Ga-N (1118.4 eV) and Ga-O (1119.0 eV) peak positions are indicated by dashed lines. The calculated intensity ratio of the Ga–O peak to the Ga–N one ($I_{Ga–O}/I_{Ga–N}$) is also shown, together with a schematic describing the result.

Fig. 2. Bidirectional *C*-*V* characteristics of sputter-deposited SiO_2/GaN MOS capacitors with and without annealing (measurement frequency: 1 MHz). The capacitance is normalized by the maximum capacitance (C_{max}) and the ideal V_{FB} position is indicated as a dotted line. Capacitance per unit area is also shown as an inset. The maximum capacitance differs among the samples corresponding to the thickness variation of SiO_2 (20 ± 1 nm).

Fig. 3. (a) Ga $2p_{3/2}$ core-level spectra of SiO_2/GaN samples without (as-depo.) and with O_2-PDA at various temperatures evaluated by SR-XPS. (b) Intensity ratio I_{Ga-O}/I_{Ga-N} estimated from XPS (black) and V_{FB} positions of MOS capacitors (blue) as a function of O_2-PDA temperature. (c) Schematic illustration describing the instability of the GaO_x layer against FGA.

Fig. 4. Depth profiles of Ga concentration in SiO_2/GaN structures without and with O_2-PDA obtained by SIMS. The position of SiO_2/GaN interface is indicated as a dashed line (depth: 20 nm).

Fig. 5. (a) Bidirectional *C*–*V* characteristics of SiO_2/GaN MOS capacitors fabricated by O_2-PDA at 600°C and FGA at 400°C for 30 min. Multi-frequency measurements ranging from 1 kHz to 1 MHz were conducted at room temperature. (b) Current density-oxide field characteristics of SiO_2/GaN MOS capacitors with (blue) and without (black) O_2-PDA and FGA.

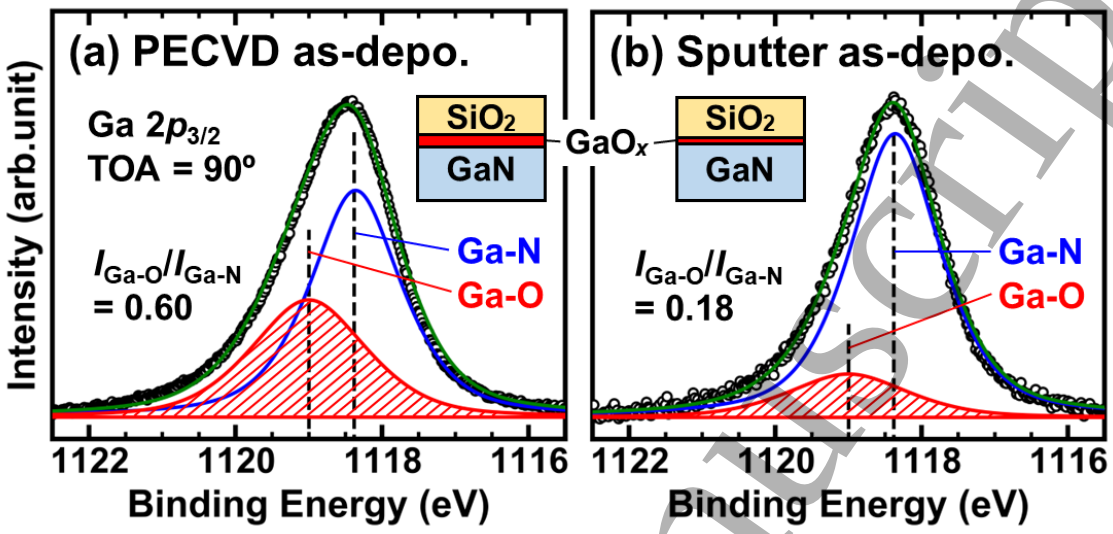

Fig. 1.

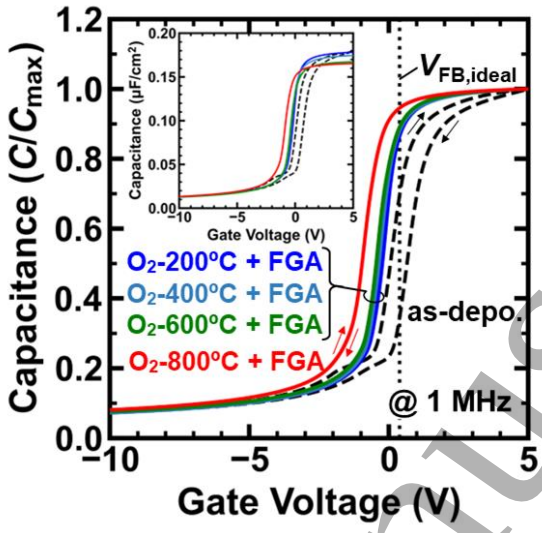

Fig. 2.

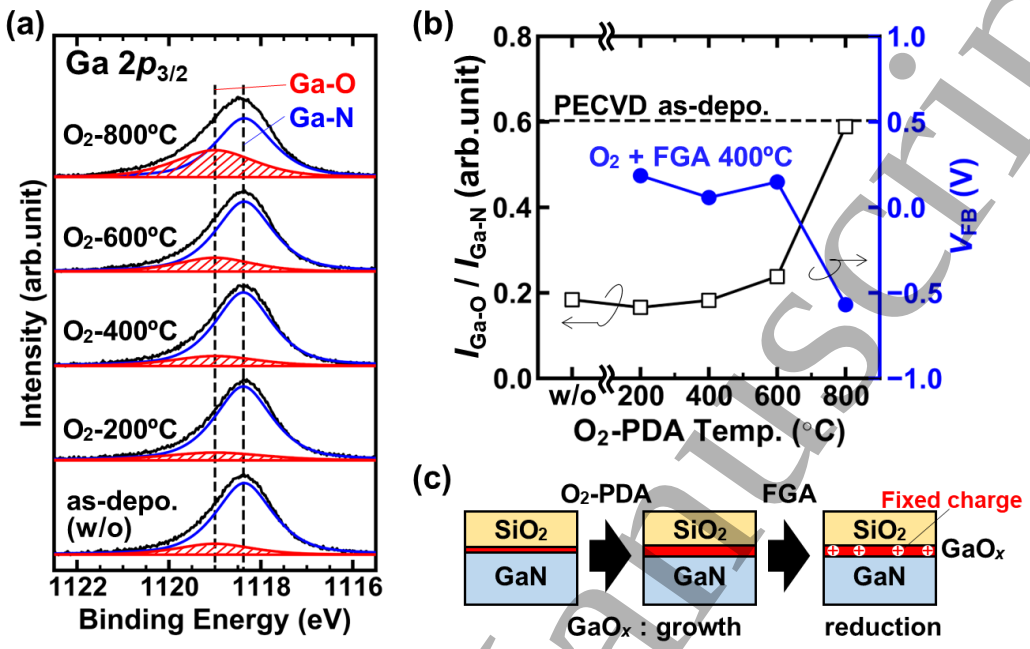

Fig. 3.

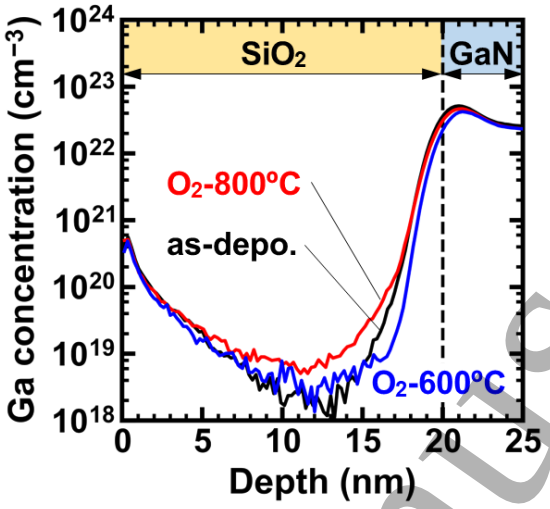

Fig. 4.

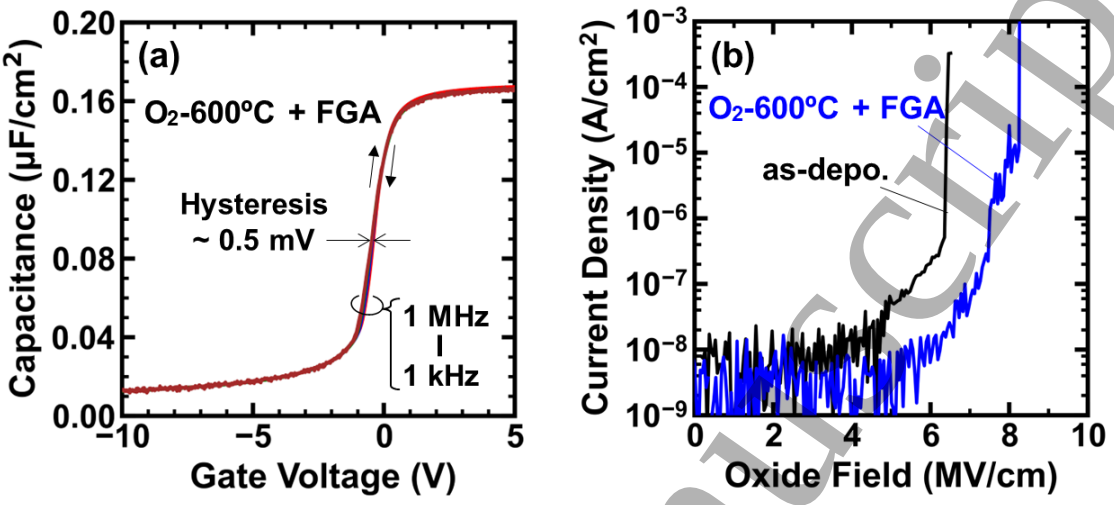

Fig. 5.