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Study on interface and oxide trap states of SiO_2/GaN metal-oxide-semiconductor capacitors and their effects on electrical properties by deep level transient spectroscopy

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The relationship between the electrical properties and the carrier trap properties of the SiO_2/GaN metal-oxide-semiconductor (MOS) capacitors was investigated using electrical measurements and deep level transient spectroscopy (DLTS). The capacitance-voltage (*C*-*V*) measurement showed that the frequency dispersion of the *C*-*V* curves became smaller after an 800 °C annealing in O_2 ambient. DLTS revealed that before the annealing, the interface trap states, in a broad energy range above the mid-gap of GaN, were detected with the higher interface state density at around 0.3 and 0.9 eV below the conduction band minimum (E_C) of GaN. Moreover, the oxide trap states were formed at around 0.1 eV below the E_C of GaN, plausibly indicating a slow electron trap with a tunneling process. Although both trap states affect the electrical reliability and insulating property of the SiO_2/GaN MOS capacitors, they were found to drastically decrease after the annealing, leading to the improvement of the electrical properties.

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1. Introduction

Gallium nitride (GaN) is one of promising materials for advanced power electronics due to its superior material properties, such as high breakdown electric field and wide band gap, compared to silicon (Si).[1-3] While successful developments of GaN-based high electron mobility transistors (HEMTs) using two-dimensional electron gas at the AlGaN/GaN heterostructures have been achieved for high efficiency and high frequency applications,[4-6] there are still issues to realize GaN-based vertical metal-oxide-semiconductor (MOS) field-effect transistors (FETs) for high performance power devices with normally-off high voltage and high temperature operations. Although intensive research and progress have been reported regarding the development of GaN MOSFETs,[7-9] the electrical characteristics have not yet been optimized. One of the important issues is the quality of the dielectric/GaN interfaces, leading to a low channel mobility, threshold voltage shift and low reliable operations. Therefore, understanding the origin of the poor interface qualities and formation of the high-quality dielectric/GaN interfaces are indispensable for realization of advanced GaN MOSFETs.

As for a dielectric on GaN, gallium oxide (Ga_2O_3) is a thermally-grown dielectric on GaN as well as silicon dioxide (SiO_2) on Si which is well known as a suitable dielectric film for Si-based large scale integrated (LSI) technologies. However, the band gap of Ga_2O_3 is around 5 eV and thus the barrier height of the Ga_2O_3/GaN interface is insufficient, thus causing a high leakage current. Therefore, a wider band gap dielectric, such as aluminum oxide (Al_2O_3),[10, 11] silicon nitride (Si_3N_4)[8, 12] and SiO_2,[13-16] should be chosen to design the appropriate band alignment of the dielectric/GaN interface. In addition, Ga_2O_3 forms large crystal grains on GaN after annealing over 850 °C,[17, 18] leading to an increase in the leakage current and surface roughness. Considering these facts, SiO_2 is a possible candidate due to the wide band gap of around 9 eV and stable amorphous structure at higher temperatures. Regarding the SiO_2/GaN structures,

previous reports revealed that the formation of a suitable thin GaO_x interlayer between SiO_2 and GaN enhanced the electrical properties of the GaN MOS devices with a low interface state density (D_{it}) below 10^{11} $cm^{-2}eV^{-1}$.[15, 19] It was also shown that the SiO_2/GaN interface degraded after a 900 °C annealing due to the interfacial reaction between SiO_2 and GaN, leading to the excess oxidation of GaN and the detrimental Ga diffusion into the SiO_2 layer.[20] As a countermeasure, the deposition of the nitrogen (N)-incorporated SiO_2 on GaN was further beneficial for the electrical properties by suppressing the excess oxidation of the GaN surface.[21] These results indicated that appropriate measures must be considered to form high-quality SiO_2/GaN interfaces. Although several techniques have been proposed for the SiO_2/GaN structures, further improvement must be achieved for higher performance of the GaN-MOS devices, especially a reduction of the electrically-active defects. Based on this point of view, it was reported that the electrical properties of not only GaN- but also silicon carbide (SiC)-based MOS devices strongly depend on their D_{it}.[21, 22] Moreover, trap states in the dielectrics, called oxide traps or near interface traps (NITs), also degrade the electrical properties of the power MOSFETs.[23-25] Among the various techniques to investigate the carrier trap properties of MOS devices, deep level transient spectroscopy (DLTS) is one of superior techniques to evaluate the energy and amount of trap states with a higher sensitivity.[26, 27] So far, whereas various intensive DLTS studies have been performed for SiC-MOS devices,[22, 28-30] a few papers have reported on evaluation of GaN-MOS devices using DLTS, for example, Al_2O_3/GaN MOS devices,[31, 32] SiN_x/GaN metal-insulator-semiconductor (MIS) devices[33] and AlGaN/GaN MIS-HEMTs.[34] Technical development to analyze the trap states of the GaN-MOS devices is also required to further enhance the performance of the GaN-MOS devices. Therefore, in this study, we investigated the trap states of the GaN-MOS devices using DLTS. Not only interface traps but also oxide traps were characterized in terms of the relationship

between the electrical properties and trap states.

2. Experimental

Free-standing GaN (0001) substrates with 4-μm-thick Si-doped *n*-type GaN epilayers (Si concentration: 2×10^{16} cm^{-3}) were used as the base substrates in this study. The GaN surface was cleaned using acetone with ultrasonics and a 50 % hydrofluoric acid (HF) solution to remove organic contaminants and the native oxide, respectively. Around 25-nm-thick SiO_2 films were deposited by plasma enhanced chemical vapor deposition (PECVD) using tetraethyl orthosilicate (TEOS) as the Si source. In the early stage of the SiO_2 film deposition (under 5-nm thick), nitrogen gas was introduced into the oxygen gas to dilute the ratio of oxygen and to form the nitrogen (N) incorporated SiO_2 layer. A previous study revealed that the N-incorporated SiO_2/GaN capacitors enhanced the electrical properties by suppressing the excess oxidation of the GaN surface which led to the detrimental Ga diffusion into the SiO_2 films.[21] After the formation of the SiO_2 films, post deposition annealing (PDA) was performed at 800 °C in O_2 ambient to improve the interface quality without the interfacial reaction of the SiO_2/GaN structure.[20] A nickel film was deposited as a gate electrode with diameters of 200 μm and 500 μm for the electrical measurements and DLTS measurement, respectively, followed by the deposition of an aluminum film as a back contact.

Capacitance-voltage (*C*-*V*) and current-voltage (*I*-*V*) measurements were conducted at room temperature to investigate the electrical properties and the insulating properties of the SiO_2/GaN MOS capacitors, respectively. Bidirectional *C*-*V* curves were obtained with measurement frequencies ranging from 10 kHz to 1 MHz. The DLTS measurement was performed to evaluate the electron trap states of the SiO_2/GaN MOS capacitors. In this study, constant capacitance (CC) DLTS was mainly conducted in which the capacitance was kept constant during the transient process by applying feedback to the

measured voltage. The CC-DLTS enables us to improve the accuracy of the energy of the trap states, because the fermi level of the MOS interface does not change during the electron emission process.[27, 28, 30] The reverse bias was set near the flatband voltage of the MOS capacitors and the pulse bias of |5 V| was applied to accumulate electrons around the SiO_2/GaN interface. The pulse width (T_P) was set at 0.02, 2 and 200 ms to investigate not only the interface traps but also the oxide traps. Generally, electrons are quickly trapped at the interface trap states. Therefore, a shorter T_P is sufficient to fill the interface trap states and D_{it} can be calculated from the DLTS spectra with the shorter T_P.[32, 35] If some electrons infiltrated into the oxide traps from the SiO_2/GaN interface, the electrons are subject to a tunneling process. This means that the electrons are captured at the oxide traps with a certain time, and as a result, the intensity of the DLTS signal varies with T_P.[27] Therefore, we also investigated the T_P dependence of the DLTS signals ranging from 10^{-5} to 10^{0} s by applying the isothermal CC measurement.

3. Results and discussion

The electrical properties of the SiO_2/GaN MOS capacitors without (as-depo.) and with the 800 °C annealing were evaluated by the bidirectional *C-V* curves, shown in Figs. 1(a) and 1(b). Both curves represented well-behaved *C-V* characteristics of the SiO_2/*n*-GaN MOS capacitors with a small hysteresis. The capacitance equivalent thicknesses (CET) of the dielectric films, estimated from the maximum of the capacitance, were around 25 nm as expected. The frequency dispersion of the *C-V* curves was found to become smaller after the annealing. These results were consistent with a previous report and indicated the impact of the combination between the N-incorporation into the SiO_2 layer and the 800 °C annealing in O_2 ambient.[21, 36] The frequency dispersion of the *C-V* curves is definitely derived from charge injection from GaN to the SiO_2 layer and/or carrier trap at the SiO_2/GaN interface caused by the

deterioration of the dielectrics and dielectric/semiconductor interfaces.[15, 37] In addition, we confirmed from the *I-V* measurement that the insulating properties of the SiO_2/GaN MOS capacitor was also improved by the annealing (data not shown), indicating that the electron injection into the SiO_2 layer were caused by the trap states. Therefore, the investigation of the carrier trap properties not only at the interface, but also in the SiO_2 layer is important for further improvements of the electrical properties of the SiO_2/GaN MOS capacitors.

To investigate the carrier trap properties of the SiO_2/GaN MOS capacitors, we performed the CC-DLTS measurement. Figure 2(a) shows the DLTS spectra of the SiO_2/GaN MOS capacitor without the annealing. Note that the DLTS signal intensity (vertical axis) was calculated by the correlation function analysis applying the sine coefficient to the transient voltages. The higher DLTS signals of the SiO_2/GaN MOS capacitor without the annealing were observed at around 130 K and 400 K. These results indicated a unique energy distribution of the trap states within the band gap of GaN. In addition, these signals increased with the T_P, suggesting that electrons were trapped not only at the SiO_2/GaN interface, but also in the SiO_2 layer. On the other hand, Fig. 2(b) shows that the DLTS signals drastically decreased over one order of magnitude after the annealing compared to those before the annealing. Figure 3 shows the energy distributions of the D_{it} in the SiO_2/GaN MOS capacitors, calculated using the DLTS spectra with the T_P of 0.02 ms. It is noted that the D_{it} was transformed from the DLTS spectra by assuming that the capture cross section (σ_c) did not depend on the energy (temperature).[27, 32, 35] The σ_c was estimated to be 6×10^{-15} cm^2 based on the DLTS spectra at around 0.3 eV for the SiO_2/GaN MOS capacitor without the annealing using the correlation function method.[30] Though the calculated σ_c contains an error margin to some extent, the value of σ_c is almost comparable to the reported values of several MOS capacitors, such as the Al_2O_3/GaN,[31, 32] and the SiO_2/SiC structures[28-30]. Considering the

σ_c of the D_{it}, the capture time constant (τ_c) is very fast at around 10^{-10} s. Therefore, the T_P of 0.02 ms is sufficient to fill electrons with the interface states. In Fig. 3, the higher D_{it} at around 0.3 eV, labeled E_1, below the conduction band minimum (E_C) of GaN was observed for the SiO_2/GaN MOS capacitor without the annealing. Previous studies revealed that a similar trap state at around 0.3 eV was detected in the Al_2O_3/GaN MOS capacitor,[32, 38] possibly speculated as the nitrogen vacancy related complexes or the bond disorder at the interface. Moreover, the D_{it} at around 0.9 eV, close to the mid-gap of GaN, was found to slightly increase. Such deep state was observed for the GaN on a sapphire substrate,[39] thin epilayers,[40] and for the GaN after the high-energy electron irradiation,[41] indicating to be likely due to dislocation-related defects and/or N interstitials. Theoretical study indicated that the origin of the deep state was plausibly derived from the N interstitials.[42] However, the assignments are still controversial and a deeper understanding is required. On the other hand, the D_{it} decreased to around 10^{10} $cm^{-2}eV^{-1}$ in all the measured energy ranges after the annealing. These results clearly indicated the improvement of the interface quality of the SiO_2/GaN MOS capacitor related to the *C-V* characteristics shown in Fig. 1.

Next, an isothermal CC measurement was performed to distinguish the oxide trap states from the interface trap states. Figure 4 shows the T_P dependence of the DLTS signals measured at several temperatures. If electrons were captured at the oxide traps with a tunneling process, the DLTS signals (ΔV) follow the equations described below.[27, 30, 35]

$$\Delta V = \frac{qA}{C_{ox}} N_I d_x kT \quad (1)$$

$$d_x = d_0 \ln\left(\frac{T_P}{\tau_c}\right) \quad (2)$$

$$\tau_c = \frac{1}{\sigma_c v_{th} n_0} \ , \ \tau_e = \frac{1}{\sigma_c v_{th} N_c} \quad (3)$$

where q is the elementary charge, A is the electrode area, C_{ox} is the capacitance of the SiO_2 layer, N_I is the density of states in the SiO_2 layer, d_x is the depth of the trapped layer, k is the boltzmann constant, d_0 is the tunnel constant, ν_{th} is the thermal velocity of the electron, n_0 is the carrier density of the samples, τ_e is the emission time constant, and N_c is the density of states of the conduction band. According to the equation (1) and (2), we can estimate the oxide trap state density ($N_I d_x$) and τ_c from the linear slope and the intersection in the ΔV with the logarithmic (ln) T_P. Using τ_c, σ_c is obtained by the equation (3) and as a result, τ_e is also estimated. It is noted that in this measurement, d_x can be regarded as the SiO_2 thickness, because the SiO_2 thickness is thin enough to fill carriers after applying the pulse bias. As shown in Fig. 2(a), the DLTS signals without the annealing at around 130 K and 400 K clearly increased with the T_P, expecting that the T_P dependence of the DLTS signals is observed. Surely, the DLTS signals without the annealing at 130 K and 400 K, shown in Fig. 4(a), exhibited a linear increase with the ln T_P of around 10^{-4} to 10^{-2} s, indicating that the electrons were captured at the oxide traps with a tunneling process. Whereas the DLTS signals at 80 K also showed a linear increase with the ln T_P, no linear increase was observed at 200 K and 300 K due to being close to the detection limit of the measurement, as expected in the results of the temperature dependence of the DLTS signals shown in Fig. 2(a). Also, the DLTS signals after the annealing, measured at 300 K and 400 K, showed a linear increase with the ln T_P of around 10^{-4} to 10^{-2} s, shown in Fig. 4(b). It is also noted that the reduction of the DLTS signals in the saturated (Filled) region was observed at the several temperatures in Fig. 4. The reason of the reduction is still unclear but probably due to another process besides the simple electron capture process in the saturated region. One possible reason is a hole injection from the electrode into the SiO_2 layer, when the longer T_P was applied to the MOS capacitors. However, the influence of the reduction of the DLTS signals in the saturated region seems to be negligible for the evaluation of the oxide trap

states. The energy distributions of the oxide trap state densities and the capture cross sections were calculated using the results of linear ranges in Fig. 4 and shown in Fig. 5. It can be considered that all the active oxide trap states in the SiO_2 layer were filled with electrons, when the DLTS signals were saturated in Fig. 4. At the saturated T_P, the energy of the trap states at the SiO_2/GaN interface (E_0) and at the d_x (E_P) was calculated using the equations (4) and (5) described below.[27, 30] We defined the averaged value (E_{mid}) as the energy of the oxide trap state by the equation (6).

$$E_0(t) = kT \ln\left(\frac{t}{\tau_e}\right) \quad (4)$$

$$E_P = E_0(t) - kT\frac{d_x}{d_0} \quad (5)$$

$$E_{mid} = E_0(t) - \frac{1}{2}kT\frac{d_x}{d_0} \quad (6)$$

Note that the results of the normal capacitance transient measurement were also plotted in Fig. 5, because it has a higher sensitivity than the CC measurement. The oxide trap state density of around 1×10^{11} $cm^{-2}eV^{-1}$ at 0.1 eV below the E_C of GaN was observed without the annealing, while very low oxide trap states were detected after the annealing. The capture cross sections are quite small at around 10^{-19} ~ 10^{-20} cm^2. This means that the capture time constants are around 10^{-5} ~ 10^{-4} s, which are also seen in the SiN_x/Si structures.[43] Therefore, the slow charge injection into the shallow states in the SiO_2 layer occurred for the SiO_2/GaN MOS capacitor without the annealing. It possibly caused the high frequency dispersion of the *C-V* curves, as shown in Fig. 1, surely leading to a deterioration of the electrical reliability of the SiO_2/GaN MOS capacitors. Finally, schematic images of the trap states in the SiO_2/GaN structure are described in Fig. 6. The conduction band offset (ΔE_C) between SiO_2 and GaN was referred for the similar structure of the SiO_2/*n*-GaN(0001).[44] The interface trap states were formed in a broad energy range above the mid-gap of GaN. Especially, the higher D_{it} values at

around 0.3 eV and 0.9 eV below the E_C of GaN were observed. The oxide trap states were found at around 0.1 eV below the E_C of GaN, representing those at around 3.6 eV below the E_C of SiO_2. Previous theoretical studies indicated that the states of positively charged oxygen vacancy sites (so-called E_1' or E_γ' center) were formed at around 3-4 eV from the E_C of SiO_2.[45, 46] Therefore, the detected oxide trap states likely stem from the oxygen vacancies in the SiO_2 layer, easily capturing electrons. Although these trap states affect the electrical reliability and insulating property of the SiO_2/GaN MOS capacitors, we confirmed that they were dramatically decreased by the 800 °C annealing in O_2 ambient.

4. Summary

In this study, we intensively investigated the carrier trap states of the SiO_2/GaN MOS capacitors using DLTS and confirmed their effects on the electrical properties. The interface trap states showed a broad energy distribution above the mid-gap of GaN and higher D_{it} values at around 0.3 eV and 0.9 eV below the Ec of GaN were found for the as-deposited sample. In addition, the oxide trap states were formed at around 0.1 eV below the E_C of GaN, plausibly indicating the slow electron trap with a tunneling process. We confirmed that the interface and the oxide trap states drastically decreased after the annealing at 800 °C in O_2 ambient, leading to the improvement of the electrical reliability and the insulating property of the SiO_2/GaN MOS capacitors. Although further investigation is required to understand the origin of the carrier trap behaviors in the SiO_2/GaN MOS capacitors, these results indicate the necessity to evaluate not only the interface traps but also the oxide traps, which surely affect the carrier transport properties and reliability of the GaN-based MOS devices.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Shingo Ogawa: Data curation (lead); Formal analysis (lead); Investigation (lead); Writing – original draft (lead); Writing – review and editing (equal). Hidetoshi Mizobata: Data curation (equal); Formal analysis (equal); Investigation (equal). Takuma Kobayashi: Formal analysis (supporting); Investigation (supporting). Takayoshi Shimura: Formal analysis (supporting); Investigation (supporting). Heiji Watanabe: Conceptualization (equal); Formal analysis (supporting); Investigation (supporting); Project administration (lead); Supervision (equal); Writing – review and editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Figure caption

Fig. 1. Bidirectional *C-V* curves of SiO_2/GaN MOS capacitors (a) without (as-depo.) and (b) with 800 °C annealing. Multi-frequency measurements ranging from 1 kHz to 1 MHz were carried out at room temperature. Capacitance equivalent thickness (CET) values, estimated from the maximum accumulation capacitance, are shown in the figures.

Fig. 2. DLTS spectra of SiO_2/GaN MOS capacitors (a) without (as-depo.) and (b) with 800 °C annealing. Pulse bias (V_P) was applied at |5 V|. Pulse width (T_P) was set at 0.02, 2 and 200 ms with period width (T_W) of 512 ms. The schematic image of voltage transient in the measurement is shown in the inset.

Fig. 3. Energy distribution of D_{it} obtained by the DLTS spectra with the pulse width (T_P) of 0.02 ms and the period width (T_W) of 512 ms. Note that the energy axis of the D_{it} was calculated by assuming capture cross section to be 6×10^{-15} cm^2.

Fig. 4. Pulse width (T_P) dependence of DLTS signals (a) without (as-depo.) and (b) with 800 °C annealing at several temperatures. Pulse bias (V_P) was applied at |5 V| with period width (T_W) of 512 ms.

Fig. 5. Energy distribution of oxide trap state density and capture cross section calculated by pulse width (T_P) dependent measurement. Note that the capture cross section was calculated at each energy. The results of the normal DLTS (capacitance transient measurement) were also shown to confirm the results of the CC-Mode.

Fig. 6. (a) Schematic illustration and (b) energy diagram of interface traps and oxide traps in SiO_2/GaN structure without 800 °C annealing (as-depo.). The value of the conduction band offset (ΔE_C) of SiO_2/GaN structure was referred for the similar structure of the SiO_2/n-GaN(0001) [44].

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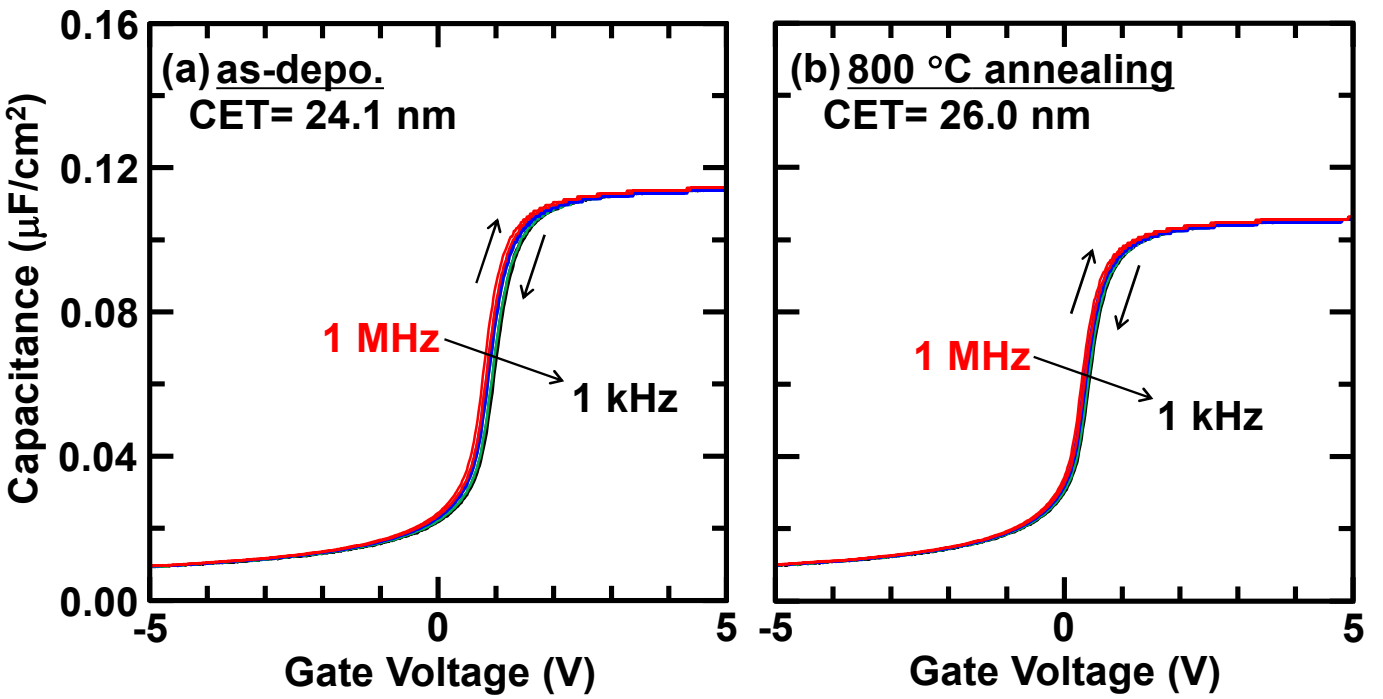

Fig. 1. Bidirectional C-V curves of SiO_2/GaN MOS capacitors (a) without (as-depo.) and (b) with 800 °C annealing. Multi-frequency measurements ranging from 1 kHz to 1 MHz were carried out at room temperature. Capacitance equivalent thickness (CET) values, estimated from the maximum accumulation capacitance, are shown in the figures.

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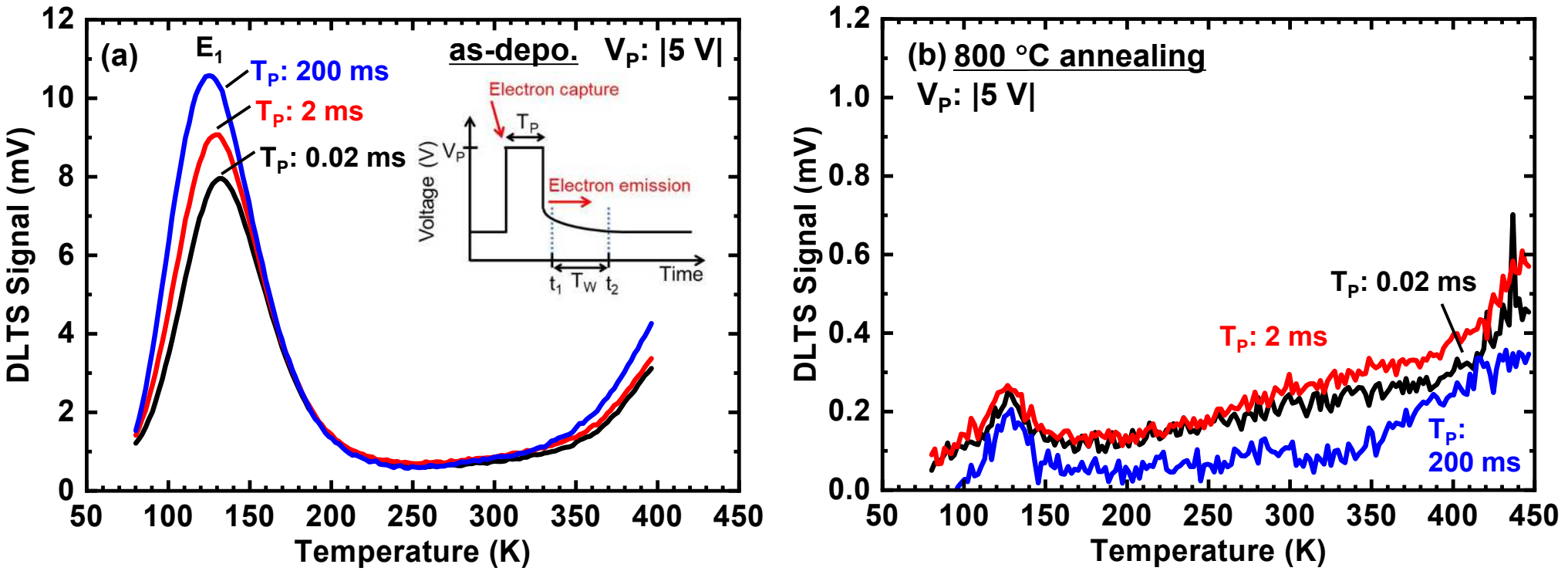

Fig. 2. DLTS spectra of SiO_2/GaN MOS capacitors (a) without (as-depo.) and (b) with 800 °C annealing. Pulse bias (V_P) was applied at |5 V|. Pulse width (T_P) was set at 0.02, 2 and 200 ms with period width (T_W) of 512 ms. The schematic image of voltage transient in the measurement is shown in the inset.

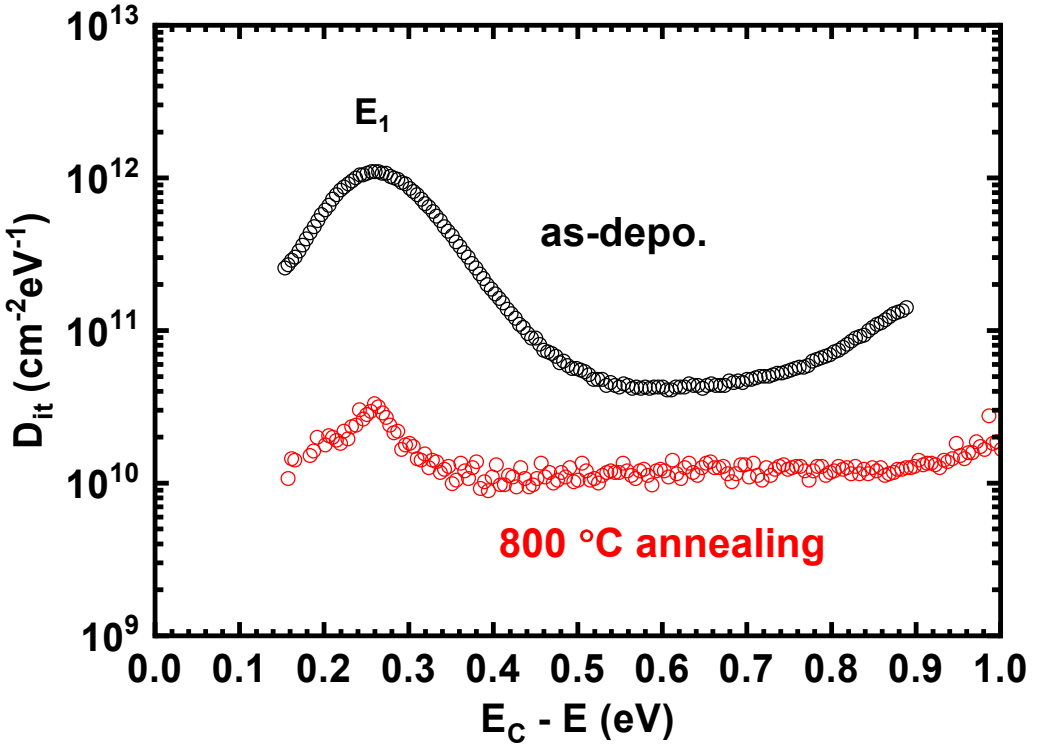

Fig. 3. Energy distribution of D_{it} obtained by the DLTS spectra with the pulse width (T_P) of 0.02 ms and the period width (T_W) of 512 ms. Note that the energy axis of the D_{it} was calculated by assuming capture cross section to be 6×10^{-15} cm^2 .

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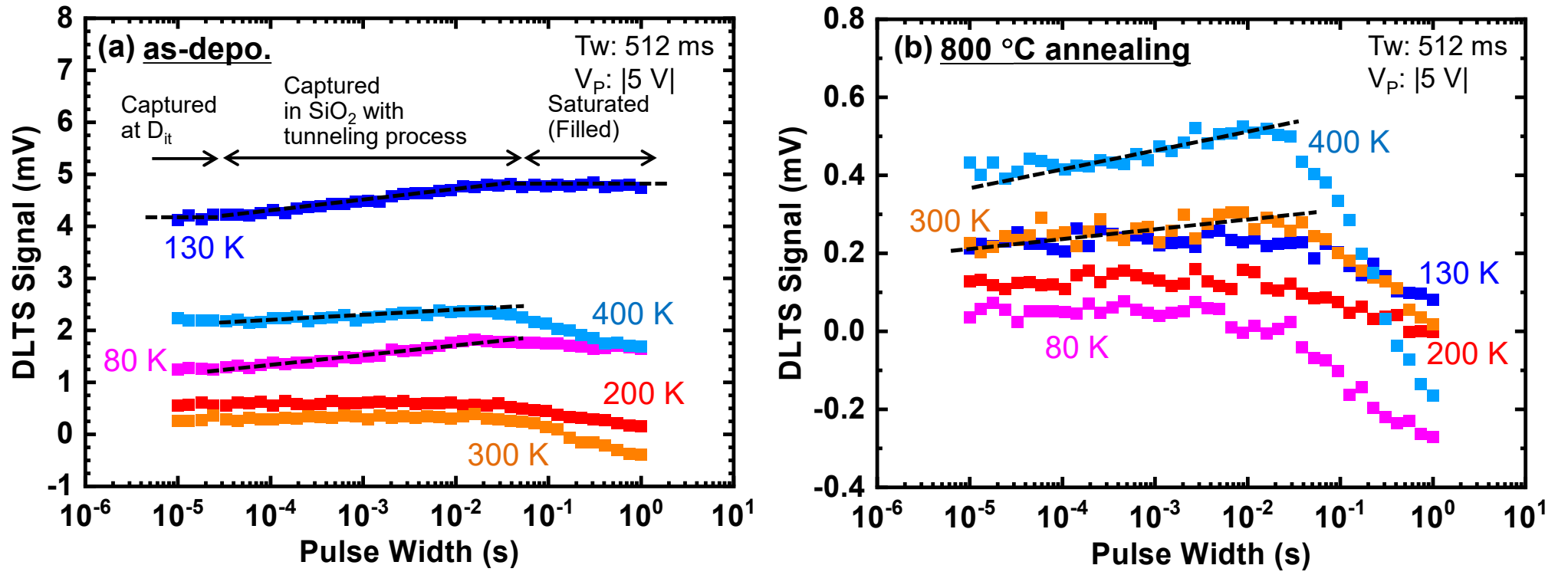

Fig. 4. Pulse width (T_P) dependence of DLTS signals (a) without (as-depo.) and (b) with 800 °C annealing at several temperatures. Pulse bias (V_P) was applied at |5 V| with period width (T_W) of 512 ms.

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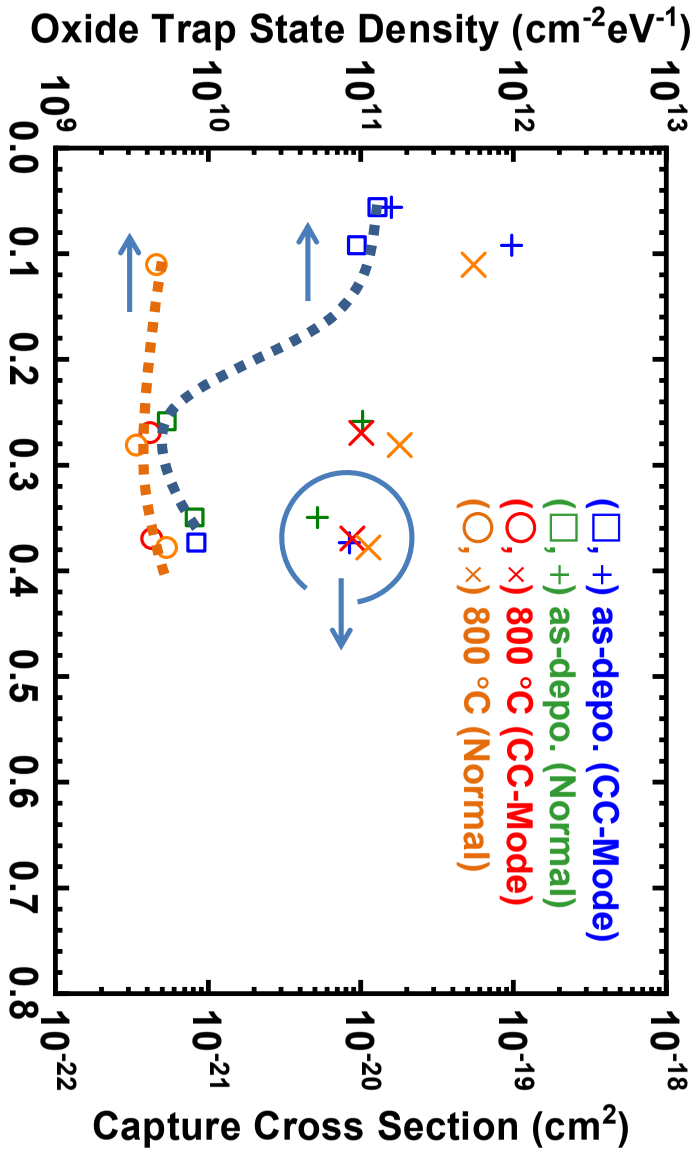

Fig. 5. Energy distribution of oxide trap state density and capture cross section calculated by pulse width (T_P) dependent measurement. Note that the capture cross section was Calculated at each energy. The results of the normal DLTS (capacitance transient measurement) were also shown to confirm the results of the CC-Mode.

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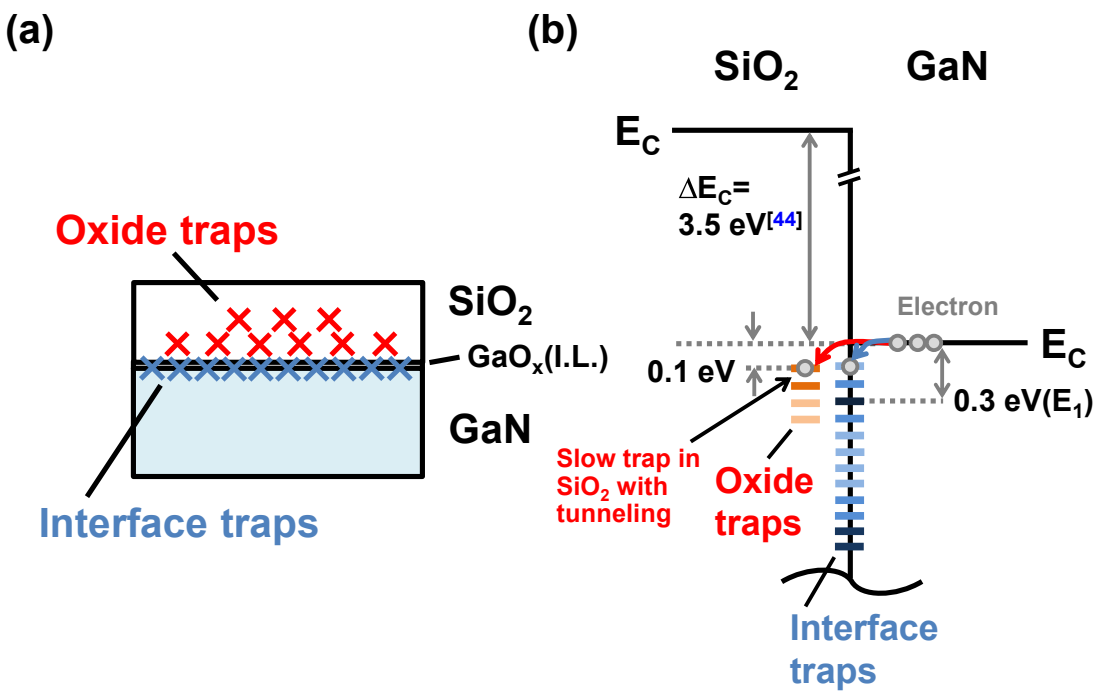

Fig. 6. (a) Schematic illustration and (b) energy diagram of interface traps and oxide traps in SiO_2/GaN structure without 800 °C annealing (as-depo.). The value of the conduction band offset (ΔE_C) of SiO_2/GaN structure was referred for the similar structure of the SiO_2/n-GaN(0001) [44].