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Passivation of hole traps in SiO_2/GaN metal-oxide-semiconductor devices by high-density magnesium doping

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A major challenge in GaN-based metal-oxide-semiconductor (MOS) devices is significant hole trapping near the oxide/GaN interface. In this study, we show that the density and energy level of the hole traps depend crucially on the concentration of magnesium (Mg) dopants in GaN layers. Although the surface potential of a conventional SiO_2/p-GaN MOS device is severely pinned by hole trapping, hole accumulation and very low interface state densities below 10^{11} cm^{-2} eV^{-1} are demonstrated for MOS capacitors on heavily Mg-doped GaN epilayers regardless of the degree of dopant activation. These findings indicate the decisive role of Mg atoms in defect passivation.

Gallium nitride (GaN) is a promising material for next-generation power devices because it is a wide-bandgap semiconductor that exhibits electrical properties superior to those of silicon (Si), such as a high breakdown electric field and high electron saturation velocity.[1–3] Among the various GaN-based electronic devices, metal-oxide-semiconductor field-effect transistors (MOSFETs) are one of the most important and fundamental devices. Since advances in GaN growth techniques have made it possible to fabricate high-quality freestanding substrates and epitaxial layers, vertical GaN MOSFETs, such as trench MOSFETs and double-diffused MOSFETs capable of high-current operation, have been intensively investigated.[4–7] To realize the inherently high level of performance of GaN-based MOSFETs, it is essential to form high-quality MOS structures with low defect densities.

Considering the wide energy bandgap of GaN, gate dielectrics for MOS devices should be oxide insulators with a sufficiently wider bandgap than that of GaN and a large band offset relative to GaN. There are a limited number of oxides with the above properties, and, previously, GaN MOS devices with silicon dioxide (SiO_2), alumina (Al_2O_3), aluminum silicate (AlSiO) dielectrics were investigated.[8–16] However, most of those studies investigated n-type GaN MOS capacitors and evaluated electrical defects near the conduction band edge located near the oxide/GaN interface. We fabricated GaN MOS capacitors with SiO_2 gate dielectrics formed by plasma-enhanced chemical vapor deposition (PECVD).[17,18] Interface engineering was conducted by means of thin Ga-oxide (GaO_x) interlayers between the SiO_2 dielectrics and GaN substrates and the subsequent post-deposition annealing (PDA). As a result, very low interface state density (D_{it}) values below 10^{11} cm^{-2} eV^{-1} and a high dielectric breakdown electric field above 8 MV cm^{-1} were demonstrated for n-type GaN MOS capacitors.[17,18]

In contrast, there are few reports on p-type GaN MOS capacitors that had well-behaved capacitance-voltage (*C-V*) characteristics.[19–24] Because of the significant number of hole traps located near the oxide/GaN interfaces, a large *C-V* hysteresis is usually observed for p-type MOS capacitors.[25] Even worse, the surface potential of GaN is pinned and an ideal amount of hole accumulation at the MOS interface hardly occurs regardless of the gate dielectric materials used. Although GaO_x layers at the oxide/GaN interface and/or disordered Mg-segregation layers at the GaN surface might be origins of the hole traps,[20,21,25,26] the details of the hole trapping mechanism remain unclear. Recently, we demonstrated good *C-V* characteristics for SiO_2/p-GaN MOS capacitors fabricated by high-dose Mg-implantation and dopant activation by means of ultra-high-pressure annealing (UHPA) at 1400°C.[27] The fabricated MOS capacitors exhibited mostly ideal *C-V* characteristics, for which there were negligible hysteresis and a reasonable amount of hole accumulation. The acceptor concentration (N_A) estimated from the *C-V* curves was about 2×10^{18} cm^{-3}, which agrees with the concentration of implanted Mg atoms and showed the superiority of UHPA for activation of implanted dopants. However, at present, we have no clear explanation why hole trapping centers are passivated in the case of the highly doped GaN substrate and what the decisive factor is in defect passivation. Additionally, the threshold voltage (V_{TH}) of the n-channel MOSFETs is controlled in accordance with the Fermi level of the p-type regions, and hole trapping near the oxide/p-GaN interface needs to be suppressed to improve the V_{TH} stability that determines the long-term reliability of MOSFETs. Therefore, in this study, we investigated the impact of varying the Mg concentration in epitaxially grown (not ion-implanted) GaN substrates on the electrical properties of the oxide/GaN interfaces to seek clues to designing high-quality dielectric/p-GaN interfaces.

We used p-type GaN epilayers with various Mg concentrations grown by metalorganic vapor-phase epitaxy (MOVPE) on n-type GaN(0001) freestanding wafers. The Mg concentration in the epilayers was varied from about 7×10^{16} to 2×10^{19} cm^{-3}. After wet-cleaning with acetone ultrasonication and a 50% hydrofluoric (HF) acid solution, the substrates were annealed in a nitrogen atmosphere at 800°C for 20 minutes to activate the Mg dopants by dehydrogenation. Then, about 5-nm-thick SiON layers serving as a Ga diffusion barrier were deposited directly on the cleaned GaN surface and 15-nm-thick SiO_2 films were subsequently deposited by PECVD using tetraethyl orthosilicate (TEOS)/O_2/N_2 and TEOS/O_2 gas mixtures. The details of the film deposition conditions and impact of the thin SiON interlayer on the reliability of GaN MOS devices are described elsewhere.[17,18] The dielectric films were patterned by conventional photolithography to form top contacts for electrical measurements. Palladium (Pd) was deposited by vacuum evaporation, and Pd/p-GaN top contacts and gate electrodes with a diameter of 100 μm on the SiO_2 layers were formed by photolithography and subsequent wet etching. We also fabricated MOS capacitors without activation (dehydrogenation) annealing of Mg-doped GaN layers. Moreover, an n-type GaN MOS capacitor was fabricated in the same manner as the p-type capacitors for comparison, in which nickel (Ni) gate electrodes and aluminum (Al) back contacts were formed by vacuum evaporation. The fabricated p-type and n-type GaN MOS capacitors were examined by making bidirectional multi-frequency *C-V* measurements to evaluate the electrical properties of the oxide/GaN interfaces.

Figures 1(a) and 1(b) show typical *C-V* curves obtained from SiO_2/GaN MOS capacitors fabricated on p-type and n-type epilayers, respectively. Bidirectional *C-V* curves were acquired at a frequency of 1 kHz by sweeping the gate bias from positive

(negative) to negative (positive) and vice versa for the p-type (n-type) capacitor, as indicated by the black lines and arrows. Then, multi-frequency measurements were conducted at frequencies ranging from 1 kHz to 1 MHz. As for the n-type capacitor (Fig. 1(b)), while a small *C*-*V* hysteresis was observed for the first bidirectional scan at 1 kHz, well-behaved *C*-*V* characteristics with negligible hysteresis and frequency dispersion were achieved even without any post annealing treatment. The capacitance-equivalent thickness (CET = 21 nm) estimated from the maximum oxide capacitance (C_{ox}) coincided with the gate oxide thickness (~21 nm) estimated from spectroscopic ellipsometry, as indicated by the horizontal dotted line. This implies an ideal electron accumulation at the SiO_2/n-GaN interface, as previously reported.[17,18] The donor concentration (N_D) determined from the relationship between $1/C^2$ and gate voltage (V_g) was 6×10^{16} cm^{-3}. On the other hand, the *C*-*V* characteristics of the p-type capacitor were severely degraded by hole trapping, as shown in Fig. 1(a). Significant hysteresis was observed in the first scan, in which the maximum capacitance was far below the expected C_{ox} value. The acceptor concentration extracted from the $1/C^2$ versus V_g plots for the depletion region ($N_A = 7 \times 10^{16}$ cm^{-3}) agreed well with the concentration of Mg atoms (about 7×10^{16} cm^{-3}), suggesting activation of Mg dopants. These results imply hard pinning of the surface potential of the p-type capacitor owing to hole trapping at the SiO_2/p-GaN interface. Furthermore, subsequently obtained *C*-*V* curves completely overlapped with the backward sweep of the first scan regardless of the measurement frequency, meaning that the trapped holes were hard to de-trap even when a positive gate bias was applied and that they acted as fixed charges in the MOS structure.

Next, we investigated the effect of varying the Mg concentration on the *C*-*V* characteristics of p-type GaN MOS capacitors. Figure 2 shows the change in the

bidirectional 1-kHz *C-V* curves of the p-type MOS capacitors depending on the Mg concentration of the GaN epilayers. The N_A values determined from $1/C^2$ versus V_g plots are indicated in the figures. It should be noted that the hole trapping phenomena are crucially dependent on N_A of the p-GaN substrates. Although the maximum capacitance for the low and medium N_A samples was far below the C_{ox} value indicated by the horizontal dotted lines (Figs. 2(a) and 2(b)), a reasonable number of holes accumulated in the high N_A sample (Fig. 2(c)). In addition, no *C-V* hysteresis was observed in the high N_A sample. These results imply a significant reduction in hole traps near the SiO_2/GaN interface only for the highly Mg-doped sample. The ideal *C-V* curves depending on the N_A of p-GaN layers are plotted as dashed red lines in the figures, where the flatband voltage (V_{FB}) is shifted to fit the *C-V* curves in the depletion regions. The ideal curve for the high N_A sample in Fig. 2(c) appears to be flat because the high N_A of the p-GaN substrate resulted in the increased minimum capacitance, but the ideal curve overlapped with the experimental one. On the other hand, as for the forward sweeps of the low and medium samples, both the maximum capacitance and the gate voltage showed a discrepancy between the experimental and ideal values that became pronounced depending on the doping conditions, suggesting a change in the density and energy distribution of hole traps near the interface. On the basis of these findings and previous reports,[19-26] it can be concluded that, rather than the UHPA process,[27] the concentration of Mg atoms and/or the Fermi level of the p-GaN substrate play a decisive role in the passivation of hole traps.

To discriminate which of the above causes plays the dominant role in defect passivation, we fabricated MOS capacitors on a heavily Mg-doped GaN epilayer (2×10^{19} cm^{-3}) without intentional dopant activation, where SiO_2 dielectrics were deposited on the GaN

epilayer without activation annealing, except for sintering at 550°C to reduce the contact resistance of the top Pd/p-GaN interface for the *C-V* measurements. As previously reported, Mg atoms exist in the form of Mg-H complexes in as-deposited GaN epilayers, so high-temperature dehydrogenation annealing over 700°C is needed to electrically activate the Mg dopants as acceptors.[28-32] Figure 3(a) shows bidirectional *C-V* curves of the GaN MOS capacitor taken at a measurement frequency of 1 kHz. The N_A value (2×10^{17} cm^{-3}) in this case was much lower than the Mg concentration (2×10^{19} cm^{-3}), indicating partial activation (ionization) of Mg dopants, as expected. Note that, whereas the MOS capacitor fabricated without activation exhibited a mostly identical N_A value to that of the medium sample in Fig. 2(b), the *C-V* characteristics in Fig. 3(a) are well-behaved. As shown by the horizontal dotted line, ideal hole accumulation corresponding to de-pinning of surface potential at the SiO_2/p-GaN interface occurred in the highly Mg-doped sample without activation. These results clearly demonstrate that the concentration of Mg atoms (and/or Mg-H complexes), not the N_A values or the Fermi level of the GaN layers, plays the decisive role in passivation of hole traps near the SiO_2/GaN interface. The passivation of hole traps is presumably caused by the interaction of highly doped Mg atoms with defects responsible for hole trapping, such as oxygen vacancies in gallium oxide interlayers. However, theoretical studies based on first-principles calculations are essential to understand detailed mechanisms, and those are issues to be addressed in the future.

Finally, the defect density at the p-type MOS interface formed on the highly Mg-doped epilayer without activation annealing was examined in two ways. Figure 3(b) represents the frequency dispersion of the forward *C-V* curves taken from the p-type GaN MOS capacitor studied in Fig. 3(a). As mentioned above, a reasonable amount of hole

accumulation was observed at low frequencies below 1 kHz, but the maximum capacitance gradually decreased as the measurement frequency increased. This is probably due to the high contact resistance at the top Pd/p-GaN interface. This means that the sintering treatment at 550°C is insufficient for obtaining a top contact with Ohmic characteristics, which makes it difficult to conduct the conventional high-low-method evaluation of the defect density. Therefore, as indicated by the solid red curve in Fig. 3(c), the measured 100-kHz *C*-*V* curve (dashed red curve) was corrected by taking the series resistance into account.[33] Note that the corrected 100-kHz *C*-*V* curve completely overlapped the measured quasi-static (QS) curve, indicating that the defect density was very low in the lower half of the bandgap of GaN.

Furthermore, we used the *C*-ψ_s method proposed by Yoshioka *et al.* to evaluate D_{it}.[34] This method utilizes the theoretical capacitance (the theoretical *C*-*V* curve) instead of high-frequency measurements and provides reasonable D_{it} values for silicon carbide (SiC) MOS devices. The red circles in Fig. 4 represent the D_{it} distribution for a p-type GaN MOS capacitor fabricated on the highly Mg-doped GaN epilayer without activation annealing. Although this method has difficulty in determining an accurate surface potential in the MOS structure, extremely low D_{it} values close to the detection limit of our electrical measurement system were obtained. Considering the hard pinning of the surface potential in conventional p-type GaN MOS devices, this is an unprecedented achievement to the best of our knowledge. Although we have no detailed model of the Mg-related defect passivation mechanism at present, the findings described above provide a valuable clue to designing high-quality MOS structures for future GaN-based devices.

In conclusion, we systematically investigated hole trapping phenomena in p-type GaN

MOS devices depending on the concentration of Mg dopants and their degree of activation. We found that, in contrast to n-type MOS devices, p-type devices are severely degraded by hole trapping near the SiO_2/GaN interface. When conventional p-type GaN substrates with low and moderate N_A of around 10^{17} cm^{-3} or less are used, the surface potential of the p-type MOS structure is severely pinned due to hole trapping and ideal hole accumulation at the MOS interface is hardly observed. However, the devices formed on highly Mg-doped GaN epilayers had ideal hole accumulation regardless of N_A i.e., the Fermi level of the GaN layers, indicating the decisive role of Mg atoms in passivation of hole traps. Consequently, an extremely low D_{it} below 10^{11} cm^{-2} eV^{-1} was demonstrated for p-type GaN MOS devices.

Acknowledgments

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Figure Captions

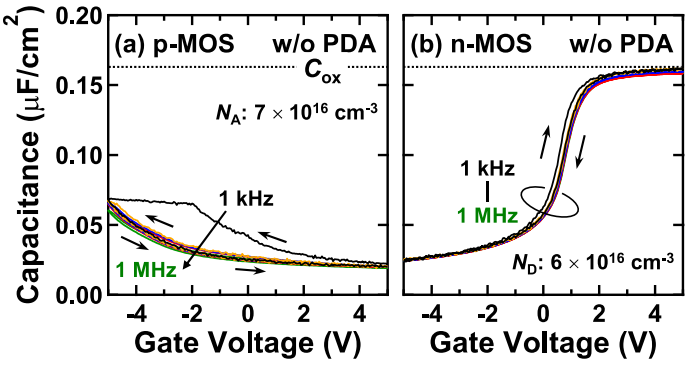
Fig. 1. Bidirectional *C-V* curves of SiO_2/GaN MOS capacitors fabricated on (a) p-type and (b) n-type GaN epilayers. Multi-frequency measurements ranging from 1 kHz to 1 MHz were carried out. The horizontal dotted black lines indicate (expected) oxide capacitance (C_{ox}).

Fig. 2. Bidirectional *C–V* curves of SiO_2/p-GaN MOS capacitors with various Mg concentrations. The measurement frequency was 1 kHz. The N_A values estimated from $1/C^2$ versus *V* plots were (a) 7×10^{16} cm^{-3} (Low N_A), (b) 1×10^{17} cm^{-3} (Medium N_A), and (c) 1×10^{19} cm^{-3} (High N_A). The dashed red lines and horizontal dotted lines represent ideal *C–V* curves and expected C_{ox} values, respectively. The ideal *C-V* curves are shifted to fit those of the depletion regions.

Fig. 3. Typical *C-V* characteristics of GaN MOS capacitor fabricated on the heavily Mg-doped GaN epilayer. No intentional activation annealing was conducted: (a) 1-kHz bidirectional *C-V* curves, (b) multi-frequency forward *C-V* curves taken at frequencies ranging from 1 kHz to 1 MHz, (c) comparison of QS (black) and 100-kHz *C-V* (red) curves. The N_A value shown in (a) corresponds to partial activation of Mg dopants. The dashed and solid red lines in (c) respectively represent the measured *C-V* curve and that corrected by taking the series resistance into account.

Fig. 4. Energy distribution of D_{it} for the SiO_2/p-GaN MOS capacitor fabricated on highly Mg-doped epilayer without dopant activation. The C-ψ_s method was used in the D_{it} evaluation.

Fig. 1.



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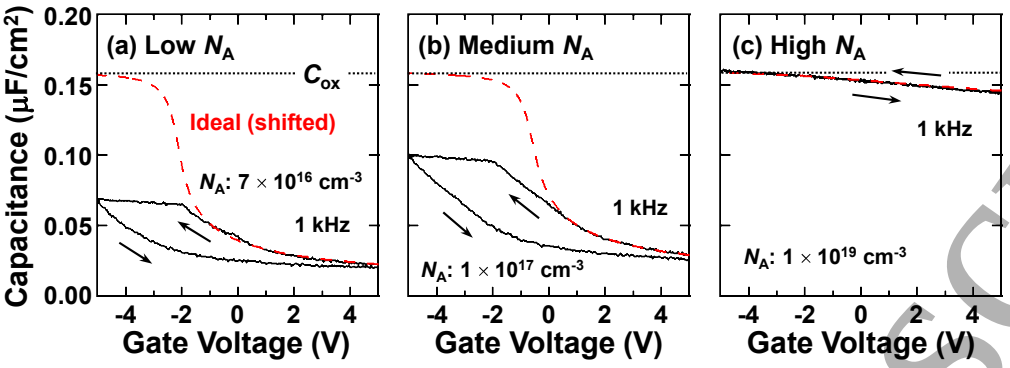

Fig. 3.

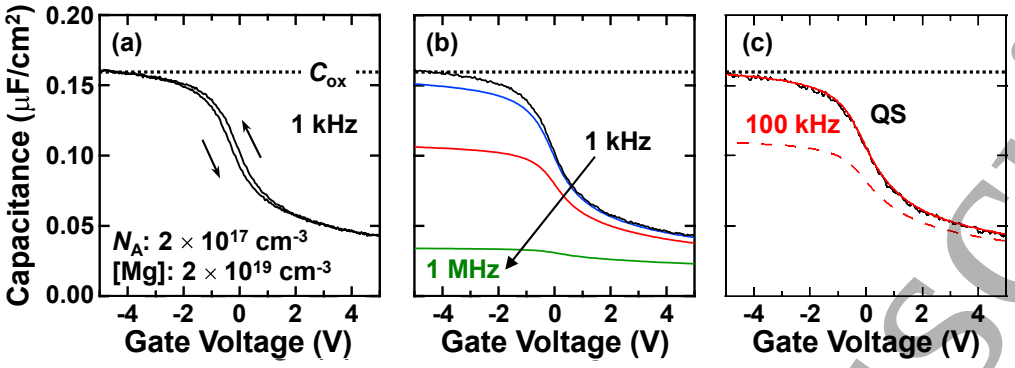

Fig. 4.