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Shallow defect layer formation as Cu gettering layer of ultra-thin Si chips using moderate-pressure (3.3 kPa) hydrogen plasma

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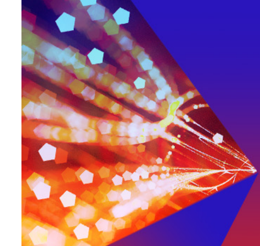
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Shallow defect layer formation as Cu gettering layer of ultra-thin Si chips using moderate-pressure (3.3 kPa) hydrogen plasma

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ABSTRACT

In this study, we developed a shallow defect layer formation process using moderate-pressure H_2 plasma at 3.3 kPa for an extrinsic gettering layer of ultra-thin Si chips aimed at three-dimensional integrated circuits. This process can be conducted in the presence of trivial amounts of air impurities (~0.01 vol. %), thereby avoiding the use of high-vacuum equipment. We investigated the dependence of defect formation behavior on various processing parameters such as H_2 flow rate, processing time, substrate temperature, and input power. It was determined that the absence of H_2 gas flow was favorable for the defect layer formation because Si etching by hydrogen atoms was suppressed. A low Si temperature and high input power are desirable for a high defect density in the shallow surface region of the extrinsic gettering layer. When pulse-modulated plasma irradiation was attempted, the defect layer that formed became thinner and had a higher defect density than that obtained by continuous plasma, demonstrating good Cu gettering performance. Without using harmless chemicals, or high-cost equipment, a shallow gettering layer can be formed using inexpensive H_2 gas.

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I. INTRODUCTION

The fabrication of ultra-thin Si wafers (~5 μm) is a key technique in three-dimensional integrated circuits (3D ICs). 3D ICs are fabricated by three-dimensionally stacking the Si wafers and interconnecting each stack using a through-silicon via (TSV).[1–3] In 3D ICs, stacking thinner Si wafers contributes to a higher integration of the device and a shorter TSV, which results in lower power consumption and a higher clock rate. However, as the Si wafer thickness decreases, it tends to break due to its lower mechanical strength. In addition, the diffusion of metal impurities from the back surface of the wafer to the device layer is a critical issue for device reliability. Metal contamination should be avoided because it can result in the degradation of transistor performance.[4] By using a thick Czochralski-grown Si (Cz-Si) wafer, oxide precipitates in the Si bulk (due to an oxygen solid solution of 10^{17}–10^{18} cm^{-3}) can trap metal impurities to protect the device layer from metal contamination,[5–8] also known as intrinsic gettering (IG). However, when the wafer is thinned down to less than 10 μm,[9] IG is no longer effective in protecting a device layer. Therefore, a metal-trapping extrinsic gettering (EG) layer should be introduced on the back surface of the wafer. Dopant diffusion gettering (DDG) is known as one of the EG methods.[10,11] However, DDG requires hazardous chemicals, such as $POCl_3$ and BCl_3, as dopant sources and high temperatures for dopant diffusion. Usage of these gases is hoped to be avoided as far as possible from the viewpoint of reducing the environmental load, although these gases are familiar in the semiconductor industry. In addition, a high-temperature process is hoped to be possibly avoided for preventing the thermally induced wafer damage. Meanwhile, intentionally induced defects in Si wafer also collect metal elements.[12] Mizushima *et al.* have proposed a mechanical damage gettering (MDG)[9] technique for a 4-μm-thick dynamic random access memory wafer. The MDG layer is formed via dry polishing (DP) after grinding for wafer thinning and chemical–mechanical polishing (CMP) for stress relief. Due to the low mechanical strength of the ultra-thin wafers, the processing pressure on the wafer during fabrication should be strictly controlled to avoid wafer breakage. Moreover, a long thinning process time for ultra-low processing pressures and a hazardous and expensive slurry for CMP are required.

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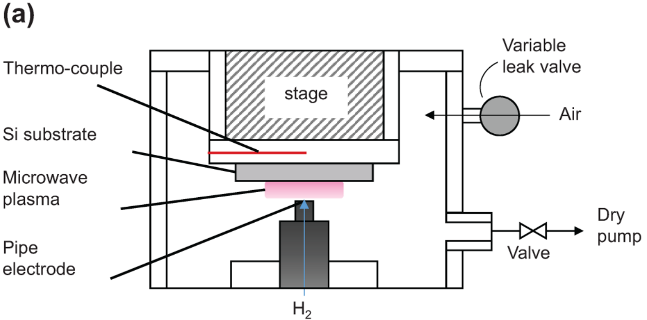
Recently, we have demonstrated a damage-free Si thinning process using a moderate-pressure (above 1.3 kPa) H_2 plasma as an alternative to the conventional mechanical thinning process,[13] regardless of the many studies on the low-pressure H_2 plasma treatment of Si substrates, demonstrating the formation of H-induced defects in the Si bulk.[14–17] In our study, a higher etching rate was important for preparing thinner and non-damaged Si wafers within a shorter process time. If the etching rate becomes lower than that of conventional low-pressure H_2 plasma, a defective layer on the Si surface can be prepared using moderate-pressure H_2 plasma. This opens a consistent H-based procedure from the wafer-thinning to shallow defect layer formation. From our previous study,[18] if a high-density defect layer can be formed on a Si surface using moderate-pressure H_2 plasma, the negligible Si etching rate should be achieved, which can be realized by stopping the H_2 gas flow and introducing trivial amounts of air impurity. These trivial amounts of air mean that the process does not require expensive high-vacuum equipment. Our technique requires only inexpensive and harmless H_2 gas. Therefore, the formation of an EG layer on ultra-thin Si wafers owing to the use of inexpensive H_2 plasma is an attractive process. Control of defect layer thickness is critical for device reliability, and it should be reduced to several hundred nanometers in the newly developed ultra-thin Si wafers for 3D ICs.[19] To control defect density and defect layer thickness, we investigated the dependence of the defect formation behavior in moderate-pressure H_2 plasma on processing parameters such as H_2 gas flow rate (F_H), processing time (t), processing temperature (T_s), and input power for plasma generation ($W_{\mu W}$). In addition, the pulse-modulated plasma generation was proposed for the formation of extremely thin- and high-density defect layers. We also demonstrate the Cu gettering performance of a defect layer prepared using the proposed technique.

II. EXPERIMENT

A schematic diagram of the experimental apparatus used in this study is shown in Fig. 1(a). In the experiment, p-type Cz-Si (001) of 525 μm thickness and n-type Fz-Si(001) of 500 μm thickness, with resistivities ranging from 1–100 and 4200–9500 Ω cm, respectively, were used as Si samples. Each 4-in. wafer was cut into 3×3 cm^2 pieces, and the square Si sample was fixed on a temperature-controlled Al stage. T_s was controlled by the coolant or heater temperature in the Al stage. The H_2 gas used in this study was purified using a Pd purifier to an impurity level of less than 1 ppb. To prepare the process atmosphere after Si sample loading, the reaction chamber was evacuated to less than 13.3 Pa using a dry pump and thereafter filled with H_2 gas up to 40 kPa. This flushing procedure was repeated three times, and H_2 gas was introduced into the reaction chamber through a Mo pipe-type electrode with inner and outer diameters of 2 and 3 mm, respectively, at a given F_H. The processing pressure was kept at 3.3 kPa by controlling the evacuation valve conductance. For $F_H = 0$ slm (standard liters per minute), the chamber was first filled with H_2 gas at 3.3 kPa, and then the H_2 gas supply was stopped. A small amount of clean air was deliberately introduced into the H_2 atmosphere through a variable leak valve at a rate of 2.1 Pa l/min during plasma exposure. The chamber held a volume of 3.2 l. The gap length between the electrode and the substrate surface was adjusted to 0.5 mm. Upon supplying microwave power (2.45 GHz) through a waveguide to the pipe-type electrode, a spatially localized plasma was generated in the gap. The microwave power output was modulated from continuous waves to pulsed waves using a pulse generator. The pulse period (p) was 10 ms, and the duty ratio (D_T) was 0.1–1. The experimental setup shown in Fig. 1(b) was used to evaluate the temperature of the substrate surface during plasma exposure under the given conditions. In this arrangement, a thermocouple with a diameter of 0.18 mm was fixed to the Cz-Si using a Cu tape. It was assumed that the temperature of the thermocouple was equal to that of the substrate surface during plasma processing.

(a)



(b)

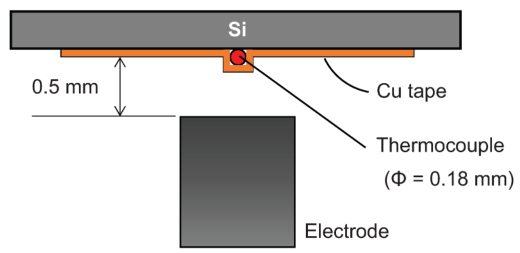


FIG. 1. Schematic of the experimental (a) and surface-temperature measurement system (b).

The defect formation behavior after the H_2 plasma treatment was evaluated using Raman scattering (RS, LabRAM HR-800; HORIBA, Kyoto, Japan) with an excitation laser wavelength of 532 nm and cross-sectional transmission electron microscopy (XTEM, JEM-2000FX; JEOL, Tokyo, Japan). The accumulation time of the RS spectra was 50 s, and the RS spectra around 520 cm^{-1} was corrected for 1 s. To quantitatively evaluate the defects among different Si samples without the influence of the RS equipment setting, the RS intensities at 1800–4200 cm^{-1} of each Si sample were normalized by each Si peak intensity (I_{Si}) at 520 cm^{-1}. Because the RS peaks assigned to Si-H_x and H_2 exist in the ranges of 1900–2300 and 4100–4200 cm^{-1}, respectively,[17,20–26] we integrated the normalized spectrum intensities in the ranges of 1900–2300 and 4100–4200 cm^{-1} and denoted them as I_{SiH} and I_{H_2}, respectively. For the XTEM observations, the Si sample was processed using a focused ion beam (FIB, FIB-2100; HITACHI, Tokyo,

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Japan) with a Ga^+ beam at an acceleration voltage of 40 kV and currents of 0.01–1.10 nA. The defect layer thickness (d) was determined from the XTEM images. The horizontal line in the image is defined as a regression line calculated from the valley depths of the surface profile. In addition, d is defined as the distance between the deepest defect and a horizontal line passing through the top point of the substrate surface. The density of SiH was calculated from I_{SiH}/d. The surface profiles of the samples were measured by using a stylus surface profiler (Surfcom 590A; TOKYO SEIMITSU, Tokyo, Japan). Because the surface etching depth distributed on the Si surface depending on the relative position to the electrode,[13] the depth etching rate (*ER*) was calculated from the depth in the position of 1.2 mm away from the central axis of the electrode. The demonstration of Cu gettering by the H-induced defect layer was conducted using the procedure illustrated in Fig. 2. Cu was selected as an impurity metal, because Cu has high diffusivity in Si[12,27] and is frequently used as a wiring metal. After plasma treatment, the Si sample was dipped into a SC2 solution (35 wt. % HCl:30 wt. % H_2O_2:H_2O = 1:2:6) at 90 °C for 10 min, and thereafter, dipped into a 1 vol. % HF aqueous solution at 20 °C for 1 min to remove metal and oxide contaminants. The sample was mounted on a clean Si wafer with the plasma-exposed surface facing downward. The sample was masked using an Al foil with a $26 \times 26\,mm^2$ aperture for Cu evaporation. A 10-nm-thick Cu film was deposited on the rear side of the plasma-exposed Si. Subsequently, the Si sample was loaded into an annealing furnace. The sample was heated up to 700 °C at a ramp rate of 50 °C/s and kept for 10 min with N_2 gas flow of 5 slm. The sample was cooled down to 200 °C by N_2 flow over 100 s in the furnace. After that, the sample unloaded from the furnace was stored in the clean-room air at around 20 °C. Twenty-two days later, the depth profiles of the Cu concentrations were evaluated at two points using secondary ion mass spectroscopy (SIMS). One measurement point was in the plasma-exposed region (p1), and the other point was outside the plasma-exposed region (p2), as shown in Fig. 2.

III. RESULTS AND DISCUSSIONS

A. Effect of H_2 gas flow

Figure 3 shows the normalized Raman spectra of Cz-Si samples prepared at various F_H. The plasma was exposed for $t = 10$ min at $T_s = 15$ °C, $W_{\mu W} = 200$ W, and $D_T = 1$ (continuous microwave). The *ER* for 0.5 and 0 slm in Fig. 3 are 13.0 and 0 μm/min, respectively. The surface temperature of the substrate during plasma exposure at $F_H = 0$ slm is 430 °C. This suppression of Si etching is due to an excessive increase in the substrate temperature because the Si etching rate decreases when the temperature increases above 80 °C.[28,29] In addition, the re-deposition of the Si etching product occurring on the Si sample surface was caused by the etching products not being exhausted from the plasma quickly enough due to the lack of a continuous H_2 gas supply from the pipe electrode.

At $F_H = 5.0$ slm, no significant Raman peaks are observed. When F_H is decreased to 0.5 slm, two broad peaks at Raman shifts of approximately 1940 and 2140 cm^{-1} appear, as shown in Fig. 3(a). These peaks are, respectively, assigned to the bonding of interstitial Si and H[17,20] and to SiH_x (x = 2 and 3) around a platelet in an early stage of growth.[21] For $F_H = 0$ slm, a significant peak appears around the Raman shift of 2100 cm^{-1}. This prominent peak is a convolution of many Gaussian peaks. A peak at 2093 cm^{-1} is reportedly caused by Si–H bonds in the H-plasma-damaged layer with a thickness of approximately 0.2 μm.[30] The most prominent broad peak at 2100 cm^{-1} is attributed to the Si–H bonds in H-induced platelets.[22] Small peaks at

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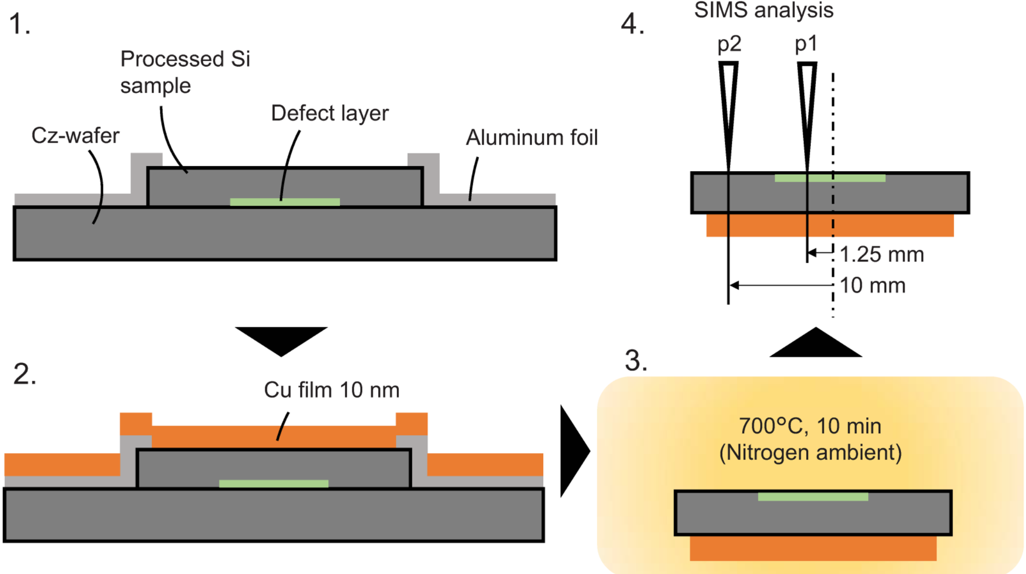

FIG. 2. Schematic of the procedure for demonstrating the Cu gettering performance of plasma-treated Si samples.

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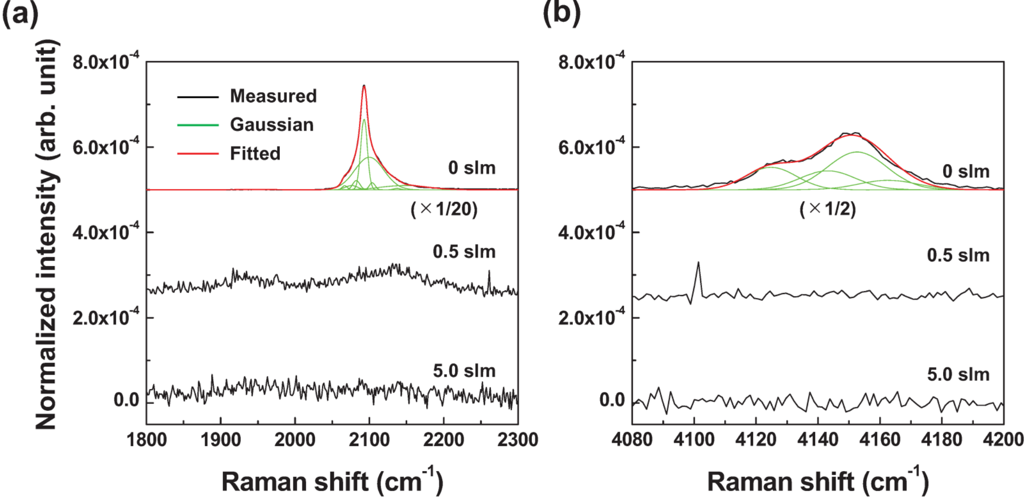

FIG. 3. Normalized Raman spectra in the range of 1800–2300 (a) and 4080–4200 cm^{-1} (b) for Cz-Si processed for 10 min at F_H = 5.0, 0.5, and 0 slm. Plasma was generated at $W_{\mu W}$ = 200 W, T_s = 15 °C, and D_T = 1. Each spectrum was normalized by the peak intensity of Si TO phonon at 520 cm^{-1}. For F_H = 0 slm, Raman intensities were scaled to ×1/20 in (a) and ×1/2 in (b).

2067 and 2082 cm^{-1} originate from the vacancy-H complex.[31,32] Thermal vacancy generation in Si requires an activation energy of 4.2 eV.[33] Reboredo *et al.* reported that the activation energy of a vacancy-H complex defect (VH_4) generation is at least 2.1 eV.[33] This relatively high activation energy for VH_4 generation is the reason for the small peaks at 2067 and 2082 cm^{-1}. In contrast, vacancies can be formed by H ion implantation into crystalline Si, and the incident energy thresholds for Si displacement by H^+, H_2^+, and H_3^+ implantation are approximately 100, 50, and 20 eV,[34] respectively. In our H_2 plasma, these H ions seem to impinge on the substrate after a few collisions with H_2 molecules.[18,35,36] However, considering that the plasma potential at $W_{\mu W}$ = 150 W should be less than 10 V, based on the previous study,[18] the ion incident energy in the present plasma did not reach the threshold values of H^+ and H_2^+ for the displacement of lattice atoms in crystalline Si. Only the thresholds for H_3^+ were comparable. In our plasma treatment, the substrate surface was exposed to high-density H atoms[37] and ions; some of the Si–Si bonds in the bulk Si could be broken by the insertion of diffused H atoms. After breaking some Si bonds, it is expected that the displacement of the Si atom occurs easily by the lower energy ions. This is because the breaking of bonds results in a decrease in bond strength, making the atoms more susceptible to displacement. Vacancy defects are then formed by H_3^+ bombardment with the assistance of Si–Si bond breaking by H atoms. In addition to the above Si–H-related peaks, a new peak appears between 4100 and 4200 cm^{-1} only when F_H is 0 slm, as shown in Fig. 3(b). This peak is deconvoluted into four Gaussian peaks at 4125, 4143, 4153, and 4163 cm^{-1}, which are assigned to the vibrations of H_2 molecules in the Q1, Q2, Q3, and Q4 branches, respectively, of the rotational energy level.[23–26] These signals from 4100 to 4200 cm^{-1} indicate that the H_2 molecules exist in voids and platelets. Based on the above results, H_2-contained voids and platelet defects are caused by plasma treatment without H_2 gas flow. When H_2 gas flow is non-existent, the temperature is increased sufficiently to form platelet defects by plasma irradiation because the platelet defect formation is a thermally activated process.[38,39] In addition, when a higher etching rate condition at F_H of more than 0.5 slm is employed, the effective formation of the defect layer becomes impossible due to the extremely high etching rate of the layer. From these results, we can conclude that the condition of F_H = 0 slm is optimal for high-density defect layer formation.

B. Influence of processing time

To control the defect layer thickness, the dependence of the defect layer thickness on processing time was investigated. Figure 4 shows XTEM images of the Si samples processed for t = 10 and 1 min. Plasma was generated at T_s = 15 °C, $W_{\mu W}$ = 150 W, F_H = 0 slm, and D_T = 1. At these conditions, the surface temperature of the substrate was 351 °C. As shown in Fig. 4(a), small platelet defects between 50 and 90 nm in size are formed after 10 min of plasma exposure, and the thickness of the defect layer reaches 1.0 μm. In addition, Fig. 4(a) shows that the 10-min plasma exposure formed a needle-like structure with heights approximately the same as the defect layer thickness. This phenomenon has been investigated and discussed in a previous paper.[18] Moreover, it is clear that needle-like Si contains many defects seen as the dark region. When the processing time is 1 min, the sizes of the H-induced defects reduce to 10 nm or less, as shown in Fig. 4(b). The diagonal black stripes in the bulk Si in Fig. 4(b) are attributed to the bend contours and not to the H-induced defects. Several dark points owing to defects are observed in the near-surface region. In contrast to t = 10 min, at t = 1 min, most defects are

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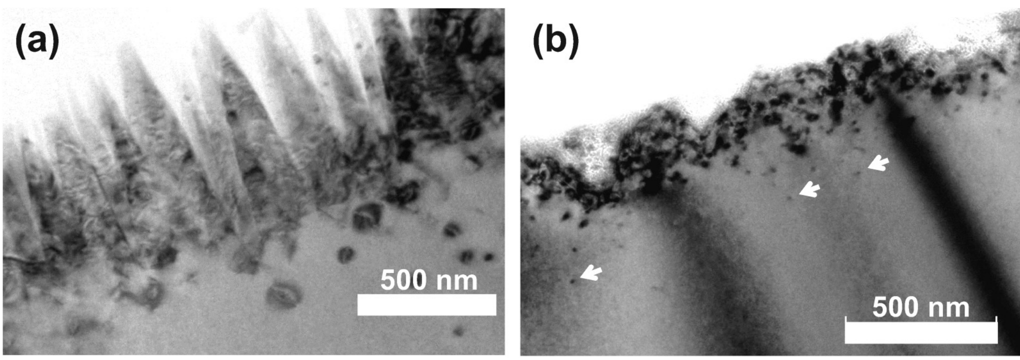

FIG. 4. XTEM images of Cz-Si processed for 10 (a) and 1 min (b). Plasma was generated at $F_H = 0$ slm, $W_{\mu W} = 150$ W, $T_s = 15$ °C, and $D_T = 1$. The white arrow in (b) indicates defects reaching 520 nm from the surface.

concentrated in the region approximately 300 nm from the surface. However, as indicated by the white arrows, some defects are observed at 520 nm from the surface. The defects generated at unexpected depths restrict the chip thickness, and therefore, it is recommended that the thickness of the chip be sufficiently greater than the sum of the device active layer and the defect layer.[19]

C. Influence of substrate temperature and input power

We investigated the dependence of the defect formation behaviors on the temperature and input power to precisely control the defect layer thickness, while retaining high-defect density. Figure 5 shows the dependence of I_{SiH} and I_{H2} on the surface temperature of the Cz-Si sample during plasma treatment. The processing conditions were $W_{\mu W} = 150$ W, $F_H = 0$ slm, and $t = 10$ min. These temperature dependences of H-induced, defect-related intensity are qualitatively in agreement with those of previous studies on H-induced platelet formation.[40,41] The intensity decrease in the higher surface temperatures (≥350 °C) is due to a reduction in the concentration of H in Si near the surface, as the defect detection method relies on the presence of H in Si. The decrease in H concentration in the Si subsurface can be attributed to two reasons: thermally enhanced H_2 effusion[42,43] and enhanced diffusion of hydrogen into the Si bulk. Figure 6 shows an XTEM image of the Si sample prepared at a surface temperature of 414 °C. Platelet defects are enclosed by red ellipses in Fig. 6, and the broad black lines observed in the needle-like Si structure and bulk Si are bend contours. Compared with the sample shown in Fig. 4(a), which corresponds to the surface temperature of 351 °C in Fig. 5, the defect density decreases, the size of the platelet increases up to 1.5 μm, and the interval between the defects increases. These results are the reason that I_{SiH} and I_{H_2} decrease with increasing

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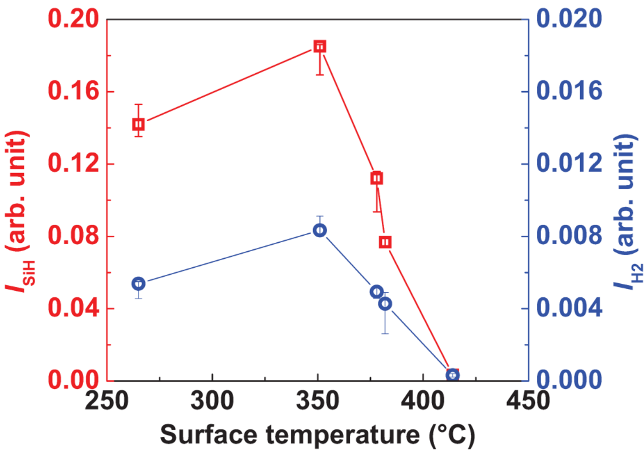

FIG. 5. Integrated Raman intensities (I_{SiH} and I_{H_2}) of Cz-Si after plasma treatment as functions of surface temperature. Plasma treatment was conducted for 10 min at $F_H = 0$ slm, $W_{\mu W} = 150$ W, and $D_T = 1$. Medians of the measured data are plotted. The error bars indicate the interquartile range.

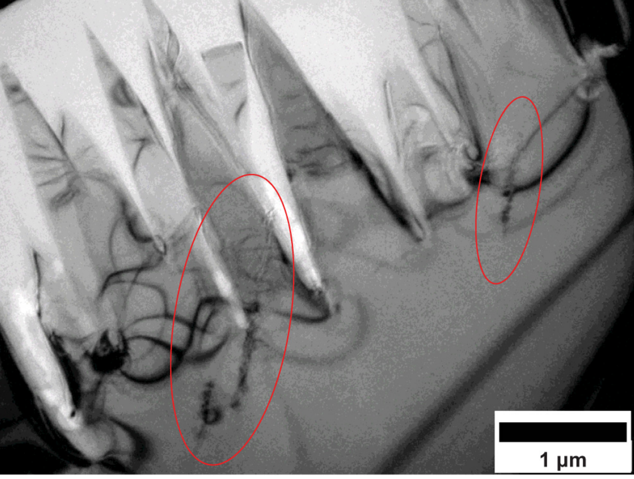

FIG. 6. XTEM image of the sample for a surface temperature of 414 °C. Plasma treatment was conducted for 10 min at $F_H = 0$ slm, $W_{\mu W} = 150$ W, and $D_T = 1$. Platelet defects are enclosed by red ellipses.

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temperature. Meanwhile, unlike the results from Leitch *et al.*,[40] I_{SiH} in Fig. 5 increases with temperature from 250 to 350 °C. As for {111} platelet defects, a reconstruction of the Si–H bonds to form H_2 molecules in a platelet is a thermally activated process with an activation energy of 1.8 eV.[38,39] As reported in the literature,[40,41] the Si–H bonds at the {111} platelets should decrease with an increase in temperature above 150 °C. However, as previously discussed in this study, the defect layers were expected to contain Si–H bonds in the vacancy-H complex. The increase in H-induced defects below 350 °C shown in Fig. 5 is due to the thermal activation of vacancy-H defect formation. Besides, as shown in Fig. 5, I_{H_2} reaches a maximum temperature of 350 °C, which is higher than that reported (250 °C) by Leitch *et al.* Owing to strong Si etching by the high-density H_2 plasma, the removal of H-induced defects near the surface becomes more remarkable than that in the reported reaction system.[13,18,37] The increase in I_{H_2} with a temperature increase from 250 to 350 °C is due to the Si etching suppression with surface temperature. Similarly, a decrease in the etching rate may increase I_{SiH}. One reason for the temperature difference between our results and those reported in the literature[40,41] is the remarkable etching caused by the high atomic H density in our plasma. To investigate the defect formation behavior in terms of whether the defects were formed with a higher density and shallower depth or with a lower density and deeper depth, the I_{SiH} was divided by the defect layer thickness. Figure 7 presents the defect layer thickness (d) and I_{SiH}/d, which indicate that the defect layer thickness significantly increases and that I_{SiH}/d decreases with the surface temperatures above 350 °C. This thicker layer with increasing temperature is due to the enhancement of H diffusion at higher surface temperatures owing to the increase in the diffusion coefficient of H in Si.[44] Therefore, the surface temperature should be reduced to less than approximately 350 °C for an extremely thin gettering layer.

We then investigated the influence of the input power. The input power is related to the gas and surface temperatures, owing to plasma heating and the atomic H density in the plasma. Figure 8 shows the dependence of I_{SiH} and I_{H_2} on $W_{\mu W}$ at $T_s = 15$ °C, $F_H = 0$ slm, $D_T = 1$, and $t = 10$ min. I_{SiH} and I_{H_2} significantly increase with an increase in input power up to $W_{\mu W} = 150$ W. An increase in the input power results in an increase in the atomic H density in the plasma $[H]_p$. In addition, the flux of the H:Si surface (Γ_H) is proportional to $[H]_p$; thus, high input power results in high H density in the Si bulk. A higher input power also results in higher gas and substrate temperatures. It was confirmed that the surface temperature depended on the input power and was lower than 350 °C when $W_{\mu W}$ was lower than 150 W. Considering the results revealed in the previous section, the increase in defect density with increasing $W_{\mu w}$ from 20 to 150 W in Fig. 8 is attributed to an increase in H density in the Si bulk and the thermal activation of defect formation. In contrast, the increases in I_{SiH} and I_{H_2} above 150 W were gradual. Moreover, the I_{SiH} decreases. The H_2 desorption rate exponentially increases with increasing substrate temperature,[43] and H density in the plasma increases with input power; therefore, I_{SiH} reduction above 150 W due to the increased desorption rate becomes more significant than the increase of Γ_H with the increase in $W_{\mu W}$. The substrate surface temperature reached over 350 °C above 150 W. This plasma heating of the Si surface with the increase in $W_{\mu W}$ leads to an enhancement of H diffusion into the Si bulk. Deeper diffusion is unfavorable for the preparation of a shallow defect layer. Based on our results, the simultaneous achievement of a high atomic H density in the plasma and a low surface temperature of the substrate is necessary to fabricate a shallow and high-defect density layer.

D. Defect formation behavior in pulsed plasma

To achieve the process condition described in the previous section, chilling the stage lower than −10 °C is employed. However, this process requires a large amount of energy and expensive coolants, such as liquid perfluorocarbons. Cooling below freezing

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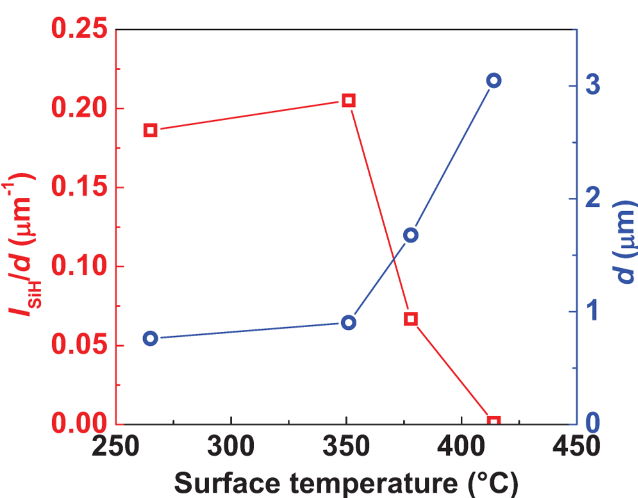

FIG. 7. Variations in I_{SiH}/d and d as functions of surface temperature. Plasma treatment was conducted for 10 min at $F_H = 0$ slm, $W_{\mu W} = 150$ W, and $D_T = 1$.

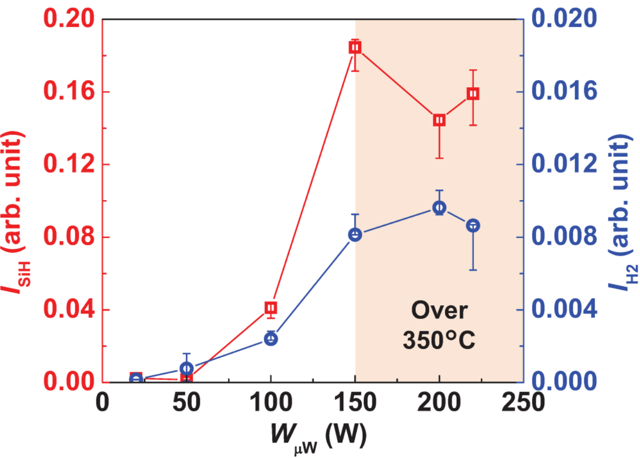

FIG. 8. Integrated Raman intensities (I_{SiH} and I_{H_2}) of Cz-Si after plasma treatment as functions of input power. Plasma treatment was conducted for 10 min at $F_H = 0$ slm, $T_s = 15$ °C, and $D_T = 1$. Medians of the measured data are plotted. The error bars indicate the interquartile range.

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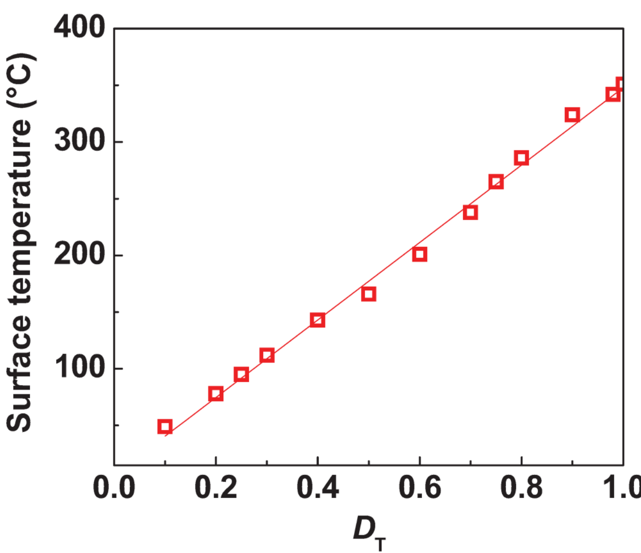

FIG. 9. Dependence of the surface temperature on the duty ratio during plasma exposure. Plasma was generated at $F_H = 0$ slm, $W_{\mu W} = 150$ W, and $T_s = 15$ °C. The red line represents the linear fitting line.

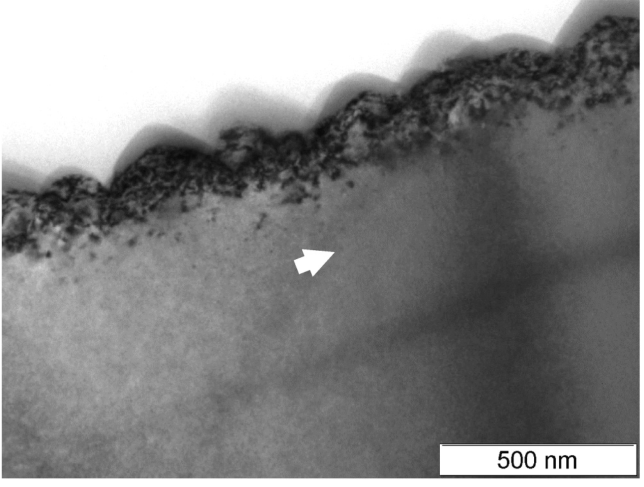

FIG. 10. XTEM image of Cz-Si processed for 20 min at $F_H = 0$ slm, $W_{\mu W} = 150$ W, $T_s = 15$ °C, and $D_T = 0.5$. The white arrow indicates the deepest defect at 410 nm from the surface.

induces the accumulation of residual humidity on the Si surface in the chamber. In addition, the excessive temperature difference between the front surface heated by the plasma and the back surface chilled by the stage induces wafer breakage caused by thermal stress. Thus, we attempted the shallow defect layer formation process without deliberate heating and cooling. A pulse-modulated plasma with high $W_{\mu w}$ was used to suppress the excessive increase of substrate temperature by providing appropriate cooling periods for Si and H_2 gas, while high atomic H density in the plasma could be momentarily obtained. Figure 9 shows the measured dependence of the time-averaged surface temperature on the plasma duty ratio. Plasma was generated at $T_s = 15$ °C, $W_{\mu W} = 150$ W, and $F_H = 0$ slm. As shown in Fig. 9, the surface temperature depends on the duty ratio.

An effective reduction in Si temperature could be expected by employing pulse-modulated plasma. So, Cz-Si was exposed to H_2 pulse-modulated plasma at $T_s = 15$ °C, $W_{\mu W} = 150$ W, $F_H = 0$ slm, and $D_T = 0.5$. The processing time was 20 min, with a total plasma exposure time of 10 min. At these conditions, the surface temperature was 175 °C. Figure 10 shows a TEM image of the Si sample surface after processing. The thick black and gray bands in Fig. 10 are not caused by defects in Si, as mentioned previously. Most defects are concentrated in an extremely thin region on the surface, and the defect, as shown by the white arrow in Fig. 10, is narrowly observed at a depth of 410 nm. This is 100 nm shallower than that shown in Fig. 4(b). The results obtained in Fig. 7 indicate that this is due to a decrease in the surface temperature from 350 to 175 °C, achieved by using pulse-modulated plasma. In addition, the I_{SiH}/d of the Si sample in Fig. 10 is 0.054 μm^{-1}. By contrast, the value shown in Fig. 4(b) is 0.030 μm^{-1}. Thus, the defect layer thickness can be decreased, while maintaining the defect density by substituting the continuous plasma for pulse-modulated plasma. To adjust the plasma irradiation condition, the thicknesses of the defect layers were reduced.

E. Demonstration of Cu gettering performance

We demonstrated the Cu gettering performance of the defect layer prepared using pulse-modulated plasma. To eliminate the gettering effect of oxide precipitates and dopants, we used Fz-Si with a low concentration of oxygen and dopant. As shown in Fig. 10, the plasma treatment was conducted using the same parameters. Figure 11 shows the depth profiles of Cu concentration on the plasma-treated and non-plasma-treated Fz-Si surfaces. As shown in Fig. 11, for the non-plasma-treated Fz-Si, the Cu concentration is 10^{17} atom/cm^3 near the surface and quickly decreases with the sample depth. Also shown is the Cu concentration below the detection limit (5×10^{15} atom/cm^3) of SIMS at a point deeper than 100 nm. Because the solubility of Cu in Si is estimated at 3.6×10^{-2} atoms/cm^3 at 25 °C and 1.1×10^{16} atoms/cm^3 at 700 °C,[27] Cu was not detected in the Si bulk. This slight Cu detection near the surface can be attributed to the fact that the concentration of Cu exceeds its solubility limit in Si around 20 °C, causing it to segregate on the Si surface during annealing. Other than this, a slight Cu contamination might occur during the Cu deposition process. However, the Cu concentration near the plasma-treated Fz-Si surface is 100 times higher than that near the non-plasma-treated Fz-Si. Indeed, the surface area of the plasma-treated Si is enlarged owing to the increasing surface roughness, but it does not reach 100 times that of the non-plasma-treated Si sample. Assuming that the impact of the surface Cu concentration of the position of p1 equals that of p2, the defect layer does collect larger amounts of Cu atoms. In addition, Cu is detected at depths of up to 400 nm from the surface. This depth approximately coincides with the depth at which the defect is narrowly observed by XTEM, as shown in Fig. 10. The peak-to-valley surface roughness

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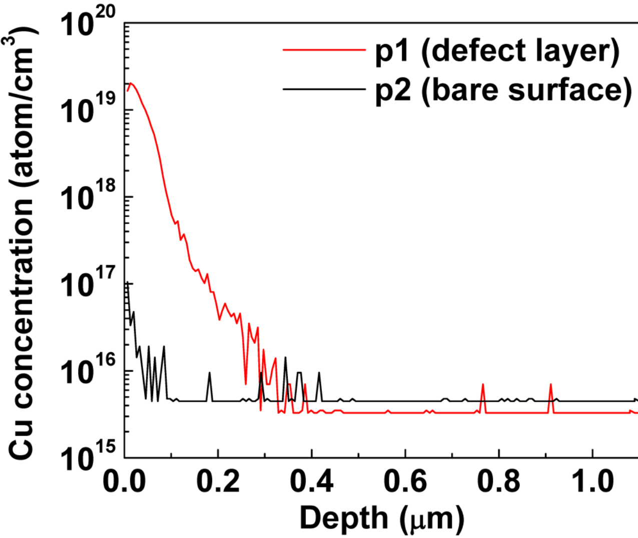

FIG. 11. Depth profile of Cu concentration for the defect layer and the untreated surface of Fz-Si. Processing parameters of the plasma are $F_H = 0$ slm, $W_{\mu W} = 150$ W, $T_s = 15$ °C, and $D_T = 0.5$. Cu diffusion annealing was conducted at 700 °C for 10 min after preparing a 10 nm-thick Cu film on the Si back surface.

of the plasma-treated Si attains 150 nm as shown in Fig. 10. Even if taking into consideration that this surface roughness influences the Cu depth profile, Cu atoms are not only segregated on the surface but also trapped in the defect layer. Considering the surface roughness, Cu trapping depth might be 400 ± 150 nm from the surface. When the Si temperature is increased to 700 °C for Cu diffusion, the H-terminated Si dangling bonds vanish. Integrating the Cu concentration from the surface to a depth of 400 nm of Fig. 11 reveals that 10^{14} atoms/cm^2 of Cu impurities are trapped in the defect layer. Because the initial Cu density on the back of Si is 10^{16} atoms/cm^2, 1% of the initially supplied Cu was trapped by the defect layer during the annealing. Considering that the Cu film is left on the back surface even after annealing, the proportion of Cu atoms trapped by the defect layer will solely increase due to the Cu atoms that have diffused into Si. Although it is known that recombination centers are activated even in Fz-Si wafers through thermal annealing of 400–800 °C,[45,46] the plasma-induced defect layer can collect Cu atoms without an influence of these recombination centers, in comparison with Fz-Si bulk. The obtained results indicate that H_2 plasma-induced defects can act as a gettering sink for Cu impurities. Thus, an extremely thin and high-density defect layer with good gettering performance for Cu can be achieved by using a moderate-pressure pulse H_2 plasma treatment. In a future study, two factors, concrete gettering efficiency and how many Cu atoms of initially supplied Cu atoms can be captured in the defect layer would be examined.

IV. CONCLUSIONS

In this study, the effects of the processing parameters in H_2 plasma treatment on the defect formation behavior of Si wafers were investigated. H-induced defects were effectively formed when the continuous gas supply was stopped, and the Si etching by the H_2 plasma was relatively suppressed. The defect density increased with increasing the substrate temperature and reached a maximum at a given temperature. However, excessively high temperatures reduced the H-induced defect density owing to the thermal effusion of H atoms from Si. In addition, high temperatures increased the thickness of the defect layer. The input power for plasma generation is a useful parameter for controlling the defect density. However, when the input power was increased, the high power resulted in an excessively high substrate temperature, leading to a decrease in the defect density. To simultaneously achieve both a low substrate temperature and a high-density H in the plasma, pulse-modulated plasma was employed. An extremely thin, high-density defect layer was fabricated on the Si surface using pulse-modulated plasma. The defect layer depth attained by pulse-modulated plasma treatment was shallower than that obtained by shortening the processing time in continuous plasma treatment. The shallow defect layer obtained by the moderate-pressure pulsed H_2 plasma displayed a good gettering performance for Cu contamination.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Toshimitsu Nomura: Data curation (lead); Formal analysis (lead); Investigation (lead); Methodology (lead); Visualization (lead); Writing – original draft (lead). **Hiroaki Kakiuchi:** Supervision (equal); Validation (equal); Writing – review & editing (equal). **Hiromasa Ohmi:** Conceptualization (lead); Funding acquisition (lead); Project administration (lead); Supervision (lead); Validation (lead); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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