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REGULAR PAPER

0.36 μW/channel capacitively-coupled chopper instrumentation amplifier in EEG recording wearable devices for compressed sensing framework

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We evaluated the effectiveness of a low-current-consumption amplifier for a compressed-sensing (CS) framework in wearable electroencephalography (EEG) recording devices. The amplifier uses a capacitively coupled chopper instrumentation amplifier (CCIA) architecture which is often used for low-noise amplifier (LNA) to achieve low consumption and low-noise characteristics. According to measurements of the designed CCIA, the power consumption was 0.36 μW/channel, and the input referred noise (IRN) was 4.47 μVrms. The measured IRN and simulations were used to confirm the effect of CCIA noise on the CS-based EEG measurement framework. The difference in the normalized mean squared error at CR = 4 to the uncompressed conditions could be reduced to 0.008. The findings show that even with the LNA specialized for low power consumption, a slight signal degradation is observed when the compression ratio is increased up to 4 in the CS framework by utilizing the sparsity of EEG in the frequency domain.

1. Introduction

In recent years, the application of electroencephalography (EEG) has not been limited to healthcare, and new technologies such as brain-computer interfaces have been developed. Wireless EEG recording devices have also attracted attention, and these devices must be wearable and lightweight to reduce the user burden and regulate user activities. However, extending the operating time of wearable devices typically involves increasing their battery size and weight. Therefore, research has recently been undertaken to reduce the power consumption of wearable devices via compressed sensing (CS)[1] with the aim of reducing the amount of data to be transmitted. For example, several reports have been made on integrated circuit implementations and low-power dissipation measurements for electrocardiographs, electromyographs, and ultrasound echo devices.[2–4] Additionally, research is underway to incorporate CS into EEG. For example, CS is vulnerable to artifact contamination.[5] However, in recent years, an EEG measurement framework using CS that is resistant to blink artifact contamination[6–8] was proposed, and its practical applicability has been enhanced. Examples are also present on low-consumption EEG measurement frameworks running on thermoelectric generation that have been implemented and confirmed to consume less power as a system.[9] Moreover, research on integrated circuits for wireless EEG recording devices is ongoing.[10]

Capacitively coupled amplifiers[11–13] with a high input impedance are used in instrumentation amplifiers for EEG measurements because of their connection electrodes.[14] The capacitively coupled chopper instrumentation amplifier (CCIA) architecture, which adds a chopping technique to the above configuration, has been extensively used as a low-noise amplifier (LNA) for EEG measurement.[15–23] In general, a tradeoff is present between the input referred noise (IRN) and the power consumption of an LNA. Research has been conducted to optimize this tradeoff, and the application of CS is considered one of the solutions. For example, in CS, the EEG signal is assumed to be sparse when mapped on a certain basis. Various bases are known[24–27]; for example, in the case of frequency-domain-based transforms,[28] flicker noise, which has strong frequency dependence, reportedly has significant effect on the reconstruction accuracy, while thermal noise, which has power over a wide bandwidth, has a weak effect on the transform.[29] Because the EEG signal is distributed mainly in the frequency band below 100 Hz,[30] reducing flicker noise is essential for improving the signal-to-noise ratio. In addition, the low power consumption of the LNA is important for the realization of wearable EEG recording devices. Considering a system using bluetooth low energy (BLE), the power consumption of the RF circuit increases only during communication,[31] and the majority of the current consumption is accounted for by the RF circuit.[32,33] Outside of communication, most of the power consumption is determined by the circuits contributing to sensing. The power consumption of the LNA, which is in constant operation, is one of the circuits that consume power on the sensing circuit. In previous studies, the power consumption of the LNA comprised a large proportion of the total system power consumption, including the analog front end.[34–36] Therefore, a lower power consumption of the LNA leads to smaller and lighter batteries, and thus, low-consumption AFE ICs and AFE ICs with RF circuits have been developed, although LNAs still account for a large proportion of power consumption in some cases.[37,38] When considering 10-to-20-channel EEG-recording devices,[39] we set a power consumption target of 0.5 μW for one LNA channel to maintain the total power consumption of LNAs below the majority of the above IC[38] even at a large number of LNAs. As described above, in the CS framework, the LNA characteristic that critically affects signal compression and reconstruction is not thermal noise but flicker noise, which mitigates the tradeoff between thermal noise and power consumption in the characteristics of LNAs. In this study, we design an LNA that is specialized for flicker noise suppression and thermal noise with some magnitude using the CCIA architecture. We aim to demonstrate that signal degradation can be mitigated within a CS framework, even when employing a low-power LNA with significant noise in the system.

In this study, we extend the research presented in our international conference paper.[40] We present the measurement results for the designed LNA and the results of signal processing using CS framework, which utilizes random

undersampling[41] based on the measured LNA data. The remainder of this paper is organized as follows. Section 2 presents the circuit configuration and features of the designed CCIA. Section 3 presents the CCIA measurement results. Section 4 presents the simulation results for signal processing using the proposed framework based on the measurement results in Sect. 3. Section 5 concludes the paper.

2. Designed CCIA

As described in the Introduction, when reconstructing using frequency domain sparsity in the CS framework, flicker noise is susceptible to reconstruction while thermal noise is not. Considering this characteristic, the use of a low-power LNA with suppressed flicker noise and high thermal noise can contribute to reducing the overall AFE power consumption while minimizing signal degradation. This section describes the design of an LNA to realize the aforementioned system. Figure 1 illustrates the CCIA designed for this study. A 180 μm CMOS process was used for the design. Because the impedance of the electrode is high in EEG measurements,[42] a capacitor for positive feedback loop was employed to increase the input impedance.[43] Although the signal characteristic of the input node of the CCIA operational amplifier is AC, it requires an appropriate DC bias to ensure proper amplification.[44] In Fig. 1, as in previous studies,[43,44] a high resistance is generated and used with NM_1 and NM_2 to ensure the stability of the capacitively coupled nodes. The N_{BIAS} node is supplied from outside the chip. Figure 2 shows the circuit diagram of the amplifier used in Fig. 1. As in a previous study, a folded cascode is used to achieve low-supply voltage operation and high gain.[16] Indirect phase compensation technology is used for phase compensation to generate zeros at high frequencies, even when the node impedance increases.[45,46] In addition, a common-mode feedback (CMFB) circuit based on the output voltage of the CCIA is used, and the signal is amplified around V_{CM}, which is half of V_{DD}. The CCIA operates with $V_{DD} = 1.8$ V.

R_{CM1} and R_{CM2} are used for the CMFB and feedback the center of the output voltage. The operational transconductance amplifier (OTA) used for CMFB is shown in Fig. 3. The circuit configuration of the CMFB circuit, including R_{CM1} and R_{CM2}, is general.[47,48] In addition to the 4-channel CCIA, V_{CM} generate circuit and CMFB circuits were designed in this study, and the simulation results indicate that the current consumption of the entire chip is 828 nA and the current consumption per channel is 207 nA. This result implies a power consumption of 0.373 μW per channel, a performance that meets the target indicated above. The chopping frequency was set at 5 kHz because of the narrow bandwidth of the amplifier resulting from its low power consumption. To reduce the spike voltage due to chopping, low pass filters (LPFs) consisting of R_{LPF1}, R_{LPF2}, C_{LPF1}, and C_{LPF2} are implemented in the chip. The LPFs are first-order filters with a cutoff frequency of 24.5 kHz and are designed with a high cutoff frequency to allow fine tuning with off-chip anti-aliasing filters. Figure 4 shows the AC simulation results for the CCIA without chopping. Figure 4 shows that the gain from 0.5 to 100 Hz is greater than 37 dB, indicating that sufficient amplification is achieved considering the frequency of the EEG signal.[30] Figure 5 shows the input EEG signal and output differential voltage waveform of the CCIA during chopping. The amplification ratio is identical to that in Fig. 4, indicating that the amplitude of the EEG signal, which was on the μV order, is amplified to the mV order as expected. Figure 6 shows the IRN spectrum of the CCIA during chopping. The maximum value at frequencies above 0.5 Hz is 1.04 μVrms/$\sqrt{\text{Hz}}$. The integrated value of the input equivalent noise calculated from Fig. 6 is 2.9 μVrms.

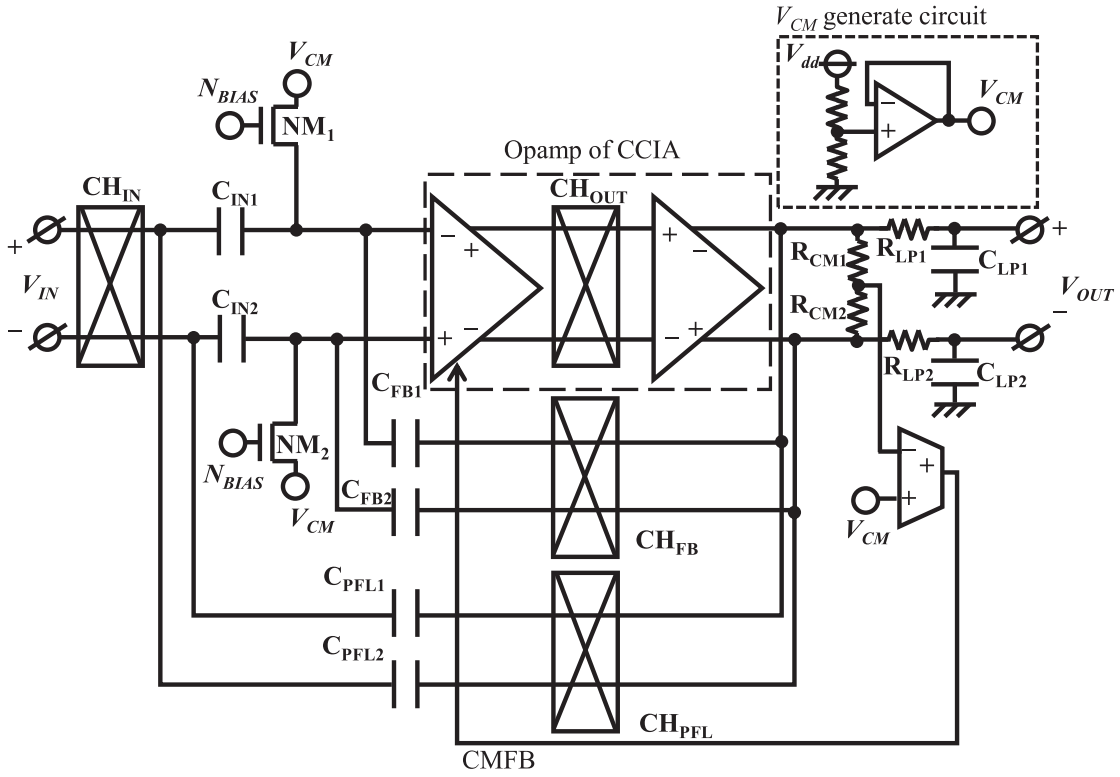


Fig. 1. Configuration of designed CCIA.

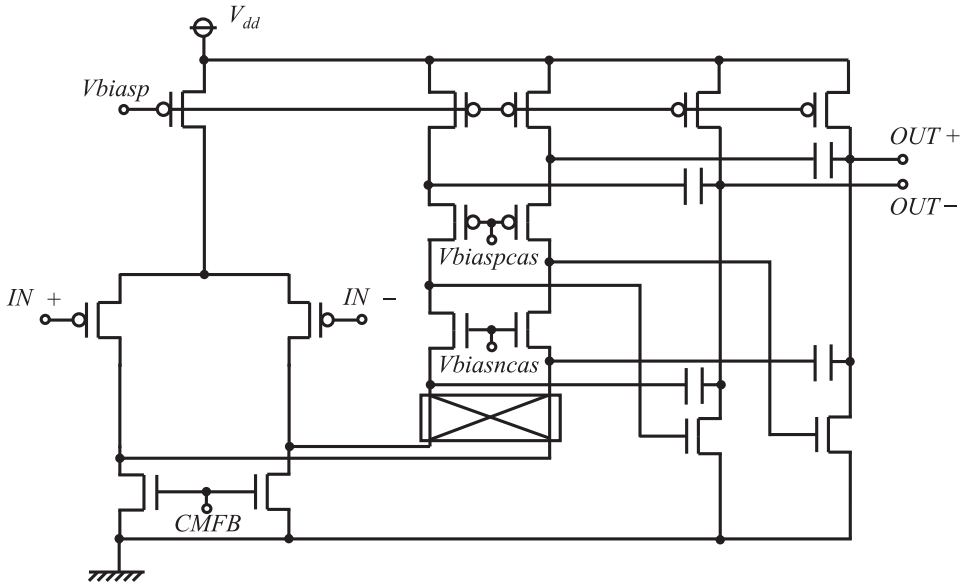


Fig. 2. Schematic of the operational amplifier of the CCIA.

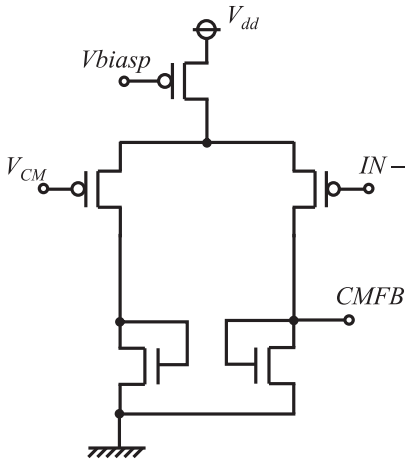


Fig. 3. Schematic of the OTA of CMFB.

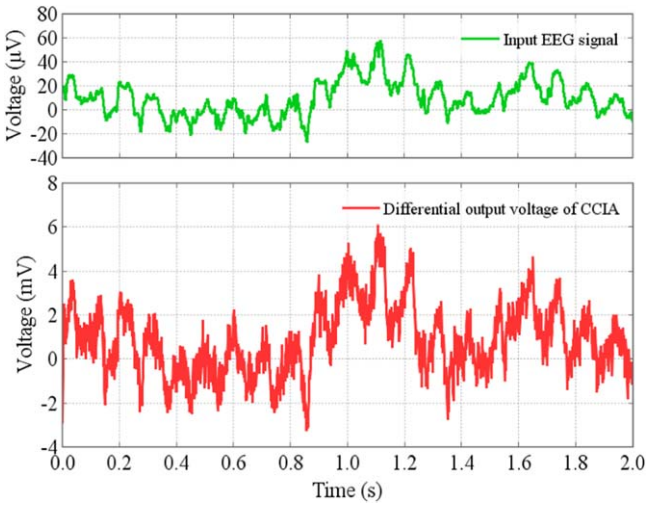


Fig. 5. Simulated input EEG signal and differential output voltage of the CCIA.

3. Measurement results for designed CCIA

Figure 7 shows a photograph of the fabricated chip. The area of each CCIA channel was 0.142 mm^2. Figure 8 shows a photograph of the printed circuit board (PCB) used for the measurements. The PCB was a general two-layer board, and an 84-PLCC was used for the chip package. Figure 9 shows the configuration of the measurement circuit, and Table I presents the conditions and equipment used for the measurement. The total measured quiescent current of the chip was 800 nA, which was approximately equal to that in the simulation, and the current consumption per channel was

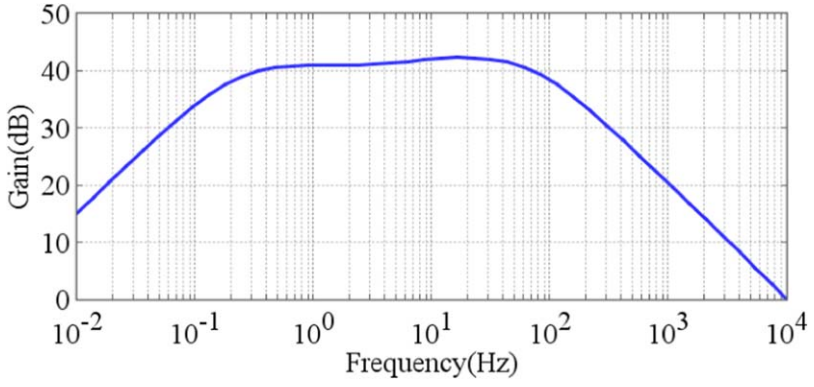


Fig. 4. Simulated gain frequency characteristic of the CCIA in the no-chopping state.

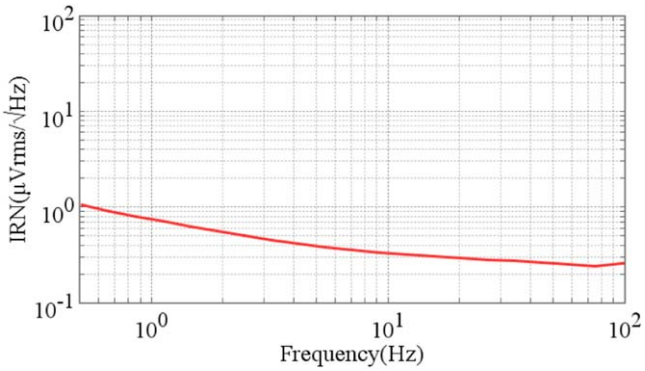


Fig. 6. Simulated noise spectral density of the designed CCIA.

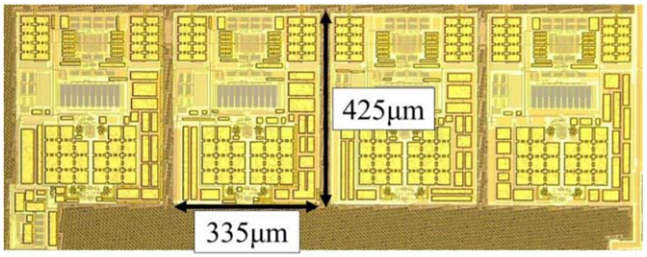


Fig. 7. Chip microphotograph of each CCIA.

200 nA. This result implies a power consumption of 0.36 μW per channel, achieving the target value, which agrees with the simulation result. Because the designed CCIA had low quiescent current, connecting the measurement probes directly to the output pins was impossible; therefore, measurements were performed using LPV542 (Texas Instruments) as a unity gain buffer. The LPV542 had sufficiently low noise and an adequately high cutoff frequency for the designed CCIA; therefore, it did not affect the measurement. In addition, as shown in Fig. 9(a), the oscilloscope output signal was input to the CCIA via an attenuator to prevent clipping of the CCIA output voltage in the gain frequency response measurement. Figure 9(b) shows circuit configuration for measuring the noise spectral density. Figure 10 shows the measured gain frequency response, which match the simulation results, confirming that amplification is possible in the EEG frequency bands. Figure 11 shows the common mode rejection ratio (CMRR) measurements during chopping. Figure 11 shows that the CMRR remains at 80 dB up to 100 Hz, which is sufficient because it is above the 60 dB target set in a previous study.[34] Figure 12 presents the IRN measurement results; the peak at 60 Hz is due to a hum in the power supply and is not due to chip characteristics. As shown, the IRN was significantly lower during chopping compared with the condition without chopping. The results obtained during chopping were generally similar to those of the simulation, with a maximum IRN of 1.78 μVrms/$\sqrt{}$Hz 0.5 Hz. The integrated IRN during chopping, which was calculated from the measurements presented in Fig. 12, is 4.47 μVrms. In the next section, according to the measurement results, we confirm the effect of LNA noise on EEG signal reconstruction by applying the designed CCIA to the CS signal-processing framework with random undersampling.

4. Evaluation results for proposed framework with designed CCIA

In this section, we confirm the implementation of the designed CCIA via a simulation of the CS framework based on the IRN measurement results obtained in the previous section. To confirm the influence of CCIA noise on the reconstruction of EEG signals, a comparison of the LNA noise with a noise-free ideal state is desirable. In this study, the measurement results were reflected in the simulation and compared with ideal conditions. Figure 13 shows the signal processing performed in this study. As shown in Fig. 13(a), the hum caused by the 60 Hz power supply was removed from the measured IRN shown in Fig. 12 and input to the noise-source model. This converted the IRN resulting from the AC measurement into a transient noise waveform that was overlaid on the input of the CCIA. For noise in the frequency band below 100 Hz, which is the critical frequency band of the EEG, the IRN measurement results were used in the simulation as described above. For noise at frequencies above 100 Hz, where the CCIA gain decreased, the simulator generated flicker noise and thermal noise from 100 Hz to 10 kHz based on the process design kit information. Figure 13(b) shows the ideal state in which no noise was generated at all, which was used for reference. In the cases of both Figs. 13(a) and 13(b), the output voltage of the CCIA

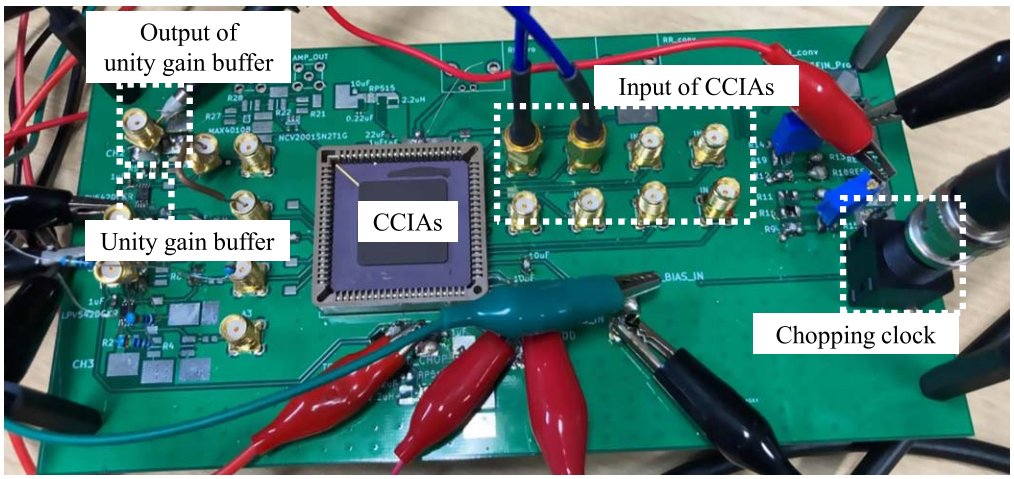
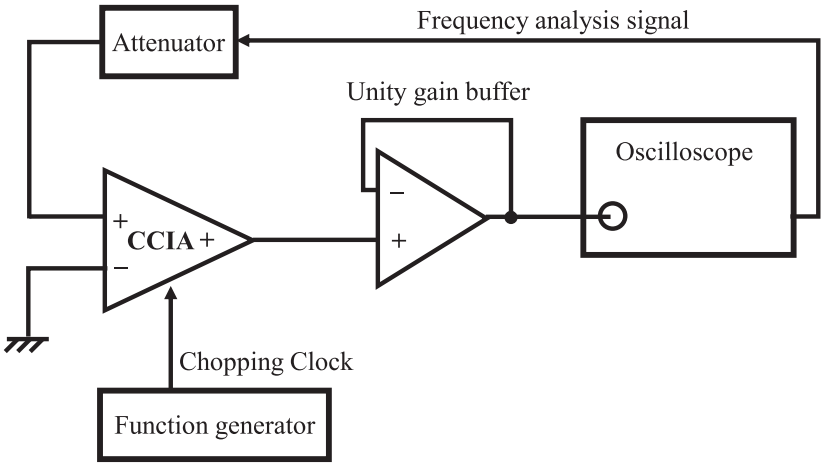
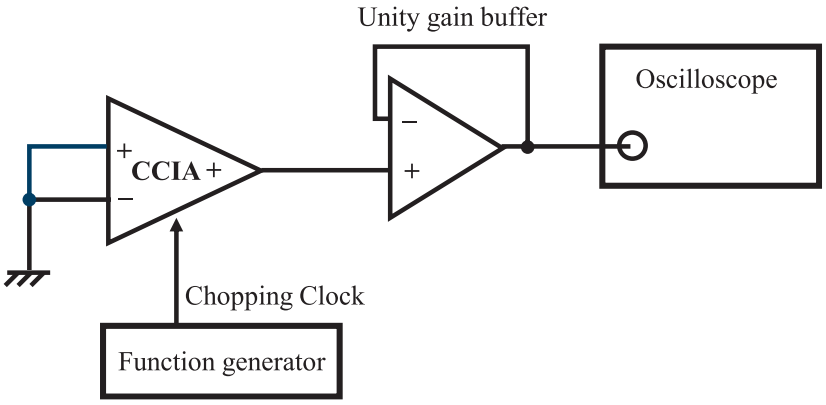


Fig. 8. Part of the PCB used for the measurement.



(a)



(b)

Fig. 9. Circuit configuration for measurement of the designed CCIA. (a) Circuit configuration for measuring the gain frequency characteristics. (b) Circuit configuration for measuring the noise spectral density.

Table I. Measurement parameters and components used.

Parameters and components	Value and model
V_{dd}	1.8 V
Total chip I_Q	800 nA
Chopping frequency	5 kHz
Attenuator	8495B
Function generator	SG-4115
Oscilloscope with frequency response analysis function	MSO44
Unity gain buffer	LPV542

was input to an anti-aliasing filter with a cutoff frequency of 0.54 kHz; then, the signal was sampled at 1 kHz. After sampling, it was converted into a single-phase voltage using a differential-to-single circuit. The single-phase signal was used as the input signal for the CS compression and reconstruction algorithm in the simulations. The amplified signal was compressed via random undersampling.[41] In this evaluation, a block-sparse Bayesian learning algorithm was used for the signal reconstruction. In addition, a discrete cosine transfer basis[28] was used for frequency-domain sparse representation in this study. $x_{noiseless}$ denotes the result obtained without considering noise in the compression and reconstruction of the EEG signal during the CS process, and x_{noise} denotes the result obtained with consideration of noise. The relationship between $x_{noiseless}$ and x_{noise} was evaluated using the normalized mean squared error ($NMSE_{comp}$) as follows:

$$NMSE_{comp} = \frac{||x_{noiseless} - x_{noise}||_2^2}{||x_{noiseless}||_2^2} \quad (1)$$

Using $NMSE_{comp}$ for the results obtained with different compression ratio (CR), the effects of noise and compression can be examined simultaneously. CR can be expressed by the following equation, where N and M represent the numbers of sample points before and after compression, respectively.

$$CR = \frac{N}{M}. \quad (2)$$

A total of 100 frames of EEG signals, such as the waveform shown in Fig. 5, were processed, with 1.5 s as one frame. Figure 14 shows the average $NMSE_{comp}$ for 100 frames. The uncompressed $NMSE_{comp}$ was 0.15, which is reasonable considering previous studies.[28,39] Although some fluctuations were present in the reconstruction due to reconstruction errors, the results in Fig. 14 indicate that for CR = 4, $NMSE_{comp}$ was 0.158, which was almost the same as that in the uncompressed case. This indicates that the CRs

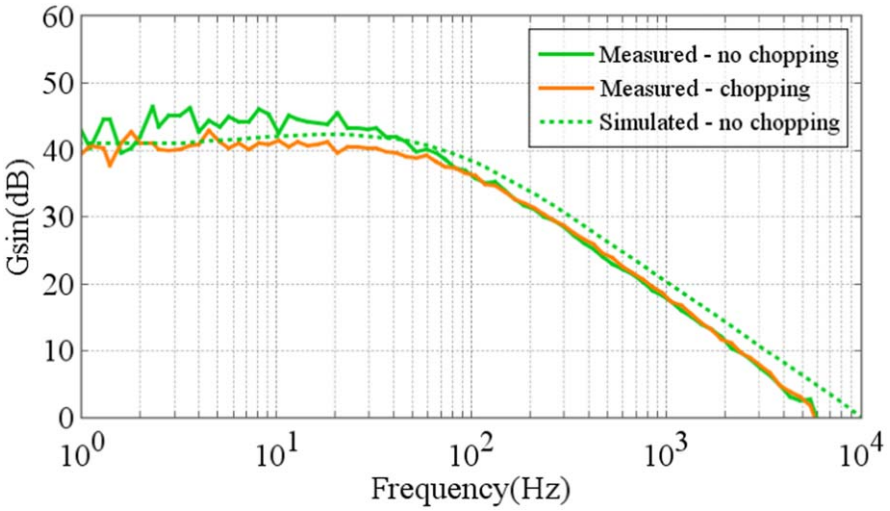


Fig. 10. Measured gain frequency characteristics of the CCIA.

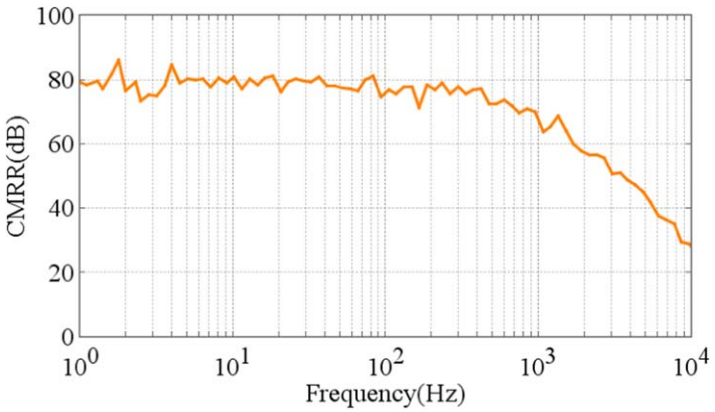


Fig. 11. Measured CMRR characteristics of the CCIA in the chopping state.

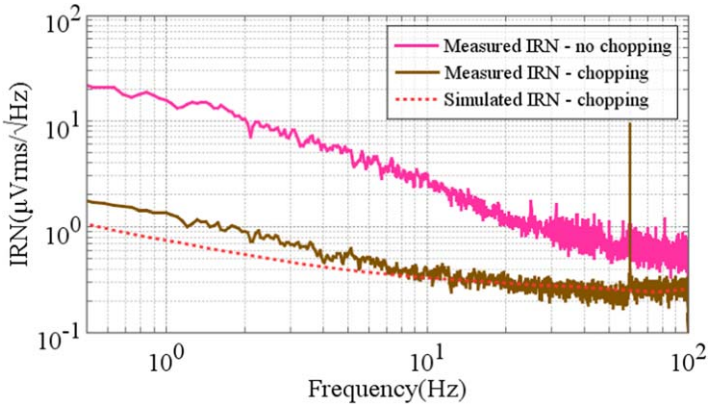
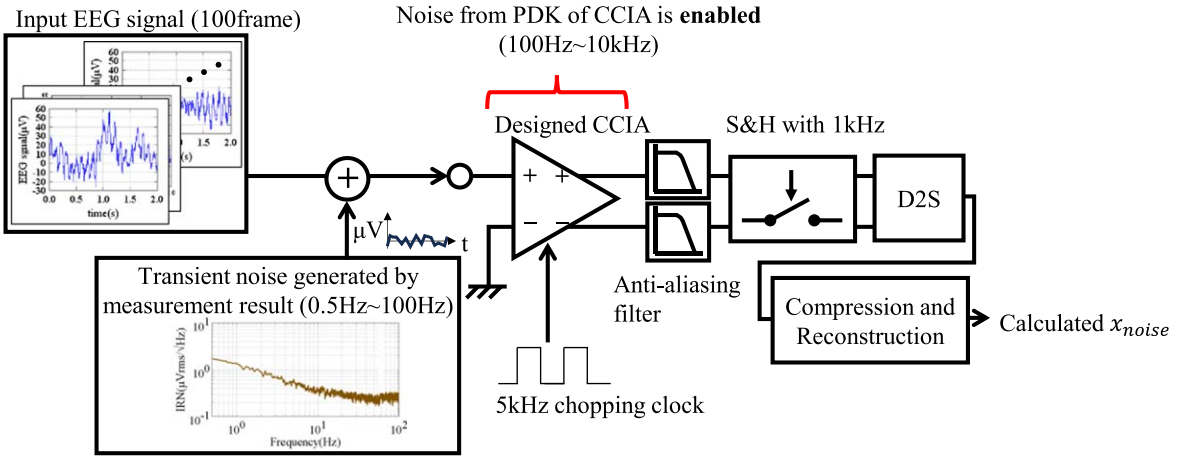


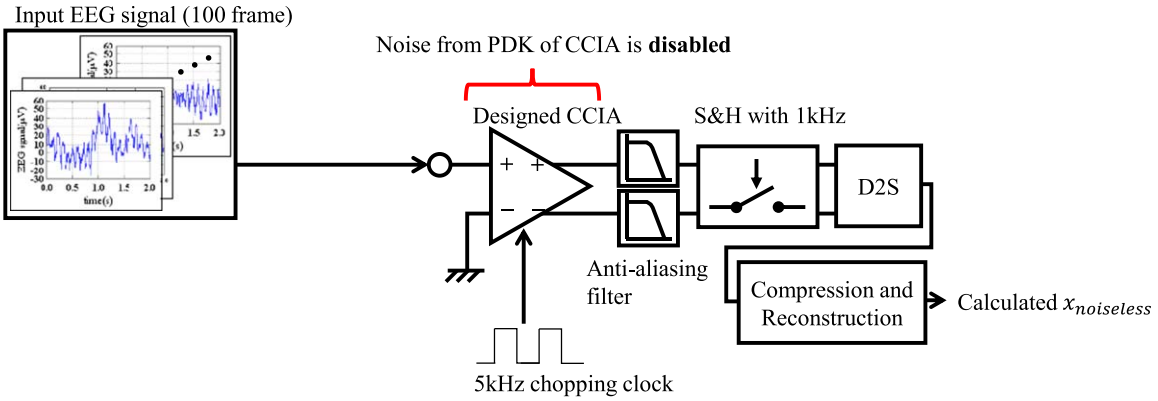
Fig. 12. Measured noise spectral density of the designed CCIA.

from 2 to 4 were reconstructed to the same quality as the uncompressed results, regardless of the presence or absence of noise from the CCIA. This suggests that the proposed CCIA, which was designed with priority for flicker noise reduction and low power consumption, can be used even with CR = 4 in the proposed framework. In this case, $NMSE_{comp}$ increases with CR larger than 5, but $NMSE_{comp}$ generally decreases as CR increases in CS because less information is used for reconstructing.[39] The optimized CR used for CS depends on the type of reconstruction algorithm that is used. In this case, when the algorithm shown above is used, the degradation of $NMSE_{comp}$ due to compression is suppressed up to CR = 4.

Table II compares the CCIA designed in this study with previous studies on LNAs for similar applications. Table II shows that the CCIA designed in this study has lower power consumption than the LNAs in previous studies. Table II also shows that the NEF of the CCIA designed in this study is not notably low. Table II and the results of Fig. 14 verify our assertion that the CS framework can reduce signal degradation even when employing a low-power LNA with significant thermal noise in the system. Therefore, the CS framework



(a) Settings for calculating x_{noise}.



(b) Settings for calculating $x_{\mathrm{noiseless}}$.

Fig. 13. Signal processing performed in this study. (a) Settings for calculating x_{noise}. (b) Settings for calculating $x_{\mathrm{noiseless}}$.

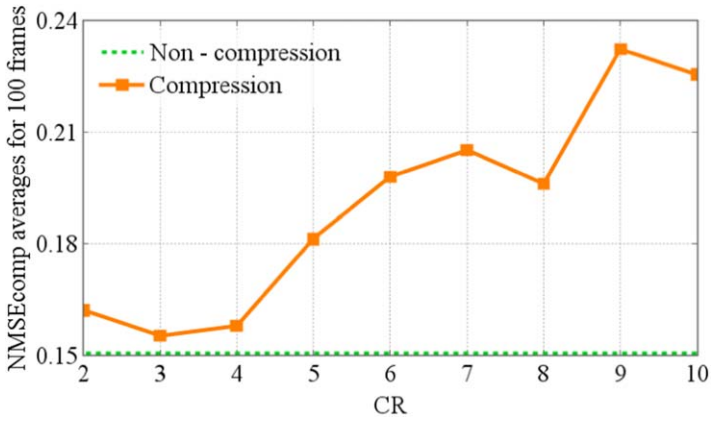


Fig. 14. $\mathrm{NMSE}_{\mathrm{comp}}$ calculation results.

can achieve a smaller battery size for wireless EEG recorders due to the availability of LNAs with low power consumption.

5. Conclusions

We designed a CCIA specialized for low-power consumption and measured its characteristics. Using the IRN measurement results for the simulation, we employed the normalized mean squared error to evaluate the reconstruction effect of the noise generated by the CCIA in a CS-based EEG measurement framework. The measurement results indicated that the power consumption was low which is 0.36 μW per channel, and the IRN was 4.47 μVrms. In simulations using the measured IRNs, the normalized mean squared error was computed for 100 EEG frames, and the result obtained at CR $=$ 4 and the uncompressed result were almost equal. This finding proves that the degradation that occurs during signal compression and reconstruction in the CS framework can be suppressed while using an LNA specialized for flicker noise suppression and low power consumption. Although the NEF of the designed CCIA is not significantly low, the simulation results

Table II. Performance comparison of the designed LNA and previously reported LNAs.

	49	50	51	This work
Application	EEG	EEG	ECG/EEG	EEG
I_Q (μA/channel)	2.3	0.57	7.06	0.2
V_{dd} (V)	1	1.5	1.8	1.8
Power consumption (μW/channel)	2.3	0.855	12.7	0.36
Gain (dB)	55	47.6	40	40
CMRR (dB)	120–95	105.6	120	80
Bandwidth (Hz)	1100	500	170	100
Input referred noise (μVrms)	2.18 (0.1–1.1 kHz)	1.22 (0.5–100 Hz)	3.8 (0.45–100 Hz)	4.47 (0.5–100 Hz)
NEF	3.8	2.91	39	7.69
Chip area of LNA (mm^2)	—	0.065	0.074	0.142

prove that compression may be achieved in the CS framework by using frequency domain sparsity, and the developed wearable EEG recording devices can operate for a long time by reducing power consumption and communication data volume during EEG sensing.

Acknowledgments

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