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REGULAR PAPER

Low quiescent current LDO with FVF-based PSRR enhanced circuit for EEG recording wearable devices

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This paper presents a low quiescent current low-dropout regulator (LDO) with an auxiliary amplifier, flipped voltage follower (FVF)-based power supply rejection ratio enhanced circuit (FBPEC) for electroencephalogram (EEG) recording devices. The FBPEC comprises a FVF filter, current mirror, and common-source amplifier. The FBPEC exploits the characteristics of FVF filter to reduce the current consumption and increase the gain at specific frequencies. The small-signal equivalent circuit reveals the dominant pole of the FBPEC, which is affected by the output impedance and load capacitance of the common-source amplifier. The proposed LDO is designed using a 0.18 μm CMOS process and has improved power supply rejection ratio (PSRR) up to 18 dB at frequencies above 10 kHz compared to the general LDO. The proposed LDO has a low no-load quiescent current 648 nA and a good figure-of-merit score compared to those of previous works, proving that the proposed circuit is an effective solution for use in wearable EEG recording devices.

1. Introduction

The development of wearable devices enables us to easily understand and manage our biometric information. Recent studies on wearable electroencephalogram (EEG) recording devices facilitate health maintenance and support the diagnosis of various diseases. In wearable devices, the battery generally occupies a large portion of the device space, preventing weight reduction. However, a trade-off exists between the battery size and the operating time of the device. Therefore, it is crucial to reduce the overall power consumption of the device to realize small wearable devices capable of operating for sustained periods. Therefore, some studies have proposed sensing frameworks to reduce the overall power consumption of wearable devices with compressed sensing to achieve long operation times using small batteries.[1–4] Research on hardware implementation methods[5,6] and verification using actual devices have been conducted,[7] and the effectiveness of the proposed framework has been determined.

However, the reduction in power consumption of the circuit is equally important. For example, the power management IC (PMIC), which supplies power to the entire system, is always operating, consuming a significant amount of power in a wearable device even in its sleep state.[8] Therefore, the demand for low-consumption current PMICs has been increasing. Low-dropout regulators (LDOs) are commonly used as PMICs owing to their ease of use and low-noise performance. LDOs play a crucial role in a wide range of applications, such as driving noise-sensitive analog, RF, mixed-signal, and digital module interfaces.[9–14] In many cases, power supply circuits use LDOs and switch-mode power supplies (SMPSs) connected in series to optimize their efficiency and achieve a low noise output voltage. Therefore, the power supply rejection ratio (PSRR) characteristic of the LDO is crucial to suppress the output voltage ripple of the SMPS.[15–17] Generally, increasing the PSRR bandwidth of an LDO requires an increase in current consumption, which prevents the realization of small-sized wearable devices capable of operating for extended periods. Studies to improve the PSRR are underway, and a typical example involves a circuit configuration using a feedforward capacitor (C_{ff}).[17–23] However, a discrepancy exists between the output resistance of the SPICE model and that of the manufactured transistor, rendering the accurate design of circuits for high-impedance nodes challenging. Moreover, as the absolute value of the capacitor used for C_{ff} is in the order of a few femtofarads, the characteristics vary drastically during manufacturing. Specific problems include difficulty in accurate design, large characteristic variation, and the requirement for a fast amplifier with high current consumption depending on the topology. Compact and long operating time biometric signal recording wearable device such as the one assumed in this study[1–7] suppresses power consumption by using duty-cycled communication.[24] When a communication method such as Bluetooth low energy is used, tens of milli Amperes of current flows through the RF circuit during wireless communication; however, during other EEG detection, the current in circuits, other than the RF circuit, is less than 1 mA, which is a light load for an LDO. It is particularly difficult to improve the bandwidth of PSRR at light loads, and existing adaptively bias techniques[25–27] that improve the PSRR by increasing the bias current based on the load current are less effective. A hybrid LDO controlled using an analog loop and a digital loop[28] has also been proposed, but its large chip size and current consumption make it unsuitable for wearable devices, despite its outstanding PSRR characteristics.

Based on previous studies, realizing an auxiliary control circuit with low power consumption for PSRR is a simple solution. The technique proposed in this study does not increase the current consumption of the operational amplifier to improve the PSRR. Instead, an auxiliary amplifier, which uses a flipped voltage follower (FVF) filter that is characterized by low power consumption and partial gain in the HF band, improves the PSRR at high bandwidths while suppressing the current consumption. In contrast to our previous work,[29] here we include an analysis using the small-signal equivalent circuit of the FBPEC and LDO measurement results to discuss its circuit behavior in more detail. The remainder of this paper is organized as follows. Sect. 2 describes the overall circuit of the proposed LDO and the ideas referred by us. In Sect. 3, we describe the operation of the FBPEC, an auxiliary amplifier used in the proposed LDO, using small-signal equivalent circuits and simulations. In

Sect. 4, we present the measured results of our prototype chip of the proposed LDO. In Sect. 5, we conclude the paper.

2. FVF-based PSRR-enhanced circuit (FBPEC) in proposed LDO

The circuit configuration of the proposed LDO is illustrated in Fig. 1. C_{out} and R_e denote the output capacitance and the parasitic resistance of the LDO, respectively; R_{f1} and R_{f2} indicate the voltage divider resistors of the LDO. R_{c1}, R_{c2}, C_{c1}, C_{c2}, and C_{c3} are used as phase compensation elements. R_d indicates the damping resistance to ensure stability during transients. The proposed circuit improves the PSRR by using an FVF-based PSRR-enhanced circuit (FBPEC) as an auxiliary amplifier. The circuit illustrated in Fig. 1 is capable of controlling the FBPEC output by using the FBPEC EN signal and a switch. The switch enables us to confirm the differences in the characteristics between the proposed LDO and a general LDO. The configuration of the FBPEC is depicted in Fig. 2. Node A shown in Fig. 2 refers to the input of the FBPEC, node B refers to the output of the FBPEC, and nodes C, D, and E correspond to the internal nodes of the FBPEC. The FBPEC comprises an FVF-filter, a current mirror, and common-source amplifier. The FVF used in the FBPEC has a low impedance at node C, low current consumption, and low-voltage operation. Recently, FVFs have been increasingly utilized to improve the PSRR characteristics of capacitor-less LDOs in systems on a chip.[30–34] In the aforementioned studies, FVFs are used in the main amplifiers for feedback or pass transistors. Specifically, they are used to increase the frequency of the dominant pole. However, previous studies require many amplification circuits, and the low current consumption characteristics for FVFs were not realized. The FVF filter is a circuit configuration that was proposed in a previous study; the filter achieved an unconventional signal amplification when a capacitor C_{cap} was added.[35] In previous studies, the small-signal analysis of the FVF filter has been conducted,[35] and the role of MN1, shown in Fig. 2, in amplifying the signal enables us to achieve HF signal amplification and low quiescent current. However, the FVF filter alone cannot be used as an auxiliary amplifier owing to its low amplifier gain. As shown in Fig. 2, the FBPEC comprises a common-source

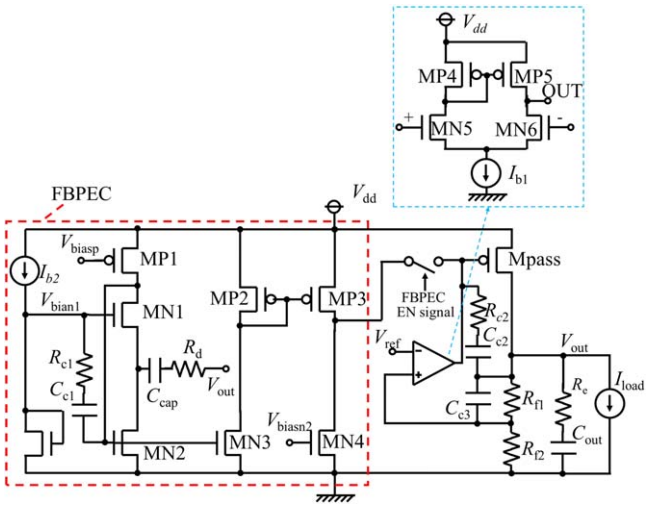

Fig. 1. Configuration of the proposed LDO.

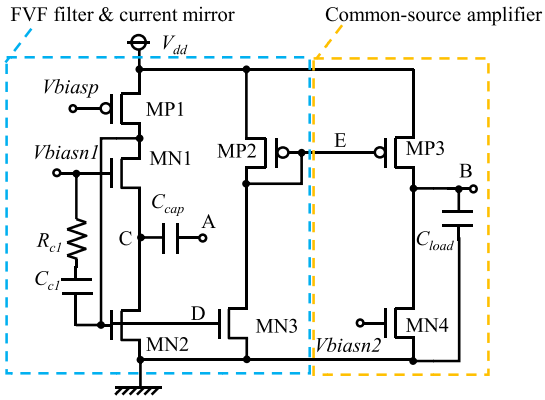

Fig. 2. Configuration of the FBPEC.

amplifier using MN4 and MP3 for the FVF filter to improve its gain, such that it can be used as an auxiliary amplifier. However, stability must be considered by adding an amplification stage composed of MP3 and MN4. R_{c1} and C_{c1} are used as phase compensation elements. In designing the FBPEC, it is crucial to determine or estimate C_{cap} and C_{load}, primarily because the parameters C_{cap} and C_{load} affect the frequency characteristics of FBPEC. As a precondition, a capacitor with a large off-chip capacitance value is used for C_{cap} in the FBPEC design. To express the parasitic capacitance of the pass transistor, a large sized C_{load} is used. The following section presents a small-signal analysis to determine the dominant pole of the FBPEC.

3. FBPEC small signal analysis and simulation results

Figure 3 shows the small-signal equivalent circuit of the FBEC. Here, C_{cap} is much larger relative to the parasitic capacitance of the transistor, and R_d is much smaller than the output resistance of the transistor such that it can be neglected in the small-signal analysis, where *ro* denotes the output resistance of the transistor, *gm* denotes the output conductance of the transistor, and C_p denotes the parasitic capacitance of the transistor. As node *C* is connected to C_{load} via C_{cap}, its parasitic capacitance is relatively small compared to C_{load} and can be ignored. If we assume that the transconductances of all the transistors in the small-signal equivalent circuit shown in Fig. 3 are equal to gm_{MN1}, and the output resistances are equal to ro_{MN1}, then we can observe that the circuit has poles p_D, p_E, and p_B, corresponding to the poles that occur at nodes D, E, and B, respectively. The equation showing the poles are as follows:

$$p_D \approx \frac{gm_{MN1}}{C_p} \tag{1}$$

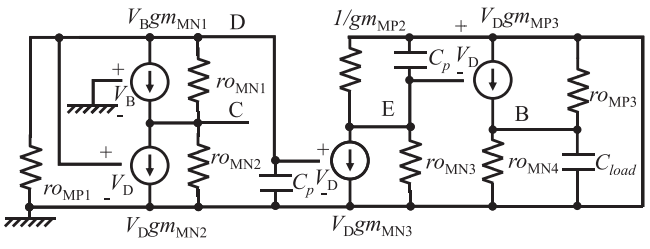

Fig. 3. Small-signal equivalent circuit of the FBPEC.

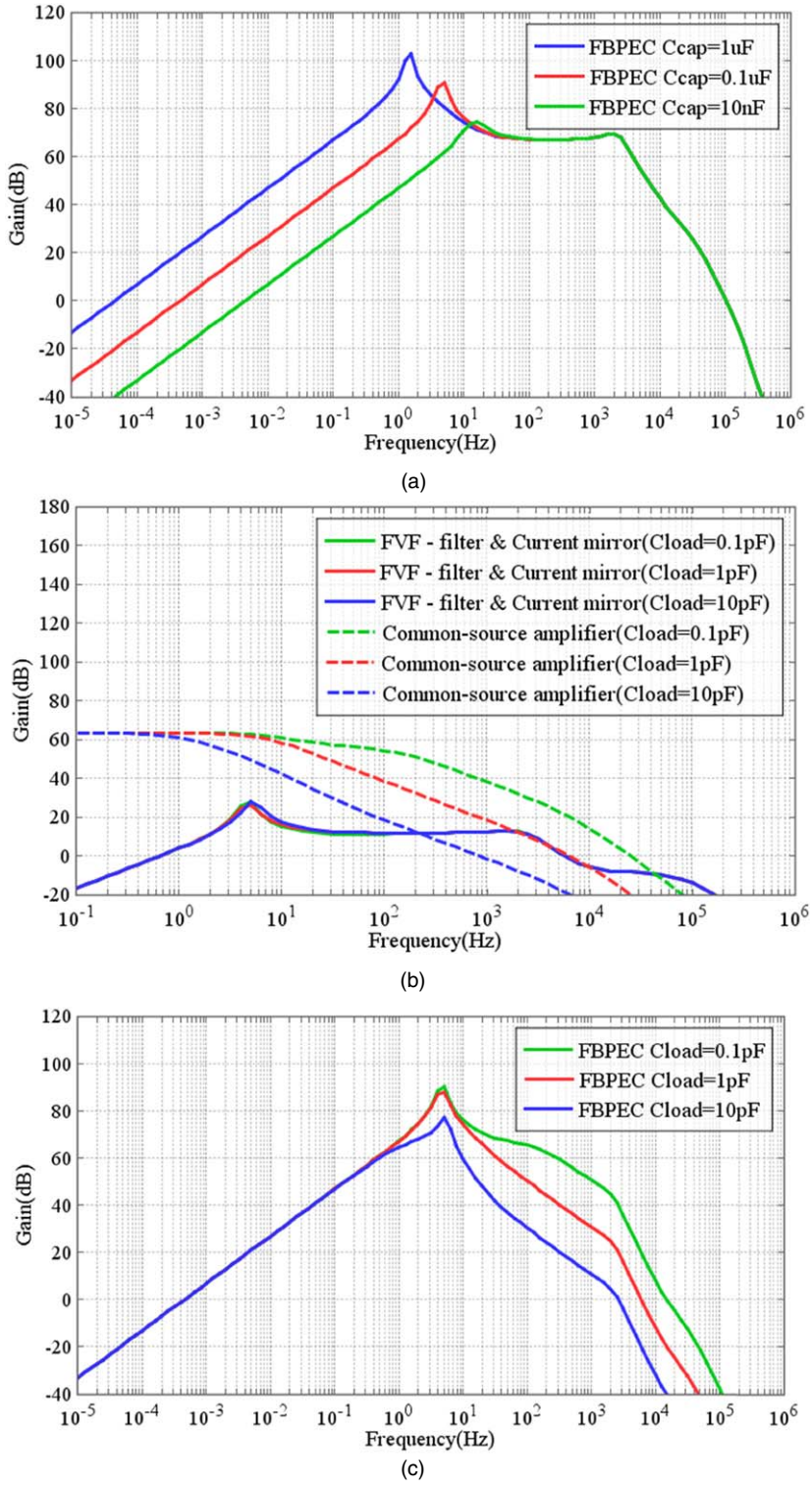

Fig. 4. Frequency response of the FBPEC and each component block at $V_{dd} = 2$ V. (a) Effect of C_{cap} ($C_{load} = 0$ pF). (b) Effect of C_{load} on the FVF-filter and current mirror and common-source amplifier ($C_{cap} = 0.1$ μF). (c) Effect of C_{load} ($C_{cap} = 0.1$ μF).

$$p_E \approx \frac{gm_{MN1}}{C_p} \tag{2}$$

$$p_B \approx \frac{2}{ro_{MN1} C_{load}} \tag{3}$$

Since C_{load} is generally designed to be greater than 100 times C_p, we can observe from Eqs. (1) to (3) that p_B is the dominant pole. In the following, the results of a simulation are used to validate the effects of C_{cap} and C_{load} on the FBPEC. The results of the SPICE simulation for the frequency response of the FBPEC and each component block are presented in Fig. 4. The FBPEC is designed based on a 0.18 μm CMOS process. The simulation condition is $V_{dd} = 2$ V and I_Q of the FBPEC is 100 nA. The simulation results of the frequency response with node A as input and node B as output, shown in Fig. 2, are shown in Fig. 4(a), indicating that the FBPEC can be optimized as an auxiliary amplifier by adjusting the frequency range of the gain of the FBPEC based on the C_{cap} setting. The frequency response characteristics owing to the C_{cap} sweep are based on the FVF filter and has been analyzed in a previous

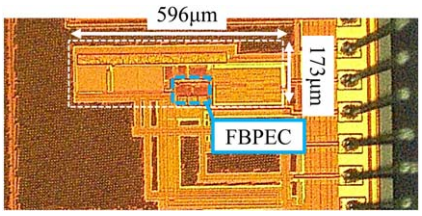

Fig. 5. Chip microphotograph of LDO.

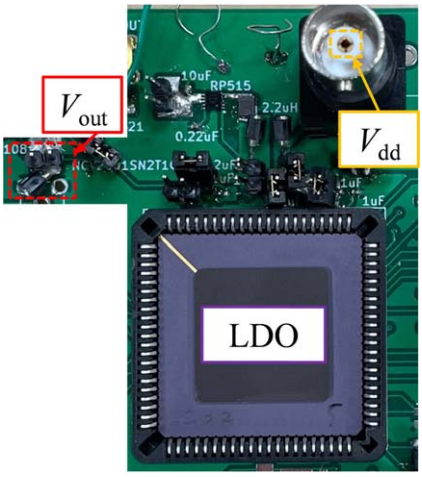

Fig. 6. A part of the PCB used for the measurement.

study.[35] Based on the results, the characteristics of the FBPEC are similar to those of the FVF filter and can function as a bandpass filter and amplifier. Figure 4(b) illustrates the frequency characteristics of the FVF filter and current mirror and the common-source amplifier stage when C_{load} sweeps, and the AC signal input/output definitions are identical to those shown in Fig. 4(a). The bandwidth of the common-source amplifier is reduced owing to the effect of C_{load}, as shown in Eq. (3). The FVF filter and current mirror are not influenced by C_{load} because they are the prior stage circuits of the common-source amplifier. As the frequency response of the FBPEC is the product of the FVF filter and current mirror and the common-source amplifier, the unity gain frequency is determined by the value of C_{load}. In fact, it is evident from the results of the small-signal analysis. The frequency response of the FBPEC when C_{load} sweeps is shown in Fig. 4(c). The dominant pole depends on the value of C_{load} according to the the characteristics of the common-source amplifier shown in Fig. 4(b), the unity gain frequency of the FBPEC with a C_{load} of 10 pF is approximately 3 kHz, and the dominant pole frequency is 5 Hz. The frequency response of the FBPEC shown in Fig. 4 is characterized by its ability to increase the gain at specific frequencies compared to general operating amplifiers. The PSRR characteristics of the proposed circuit shown in Fig. 1 are determined by the sum of the frequency response characteristics of the conventional LDO and the frequency response characteristics of the FBPEC, which improves the PSRR in a specific bandwidth compared to the conventional circuit.

4. Measurement results of the proposed LDO

The proposed LDO, shown in Fig. 1, was designed using a 0.18 μm CMOS process. The maximum I_{load} of the LDO was designed to be 100 mA. The chip microphotograph is displayed in Fig. 5, where the active area is 0.103 mm^2. The PCB used for the measurement is shown in Fig. 6. The PCB is a general two-layer board. An 84-PLCC package was used as the chip. The measured no-load I_Q of the proposed LDO is 648 nA. The measurement parameters and used components are listed in Table I.

Table I. Measurement parameters and used components.

Parameters and components	Value and model
V_{dd}	2 V
I_{load} (resistive load)	1 mA
R_d	5 kΩ
C0603C103K2RACTU	10 nF (for C_{out})
0603BB104K500NGT	0.1 μF (for C_{cap})
Oscilloscope with frequency response analysis function	MSO44
Line injector	J2120A

Figure 7 shows the measured start-up waveforms of the LDO by the EN signal and the start-up signal. Setting the startup signal to "H" increases the current consumption of the LDO during startup and setting it to "L" shifts the LDO to normal operation. The details of the role of the startup signal are described below. As indicated in the waveform in Fig. 7, the output voltage of the LDO is 0.938 V. The EN signal controls the ON and OFF of the LDO. The startup signal is used to activate the bias cell of the LDO. In Fig. 7, the EN signal is set to "high" after V_{DD} is applied, preventing the occurrence of a high-impedance node during startup. Subsequently, by setting the startup signal to "low," the start-up state of the internal bias cell is terminated and the LDO transitions to its normal state. The bias cell of the LDO is depicted in Fig. 8. The cell generates the bias voltages V_{biasp} and V_{biasn}. These bias voltages are used as current

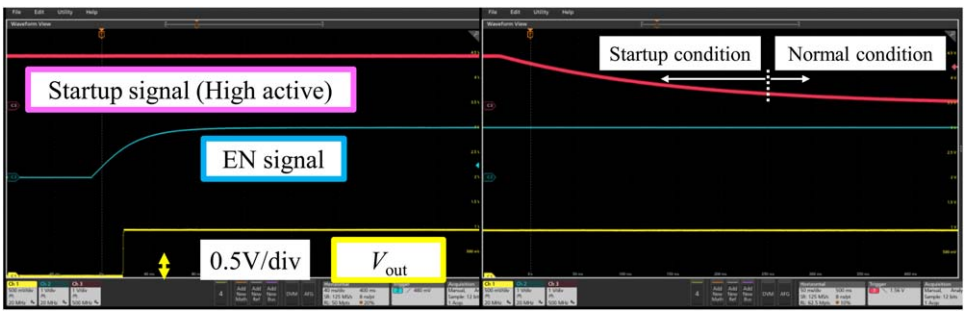

Fig. 7. Start-up waveform of the proposed LDO.

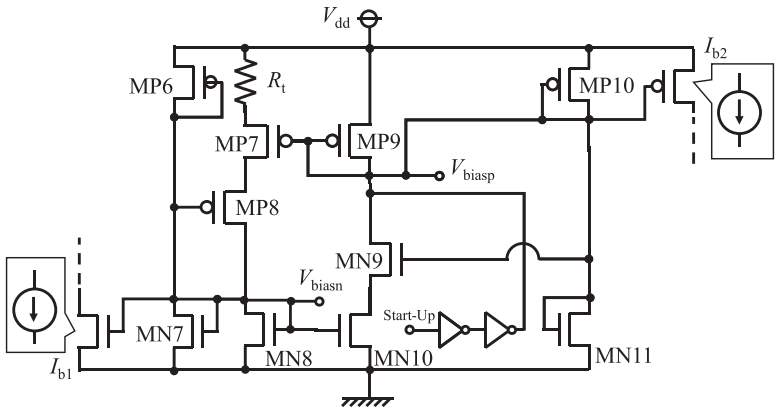

Fig. 8. Bias cell of the proposed LDO.

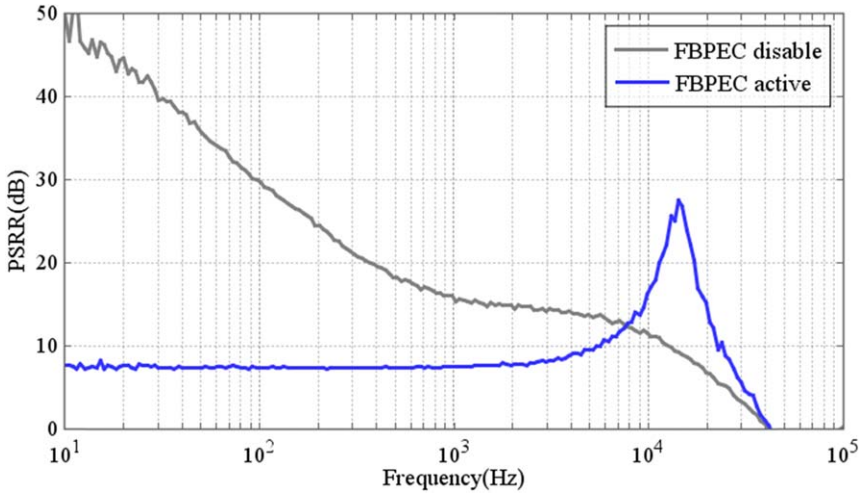

Fig. 9. PSRR of the proposed LDO.

mirrors. For instance, as illustrated in Fig. 8, V_{biasn} and NMOS realize I_{b1} shown in Fig. 1, and V_{biasp} and PMOS realize I_{b2} in Fig. 1. The bias voltages V_{biasn} and V_{biasp} are determined by MN8, MN10, MP7, MP9, and R_t. The resistor R_t is used to improve the temperature characteristics. MN9 and MP8 are used as a cascode transistors; MN7, MN11, MP6, and MP10 generate the bias for the cascode transistors based on V_{biasn} and V_{biasp}. The bias circuit requires a startup circuit for proper operation.[36] In this study, the startup circuit was configured with inverters and an externally applied startup signal. The V_{biasp} node is pulled down by the startup signal and the inverter, thereby increasing the reference current. In the startup condition, the device is activated by increasing the current in the bias cell. Following its activation, the device operates as a low-consumption LDO in the normal condition.

Figure 9 shows the measurement results of PSRR. Figure 9 shows that the HF PSRR characteristic increases when the FBPEC is changed from disabled to active state in the proposed circuit. It can also be observed that the proposed circuit with the FBPEC in active condition improves the PSRR at frequencies above 8 kHz owing to the effect of the FBPEC compared to the general circuit configuration. During EEG sensing of wearable devices, the SMPS is controlled in the pulse frequency modulation (PFM) mode owing to the light load. The control scheme reduces the switching frequency at light loads, and in this study, the proposed LDO is most effective when the switching frequency is assumed to be 15 kHz, which is a reasonable frequency for an SMPS that is regulated by pulse frequency modulation control. The proposed LDO has a PSRR of 27.5 dB at 15 kHz, which is approximately 18 dB higher than that of the general configuration. At frequencies below 8 kHz, the PSRR of the proposed LDO is lower than that of the general configuration; however, it is not a problem because the characteristic below the lowest switching frequency is meaningless. Moreover, there is no problem in the DC characteristics because it is regulated in the loop of the differential amplifier. In PSRR measurements, since low-frequency characteristics could not be shown owing to limitations of the measurement equipment, an alternative measurement is employed via line regulation. Figure 10 presents the line regulation measurement results. In all condition, line regulation is within 1% and is well regulated by the differential amplifier of the conventional circuit. The frequency of the EEG signal is mainly distributed below 100 Hz, which is far from 15 kHz, the frequency of the power supply ripple. However, the analog-to-digital converter (ADC) must operate in a time-division manner to handle multiple channels, so the operating frequency must be 200 Hz multiplied by the number of channels or higher.[5] It is known that power supply fluctuations, even if it is a power supply ripple at a

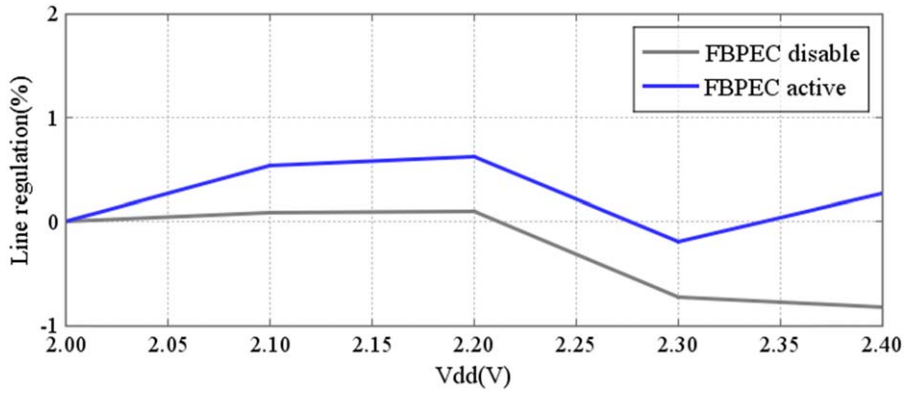

Fig. 10. Line regulation of the proposed LDO.

Table II. Performance comparison of the proposed LDO with past works.

	[28]	[38]	[39]	This work
Process	14 nm	180 nm	250 nm	180 nm
Active area (mm^2)	0.01	0.039	0.108	0.103
V_{ddMAX}(V)	1.2	1.8	3.3	3.3
Load Capacitor (μF)	$C_{out} = 0.004$	$C_{out} = 0.47$	$C_{out} = 1$	$C_{out} = 0.01$ + $C_{cap} = 0.1$
I_Q (nA)	27300	900	1240	648
$I_{loadMAX}$ (mA)	15	50	150	100
PSRR @15 kHz (voltage ratio)	126 @ $I_{load} = 1.5$ mA	178 @ $I_{load} = 50$ mA	17.8 @ $I_{load} = 150$ mA	23.7 @ $I_{load} = 1$ mA
F.O.M. (PSRR @15 kHz/I_Q @no-load)	0.005	0.198	0.014	0.037

frequency far from the measurement signal, affect the characteristics of the ADC, such as reducing the dynamic range of the ADC.[37] In other words, the power supply fluctuation at 15 kHz affects the characteristics of the ADC so that it contributes to the improvement of the system performance.

If the device performs wireless communication, then the load current of the LDO and the SMPS connected in series with the LDO increases, and the switching frequency of the SMPS becomes even higher by PFM control; however, it is allowed to increase the self-consumption current of the LDO in this case. Thus, if the switching frequency of the SMPS increases as the load current increases, it is not a problem either, particularly since the PSRR characteristics can be easily improved by using adaptively bias techniques,[23–25] as described in the Introduction.

This study and previous studies are compared in Table II. The figure-of-merit (FOM) is defined as the PSRR at 15 kHz divided by the I_Q at no-load in a trade-off relationship, with higher values indicating better performance. The good performance of this study is shown in terms of the FOM. The FOM of previous study[38] is also a higher value. The PSRR result in the previous study[38] was measured at $I_{load} = 50$ mA. In previous study,[38] the adaptive bias technique[25–27] has been used, which improves the PSRR at a large I_{load}, and thus appears to be superior as a FOM. It is not equally comparable in terms of improving the PSRR at light loads, which is the target of the proposed technology. Furthermore, $I_{loadMAX}$ of this study can handle load currents up to 100 mA, which is considered advantageous as the current is increased during communication in wearable devices. The proposed circuit using FBPEC does not improve the load transient response. Therefore, it is recommended that the proposed circuit be used in combination with a circuit that improves the load transient response[35] when a fast response is required.

5. Conclusions

This paper proposed an LDO with improved PSRR characteristics for EEG recording wearable devices. We designed an LDO that improves the PSRR at a specific frequency, as shown in the measurement results shown in Fig. 9 in Sect. 4. The proposed LDO was designed and fabricated using a 0.18 μm CMOS process. Compared with the general configuration, the PSRR of the proposed LDO was improved by 18 dB at 15 kHz through measurement results. The measured no-load I_Q was as low as 648 nA, and the FOM confirmed the improved trade-off with PSRR. The results of the study validated that the proposed LDO could be a solution to address the battery size versus operating time trade-off of EEG recording wearable devices.

Acknowledgments

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