PAPER

A High Dynamic Range and Low Power Consumption Audio Delta-Sigma Modulator with Opamp Sharing Technique among Three Integrators*

Daisuke KANEMOTO[†a)], ***Member***, **Toru IDO**[†], ***Nonmember***, ***and*** **Kenji TANIGUCHI**[†], ***Member***

SUMMARY A low power and high performance with third order delta-sigma modulator for audio applications, fabricated in a 0.18 μm CMOS process, is presented. The modulator utilizes a third order noise shaping with only one opamp by using an opamp sharing technique. The opamp sharing among three integrator stages is achieved through the optimal operation timing, which makes use of the load capacitance differences between the three integrator stages. The designed modulator achieves 101.1 dB signal-to-noise ratio (A-weighted) and 101.5 dB dynamic range (A-weighted) with 7.5 mW power consumption from a 3.3 V supply. The die area is 1.27 mm^2. The fabricated delta-sigma modulator achieves the highest figure-of-merit among published high performance low power audio delta-sigma modulators.

key words: *opamp sharing technique, switched capacitor integrator, delta-sigma analog-to-digital converter, audio application*

1. Introduction

The recent growth of portable consumer applications, such as cell phones and portable audio recorders, has increased the demand for low power audio analog-to-digital converters (ADCs). Most of audio ADCs utilize delta-sigma modulators to achieve high performance over 100 dB signal-to-noise ratio (SNR) and dynamic range (DR). There are two kinds of delta-sigma modulator types, continuous-time and discrete-time. Continuous-time delta-sigma modulators using continuous time loop filters such as an active RC filter or a Gm-C filter provide lower power consumption [1]. However, discrete-time delta-sigma modulators using switched capacitor circuits have been widely used in consumer products because switched capacitor integrators offer good coefficient matching and low sensitivity to clock jitter on feedback digital-to-analog converters (DACs). Thus, low power consumption technique for discrete-time delta-sigma modulators is important.

A key component of delta-sigma modulator regarding power consumption is switched capacitor integrators with opamps. High performance delta-sigma modulators require several integrator stages, equal to the modulator order number. The opamps in those integrator stages dissipate a massive amount of total modulator power consumption. Therefore, an opamp number reduction using an opamp sharing technique is an effective technique to reduce power consumption, as reported for a switched capacitor filter and a pipelined ADC [2], [3]. Even for a delta-sigma modulator, a basic concept of the opamp sharing technique among three integrator stages is reported [4]. However a fabricated chip with the opamp sharing technique for delta-sigma modulator is not presented.

This paper, which is based on proceeding of [5], presents a fabricated a high SNR and low power consumption audio delta-sigma modulator with opamp sharing technique. The delta-sigma modulator, designed and fabricated in a 0.18 μm CMOS process, achieves high SNR 101.1 dB and DR 101.5 dB with very low power 7.5 mW.

The organization of the paper is as follows: Sect. 2 provides the architecture of the designed the low power high dynamic range modulator. Section 3 will show the details of the circuit level implementation. In Sect. 4, measurement results will be reported. Finally, Sect. 5 concludes this paper.

2. Modulator Architecture

Figure 1 shows a topology of the designed delta-sigma modulator composed of a third order loop filter, a 1.5 bit quantizer and a dynamic element matching (DEM). The loop filter of the modulator utilizes an opamp sharing technique among three stage integrators to reduce power dissipation. The three stages opamp sharing is achieved by effective use of characteristic differences between the three stages. The first stage must have large capacitances to satisfy the SNR requirement. Therefore, the opamp for the first stage becomes a power consuming design to drive large capacitances with sufficient speed. The noise requirement on the second stage is far smaller than the first stage because of noise scaling, thus required capacitances on the second stage are smaller than the first stage. If the same opamp as the first stage drives the second stage capacitances, operation speed becomes faster than the first stage. The third stage also has smaller capacitances than the second stage. This means operation speed of the third stage is faster than the first and the

Manuscript received February 8, 2012.
Manuscript revised April 25, 2012.

[†]The authors are with Division of Electrical, Electronic and Information Engineering, Osaka University, Suita-shi, 565-0871 Japan.

*This paper is based on "A 7.5 mW 101 dB SNR Low-Power High-Performance Audio Delta-Sigma Modulator Utilizing Opamp Sharing Technique," by D. Kanemoto, T. Ido, and K. Taniguchi which appeared in Proceedings of International SoC Design Conference (ISOCC), November 2011. ©2011 IEEE.

a) E-mail: kanemoto@ed.kyushu-u.ac.jp

DOI: 10.1587/transele.E95.C.1427

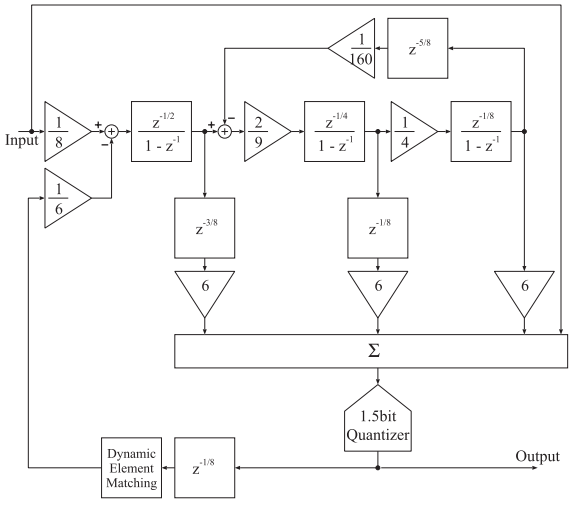


Fig. 1 Delta-sigma modulator topology.

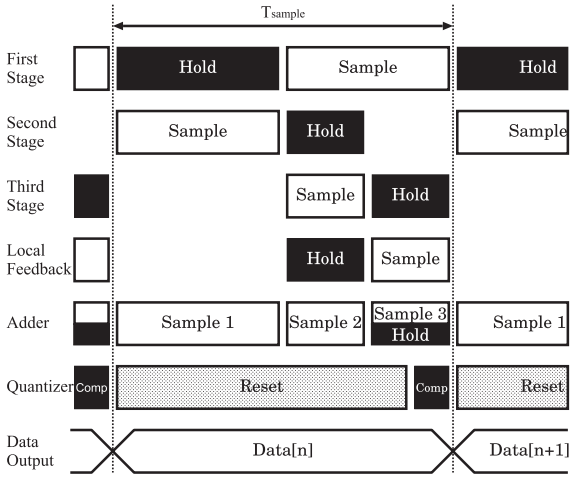


Fig. 2 Operating timing chart.

second stage. These differences of operation speed enable the opamp sharing among the three stage integrators.

The designed operation timing chart of the fabricated modulator is shown in Fig. 2. In the timing chart, each hold mode period of the second and the third stage is half of the first stage. This short hold mode period is achieved by the differences of the stage characteristics. Therefore, the hold modes of the three integrator stages without an overlapped period in a T_{sample} clock cycle can share an opamp.

The modulator also has the local feedback path from the third stage output to the second stage input. This local feedback performs sampling when the third stage is in the hold mode and holding when the second stage is in the hold mode. The adder block in Fig. 1, summing the three integrator stages output, samples the first stage output at the first half period of a clock cycle. At the latter half period, the adder block samples the second stage output, after that simultaneously samples the third stage output and holds summing output at the last quarter of the clock cycle. The quantizer operates at the last timing of the adder block hold mode, and the results control the feedback DAC of the modulator through the DEM. The loop filter has the direct feedforward path from the input of the modulator to the quantizer input, which results in suppression of the input signal component in the loop filter [6]. The power dissipation of the delta-sigma modulator utilizing this opamp sharing technique is much lower than conventional third order delta-sigma modulators because the modulator utilizes only one opamp.

3. Circuit Implementation

3.1 Third Order Loop Filter and Opamp

The third order loop filter circuit schematic of the delta-sigma modulator with the three-stage opamp sharing is depicted in Fig. 3. It is noted that the schematic is a single-ended equivalent form of the actual designed differential circuit. The loop filter circuit utilizes only one opamp to implement the three stage integrators, composed of the sampling capacitor C_{s1} and the holding capacitor C_{h1} for the first stage, C_{s2} and C_{h2} for the second stage, and C_{s3} and C_{h3} for the third stage. The capacitors C_{D1} and C_{D2} are for the feedback DAC. The reference voltage V_{ref} is sampled by C_{D1} and C_{D2}. And those capacitors are connected to the opamp through 1 or -1 coefficient, based on the feedback digital signal from the DEM. In the designed circuit using the differential configuration, 1 or -1 coefficient is implemented by straight or cross connection from the differential capacitor to the opamp input. Capacitors C_{zx} (x= 1, 2 and 3) compose the sampling capacitors for the local feedback loop, which are required to be relatively small capacitances. -1 coefficient at the front of the local feedback circuit is also implemented by cross connection of the differential circuit. All switches are controlled by 4 phases clock, P1, P2, P3 and P4 in Fig. 4. The modulator sampling clock frequency is 6.144 MHz, thus the required supply clock frequency to the fabricated chip is 12.288 MHz to produce clock P3, P4 and P5. The clock phases P1 and P2 correspond to the holding and the sampling mode of the first stage integrator. The clock phases P2 and P3 are for the sampling and the holding of the second stage integrator, and P3 and P4 are for the third stage. The clock phase P5 in Fig. 4 controls the timing of the 1.5 bit quantizer operation.

Figure 5 shows the implemented opamp for the delta-sigma modulator. The opamp is composed of the one-stage conventional cascode structure. A simple one-stage opamp is suitable for the opamp sharing technique in order to achieve stability. Because stability of an one-stage opamp does not depend on a load capacitance, otherwise settling speed is changed. On the other hand, a multi-stage opamp suffers from load capacitance differences among three integrator stages. Because stability of a multi-pole system is usually decided by the relationship between a compensation capacitance and a load capacitance [7], and a load capacitance of each integrator stage is changed in an opamp sharing technique.

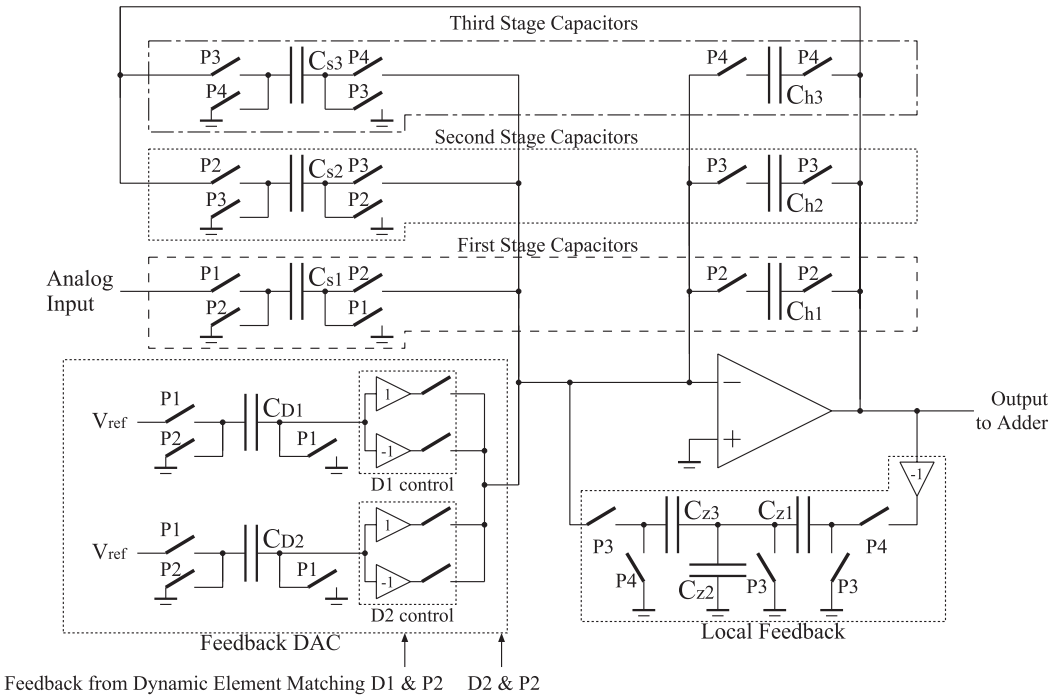


Fig. 3 Schematic of the loop filter.

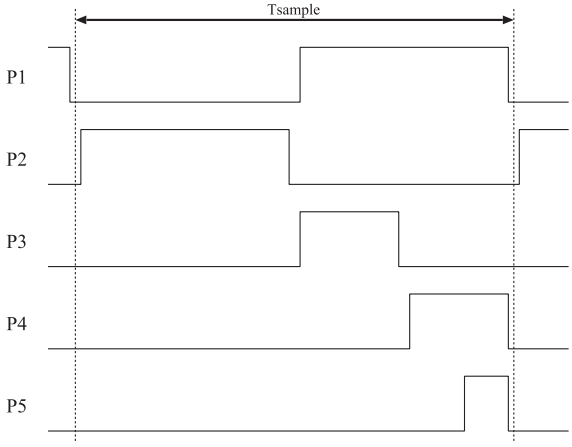


Fig. 4 Clock phases for modulator operation.

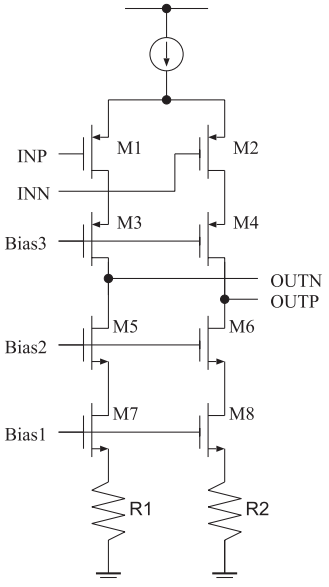


Fig. 5 Cascode structure opamp.

To achieve high dynamic range, the opamp's noise has to be suppressed enough. In this design, resistors, R1 and R2, are implemented in order to reduce an effect of flicker noise coming from NMOS transistors, M7 and M8, of which the size are smaller than the size of input PMOS transistors M1 and M2. The mean-square value of M7(M8)'s flicker noise current, $\overline{i_{fn}}$, is

$$\overline{i_{fn}} = \frac{g_{mn}}{g_{mn}R + 1}\overline{v_{fn}} \tag{1}$$

$$\approx \frac{1}{R}\overline{v_{fn}} \qquad \left(R \gg \frac{1}{g_{mn}}\right) \tag{2}$$

where $\overline{v_{fn}}$ is mean-square value of M7(M8)'s flicker noise voltage, g_{mn} and R show transcondactance of M7(M8) and resistance value of R1(R2), respectively. Therefore, Eq. (2), flicker noise current can be decreased if large resistor value is selected. We know chopper stabilization technique [8] is also used in order to reduce flicker noise effect. However, a chopping technique does not suitable for the opamp sharing technique. Because the timing of chopping operation becomes complicated, the modulator has twice control phases compared to conventional delta-sigma modulators, and large number of switches makes large parasitic capacitances of opamp.

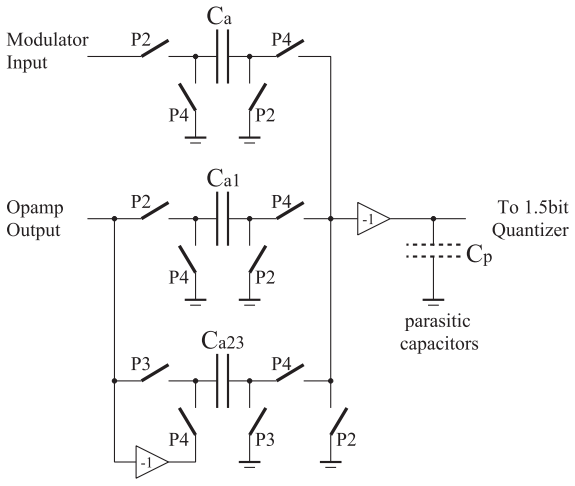


Fig. 6 Adder circuit schematic.

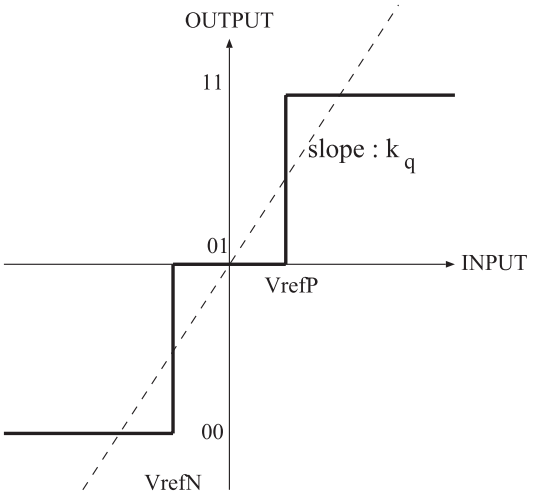


Fig. 7 Equivalent gain of 1.5 bit Quantizer.

3.2 Adder Block

Figure 6 shows the adder realized by switched capacitor circuits without any opamps, suitable for low power modulator implementation. The adder samples the holding output of the first stage at the clock phase P2, through the capacitor C_{a1}, and the second stage at the clock phase P3 through C_{a23}. At the clock phase P4, sampling of the third stage output and summation of all stages output are performed simultaneously. The holding output of the adder circuit is stored by the parasitic capacitor C_p of 1.5 bit quantizer input and connecting wire. The gains from the modulator input, 1st, 2nd or 3rd output integrator stages to the 1.5 bit quantizer, G_{input}, G_{1st}, $G_{2nd,3rd}$, are given by

$$G_{input} = \frac{C_a}{C_a + C_{a1} + C_{a23} + C_p} \tag{3}$$

$$G_{1st} = \frac{C_{a1}}{C_a + C_{a1} + C_{a23} + C_p} \tag{4}$$

$$G_{2nd,3rd} = \frac{C_{a23}}{C_a + C_{a1} + C_{a23} + C_p}. \tag{5}$$

It is noticed that careful estimation of the total parasitic capacitance is required to design the adder circuit. Here, from Eqs. (3), (4), and (5), G_{input} G_{1st} and $G_{2nd,3rd}$ cannot be larger than 1.Thus, by using a multi-level quantizer equivalent gain coming from the slope of input-output transfer function, the gain of the each path is prepared to meet Fig. 1 block diagram.

3.3 1.5 bit Quantizer

1.5 bit quantizer, which consists of two 1 bit quantizers, is utilized in the modulator. Figure 7 shows input-output characteristic of 1.5 bit quantizer. The slope, k_q, means equivalent gain and designers can arbitrarily assign the equivalent gain for suitable value by designing the threshold voltages, V_{refN} and V_{refP}. Figure 8 shows gain blocks of adder

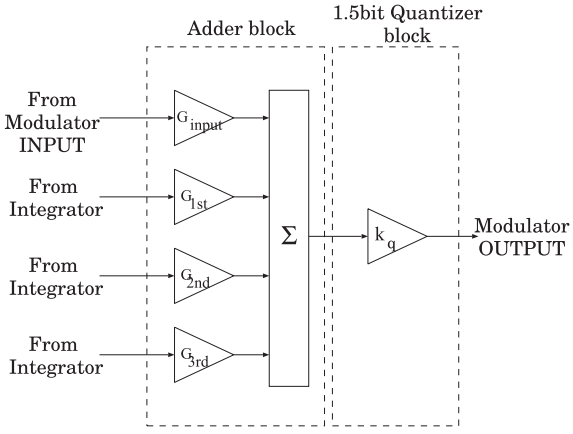


Fig. 8 Block diagram of adder and 1.5 bit quantizer.

circuit and 1.5 bit quantizer. The total gain of the each path is described by using G_{input}, G_{1st}, G_{2nd}, G_{3rd} and k_q. In this modulator design, the values of capacitances are C_a=100 [fF],C_{a1}=600 [fF],C_{a23}=600 [fF] and $C_p \approx$ 100 [fF]. Therefore, from $G_{input} = \frac{1}{14}$, $G_{1st} = G_{2nd} = G_{3rd} = \frac{6}{14}$, the reference voltages, V_{refP} and V_{refN}, are designed in order to realize $k_q = 14$.

3.4 Other Building Blocks

Figure 9 shows 1.5 bit quantizer and the DEM block. The outputs from those two comparators are processed by DEM block and connected to polarity switches in the feedback DAC circuit of the loop filter, Fig. 3. A data weighted averaging [9], which aims to make the long-term average of each DAC element $D1$ and $D2$ in mid-code output, is used for the algorithm of the DEM.

4. Measurement Results

A prototype chip was fabricated using 3.3 V I/O devices in a

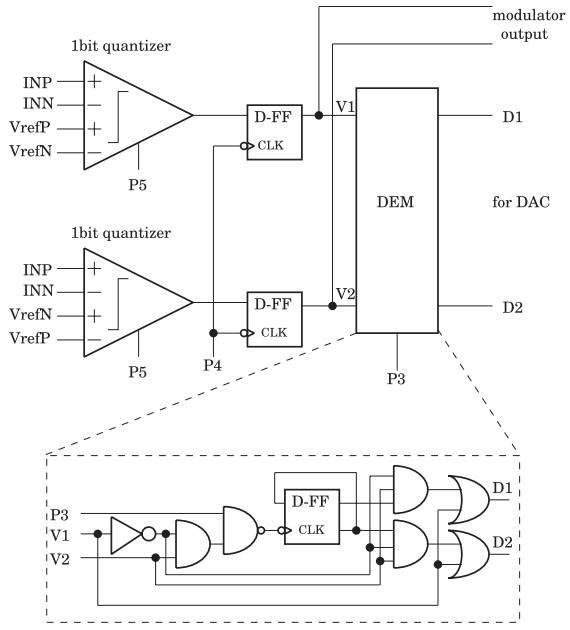


Fig. 9 1.5 bit quantizer and DEM.

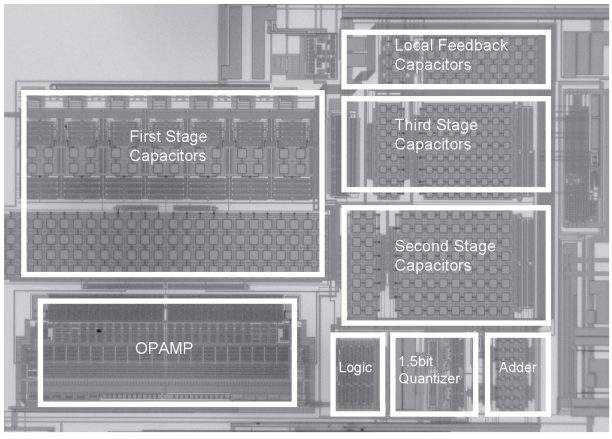


Fig. 10 Microphotograph of the prototype chip.

0.18 μm single poly silicon and six-layers metal CMOS process. Figure 10 shows a micrograph of the prototype chip. The prototype chip has the one opamp surrounded by the capacitors for the three stage integrators. The total area of the modulator is 1.27 mm^2. The chip has rail-to-rail 6.6 V peak-to-peak input capability with differential configuration. Figure 11 shows the measured THD+N as a function of the input signal amplitude by 1 kHz input sine wave. THD+N at 0 dBFS input signal is −85 dB. A slight distortion component is observed over −20 dB input amplitude, however characteristic of THD+N has linearity at small signal range under −20 dBFS. The performance is sufficient for audio applications. The A-weighted SNR and DR are 101.1 dB and 101.5 dB respectively. Figure 12(a) shows the output spectrum obtained with the sinusoidal input of −60 dBFS. No harmonic component is observed. Output spectrum with full scale input is shown in Fig. 12(b). A dominant harmonic of

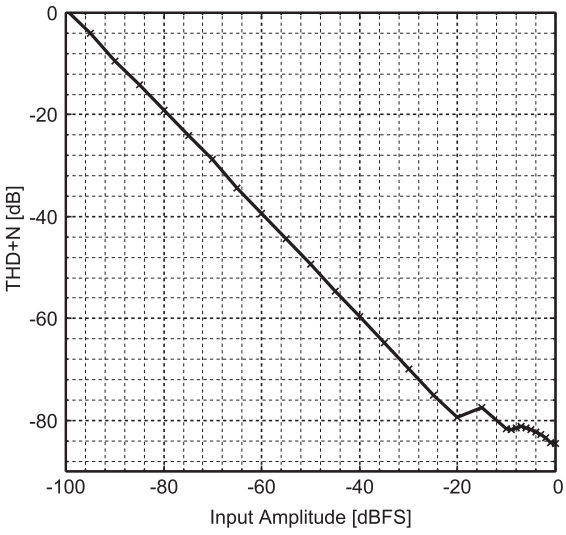
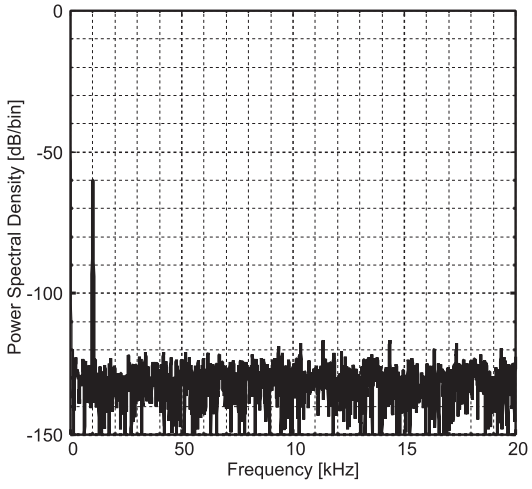
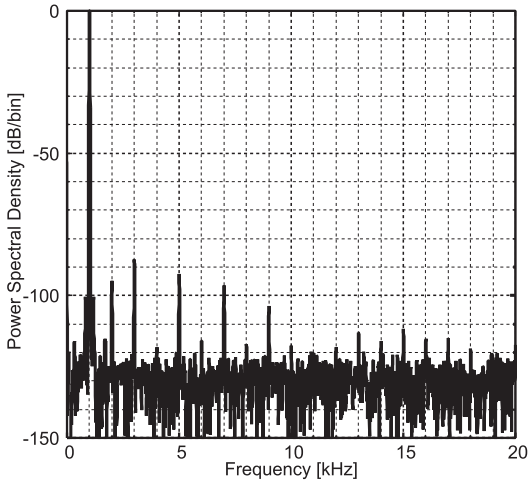


Fig. 11 THD+N vs. 1 kHz input signal amplitude.



(a)



(b)

Fig. 12 Output spectrum with (a) −60 dBFS@1 kHz and (b) 0 dBFS@1 kHz.

Table 1 Measurement comparison.

Parameter	This work	[1]	[10]	[11]	[12]
Technology	0.18 μm	65 nm	0.35 μm	0.18 μm	0.13 μm
VDD	3.3 [V]	3.3 [V]	N/A	3.3 [V]	3.3 [V]
bandwidth	20-20 [kHz]	20-20 [kHz]	20 [kHz]	20 [kHz]	20 [kHz]
Sampling frequency	6.144 [MHz]	12.288 [MHz]	N/A	6.144 [MHz]	6.144 [MHz]
DR (A-Weighted)	101.5 [dB]	101 [dB]	106 [dB]	102 [dB]	105.5 [dB]
SNR (A-Weighted)	101.1 [dB]	101 [dB]	106 [dB]	102 [dB]	101.9 [dB]
THD+N(dB)	−85	−94	−97	N/A	N/A
Power dissipation	7.5 [mW]	15 [mW]	18 [mW]	37.3 [mW]	9.9 [mW]
FOM	0.49 [conv/pJ]	0.24 [conv/pJ]	0.36 [conv/pJ]	0.11 [conv/pJ]	0.41 [conv/pJ]

the output is the third order distortion. The power consumption of the chip is 7.5 mW. Table 1 summarizes the performance of the implemented low power delta-sigma modulator and other published over 100 dB SNR and DR audio delta-sigma modulators [1], [10]–[12]. In this paper, FOM equation, which is based on SNR and power dissipation [13],

$$FoM = \frac{2^{SNRbit} \times f_{sample}}{Power} \quad (6)$$

is used and this prototype chip achieves the highest FOM among the published audio delta-sigma modulators.

5. Conclusion

A high performance low power audio delta-sigma modulator with opamp sharing among three integrator stages is presented. The delta-sigma modulator utilizes only one opamp to implement a third order loop filter by an opamp sharing technique. The opamp sharing makes use of an optimal operation timing, based on load capacitance differences between the three stages coming from noise scaling of the integrator stages. Therefore, power consuming analog blocks are only one opamp and two comparators for a 1.5 bit quantizer. A designed prototype chip on a 0.18 μm CMOS process achieves high performance 101.1 dB SNR and 101.5 dB DR with very low power 7.5 mW.

Acknowledgments

This research was partly supported by a grant from the Global COE Program, "Center for Electronic Devices Innovation," from the Ministry of Education, culture, sports, science and Technology of Japan.

This research has been carried out at the Frontier Research Base for Global Young Researchers, Osaka University, on the Program of Promotion of Environmental Improvement to Enhance Young Researchers' Independence, the Special Coordination Funds for Promoting Science and Technology, Japan Ministry of Education, Culture, Sports, Science and Technology.

References

[1] M.-Y. Choi, S.-N. Lee, S.-B. You, W.-S. Yeum, H.-J. Park, J.-W. Kim, and H.-S. Lee, "A 101-dB SNR hybrid delta-sigma audio ADC using post integration time control," IEEE Custom Integrated Circuits Conf. (CICC), pp.89–92, Sept. 2008.

[2] P.W. Bosshart, "A multiplexed switched-capacitor filter bank," IEEE J. Solid-State Circuits, vol.SC-15, no.6, pp.939–945, Dec. 1980.

[3] P.C. Yu and H.S. Lee, "A 2.5-V, 12-b, 5-Msample/s pipelined CMOS ADC," IEEE J. Solid-State Circuits, vol.31, no.12, pp.1854–1861, Dec. 1996.

[4] D. Kanemoto, T. Ido, and K. Taniguchi, "A novel third order delta sigma modulator with one opamp shared among three integrator stages," IEICE Electron. Express, vol.5, no.24, pp.1088–1092, 2008.

[5] D. Kanemoto, T. Ido, and K. Taniguchi, "A 7.5 mW 101 dB SNR low-power high-performance audio delta-sigma modulator utilizing opamp sharing technique," Proc. IEEE International SoC Design Conference (ISOCC), pp.66–69, Nov. 2011.

[6] J. Silva, U. Moon, J. Steensgaard, and C.G. Temes, "Wideband low-distortion Δ Σ ADC topology," Electron. Lett., pp.737–738, June 2001.

[7] P.E. Allen and D.R. Holberg, CMOS Analog Circuit Design. Oxford University Press, 2002.

[8] H. Chen, P. Chen, and J. Chiang, "A low-offset low-noise sigma-delta modulator with pseudorandom chopper-stabilization technique," IEEE Trans. Circuit Syst. I, vol.56, no.12, pp.2533–2543, Dec. 2009.

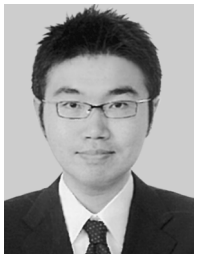
[9] R. Schreier and C.G. Temes, Understanding Delta-Sigma Data Converters, John Wiley & Sons, 2005.

[10] K. Nguyen, B. Adams, K. Sweetland, H. Chen, and K. McLaughlin, "A 106 dB SNR hybrid oversampling ADC for digital audio," ISSCC Dig. Tech. Papers, pp.176–177, Feb. 2005.

[11] P. Morrow, M. Chamarro, C. Lyden, P. Ventura, A. Abo, A. Matamura, M. Keane, R. O'Brien, P. Minogue, J. Mansson, N. McGuinness, M. McGranaghan, and I. Ryan, "A 0.18 μm 102 dB-SNR mixed CT SC audio-band ΔΣ ADC," ISSCC Dig. Tech. Papers, pp.178–179, Feb. 2005.

[12] Y.-G. Kim, M.-H. Cho, K.-D. Kim, J.-K. Kwon, and J. Kim, "A 105.5 dB, 0.49 mm^2 audio ΔΣ modulator using chopper stabilization and fully randomized DWA," IEEE Custom Integrated Circuits Conf. (CICC), pp.503–506, Sept. 2008.

[13] R.H. Walden, "Analog-to-digital converter survey and analysis," IEEE J. Sel. Areas Commun., vol.17, no.4, pp.539–550, April 1999.



Daisuke Kanemoto received the B.S. degree in Electronic Engineering from Kyoto Institute of Technology, Kyoto, Japan, in 2004 and received the M.S. degree in Electronic Engineering from Osaka University, Osaka, Japan, in 2006. Since November 2010, he has been an assistant professor with Department of Electronics, Graduate School of Information Science and Electrical Engineering, Kyushu University, Fukuoka, Japan. His research interests include analog and mixed-signal integrated circuits. He is a member of the IEEE.

Toru Ido received the B.S., M.S. and Ph.D. degrees from Osaka University, Osaka, Japan, in 1998, 2000, and 2003, respectively. From 2003 to 2007 he was with Texas Instruments Japan, Atsugi, Japan, where he designed data converters for audio applications. Since 2007, he has been an Associate Professor of Electrical, Electronic and Information Engineering and Frontier Research Base for Global Young Researchers at Osaka University, researching high performance data converters, low power analog circuits and mixed-signal processing.

Kenji Taniguchi received the B.S., M.S. and Ph.D. degrees from Osaka University, Osaka, Japan, in 1971, 1973 and 1986, respectively. From 1973 to 1986, he worked for Toshiba Research and Development Center, Kawasaki, Japan where he was engaged in process modeling and the design of MOS LSI fabrication technology. He was a Visiting Scientist at Massachusetts Institute of Technology, Cambridge, from July 1982 to November 1983. Presently, he is a Professor of Electrical, Electronic and Information Engineering at Osaka University. His current research interests are analog circuits, radio frequency circuits, device physics and process technology. Prof. Taniguchi is a member of the Japan Society of Applied Physics. He is a fellow of the IEEE.