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A novel third order Delta Sigma Modulator with one opamp shared among three integrator stages

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Abstract: A novel third order delta sigma modulator (DSM) is presented. The third order loop filter in the proposed DSM shares one opamp among three integrator stages through an optimal operation timing, which makes use of load capacitance differences between integrator stages. The power dissipation of the proposed DSM is much lower than conventional third order DSM because power consuming blocks in the DSM are only one opamp and a comparator. The proposed DSM, designed on 0.35 μm CMOS process under 3.3 V supply achieves 1 mW power dissipation with 100-11 kHz band width and 96 dB SQNR.

Keywords: amplifier sharing technique, delta sigma modulator, low power consumption

Classification: Integrated circuits

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1 Introduction

A switched-capacitor (SC) integrator has a sampling phase and an integration phase. The amplifier in a SC integrator is actually used during only integration phase, which is half of a clock cycle. A way to keep SC integrators busy during both phases of the clock period is the amplifier sharing technique. In SC filter applications or pipelined ADCs, amplifier sharing techniques are widely used and many integrated circuits are presented [1, 2]. This basic amplifier sharing technique is also applied to delta sigma modulators (DSMs) [3, 4] and the conventional amplifier sharing technique achieves a second order DSM with an opamp.

In this paper, a novel third order DSM with one opamp in the loop filter is presented. The proposed DSM shares an opamp among three integrator stages to achieve third order DSM.

In section II, the proposed third order DSM is discussed. In section III, the Hspice simulation result is shown. Finally, Section IV concludes this paper.

2 Proposed Amplifier Sharing Technique

Fig. 1 (a) illustrates the block diagram of the proposed DSM. The DSM has third order loop filter with shorter loop delay than conventional third order configuration. This is because of the optimal operation timing of the proposed sharing technique. Fig. 1 (b) depicts the single-ended circuit schematic of the DSM while actual circuit is designed in differential form. The circuit is composed of a 1 bit quantizer, a DAC, an analog adder and an opamp with three sets of capacitors corresponding to three stages of a third order integrator. The capacitors, C_{s1} and C_{i1} are a sampling capacitor and an integration capacitor respectively, composing the first stage integrator. C_{s2} and C_{i2} compose the second stage integrator. C_{s3} and C_{i3} are for the third stage. The output of the opamp is connected to the analog adder composed of three capacitors C_{a0}, C_{a1} and C_{a23}. The adder samples the output of the first stage integrator with the capacitor C_{a1}. The outputs of the second and the third integrators are sampled by the capacitor C_{a23}. The capacitor C_{a0} is for the input signal feed forward, which is effective technique to reduce opamp's output signal requirements [5]. All capacitors are connected through switches operating optimal timing, shown in Fig. 1 (c), to achieve a third order integrator and an analog adder with shared only one opamp. The optimal operation timing of switches are controlled by five phases of the clock signal, P1–P5. In the clock phases, P1–P4 have its delayed clock signals, P1d–P4d, drawn by dashed line in Fig. 1 (c). The first stage integrator, composed of C_{s1} and C_{i1}, performs sampling at the clock P1 and integration at the clock P2. The second stage integrator, as C_{s2} and C_{i2}, operates sampling and integration at clock P2 and P3 respectively. It is noted that active period of the clock P3 is a half of P1 and P2. This means available time for the second stage integration settling becomes a half of the first stage operation. This operation timing is achieved by capacitance differences be-

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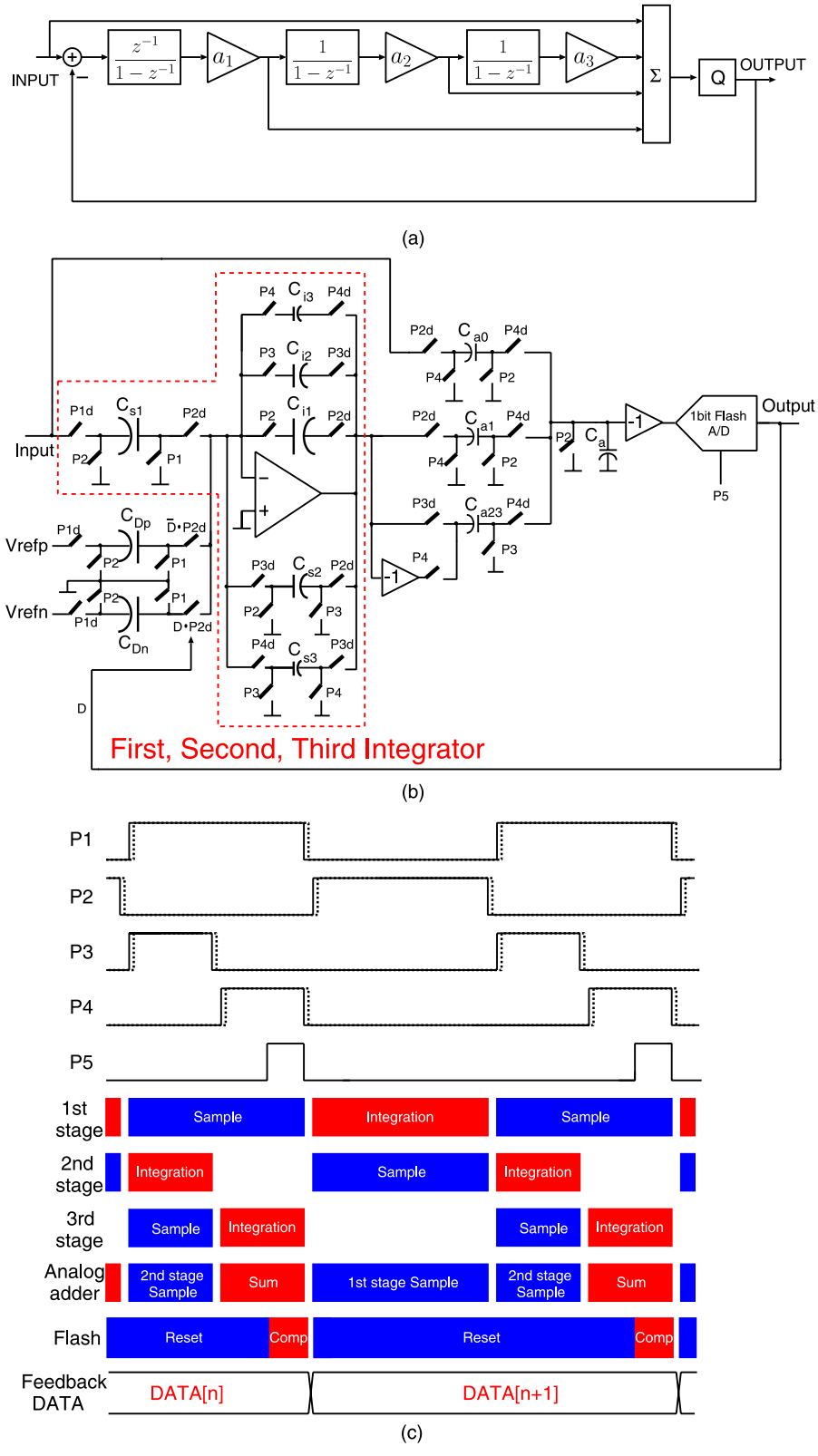

Fig. 1. (a) Block diagram, (b) circuit schematic and (c) timing diagram of the proposed DSM.

tween integration stages. Generally capacitances are determined by kT/C noise scaling provided from previous stage gains, thus capacitances of the first stage become largest and capacitances of the third stage are smallest. In the proposed opamp sharing technique, the opamp must be designed to

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have sufficient high speed settling even with largest capacitances of the first stage. Therefore the second stage, which have smaller capacitances C_{s2} and C_{i2} by kT/C noise scaling, is able to achieve sufficient settling even with a half period clock. The third stage, as C_{s3} and C_{i3}, operates clock P3 and P4 with sufficient output signal settling speed, while the available settling time of the third stage is also a half of the first stage, because capacitances of the third stage are far smaller than those of the first stage. The analog adder samples the output of the first stage at the clock P2 through the capacitor C_{a1}, the second stage at the clock P3 through C_{a23}. At the clock P3, summation of the third stage output by the capacitor C_{a23} through -1 gain and holding adder output are performed simultaneously. In the actual circuit design, the -1 gain is an inverted connection of differential output signal, thus no special circuit for -1 gain is required. The flash A/D compares the input signal at the clock P5 and the result of the flash A/D is latched at the negative edge of the clock P5. The latched data is provided to the DAC block and selects C_{Dp} or C_{Dn} to be connected to the first stage integrator as a feedback signal.

3 Design and simulation result

The proposed third order DSM is designed on 0.35 μm CMOS process with 3.3 V supply. In the design, the modulator sampling clock frequency is $f_s =$ 3.25 MHz, thus the required supply clock frequency is 6.5 MHz to produce clock P3 and P4. Integrator gains, a_1, a_2 and a_3 are designed to be 1, 1/4 and 1/10. The capacitances $C_{s1} = C_{i1} = 2$ [pF] $C_{s2} = 0.4$ [pF] $C_{i2} = 1.6$ [pF] $C_{s3} = 0.1$ [pF], $C_{i3} = 1.0$ [pF], $C_a = C_{a0} = C_{a1} = C_{a23} = 0.2$ [pF] are chosen based on kT/C noise scaling and the integrator gains.

Fig. 2 shows the output spectrum of Hspice simulation result with a -6 dBFS sine-wave input and the achieved SQNR is 96 dB. The performance of the proposed DSM is summarized in Table I.

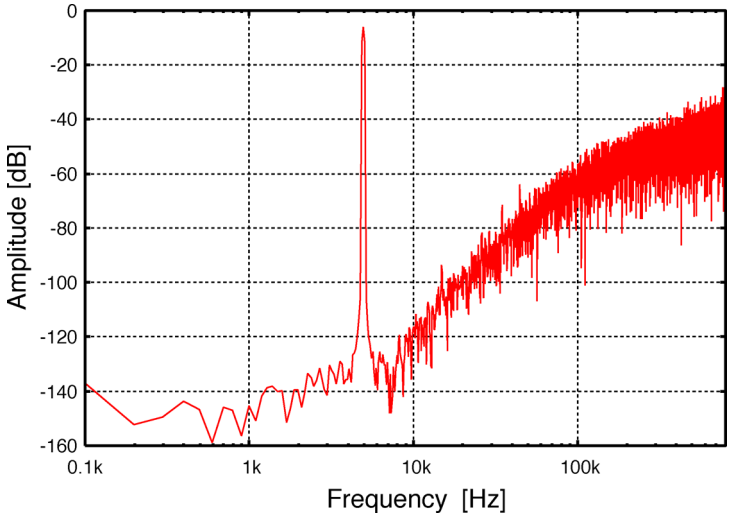

Fig. 2. Output spectrum with a -6 dBFS sine-wave input.

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Table I. Performance summary of the designed proposed DSM.

Parameter [Unit]	value
Bandwidth [Hz]	100-11 k
Sampling Frequency [Hz]	3.25 M
SQNR (-6 dBFS input) [dB]	96
Maximum Input Voltage [V]	165 m
Supply Voltage [V]	3.3
Power dissipation	1 mW

4 Conclusion

A novel third order DSM with one shared opamp achieved by optimal operation timing is presented. The operation timing of the DSM makes use of capacitance scaling by kT/C noise scaling to realize third order DSM with an opamp. The proposed DSM, designed on 0.35 μm CMOS process under 3.3 V supply achieves 1 mW power dissipation with 100-11 kHz band width and 96 dB SQNR.

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