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Note	

Gate stress-induced mobility degradation in NO-nitrided SiC(0001) MOSFETs

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The impacts of gate voltage stress on the on-state characteristics of NO-nitrided SiC(0001) MOSFETs were examined. A strong negative voltage stress at 300ºC induced a decrease in the channel mobility of the MOSFETs. This mobility decrease occurred along with an increase in the interface state density. Through MOS Hall effect measurements, we proposed a model in which the stress-induced interface states are located on the SiC side of the interface, close to where free electrons in the MOS channel are confined, thereby acting as a strong source of Coulomb scattering.

Silicon carbide (SiC) is a material characterized by a wide bandgap, high critical electric field, and high thermal conductivity[1)]. These properties make SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) promising as power switching devices. However, the performance of practical SiC MOSFETs is limited by their high channel resistance (R_{ch})[2)]. R_{ch} is governed by two factors: the free carrier density (n_{free}) and the mobility of free electrons[3)]. The n_{free} is determined by the interface state density (D_{it}) of the MOS structure; increased electron trapping results in fewer free electrons in the MOS channel. D_{it} values are known to be very high in SiC MOS structures, exceeding 10^{14} $cm^{-2}eV^{-1}$ near the conduction band edge (E_C) of SiC[3)–5)]. Although the origin of the interface states is uncertain, carbon-related defects generated during the thermal oxidation of SiC are a primary candidate, as suggested both experimentally[6)–8)] and theoretically[9)–12)]. Interface nitridation in a nitric oxide (NO) ambient is the standard method for defect passivation at the SiC MOS interface[13),14)]. While there are reliability concerns with nitridation[15)–17)], it is evident that D_{it} passivation leads to an increase in n_{free}. The mobility of free electrons is typically represented by the Hall mobility (μ_{Hall}) obtained from MOS Hall effect measurements. However, clarifying the limiting factors of μ_{Hall} is not straightforward. Previous studies have reported that nitridation unexpectedly results in a decrease in μ_{Hall}[3),18)]. The difficulty lies in the fact that while nitridation passivates interface states, it can also lead to the generation of fast interface states[19),20)], fixed charges[21)], and interface dipoles[16),22)]. Although both experimental[23)–26)] and theoretical studies[27),28)] have investigated the limiting factors of μ_{Hall}, the complicated situation makes it difficult to resolve the factors that determine mobility. Thus, a means to change the density of interface states and fixed charges in a controlled manner is needed to help clarify the mobility-limiting factors.

In the present study, we focused on how gate voltage stress affects the on-state characteristics of MOSFETs. In terms of reliability, the effect of gate stress has been extensively studied[16),29)–32)], highlighting the impacts of post-deposition annealing[30)], crystal faces[16)], measurement methods[31)], and practical device processing[32)]. While it is well known that gate voltage stress induces carrier trapping in the oxide, it can also cause additional interface states depending on the stress conditions[33),34)]. We aim to control the density of interface states and fixed charges by adjusting the stress conditions, thereby gaining insight into the mobility-limiting factors of SiC MOSFETs.

Figure 1(a) describes the gate stack formation process of MOSFETs and MOS Hall bars in this study. We used p-type SiC(0001) epilayers (acceptor density: 8×10^{15} cm^{-3}). After wet cleaning, the oxide was formed by dry oxidation and Ar annealing at 1200°C, followed by

NO annealing at 1250°C for either 10 or 120 min. Poly-Si was used as the gate electrode material. The channel length and width of the MOSFETs (MOS Hall bars) were 5 (300) and 200 (40) μm, respectively. We focused on the impact of negative gate voltage stress in this study. A gate voltage stress corresponding to an oxide field of −8 $MVcm^{-1}$ was applied for up to 5000 s at either room temperature (RT) or 300°C, and gate characteristics (Hall effect characteristics) were repeatedly measured for the MOSFETs (MOS Hall bars). The source and drain contacts were floating, and the body contact was grounded when the stress voltage was applied. The voltage sweep direction was negative to positive (positive to negative) with a sweep rate of approximately 1.0 Vs^{-1} (0.14 Vs^{-1}) when measuring the gate characteristics (Hall effect characteristics). As shown in the schematic illustration of MOS Hall bars in Fig. 1(b), Hall voltage was measured using external voltage terminals. A magnetic field of 0.2 T was applied perpendicularly to the SiO_2/SiC interface during the Hall effect measurements.

Figure 2 shows the variation of drain current (I_d) and field-effect mobility (μ_{FE}) as a function of gate voltage (V_g) for the 120-min nitrided SiC MOSFET during the stress test measurements. Both bias stress and measurements were performed at (a)(b) RT and (c)(d) 300°C. I_d was normalized by the channel length (L) and channel width (W), and the drain voltage was set to 0.1 V. For RT stress, the I_d-V_g characteristic drifted with the application of stress (Fig. 2(a)). During the negative voltage stress, holes in the MOS channel are captured into the near-interface oxide traps, resulting in a negative threshold voltage (V_{th}) drift. Although generation of interface hole traps is also a possible explanation of the negative V_{th} drift, the holes captured into interface traps would immediately recombine with electrons as soon as electrons are induced in the MOS channel. As a hump due to electron-hole recombination is not evident in the characteristic, it is likely that the holes are rather injected into oxide traps where the recombination does not easily occur. The mobility characteristic also experienced the drift, but its maximum value remained almost constant before and after the stress (Fig. 2(b)). This indicates that the oxide traps have a limited impact on μ_{FE}. As a result of high-temperature stress at 300°C, degradation in the subthreshold characteristic was observed in addition to the drift (Fig. 3(c)). This indicates an increase in the D_{it} values. In addition, a strong decrease in the μ_{FE} was observed (Fig. 2(d)). Thus, in contrast to oxide traps, the stress-induced interface states seem to have a strong impact on the μ_{FE}. Figure 3 summarizes the threshold voltage drift (ΔV_{th}), subthreshold swing (SS), and maximum μ_{FE} ($\mu_{FE,max}$) of a 120-min nitrided SiC MOSFET as a function of stress time: (a) the relationship between ΔV_{th} and SS, and (b) that between $\mu_{FE,max}$ and SS. Here, V_{th} was determined as the gate voltage where $I_d \times L/W$ equals 10^{-9} A, and SS was evaluated within the drain current range of 10^{-11} A < I_d×L/W < 10^{-10} A. Although V_{th} drifted negatively with applied RT stress, the *SS* value hardly changed (Fig. 3(a)). Thus, the capture of holes into the oxide traps is irrelevant to the generation of interface states. At 300°C stress, V_{th} slightly drifted negatively until 100 s, but then drifted positively. The positive drift of V_{th} is accompanied by an increase in *SS* and thus caused by an increase in D_{it}. Although the mechanism of D_{it} increase remains uncertain, high electric field and high temperature conditions likely lead to bond-breaking reactions, thereby generating additional defects. The $\mu_{FE,max}$ and *SS* were both unchanged by RT stress (Fig. 3(b)). However, as a result of 300°C stress, the decrease in the $\mu_{FE,max}$ occurred in accordance with the increase in the *SS*. Thus, it is clear that the stress-induced interface states strongly reduce the μ_{FE}.

Figure 4 shows the energy distribution of D_{it} values of 10-min nitrided (NO10) and 120-min nitrided (NO120) SiC MOS structures obtained from the *SS* values within the drain current range of 10^{-11} A < I_d×L/W < 10^{-7} A. The detailed method of D_{it} evaluation is described in Ref.[35]. The change in the D_{it} values when applying stress at 300°C is also shown for sample NO120. The trap energy level (horizontal axis) was determined as the average Fermi level that corresponds to the minimum and maximum drain current where the *SS* values were evaluated. For example, when the *SS* value was obtained within the drain current range of 10^{-11} A < I_d×L/W < 10^{-10} A, the trap energy level equals the mean value of Fermi levels, which gives I_d×L/W of 10^{-11} A and 10^{-10} A. To calculate the Fermi level corresponding to a given drain current, free electron mobility should be assumed. We assumed the free electron mobilities of NO10 and NO120 to be 70 $cm^2V^{-1}s^{-1}$, and those of NO120 after 10, 1000, 2000, 3000, and 4000 s of stress to be 70, 60, 40, 20, and 20 $cm^2V^{-1}s^{-1}$, respectively, referring to the μ_{Hall} at a low free electron density (n_{free} = $1×10^{11}$ cm^{-2}). The gate voltage dependence of free electron mobility was neglected for the sake of simplicity. As a result, D_{it} in the energy range of approximately 0.15 eV < $E_C − E_T$ < 0.30 eV increased as the stress was applied to sample NO120 (Fig. 4). Nevertheless, the D_{it} values were still lower compared with the sample with insufficient nitridation (NO10).

We then examined the μ_{Hall} of the samples as shown in Fig. 5: (a) NO120 before applying stress (NO120 w/o stress), (b) NO120 after applying 4000-s stress at 300°C (NO120 w/ stress), and (c) NO10 without stress. Unlike the μ_{FE} which is affected by both the density and mobility of free electrons by its definition, μ_{Hall} represents the actual free electron mobility and thus is useful for discussing the carrier scattering mechanisms. A body bias was applied to control the surface electric field (E_s) of SiC, and the measurements were performed at RT. When comparing the results without the application of the body bias (0 V), the samples

NO120 w/o stress (Fig. 5(a)) and NO10 w/o stress (Fig. 5(c)) showed similar μ_{Hall}, while the sample NO120 w/ stress showed significantly lower μ_{Hall} especially at lower n_{free}. With the application of the body bias, this difference is even more pronounced. The sample NO120 w/ stress exhibited a strong decrease in the μ_{Hall} when applying a negative body bias. Since a negative body bias increases the surface electric field of SiC, free electrons become more strongly confined to the MOS channel, leading to enhanced carrier scattering, in particular for the sample NO120 w/ stress. Focusing on the n_{free} dependence of μ_{Hall}, μ_{Hall} increases with the n_{free} in the sample NO120 w/ stress. This is a clear signature of Coulomb scattering, where electron shielding results in increased mobility as the n_{free} increases[36]. However, the D_{it} values are still lower in the sample NO120 w/ stress than in the sample NO10 (Fig. 4). Thus, the high D_{it} does not necessarily lead to a decrease in the μ_{Hall}.

To discuss the cause of the μ_{Hall} decrease observed in the sample NO120 w/ stress, we further analyzed the Hall mobility data, considering the spatial distribution of free electrons in the MOS channel. The free electron wave function in the first subband of the inversion layer, $\zeta_0(z)$ under the triangular potential approximation is given by[37]

$$\zeta_0(z) = \mathrm{Ai}\left[\left(\frac{2m_z qE_s}{\hbar^2}\right)^{\frac{1}{3}}\left(z - \frac{E_0}{qE_s}\right)\right], \quad (1)$$

where Ai represents the Airy function. z, m_z, $\hbar$, and E_0 are the depth in SiC measured from the SiO_2/SiC interface, the electron effective mass in SiC perpendicular to the interface, Dirac's constant, and the energy level of first subband, respectively. Then, the averaged distance of electrons from the interface, z_{AV} can be estimated by[37]

$$z_{\mathrm{AV}} = \frac{\int z\zeta_0^2 dz}{\int \zeta_0^2 dz}. \quad (2)$$

Figure 6(a) plots the μ_{Hall} at a low free electron density ($n_{\mathrm{free}} = 5\times10^{11}$ cm^{-2}) as a function of z_{AV}. z_{AV} was changed by applying body bias for each sample. As a result, while μ_{Hall} took similar values for the samples NO120 w/o stress and NO10 at a given z_{AV}, the sample NO 120 w/ stress showed lower μ_{Hall}. When shifting the data points of NO120 w/o stress and NO10 towards larger z_{AV} by a few angstroms, it seems that they match well with those of NO120 w/ stress. This suggests that the stress-induced D_{it} is located slightly deep inside the SiC and thus behaves as a strong Coulomb scattering source, as shown in Fig. 6(b). In the present case, the origin of D_{it} at the SiC side is presumably nitrogen-related defects that are activated by the gate voltage stress. As a result, we pointed out that, while of relatively low trap density, D_{it} located on the SiC side of the interface can behave as a strong source of Coulomb scattering.

In conclusion, we investigated the impact of gate stress on the on-state characteristics of nitrided SiC MOSFETs. We found that, while hole trapping into the oxide has a limited impact on field-effect mobility, the stress-induced D_{it} severely degrades the mobility. Through MOS Hall effect measurements, it is highly likely that the mobility of MOSFETs subjected to high-temperature stress is limited by Coulomb scattering. We proposed that D_{it} on the SiC side of the interface, although of comparably low density, can behave as a strong source of Coulomb scattering.

Acknowledgments

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Figures

Fig. 1. (a) Process flow of gate stack formation in this study. (b) Schematic of MOS Hall bar structures.

Fig. 2. Drain current and field-effect mobility as a function of gate voltage for the 120-min nitrided SiC MOSFET during stress test measurements: negative bias stress and measurement were performed at (a)(b) RT and (c)(d) 300°C.

Fig. 3. Threshold voltage drift, subthreshold swing, and maximum field-effect mobility of the 120-min nitrided SiC MOSFET as a function of stress time: (a) the relationship between threshold voltage drift and subthreshold swing, and (b) that between maximum field-effect mobility and subthreshold swing.

Fig. 4. Energy distribution of interface state density for the 10-min nitrided (NO10) and 120-min nitrided (NO120) SiC MOS structures obtained from the subthreshold swing.

Fig. 5. Hall mobility of SiC MOS devices: (a) NO120 before applying stress, (b) NO120 after 4000-s stress at 300°C, and (c) NO10 without stress.

Fig. 6. (a) Hall mobility of SiC MOS devices at a low free electron density (n_{free} = 5×10^{11} cm^{-2}) as a function of the average distance of free electrons from the SiO_2/SiC interface. (b) Schematic describing a model where stress-induced interface states are located on the SiC side of the interface, behaving as a strong source of Coulomb scattering.

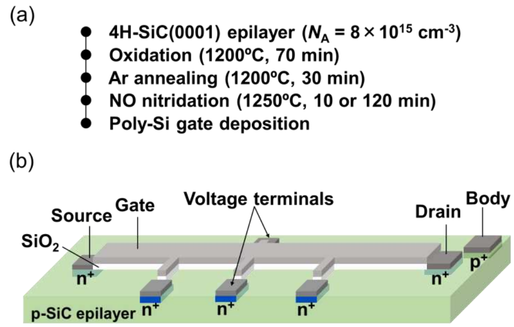

Fig. 1

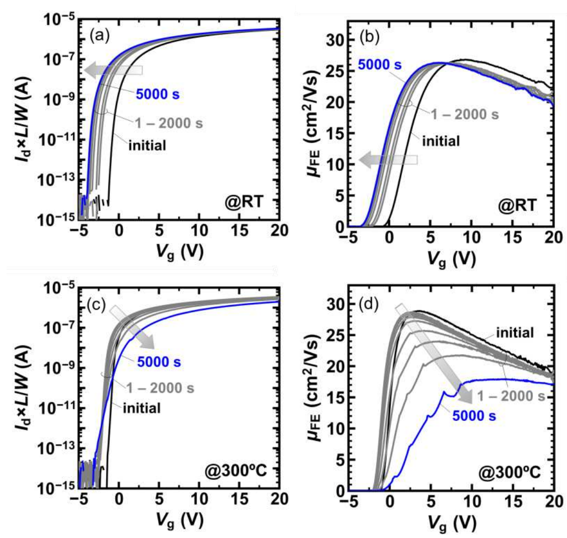

Fig. 2

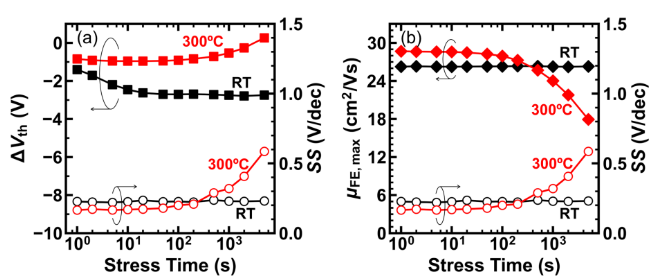

Fig. 3

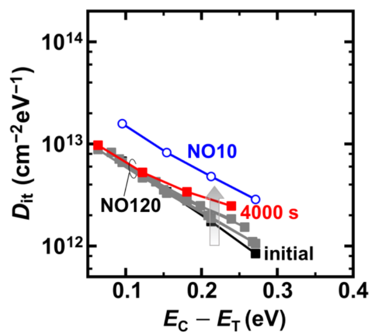

Fig. 4

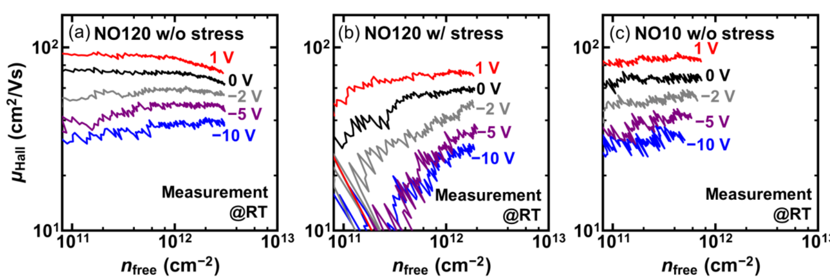

Fig. 5

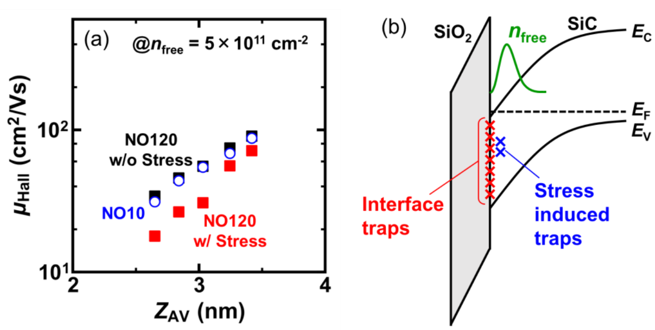

Fig. 6