Formation of high-quality SiO_2/β-Ga_2O_3(001) MOS structures: the role of post-deposition annealing

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We investigated the effect of post-deposition annealing on the electrical characteristics of SiO_2/β-Ga_2O_3(001) MOS structures. While oxygen annealing effectively improves the interface properties, it induces acceptor defects in Ga_2O_3, leading to a decrease in net donor density. With the combination of oxygen and nitrogen annealing, carrier compensation was suppressed, and a low interface state density of about 1×10^{11} $cm^{-2}eV^{-1}$ was obtained near the conduction band edge of Ga_2O_3. High immunity against positive gate bias stress was also confirmed.

Gallium oxide (Ga_2O_3) is an ultra-wide bandgap semiconductor that shows promise for next-generation power electronics and solar-blind deep ultraviolet photodetectors[1)–5)]. Among the confirmed polytypes (α, β, γ, δ, ε), the monoclinic β-Ga_2O_3 is the most stable, with a large bandgap energy of 4.9 eV. The major advantage of Ga_2O_3 over other wide bandgap semiconductors is the availability of the melt growth process, which can produce large, uniform substrates at a lower cost compared with vapor growth techniques. Ga_2O_3 metal-oxide-semiconductor field-effect transistors (MOSFETs) are attractive for power switching applications. Typically, *n*-channel power MOSFETs (e.g., DMOSFETs[6)]) have a *p*-type body layer, whose surface is inverted to *n*-type by the application of a gate voltage in the on-state of the devices. In the off-state, the depletion layer vertically extends from the *p*-*n* junction to a thick *n*-type drift layer to withstand high voltage. However, obtaining *p*-type conductivity in Ga_2O_3 is challenging due to the presence of self-trapping holes (hole polarons)[7)–9)], the high effective mass of holes[10),11)], and a high abundance of Ga interstitials under *p*-type conditions[12)–14)]. Despite the lack of *p*-type doping, various power devices, including depletion-mode[15),16)] and enhancement-mode MOSFETs[17),18)], MOS junction FETs[19)], and superjunction-equivalent MOSFETs[20)], have been demonstrated for Ga_2O_3. The choice of dielectrics is particularly important for achieving high performance, stability, and reliability of MOS devices. Aluminum oxide (Al_2O_3) is the best-studied dielectric for Ga_2O_3[21)–26)], but it suffers from small band offsets (1.5–1.6 eV for the conduction band and 0.7 eV for the valence band[27)]) and Ga diffusion into the dielectric during thermal annealing[22)]. Given the wide bandgap of Ga_2O_3, silicon dioxide (SiO_2) would be a better dielectric to ensure sufficiently large band offsets[28)]. SiO_2 also has advantages in terms of its high thermal stability. In addition to the deposition process of dielectrics, a key factor in optimizing MOS structures is post-deposition annealing (PDA). Although there are few reports on the improvement of SiO_2/Ga_2O_3 MOS structures by PDA[29),30)], the practical role of PDA has not been well studied. To establish a method for obtaining a high-quality interface between SiO_2 and Ga_2O_3, the role of PDA should be further investigated.

In the present study, we extensively studied the effect of oxygen (O_2) and nitrogen (N_2) PDA on the electrical characteristics of SiO_2/β-Ga_2O_3(001) MOS structures. We investigated the dependence on annealing temperature and examined the effectiveness of a two-step annealing treatment (i.e., O_2 annealing followed by N_2 annealing) on the device characteristics. In particular, we focused on the impact of PDA on the interface properties, bulk carrier density, and reliability of the MOS structures. We aim to develop a strategy for forming a high-quality SiO_2/Ga_2O_3 MOS structure.

Figure 1 illustrates the fabrication process flow of Ga_2O_3 MOS capacitors. β-Ga_2O_3(001) epilayers with a donor density of approximately 1×10^{16} cm^{-3} were used in this study. After wet cleaning the samples with methanol, acetone, and piranha solution, SiO_2 films were deposited using plasma-enhanced chemical vapor deposition (PECVD). Under a radiofrequency (RF) power of 30 W and pressure of 79 Pa, a gas mixture of tetraethyl orthosilicate (TEOS) and O_2 was introduced into the PECVD chamber, and SiO_2 was deposited at a substrate temperature of 400°C. The samples were then subjected to O_2 or N_2 annealing at 600–1000°C for 30 min, or a combination of these annealing conditions. Finally, nickel (Ni) gate electrodes and aluminum (Al) back contacts were formed by vacuum evaporation to fabricate the MOS structures. Table I summarizes the names and capacitance equivalent SiO_2 thickness of Ga_2O_3 MOS structures prepared in this study. In addition, a reference Schottky barrier diode without a SiO_2 film was also prepared to investigate the bulk properties of Ga_2O_3. All electrical measurements were conducted at room temperature.

Figure 2 shows the bidirectional capacitance-voltage (*C*-*V*) characteristics of Ga_2O_3 MOS capacitors measured at a probe frequency of 1 MHz: (a) samples with and without O_2 annealing and (b) those with N_2 annealing or combined O_2 and N_2 annealing. As shown in Fig. 2(a), the as-deposited sample exhibited a large *C*-*V* hysteresis due to a high number of interface traps. While O_2 annealing at 600°C resulted in an even degraded characteristic indicating trap formation at the interface, the situation was improved after annealing at 1000°C. Although high-temperature O_2 annealing was effective in reducing the traps, a relatively large hysteresis remained even after annealing at 1000°C. With additional N_2 annealing, the situation improved significantly (Fig. 2(b)). In particular, after O_2 and N_2 annealing at 1000°C, a steep *C*-*V* characteristic with minimal hysteresis was obtained. On the contrary, the sample with N_2 annealing at 1000°C alone resulted in a limited improvement. These results suggest that the combination of O_2 and N_2 annealing is effective in reducing interface traps in SiO_2/Ga_2O_3 MOS structures. A slight negative shift in the *C*-*V* characteristic was confirmed, which is likely due to the presence of positive fixed charges at the interface. Since the maximum capacitance varies among the samples without a clear trend with respect to the PDA conditions, the variation is mainly attributed to the differences in the deposited SiO_2 thickness (Table I). In addition to the maximum capacitance, we found that the minimum capacitance also depends on the sample conditions (Figs. 2(a) and (b)). This indicates that PDA affects the donor concentration in bulk Ga_2O_3.

We then evaluated the net donor density from the $1/C^2$-*V* characteristics of Ga_2O_3 MOS capacitors in the deep-depletion range. The donor density as a function of depth from the

SiO_2/Ga_2O_3 interface is shown in Fig. 3. Initially, the as-deposited sample showed a doping profile identical to that of a Schottky diode formed directly on the epilayer surface (as-epi.). This indicates that SiO_2 formation by PECVD has a limited impact on donor density. This is likely due to the low-temperature deposition, which should be favorable in suppressing unwanted defect formation in bulk Ga_2O_3 due to the thermal budget. The slight increase in density observed in deeper Ga_2O_3 is likely due to imperfect doping control during the epitaxy process. After O_2 annealing at 1000°C, an order-of-magnitude decrease in donor density was observed. Since oxygen interstitials act as deep acceptors in Ga_2O_3[12)–14)], this suggests that oxygen diffuses into the Ga_2O_3 during O_2 annealing, leading to a reduction in donor density via the carrier compensation effect. The formation of oxygen interstitials is preferred in Ga_2O_3 because they have quite low formation energies especially under oxygen-rich and *n*-type conditions[12)–14)]. However, the diffusion barrier of oxygen atoms in the [100] direction in β-Ga_2O_3 has been experimentally determined to be as high as (3.2 ± 0.4) eV[31)]. Thus, a crystal orientation dependent or a defect mediated diffusion process is responsible for explaining the oxygen diffusion on the μm scale. Another possibility is the formation of gallium vacancies during O_2 annealing, which also act as deep acceptors in Ga_2O_3[12)–14)]. The formation of gallium vacancies is favored under an oxygen-rich condition because it corresponds to a gallium-poor condition[12)–14)]. In fact, their formation during O_2 annealing is experimentally discussed as the cause of the resistivity increase observed in β-Ga_2O_3[32)]. Although further studies are needed to clarify the origin of the deep acceptors, a clear recovery of donor density towards its initial values was observed with additional N_2 annealing (Fig. 3). With N_2 annealing at 1000°C after O_2 annealing, the doping profile of the as-deposited sample was reproduced. Note that the differences in the profiles of as-epi., as-depo., N_2-1000°C, and O_2-1000°C→N_2-1000°C samples are small and well within the experimental variation. In bulk Ga_2O_3, it has also been reported that O_2 annealing reduces donor density, while N_2 annealing is effective in suppressing carrier compensation[33)]. Thus, additional N_2 annealing appears to reduce the deep acceptors in Ga_2O_3. Overall, the combination of O_2 and N_2 annealing not only improves interface properties (Fig. 2(b)) but also suppresses unwanted carrier compensation caused by acceptor-type defects (Fig. 3).

To further assess the interface properties, we evaluated the interface state density (D_{it}) using the high (1 MHz)-low method. Note that the D_{it} distribution is evaluated by taking into account the SiO_2 thickness of each sample and the results are not affected by the variation in the thickness. Figure 4 shows the energy distribution of D_{it} for Ga_2O_3 MOS capacitors. To determine the trap energy level ($E_c - E$), the donor density value is needed. Since the donor

density varies with depth for the samples in this study (Fig. 3), we assumed the donor density at depth of approximately 0.5 μm from the interface for each sample. As shown in Fig. 4, the as-deposited sample exhibited a relatively high D_{it} of about 7×10^{11} $cm^{-2}eV^{-1}$ at $E_c - E = 0.2$ eV. However, D_{it} was reduced to about $(3–4)\times10^{11}$ $cm^{-2}eV^{-1}$ after either O_2 or N_2 annealing at 1000°C. The combination of O_2 and N_2 annealing resulted in further improvement of D_{it} ($\sim 1\times10^{11}$ $cm^{-2}eV^{-1}$). This result aligns well with the *C-V* measurements (Fig. 2), indicating the effectiveness of combined O_2 and N_2 annealing in improving interface properties.

Finally, we investigated the reliability of the MOS structures in response to charge injection into the SiO_2 film. Specifically, a constant gate voltage stress corresponding to an oxide field of + 4 $MVcm^{-1}$ was applied to the MOS structures for up to 2000 s, and *C-V* characteristics were repeatedly measured to monitor any changes. Here, the stress field was determined for each sample from the over drive voltage, i.e., $(V_G - V_{FB})/t_{OX}$, where V_G, V_{FB}, and t_{OX} are the gate voltage, the flatband voltage, and the SiO_2 thickness, respectively. Figure 5(a) shows the measurement results for typical samples. While the as-deposited sample exhibited significant drift in the characteristics under stress, the sample with combined O_2 and N_2 annealing showed substantially less drift. The flatband voltage drift (ΔV_{FB}) as a function of stress time was quantified for the fabricated samples, as summarized in Fig. 5(b). The as-deposited sample exhibited a large ΔV_{FB} of about 8 V after 2000 s of stress. O_2 annealing at 600°C resulted in an even larger drift (~11 V), indicating that low-temperature oxidation induces near-interface traps. When the annealing temperature was increased to 1000°C, a much smaller drift (~3 V) was observed, likely due to trap passivation. The sample with combined O_2 and N_2 annealing exhibited a drift of less than 2 V. Thus, the combination of O_2 and N_2 annealing effectively improves reliability. Since the reliability is also improved by N_2 annealing alone, thermal effects are likely responsible for the improved reliability.

In conclusion, we investigated the impact of PDA on the electrical characteristics of SiO_2/β-Ga_2O_3(001) MOS structures. While O_2 annealing was effective in improving the *C-V* characteristics to some extent, we found that it leads to a decrease in net donor density in Ga_2O_3, indicating the formation of deep acceptor defects, likely due to oxygen interstitials or gallium vacancies. However, by performing N_2 annealing in addition to O_2 annealing, the donor density recovered to its initial values observed after the epitaxial growth of Ga_2O_3. The combination of O_2 and N_2 annealing resulted in a very low D_{it} of approximately 1×10^{11} $cm^{-2}eV^{-1}$ near the conduction band edge ($E_c - E = 0.2$ eV) of Ga_2O_3, while a slight negative shift in the *C-V* characteristics due to positive fixed charges was observed after the improvement. On the contrary, O_2 or N_2 annealing alone resulted in limited improvement in

the D_{it} (about (3–4)×10^{11} $cm^{-2}eV^{-1}$). Gate bias stress measurements also confirmed high immunity against positive gate bias for the sample with combined O_2 and N_2 annealing. Since high immunity was also achieved by N_2 annealing alone, the improved reliability is mostly due to thermal effects. After all, the two-step annealing treatment is effective in reducing the D_{it} values and improving the reliability of SiO_2/β-Ga_2O_3(001) MOS structures.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Figures

Table I. Names and SiO_2 thickness of Ga_2O_3 MOS structures prepared in this study. The SiO_2 thickness was evaluated from the maximum capacitance of MOS capacitors.

Fig. 1. Fabrication process flow of Ga_2O_3 MOS capacitors.

Fig. 2. Bidirectional *C*-*V* characteristics of Ga_2O_3 MOS capacitors measured at a frequency of 1 MHz: (a) samples with and without O_2 annealing, and (b) those with N_2 annealing or combined O_2 and N_2 annealing.

Fig. 3. Net donor density in Ga_2O_3 evaluated from the $1/C^2$-*V* characteristics of Ga_2O_3 MOS capacitors in the deep-depletion range as a function of depth from the SiO_2/Ga_2O_3 interface. The result for the Ga_2O_3 Schottky diode formed on the epilayer is also shown (as-epi).

Fig. 4. Energy distribution of D_{it} for SiO_2/Ga_2O_3 MOS capacitors evaluated using the high (1 MHz)-low method.

Fig. 5. (a) Change in the *C*-*V* characteristics of SiO_2/Ga_2O_3 MOS capacitors under positive gate bias stress (E_{OX} = + 4 $MVcm^{-1}$). The stress was applied for up to 2000 s. (b) Flatband voltage drift (ΔV_{FB}) as a function of stress time for SiO_2/Ga_2O_3 MOS capacitors.

Table I

Sample Name	SiO_2 Thickness [nm]
as-depo.	35.0
O_2-600°C	37.1
O_2-1000°C	37.6
O_2-1000°C→N_2-600°C	32.5
O_2-1000°C→N_2-800°C	37.1
O_2-1000°C→N_2-1000°C	41.5
N_2-1000°C	37.0

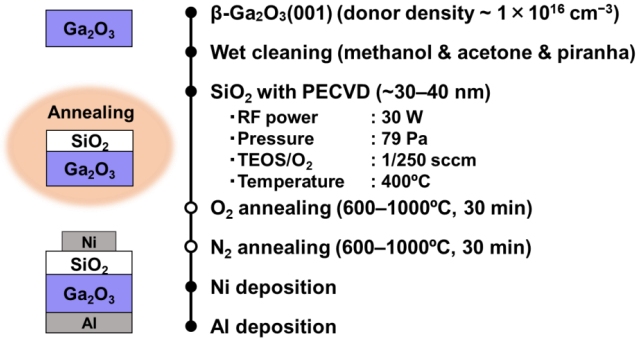

Fig. 1

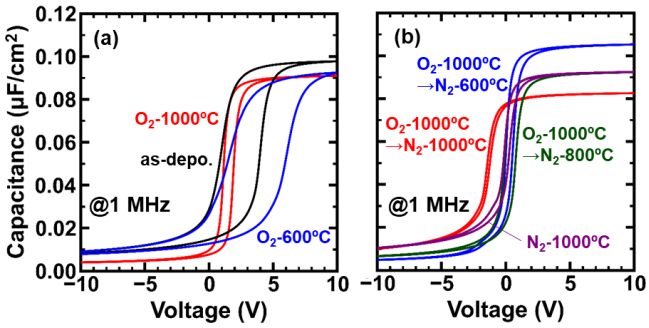

Fig. 2

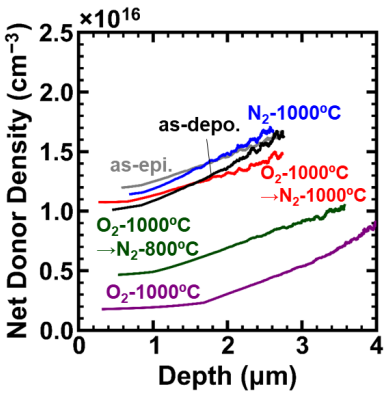

Fig. 3

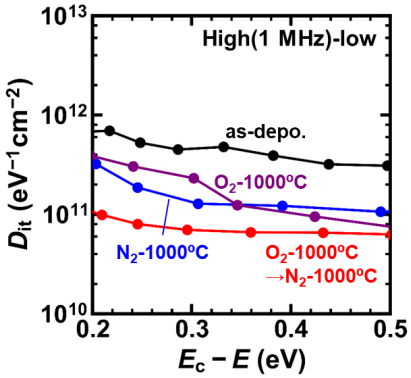

Fig. 4

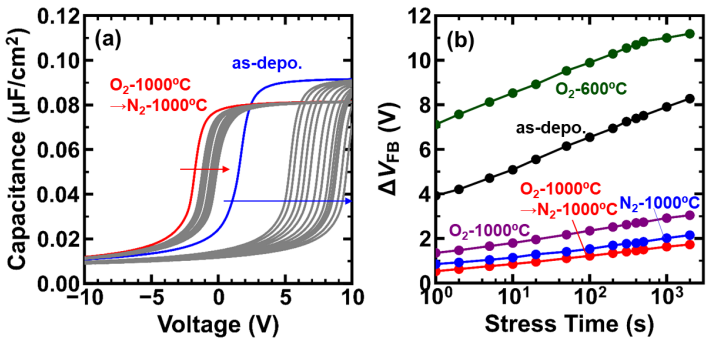

Fig. 5