GaO_x interlayer-originated hole traps in SiO_2/*p*-GaN MOS structures and their suppression by low-temperature gate dielectric deposition

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In this study, we investigated the impact of SiO_2 deposition temperature during plasma-enhanced chemical vapor deposition (PECVD) on the generation of fast hole traps, which cause surface potential pinning, in p-type GaN MOS structures. The thickness of a gallium oxide (GaO_x) layer at the SiO_2/GaN interface was estimated and correlated with the hole trap generation. The 200°C-deposited SiO_2/GaN MOS structures exhibited a smaller amount of fast hole traps and a thinner GaO_x interlayer than the 400°C-deposited samples. In the 200°C-deposited samples, annealing at a temperature below 600°C did not lead to an increase in the fast hole trap and GaO_x layer thickness, while the amount of fast traps significantly increased just after 800°C-annealing in O_2 ambient, accompanied by the growth of the GaO_x interlayer. These findings suggest that the major origin of fast hole traps in SiO_2/GaN MOS structures is a thermally induced defect existing inside a GaO_x interlayer and that the low-temperature SiO_2 deposition is effective in reducing the fast traps.

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The wide bandgap, high critical electric field, and high electron saturation velocity of gallium nitride (GaN) make it an attractive material for high-voltage and high-frequency power device applications[1–3]. So far, extensive research and development have been dedicated to high electron mobility transistors (HEMTs), which utilize a two-dimensional electron gas (2DEG) induced at aluminum gallium nitride (AlGaN)/GaN hetero interfaces[4,5], and GaN-based HEMTs are already in commercialization. While HEMTs have a lateral device structure and are usually fabricated with GaN grown on foreign substrates, high-quality GaN freestanding substrates have become available in the last decade[6–10]. As a result, GaN-on-GaN vertical power switching devices, including metal-oxide-semiconductor field-effect transistors (MOSFETs), have attracted increasing attention for high-voltage applications[11,12].

Silicon dioxide (SiO_2) is a gate dielectric suitable for the fabrication of GaN MOS structures, thanks to its sufficiently large band offset and high thermal stability. Thus, the formation of a high-quality SiO_2/GaN interface, namely, reduction of electron and hole traps near the interface, is crucial for achieving power MOSFETs with high performance and reliability. Regarding electron traps, an interface state density (D_{it}) near the conduction band edge (E_C) has been intensively studied using n-type GaN MOS capacitors[13–16], and a gate dielectric formation process that can achieve a very low D_{it} ($\sim 10^{11}$ cm^{-2}eV^{-1}) has been developed[17,18]. Thanks to the excellent interface property near E_C, GaN MOSFETs exhibiting a high channel mobility over 100 cm^{2}V^{-1}s^{-1} have been demonstrated in several studies[19–23].

In contrast to the low electron trap density in GaN MOS structures, a high-density hole trap near the valence band edge (E_V), which causes a large shift of the threshold voltage during an OFF-state operation of MOSFETs, has been a significant issue degrading the device reliability. Hole trap density is so high that reasonable accumulation of holes has barely been observed in typical p-type GaN MOS capacitors[24–26]. Our group recently found that SiO_2/GaN MOS structures fabricated on heavily magnesium (Mg)-doped p-GaN ($\sim 10^{19}$ cm^{-3}) exhibit an exceptionally low hole trap density[27,28]. Although this finding provides us with an important clue for a physical understanding of the hole trap, the origin is still under debate[29–31], and an optimum process that can achieve a sufficiently low hole trap density has not yet been established.

We recently reported that there are two different types of hole traps existing near SiO_2/GaN interfaces based on photo-assisted capacitance–voltage (C–V) measurement with n-type GaN MOS capacitors utilizing sub- and above-bandgap light illumination[32]. One is a "fast trap," which responds to voltage sweeping during C–V measurement and makes the surface Fermi level strongly

pinned at the interface. The other is a "slow trap," in which hole capturing becomes more significant with a higher oxide field. Of these two, our recent research found that the density of fast traps in SiO_2/p-type GaN MOS structures significantly increases with elevating the temperature of post-deposition annealing (PDA), regardless of the annealing atmosphere (oxygen: O_2 or nitrogen: N_2)[33]. This result suggests that lowering the thermal budget during the fabrication of GaN MOS structures is vital to suppress the hole trap generation.

Since fast traps exist very near the dielectric/GaN interface, not only the PDA temperature but also process conditions for the SiO_2 deposition should significantly impact the hole trap density. In this sense, we have focused on the SiO_2 deposition temperature as a critical parameter to reduce the thermally induced fast hole traps. Our previous work adopted the substrate temperature of 400°C during plasma-enhanced chemical vapor deposition (PECVD)[33], but in this case, the density of fast hole traps in the SiO_2/GaN MOS structures fabricated without PDA or with 200°C-PDA was not sufficiently low ($2–3 \times 10^{12}$ cm^{-2}). Therefore, SiO_2 deposition at a lower temperature is likely effective in further reducing the fast hole traps. In this study, we fabricated SiO_2/p-type GaN MOS structures while varying the substrate temperature during PECVD and systematically investigated the impact of the SiO_2 deposition temperature on the generation of fast hole traps.

The starting material was a p-type GaN epitaxial layer with an Mg atom density of 7×10^{16} cm^{-3} grown on n-type GaN(0001) substrates. Note that, since p-type GaN substrates are unavailable, heavily doped p- and n-type GaN buffer layers with an Mg and silicon (Si) atom density of 3×10^{18} and 2×10^{18} cm^{-3}, respectively, were prepared at the epilayer/substrate interface to minimize the parasitic capacitance at the p-n junction and to form a backside contact. After the samples were cleaned with acetone and 50% HF solution, activation annealing for dehydrogenation was conducted at 800°C in N_2 ambient for 30 min. Wet cleaning was again conducted with the same procedure, and SiO_2 was deposited by PECVD, varying the deposition temperature from 200°C to 400°C. As for the other conditions for PECVD, the gas flow of tetraethyl orthosilicate (TEOS) and oxygen was 1 and 250 sccm, respectively, the pressure was 79 Pa, and the RF power was 30 W. The SiO_2 thickness was measured to be 27–33 nm by spectroscopic ellipsometry. It was found that the SiO_2 deposition rate was as high as 70 nm/min at 200°C, which is about three times higher than that for 400°C ($\sim$ 20 nm/min). Thus, the SiO_2 thickness was controlled to be almost identical among different substrate temperatures by properly conditioning the deposition time (28 s–80 s). After depositing SiO_2, PDA in O_2 ambient (O_2-PDA) was carried out in the temperature range of 200–800°C, followed by the formation of circular-shaped Ni gate electrodes

(diameter: 50–100 μm) and Al backside contacts through resistive heating evaporation under the pressure of 5×10^{-4} Pa. *C–V* characteristics of the p-GaN MOS capacitors were measured with the voltage sweep rate of about 0.5 V/s from depletion (positive voltage) to accumulation (negative voltage) and again back to depletion. Although the frequency-dependent *C–V* measurements are useful in discussing the time response of a trapping phenomenon, the series resistance is so high that the maximum capacitance (C_{max}) does not reach the oxide capacitance (C_{ox}) even with hole accumulation[28]. Thus, the probe frequency of 1 kHz was chosen to minimize the parasitic resistance. Hole trapping behavior was investigated based mainly on the hump in the *C–V* characteristics, which reflects the surface potential pinning due to hole traps.

Figure 1 shows the *C–V* characteristics of the p-GaN MOS structures fabricated with 400°C-deposited SiO_2 and O_2-PDA at various temperatures, which is the same process condition as the literature[33]. The voltage range of the hump where $C \sim 0.03$ μF (defined as hump width) gradually increased with elevating the PDA temperature from 200°C to 800°C. The C_{max} value of 0.11–0.12 μF/cm^2 (corresponding to the capacitance equivalent thickness of 29–31 nm) is very close to $C_{ox} \sim 0.13$ μF/cm^2 that is expected from the SiO_2 thickness (27 nm) measured by spectroscopic ellipsometry, indicating the accumulation of reasonable amount of holes at the PDA temperature lower than 400°C. In contrast, hole accumulation was barely achieved when the PDA temperature exceeded 600°C ($C_{max} \ll C_{ox}$). The observed PDA temperature dependence of the hump width suggests that fast hole traps generate at each PDA temperature and their density continuously increases by higher-temperature PDA.

On the other hand, the situation is dramatically changed for the SiO_2 deposition at a lower temperature. The *C–V* characteristics of the (a) 300°C- and (b) 200°C-deposited SiO_2/p-GaN MOS structures are presented in Fig. 2. *I–V* characteristics of each sample are also shown in Fig. 2(c) and (d). For the 300°C-deposited samples, the hump width was not much increased by low-temperature PDA ($\leq$ 400°C) and was smaller than that for the 400°C deposition, as seen in Fig. 2(a). Although PDA at 600°C generated a certain amount of fast hole traps, a part of the holes still accumulated. A significant increase in the hump width and generation of fast hole traps was observed just after annealing at 800°C, causing severe surface potential pinning. Regarding insulating properties, the gate leakage current was larger than that for the 400°C-deposited samples without performing PDA, as shown in Fig. 2(c). It was found that the leakage current was reduced by O_2-PDA at a temperature above 600°C and became comparable to that for the 400°C deposition after 800°C-annealing, which may be due to a denser SiO_2 film associated with oxygen diffusion

during high-temperature O_2-PDA.

The hump width was further reduced by SiO_2 deposition at 200°C and was almost 0 V when the PDA temperature was lower than 600°C, as seen in Fig. 2(b). Note that the maximum capacitance of the 200°C-deposited samples annealed at a temperature below 400°C was higher than the C_{ox} value (~ 0.10 μF) expected from the actual oxide thickness, which is likely due to the poor insulating property of low-temperature deposited SiO_2 without sufficient oxygen incorporation during O_2-PDA, as found in Fig. 2(d). When samples were annealed at 600°C, the leakage current was reduced, and the hole accumulation (i.e., $C_{max} \simeq C_{ox}$) was observed with almost no hump in the *C–V* characteristics, indicating that thermal generation of fast hole traps did not occur even at 600°C. Although the hump width was increased just after O_2-PDA at 800°C, the 200°C-deposited samples still exhibited an accumulation of a part of the holes even at such a high-temperature annealing. These results demonstrate that the substrate temperature of PECVD has a huge impact on the PDA temperature-dependent hole trap generation in SiO_2/p-GaN MOS structures. Note that atomic layer deposition (ALD) is also a useful technique for low-temperature formation of SiO_2. While reports on ALD-SiO_2/p-GaN MOS structures are limited, it is expected based on the present results that reduced hole traps could be achieved with ALD by optimizing process conditions, including the SiO_2 deposition temperature, which is an important future work.

To elucidate the critical factor that leads to the different PDA temperature dependence of the hump width in *C–V* curves (i.e., the density of fast hole traps), we have focused on a gallium oxide (GaO_x) layer formed at a SiO_2/GaN interface. It is known that a very thin GaO_x layer, whose thickness would be about 1 nm or less, is grown by the surface oxidation due to O_2 plasma at an early stage of the SiO_2 deposition with PECVD, and the thickness of the GaO_x layer increases by O_2-PDA at 600–800°C due to thermal oxidation[16,34]. While the typical substrate temperature of PECVD was over 300°C in the literature, we speculate that the low-temperature SiO_2 deposition can suppress the GaO_x growth because of the high deposition rate mentioned above. Since several theoretical studies have predicted that GaO_x interlayer can be an origin of hole traps in GaN MOS structures[30,31], suppression of GaO_x growth is presumably the main cause of the reduced hole traps.

Therefore, we next tried to estimate the SiO_2 deposition temperature dependence of the GaO_x thickness. We adopted a simple technique utilizing n-type GaN MOS capacitors for estimating the GaO_x growth, which is based on our previous work combining the electrical and x-ray photoelectron spectroscopy (XPS) measurements[35,36]. When post-metallization annealing in diluted

hydrogen (H_2) ambient (forming gas annealing (FGA)) was performed for SiO_2/n-type GaN MOS capacitors fabricated with O_2-PDA at various temperatures (600–800°C), a large negative shift of the *C*–*V* curve was observed. The FGA-induced flat-band voltage shift (ΔV_{FB}) and XPS peak intensity ratio of Ga-O bonding and Ga-N bonding ($I_{\mathrm{Ga-O}}/I_{\mathrm{Ga-N}}$) both increased at a higher O_2-PDA temperature. As a result, it was revealed that the density of FGA-induced positive fixed charges was strongly correlated with the GaO_x thickness. Thus, in this study, n-type GaN MOS capacitors were fabricated with various substrate temperatures of PECVD and the ΔV_{FB} value was analyzed to estimate the thickness of the GaO_x interlayer and its dependency on the SiO_2 deposition temperature. The fabrication process was almost identical to that for p-type GaN MOS capacitors. The Si atom density in the n-type GaN epitaxial layer was about 3×10^{16} cm^{-3}, and the SiO_2 thickness deposited by PECVD was 14–21 nm. After O_2-PDA at 200–800°C and the electrode formation, FGA (H_2/N_2: 3%) was performed at 500°C for 30 min, and ΔV_{FB} was determined from the difference in the flat-band voltage between the samples fabricated with and without performing FGA. Note that the flat-band voltage was extracted by the extrapolation of $1/C^2$–*V* plots.

Figure 3(a) shows the typical *C*–*V* characteristics of the SiO_2/n-GaN MOS capacitors acquired with a probe frequency of 1 MHz. The 200°C-deposited sample (dashed lines) showed a smaller *C*–*V* curve shift after FGA than the 400°C-deposited one (solid lines), indicating the presence of a thinner GaO_x interlayer in the case of the 200°C deposition. In Fig. 3(b), the fixed-charge density, calculated with $N_{\mathrm{fix}} = C_{\mathrm{ox}}|\Delta V_{\mathrm{FB}}|/e$, where e is the elementary charge, is plotted against the O_2-PDA temperature for each deposition temperature. Among the as-deposited samples (w/o PDA), SiO_2 deposition at 200°C led to a lower N_{fix} value compared to the deposition at 400°C, implying that only a sub-nm-thick GaO_x layer is grown during low-temperature PECVD. The N_{fix} value increased by performing O_2-PDA, especially at a temperature above 600°C, for all the samples, but the 200°C-deposited sample still exhibited a lower value of N_{fix} even after O_2-PDA at 800°C. These results indicate that the thickness of the GaO_x interlayer is strongly dependent on the substrate temperature of PECVD, and low-temperature SiO_2 deposition suppresses the GaO_x growth. To validate the GaO_x growth and quantitatively discuss the SiO_2 deposition temperature dependence of the GaO_x thickness, physical and chemical analyses utilizing high-resolution transmission electron microscopy (HR-TEM) and synchrotron-radiation XPS (SR-XPS) are necessary in the future.

Based on the results for p- and n-GaN MOS capacitors fabricated with various SiO_2 deposition temperatures, we propose a model to describe the generation of fast hole traps, as schematically

illustrated in Fig. 4. Without performing O_2-PDA, low temperature-deposited SiO_2/GaN MOS structures whose GaO_x interlayer thickness was very thin showed a smaller hump width (i.e., lower density of fast traps) than the 400°C-deposited one with a thicker GaO_x. This finding indicates that the density of fast hole traps is strongly linked to the GaO_x layer thickness. In the 400°C-deposited samples having a GaO_x layer with a certain thickness, fast trap density gradually increased with elevating the PDA temperature. On the other hand, in the 200°C-deposited sample with a thinner pre-existing GaO_x layer, elevated PDA temperature caused no significant increase in the density of fast hole traps when the PDA temperature was 600°C or lower. After O_2-PDA at 800°C, where GaO_x growth begins to occur by thermal oxidation[16], increased density of fast hole traps was commonly observed regardless of the SiO_2 deposition temperature. Consequently, it would be suggested that the major origin of fast hole traps in SiO_2/GaN MOS structures that are generated by thermal treatment is a defect existing inside the GaO_x interlayer. To separate the effects of heat itself and oxidation caused by O_2-PDA at a high temperature ($\sim$ 800°C), the impact of PDA with non-oxidant gases, such as N_2 and H_2, on the generation of fast hole traps must be investigated in the future. Besides, although a physical understanding of hole traps in GaN MOS structures has progressed, the origin of slow hole traps remains unclear because a large hysteresis of the experimental *C–V* curve is found even in the 200°C-deposited SiO_2/GaN MOS structures with O_2-PDA at 600°C, which have very few fast hole traps. This indicates that fast and slow hole traps originate from totally different defects, and thus, further investigation of these hole traps is necessary in the future.

In summary, we investigated how the SiO_2 deposition temperature impacts the PDA temperature-dependent generation of fast hole traps in p-GaN MOS structures. There existed only a few fast hole traps when the PDA temperature was below 600°C for the 200°C-deposited SiO_2/GaN MOS structures, in which the GaO_x interlayer thickness was speculated to be only on the sub-nm order. When performing O_2-PDA at 800°C on the 200°C-deposited sample, the amount of fast hole traps significantly increased, accompanied by the GaO_x growth. Therefore, we presume that the fast hole trap in SiO_2/GaN MOS structures mainly originates from a thermally induced defect inside the GaO_x interlayer and that lowering the SiO_2 deposition temperature is effective in suppressing the generation of fast hole traps. The present results should prove helpful in the development of a fabrication process for GaN power MOSFETs with improved reliability.

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

CONFLICT OF INTEREST

The authors have no conflicts to disclose.

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FIGURE CAPTIONS

FIG. 1. *C–V* characteristics of 400°C-deposited SiO_2/p-GaN MOS capacitors fabricated with various O_2 annealing temperatures.

FIG. 2. *C–V* characteristics of (a) 300°C- and (b) 200°C-deposited SiO_2/p-GaN MOS capacitors. *I–V* characteristics of (c) 300°C- and (d) 200°C-deposited SiO_2/p-GaN MOS capacitors. Data for the MOS structures annealed in O_2 at various temperatures are shown. *I–V* characteristics of the non-annealed sample with 400°C-deposited SiO_2 are also shown in (c) and (d) as a reference.

FIG. 3. (a) Typical *C–V* characteristics of n-type GaN MOS capacitors with 400°C- or 200°C-deposited SiO_2 before and after forming gas annealing (FGA). (b) O_2 annealing temperature and SiO_2 deposition temperature dependence of fixed-charge density generated by forming gas annealing in the SiO_2/n-GaN MOS structures. Higher fixed-charge density indicates the presence of a thicker gallium oxide (GaO_x) interlayer at the SiO_2/GaN interface.

FIG. 4. Schematic of the model to describe the effect of SiO_2 deposition temperature and O_2 annealing temperature on hole trap generation.

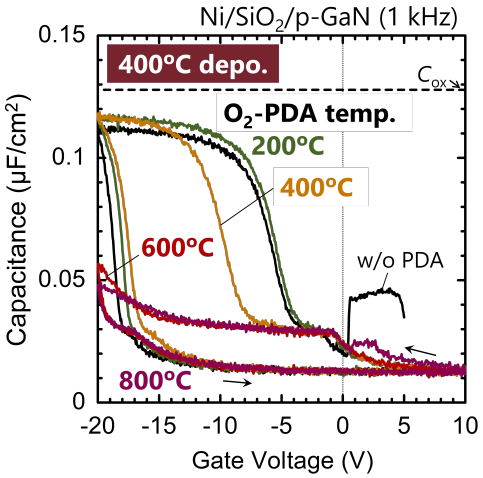

FIG. 1.

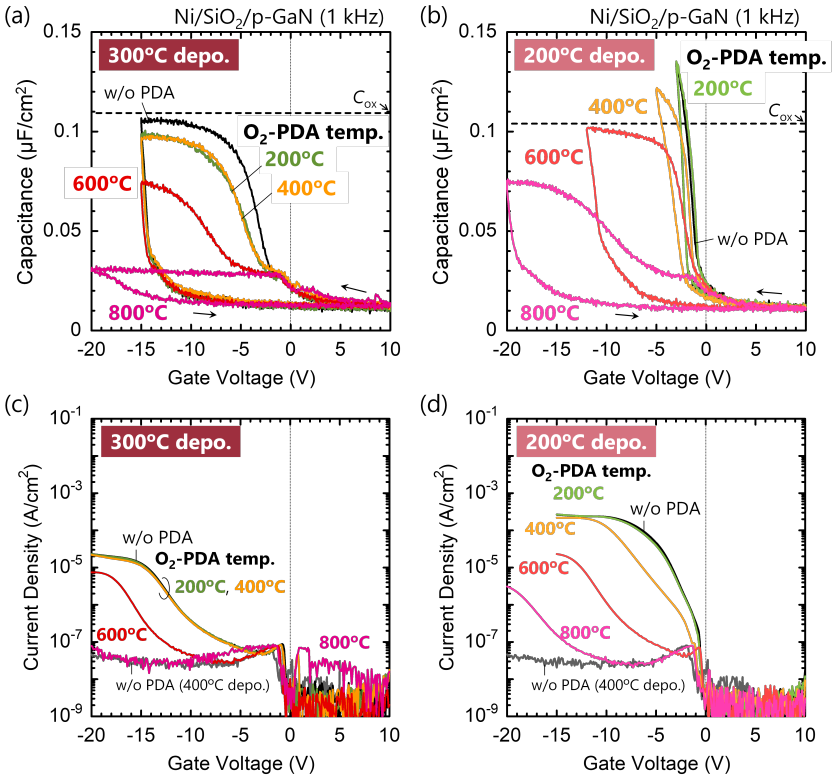

FIG. 2.

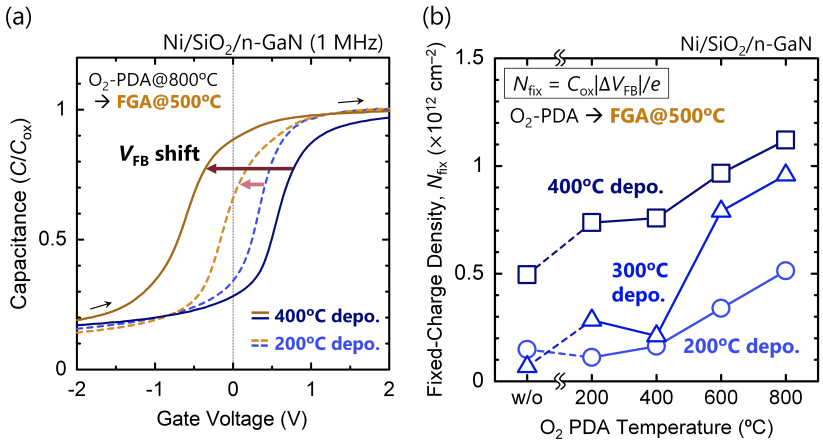

FIG. 3.

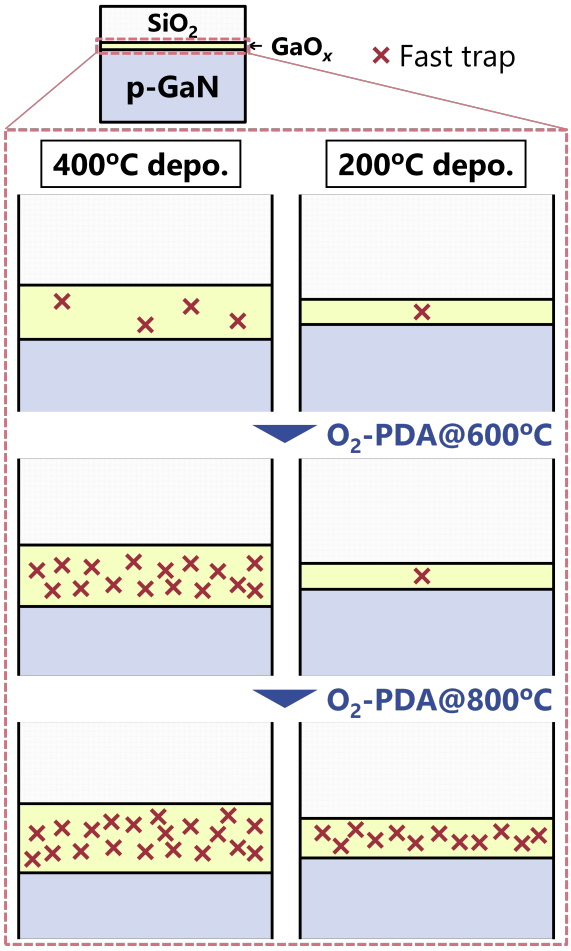

FIG. 4.